Title	***Engineering Prototype Report for EP-68 – 6.6 W DC-DC Flyback Converter Using DPA-Switch™ (DPA423G)***
Specification	Input: 36-57 VDC, Output: 3.3 V / 2 A
Application	Power over Ethernet (PoE) Power Supply
Author	Power Integrations Applications Department
Document Number	EPR-68
Date	19-Jul-2005
Revision	1.1

Summary and Features

- High efficiency, low parts count and low cost power supply
- Ideally suited for PoE, VoIP, standby and other distributed 48 V DC-DC conversion applications
  - Signature circuit is fully compatible with IEEE 802.3af requirements
- *DPA-Switch* Integrates
  - PWM controller and 220 V MOSFET switching device
  - Accurate input voltage UV detection and OV protection
  - Thermal, overload, short-circuit and open loop protection
  - Regulation at zero load (cycle skipping)
  - Accurate 400 kHz trimmed internal oscillator
- Small footprint 2" × 1", low overall height 0.9", dual layer PCB
- 100% surface mount construction

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Important Note:
Although this board is designed to satisfy safety telecom isolation requirements, this engineering prototype has not been agency approved.

1 Introduction

This engineering report describes a 3.3 V / 2 A (6.6 W) DC-DC converter that is based on a DPA423G device. This design is intended as an evaluation platform for *DPA-Switch* devices in the low cost surface-mount DIP package. High operating efficiency, low parts count, small footprint and low height make this an ideal choice for Power over Ethernet (PoE) and VoIP DC-DC converter applications.

This report contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit board layout, and performance data.

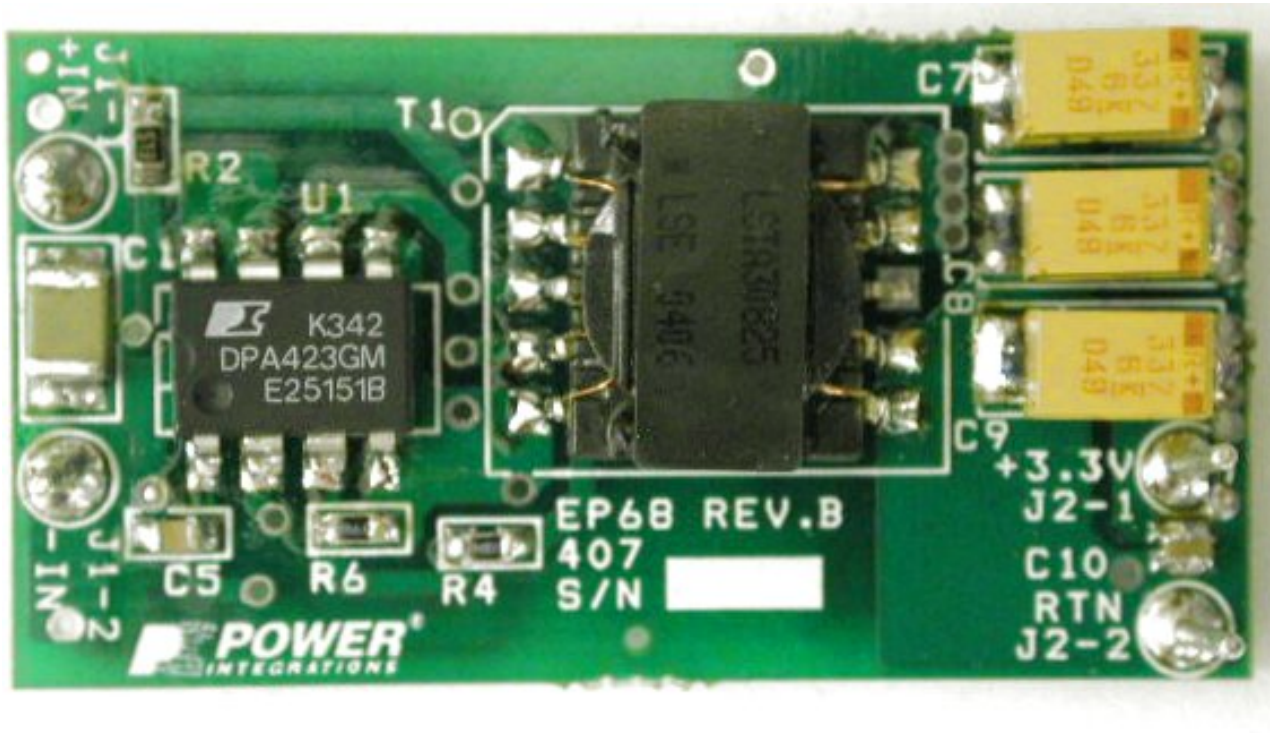

Figure 1 - EP68 Populated Circuit Board Photograph.

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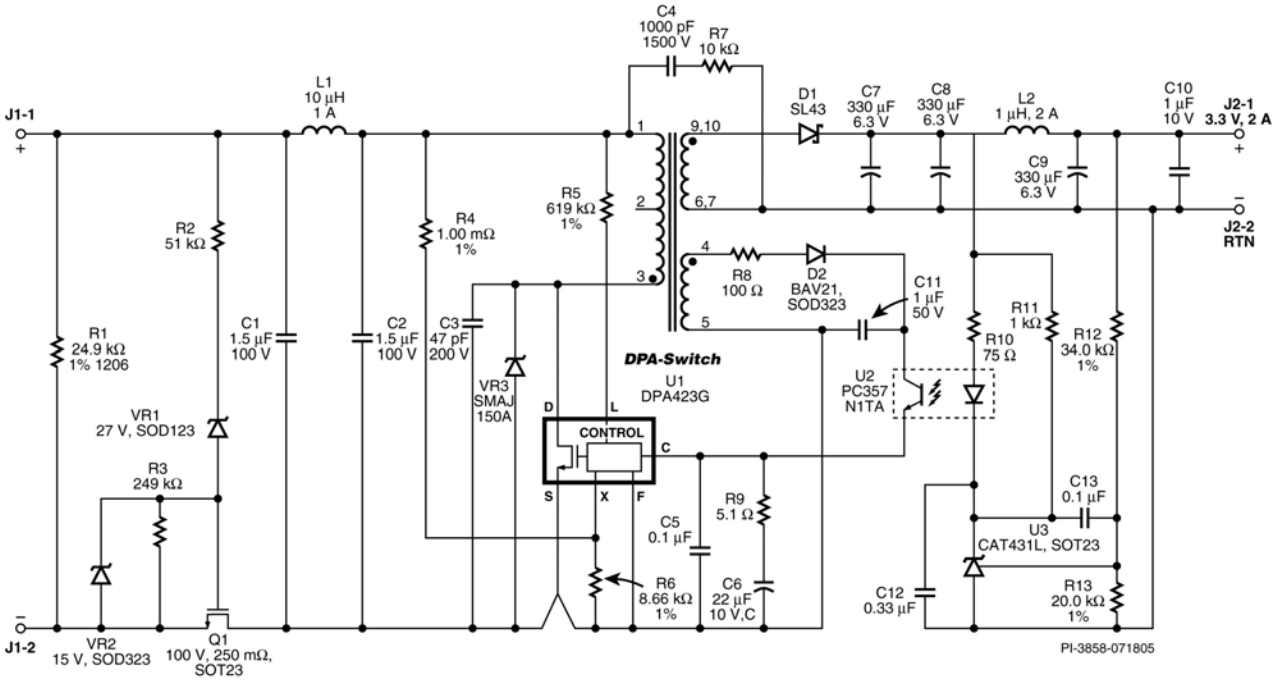
2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	36		57	VDC	PoE input range specification
Output						
Output Voltage	V_{OUT1}	3.20	3.30	3.40	V	±3% including set point and line/load regulation
Output Ripple Voltage	$V_{RIPPLE1}$		35	50	mVpp	20 MHz bandwidth
Continuous Output Current	I_{OUT}	2.0			A	
Peak Output Current	I_{OUT}		2.5		A	
Total Output Power						
Continuous Output Power	P_{OUT}			6.6	W	
Peak Output Power	P_{OUT_PEAK}		8.3		W	
Efficiency	η	77	78		%	Measured at 48 V, P_{OUT} (6.6 W), 25 °C
Environmental						
Safety Isolation		1500			VDC	1 min.
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

3 Schematic



*All resistors and capacitors are 0805 size unless otherwise specified

Figure 2 - EP68 Schematic.

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4 Circuit Description

The Flyback topology was used to minimize circuit board size, parts count and cost, while attaining excellent operating efficiency across the input voltage range.

4.1 DPA-Switch Primary

The DPA423G IC provides PWM control, startup, feedback, under/over voltage and over-temperature protection functions. The integrated 220 V MOSFET provides excellent switching characteristics at the selected 400 kHz operating frequency. The MOSFET and controller consume minimal power, enabling a typical operating efficiency of 74%-78% across the operating input voltage range (see Figure 7).

R1 provides a 25 kΩ input impedance, consistent with PoE Class 0 requirements. Above 30 V, Zener VR1 conducts, allowing n-channel MOSFET Q1 to turn on. Zener diode VR2 protects the gate of Q1 from overvoltage damage. Resistors R2 and R3 provide repeatable on and off timing.

Resistor R5 programs the typical input under-voltage ON threshold to 33 VDC. Resistors R4 and R6 program the internal device current limit to reduce with increasing input voltage. Maximum output (overload) current varies less than 5% across the operating voltage range. The reduction in overload output current reduces secondary transformer leakage spikes and allows the use of a 30 V Schottky diode, for the output rectifier D1.

The primary-side Zener clamp, VR3, provides protection of the DPA423G drain under input surge and overvoltage conditions. Zener diode VR3 does not conduct under normal operating conditions.

The primary bias winding provides CONTROL pin current after start-up. Diode D2 rectifies the bias winding, while components R8 and C11 reduce the high frequency switching noise and reduce the peak charging of the bias voltage.

The DPA423G operates well within the recommended junction temperature limits (100 °C) at an elevated ambient of 50 °C, in a free-convection cooled environment (see Section 11).

4.2 Output Rectification

Schottky output diode D1 enables low-loss rectification of the secondary winding voltage. Low ESR tantalum output capacitors, C7-9, reduce switching ripple and minimize losses. Secondary output choke L1 and ceramic output capacitor C10 reduce high frequency noise and ripple at the output.

4.3 Output Feedback

The output voltage is sensed via the resistor divider formed by R12 and R13 and fed into the reference pin of the low voltage reference, U3. Feedback compensation components R10, R11, and C13 ensure stable operation and optimum line and load transient response. Capacitor C12 provides a soft-finish characteristic, preventing output voltage overshoot during startup of the converter.

5 PCB Layout

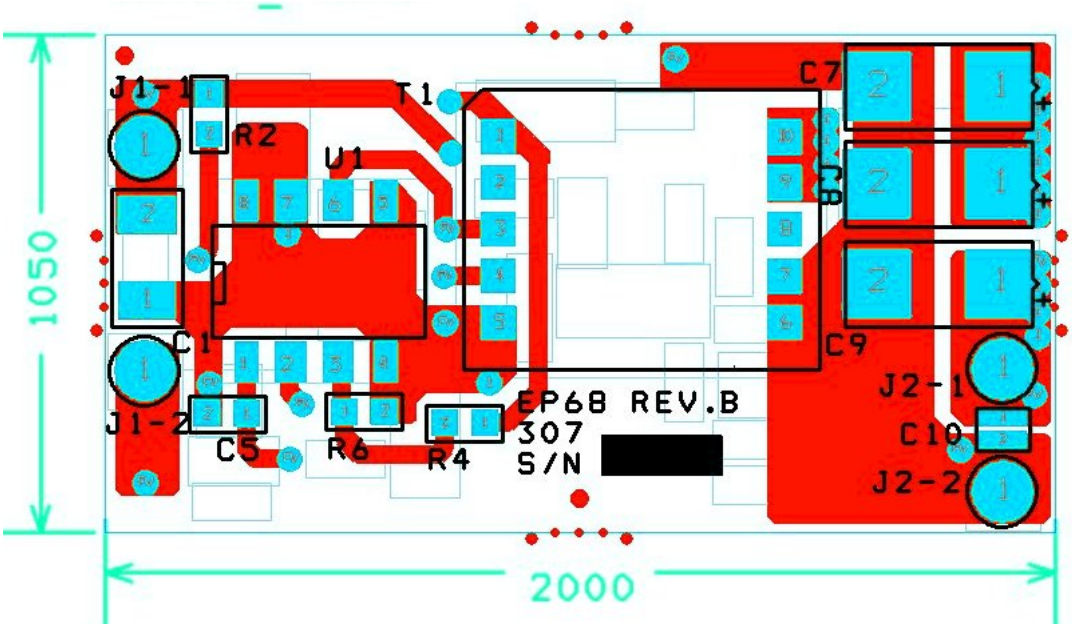

Figure 3 - Top Side, SMT Printed Circuit Layout (Top View).

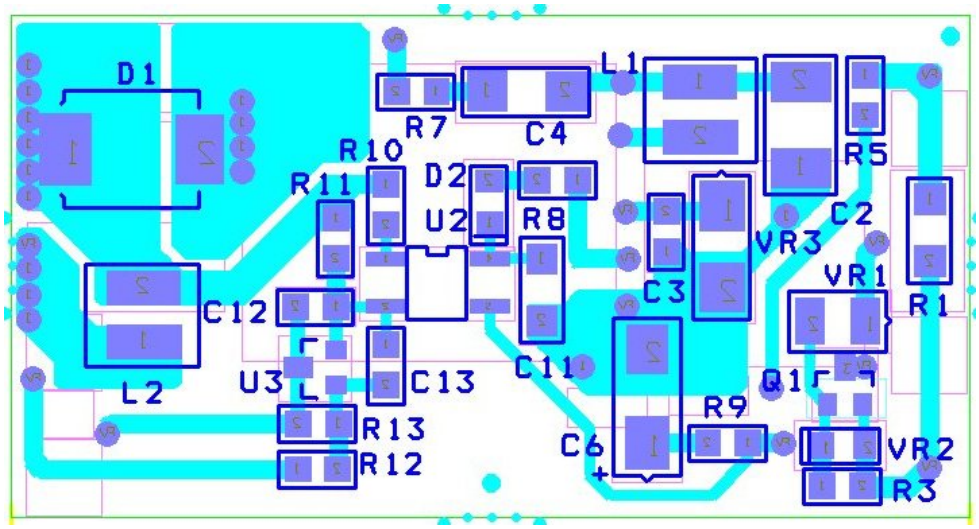

Figure 4 - Bottom Side, SMT Printed Circuit Layout (Top View).

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6 Bill of Materials

Item	Qty	Reference	Description	P/N	Manufacturer
1	1	U1	*DPA-Switch*	DPA423G	Power Integrations
2	1	U2	Optocoupler, 80-160% graded CTR	PC357N1TA	Sharp
3	1	U3	Low voltage shunt regulator, SOT23	CAT431L	Catalyst Semiconductor
4	1	C1, C2	1.5 µF, 100 V, 1812	THCS50E2A155ZT	UCC
5	1	C3	47 pF, 200 V	ECJ-2VC2D470J	Panasonic
6	1	C4	1000 pF, 1500V, 1808	1808SC102KAT1A	AVX
7	2	C5, C13	0.1 µF, 50 V	ECJ-2YB1H104K	Panasonic
8	1	C6	22 µF, 10 V, tantalum, C size	ECST1AC226R	Panasonic
9	3	C7-9	330 µF, 6.3 V, tantalum, X size	T495X337K006AS	Kemet
10	1	C10	1 µF, 10 V, 0508 alternative geometry	ECY-29RA105KV	Panasonic
11	1	C11	1 µF, 50 V, 1206	ECJ-3FF1H105Z	Panasonic
12	1	C12	0.33 µF, 50 V	ECJ-2YB1C334K	Panasonic
13	1	D1	30 V, 4 A Schottky	SL43	Vishay
14	1	D2	200 V, 200 mA	BAV21	generic
15	4	J1-1,2 J2-1,2	Pin, Surface Mount, 0.040 x 0.375”	4531051-0000	Zierick
16	1	L1	10 µH, 1 A	SCD-0403-100MT	Chilisin
17	1	L2	1 µH, 2 A	SCD-0403-1R0M	Chilisin
18	1	Q1	MOSFET, N Channel, 100 V, 250 mΩ	Si2328DS-T1	Vishay
19	1	R1	24.9 kΩ, 1%, 1206	ERJ-8ENF2492V	Panasonic
20	1	R2	51 kΩ	ERJ-6GEYJ513V	Panasonic
21	1	R3	249 kΩ	ERJ-6GEY2493V	Panasonic
22	1	R4	1.00 MΩ, 1%	ERJ-6ENF1004V	Panasonic
23	1	R5	619 kΩ, 1%	ERJ-6ENF6193V	Panasonic
24	1	R6	8.66 kΩ, 1%	ERJ-6ENF8661V	Panasonic
25	1	R7	10 Ω	ERJ-6GEYJ100V	Panasonic
26	1	R8	100 Ω	ERJ-6GEYJ101V	Panasonic
27	1	R9	5.1 Ω	ERJ-6GEYJ5R1V	Panasonic
28	1	R10	75 Ω	ERJ-6GEYJ750V	Panasonic
29	1	R11	1 kΩ	ERJ-6GEYJ102V	Panasonic
30	1	R12	34.0 kΩ, 1%	ERJ-6ENF3402V	Panasonic
31	1	R13	20.0 kΩ, 1%	ERJ-6ENF2002V	Panasonic
32	1	T1	ER14.5 Transformer	LSTA30825 SIL6029 IM 040 202 31	L.S.E. HiCal Vogt
33	1	VR1	27V, 500 mW, SOD123	BZT52C27-7	Diodes, Inc. or Generic
34	1	VR2	15V, 200 mW, SOD323	BZT52C15S-7	Diodes, Inc. or Generic
35	1	VR3	150V TVS	SMAJ150A	Generic

*Resistors and capacitors are size 0805, unless otherwise specified.

7 Transformer Specification

7.1 Electrical Diagram

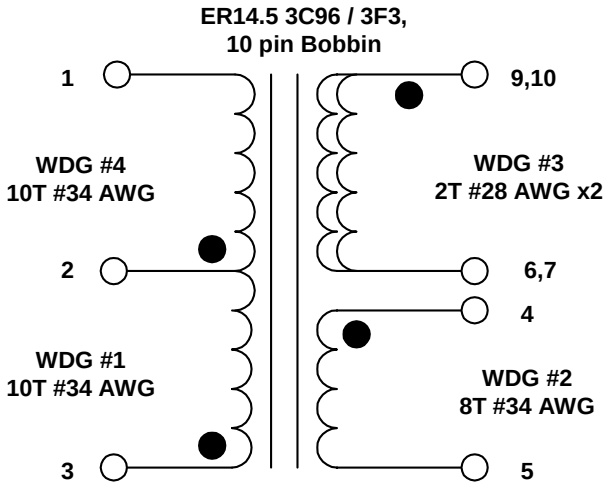

Figure 5 - Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1-5 to Pins 6-10	1500 VDC
Primary Inductance	Pins 1-3, all other windings open	120 μH, +/-10%
Resonant Frequency	Pins 1-3, all other windings open	7.5 MHz (min.)
Primary Leakage Inductance	Pins 1-3, with Pins 6/7-9/10 shorted	3.0 μH (max.)

7.3 Materials

Item	Description
[1]	Core: ER14.5, Ferroxcube 3C96, 3F3 (or equivalent), ALG = 312 nH/T^2
[2]	Bobbin: ER14.5, 10 pin
[3]	Magnet Wire: #34 AWG, Double Coated (Heavy Nyleze)
[4]	Magnet Wire: #28 AWG, Double Coated (Heavy Nyleze)
[5]	Tape: 3M 1298 Polyester Film (or equivalent), 1.8 mm wide
[6]	Core Clamp ER14.5 Ferroxcube CLM14.5 (optional)
[7]	Varnish (DIPPED ONLY, NOT IMPREGNATED)

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7.4 Transformer Build Diagram

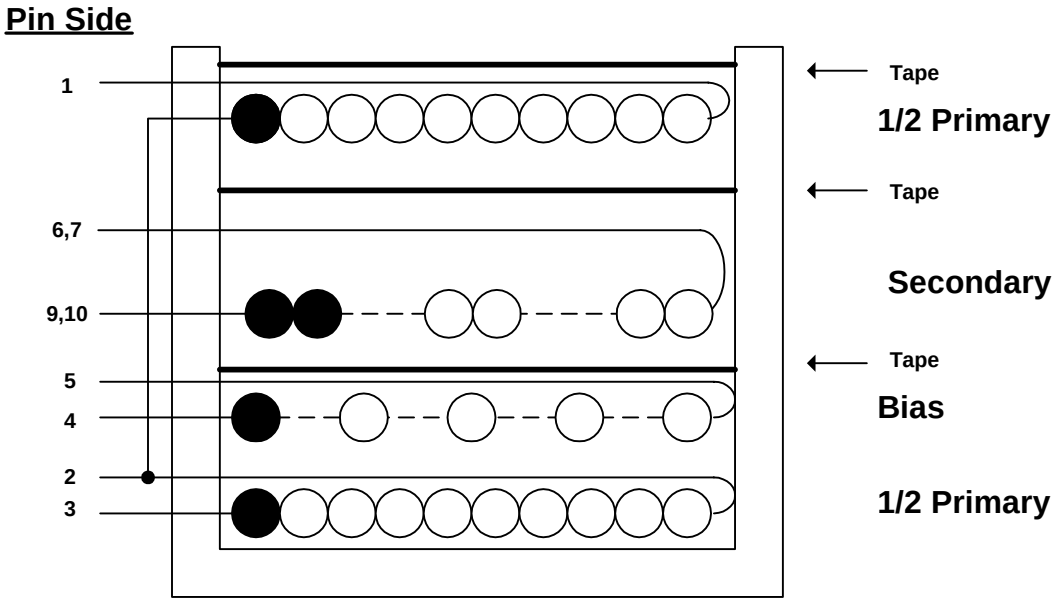

Figure 6 - Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Arrange bobbin & rotation such that primary start/finish wires do not overlap.
½ Primary	Start at Pin 3. Wind 10 turns of item [3] in 1 layer. Bring finish lead back and terminate on Pin 2.
Bias Winding	Starting at Pin 4, wind 8 turns of item [3]. Spread turns evenly across bobbin in a single layer. Bring finish lead back and terminate on Pin 5.
Basic Insulation	Use one layer of item [5] for basic insulation.
Secondary Winding	Start at Pins 9 and 10. Wind 2 turns of bifilar item [4] in 1 layer. Bring finish lead back and terminate on Pins 6 and 7.
Basic Insulation	Use one layer of item [5] for basic insulation.
½ Primary	Continue from Pin 2. Wind 10 turns of item [3] in 1 layer. Bring finish lead back and terminate on Pin 1.
Outer Insulation	Use one layer of item [5] for basic insulation.
Final Assembly	Assemble and secure (glue or clamp, item[6]) core halves. Dip varnish item [7] and cure.

8 Transformer Spreadsheet

	A	B	D	F	G	I
1	DCDC_DPASwitch_Flyback_013004_Revision1J. Copyright Power Integrations 2004	INPUT	INFO	OUTPUT	UNITS	DPASwitch_Flyback_013004 - Continuous/Discontinuous mode Spreadsheet. Copyright 2004 Power Integrations
2	**ENTER APPLICATION VARIABLES**					**DC-DC Converter**
3	**VDCMIN**	**36**			**Volts**	**Minimum DC Input Voltage**
4	**VDCMAX**	**57**			**Volts**	**Maximum DC Input Voltage**
5	VO	3.3			Volts	Output Voltage
6	**PO**	**6.6**	Comment		**Watts**	**Verify temperature rise for continuous power. P and G packages may be thermally limited**
7	n	0.8				Efficiency Estimate
8	Z			0.7		Loss Allocation Factor, (0.7 Recommended)
9	**VB**	**14**			**Volts**	**Bias Voltage (Recommended between 12V and 18V)**
10						
11	**UV AND OV PARAMETERS**					
12			min	max		
13	VUVOFF		30.0	33.1	Volts	Minimum undervoltage On-Off threshold
14	VUVON		32.2	34.7	Volts	Maximum undervoltage Off-On threshold (turn-on)
15	VOVON		74.9	-	Volts	Minimum overvoltage Off-On threshold
16	VOVOFF			94.7	Volts	Maximum overvoltage On-Off threshold (turn-off)
17	RL			619.0	k-Ohms	
18						
19	**ENTER DPASWITCH VARIABLES**					
20	***DPASWITCH***	**DPA423G**			*16VDC*	*36VDC*
21	*Chosen Device*	*DPA423G*		*Power Ou*	*6W*	*13W*
22	ILIMITMAX	*1.16*	*1.34*		Amps	From DPASWITCH Data Sheet
23	**Frequency**	**F**				**Enter 'F' for fS = 400KHz and 'L' for fS = 300KHz**
24	fS	375000			Hertz	DPASWITCH Switching Frequency
25	**VOR**	**38**		**38**	**Volts**	**Reflected Output Voltage**
26	KI	0.70		0.7		Current Limit Reduction Factor
27	ILIMITEXT			0.812	Amps	Minimum External Current limit
28	RX			11.0	k-Ohms	Resistor from X pin to source to set external current limit
29	VDS	1			Volts	DPASWITCH on-state Drain to Source Voltage
30	VD	0.5			Volts	Output Winding Diode Forward Voltage Drop
31	VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
32	KRP/KDP	0.62				Ripple to Peak Current Ratio (0.2 < KRP < 1.0 : 1.0< KDP<6.0)
33						
34	**ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES**					
35	**Core Type**	**ER14.5**				
36	**Core Manuf**					
37	**Bobbin Manuf**					
38	*Core*		*ER14.5*		*P/N:*	*ER14.5-3F3-S*
39	*Bobbin*		*ER14.5_Bob*		*P/N:*	*CPVS-ER14.5-1S-10P*
40	AE			0.176	cm^2	Core Effective Cross Sectional Area
41	LE			1.9	cm	Core Effective Path Length
42	AL			1400	nH/T^2	Ungapped Core Effective Inductance
43	BW			1.9	mm	Bobbin Physical Winding Width
44	M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
45	L	2				Number of Primary Layers
46	NS	2				Number of Secondary Turns
47						
48	**CURRENT WAVEFORM SHAPE PARAMETERS**					
49	**DMAX**			**0.52**		**Maximum Duty Cycle**
50	IAVG			0.23	Amps	Average Primary Current
51	**IP**			**0.64**	**Amps**	**Peak Primary Current**
52	IR			0.39	Amps	Primary Ripple Current
53	IRMS			0.33	Amps	Primary RMS Current
54						
55	**TRANSFORMER PRIMARY DESIGN PARAMETERS**					
56	LP			120	uHenries	Primary Inductance
57	NP			20		Primary Winding Number of Turns
58	NB			8		Bias Winding Number of Turns
59	ALG			300	nH/T^2	Gapped Core Effective Inductance
60	**BP**			**2768**	**Gauss**	**Peak Flux density during transients (Limit to 3000 Gauss)**
61	**BM**			**2168**	**Gauss**	**Maximum Flux Density**
62	**BAC**			**667**	**Gauss**	**AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)**
63	ur			1203		Relative Permeability of Ungapped Core
64	**LG**			**0.06**	**mm**	**Gap Length (Lg >> 0.051 mm)**
65	BWE			3.8	mm	Effective Bobbin Width

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66						
67	**TRANSFORMER SECONDARY DESIGN PARAMETERS**					
68	ISP			6.36	Amps	Peak Secondary Current
69	ISRMS			3.15	Amps	Secondary RMS Current
70	IO			2.00	Amps	Power Supply Output Current
71	IRIPPLE			2.43	Amps	Output Capacitor RMS Ripple Current
72						
73	**VOLTAGE STRESS PARAMETERS**					
74	**VDRAIN**			**157**	**Volts**	**Maximum Drain Voltage (Includes Effect of Leakage Inductance)**
75	PIVS			9	Volts	Output Rectifier Maximum Peak Inverse Voltage
76	PIVB			36	Volts	Bias Rectifier Maximum Peak Inverse Voltage
77						
78	**ADDITIONAL OUTPUTS**					
79	V_OUT2				Volts	Auxiliary Output Voltage
80	VD_OUT2				Volts	Auxiliary Diode Forward Voltage Drop
81	N_OUT2			0.00		Auxiliary Number of Turns
82	PIV_OUT2			0	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage
83	V_OUT3				Volts	Auxiliary Output Voltage
84	VD_OUT3				Volts	Auxiliary Diode Forward Voltage Drop
85	N_OUT3			0.00		Auxiliary Number of Turns
86	PIV_OUT3			0	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage
87						

9 Performance Data

All measurements were taken at room temperature utilizing a DC input source and dynamic DC loads. Input and output voltages and output current were measured with dedicated DVMs.

9.1 Efficiency

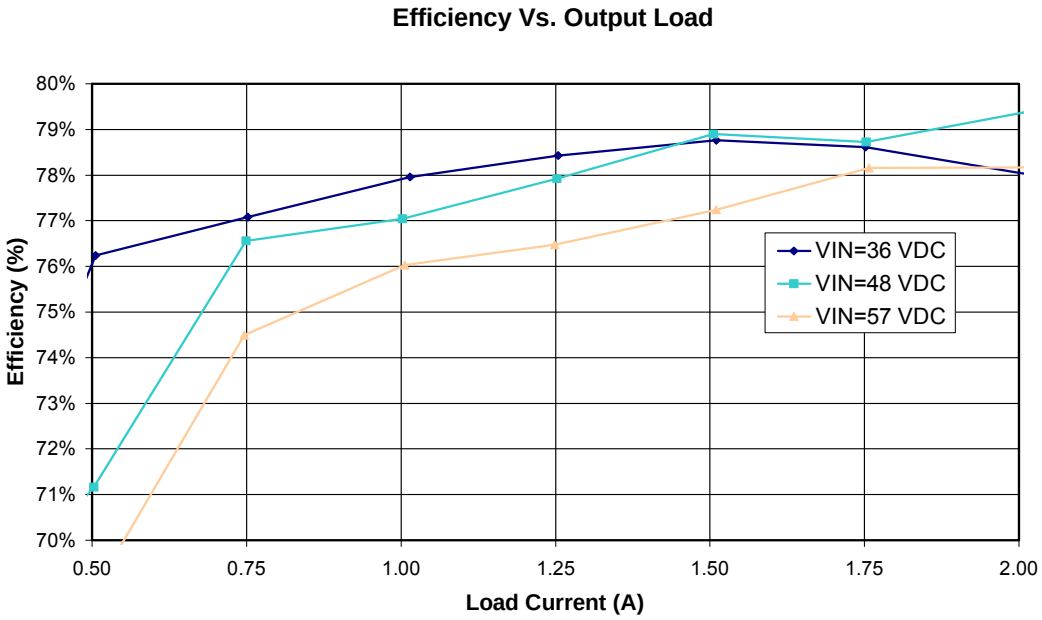

Figure 7 - Efficiency vs Output Load, Room Temperature.

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9.2 Regulation

9.2.1 Load

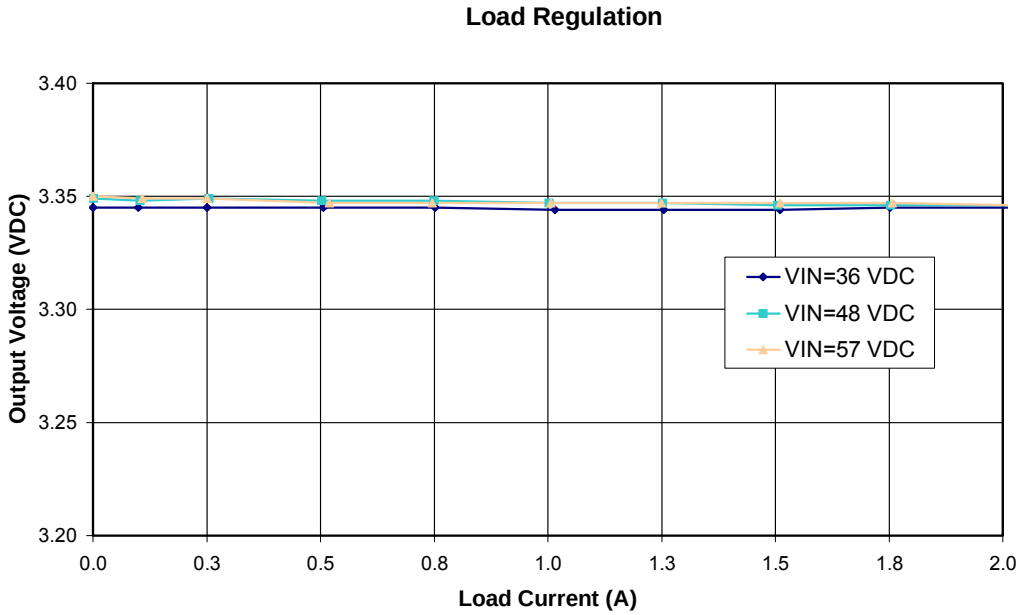

Figure 8 - Load Regulation, Room Temperature.

9.2.2 Line

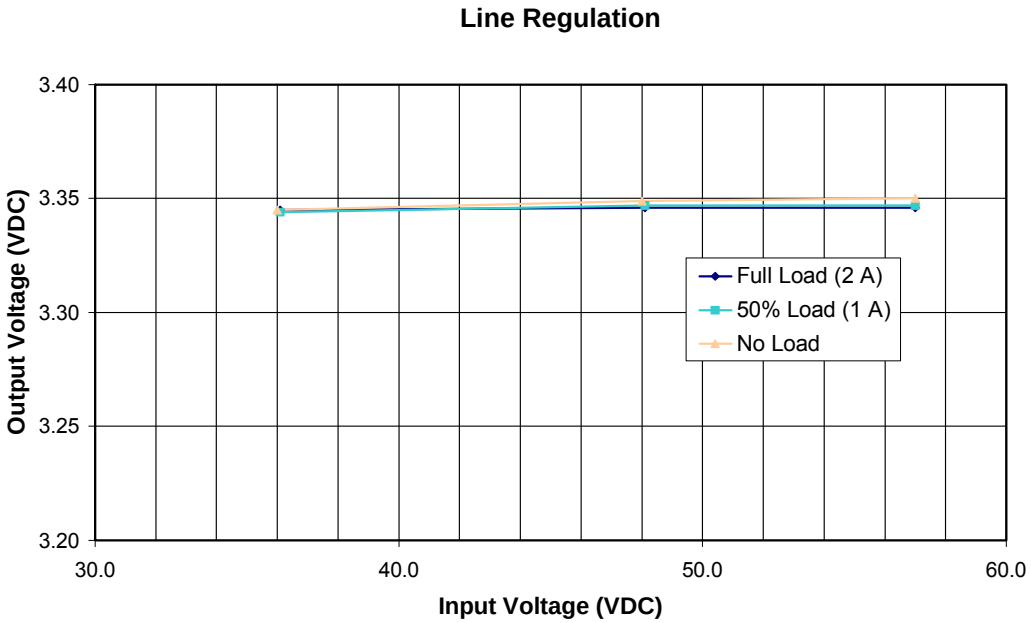

Figure 9 - Line Regulation, Room Temperature.

9.3 Peak Power

The DC output load current was recorded just prior to the auto-restart operation.

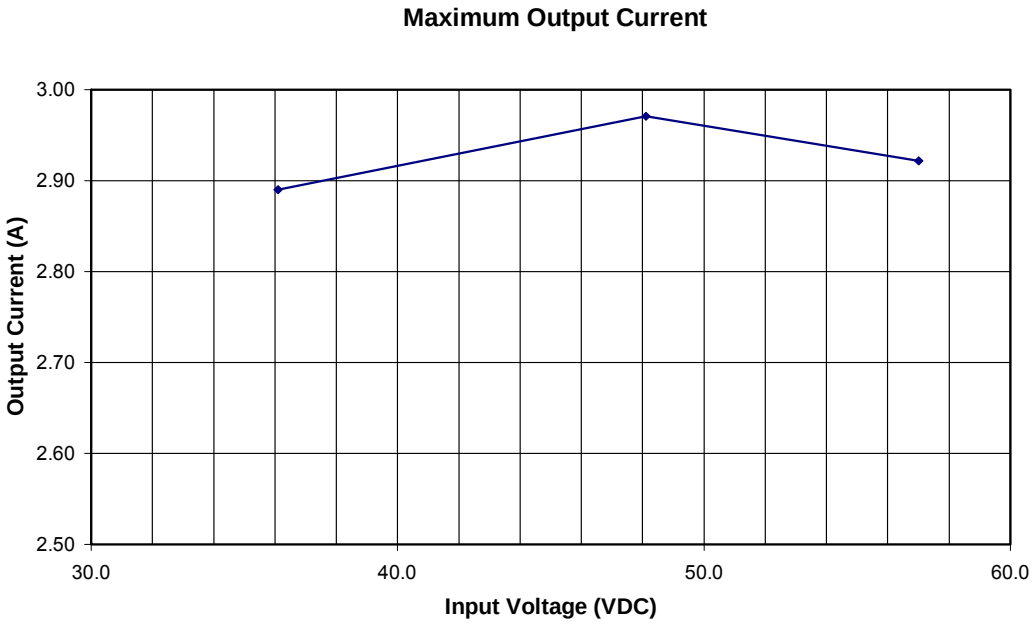

Figure 10 - Maximum Output Overload Current, Room Temperature.

10 Waveforms

10.1 Drain Voltage and Current, Full Load Operation

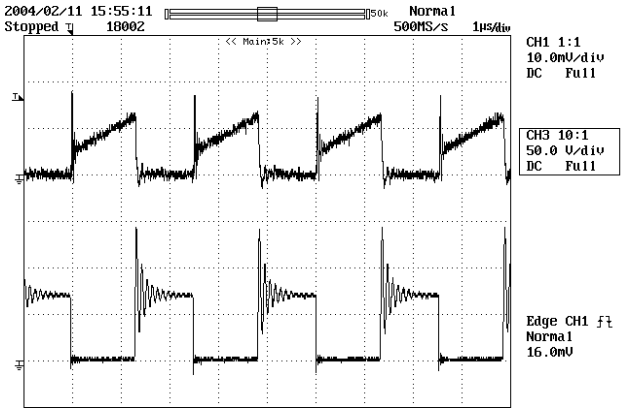

Figure 11 – 36 VDC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V, 1 μs / div.

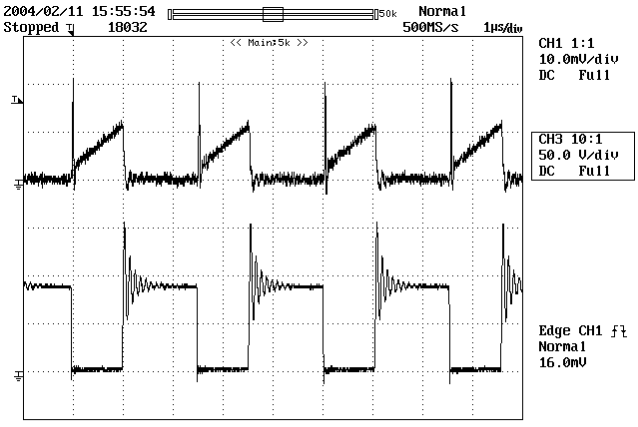

Figure 12 – 57 VDC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V, 1 μs / div.

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10.2 Output Voltage Start-Up Profile

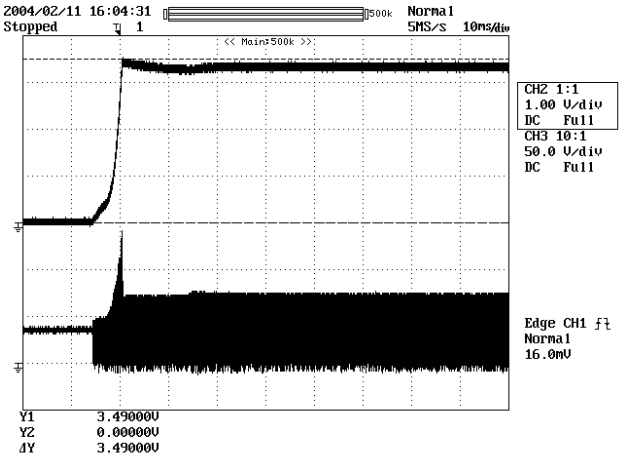

Figure 13 - Start-Up Profile, 36 VDC, No Load (worst-case).
Upper: V_{OUT}, 1 V / div.
Lower: V_{DRAIN}, 50 V, 10 ms / div.

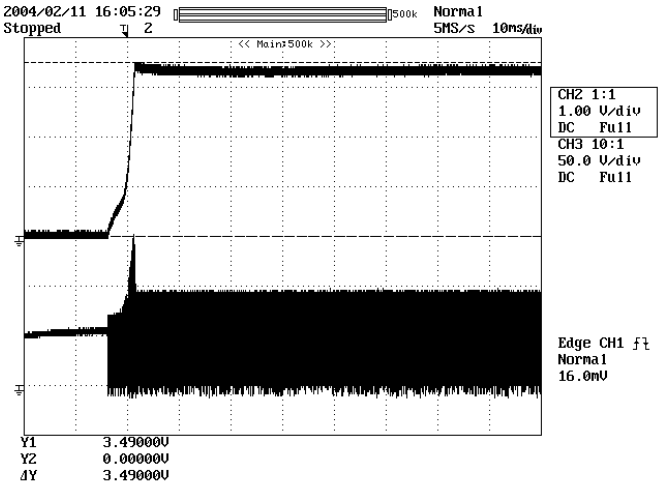

Figure 14 - Start-Up Profile, 57 VDC, No Load (worst-case).
Upper: V_{OUT}, 1 V / div.
Lower: V_{DRAIN}, 50 V, 10 ms / div.

10.3 Drain Voltage and Current Start-Up Profile

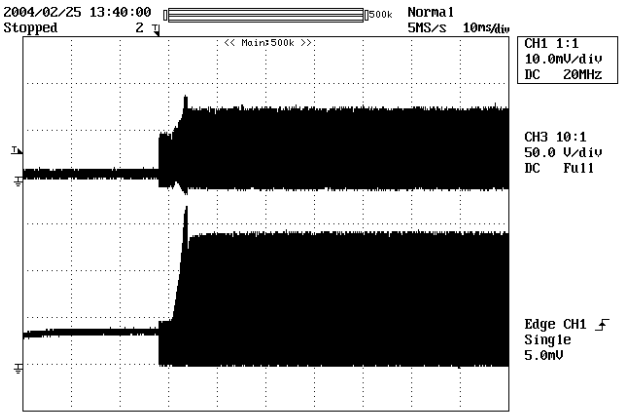

Figure 15 – 36 VDC Input, 2 A Resistive Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V, 10 ms / div.

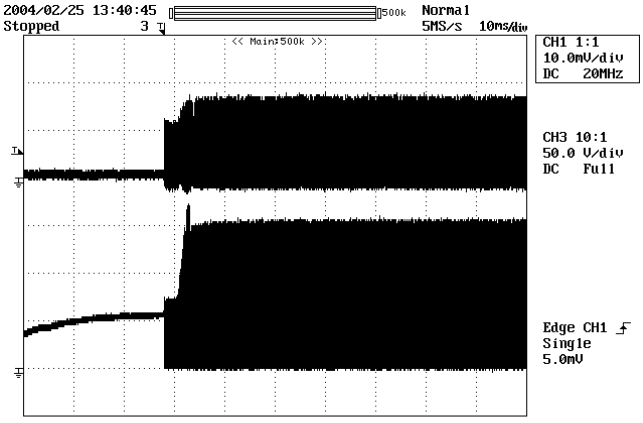

Figure 16 – 57 VDC Input, 2 A Resistive Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V, 10 ms / div.

10.4 Load Transient Response (75% to 100% Load Step)

In the following two oscilloscope screen shots (Figures 17 and 18), signal averaging was used to more clearly capture the output voltage response to a load transient. Averaging minimizes the appearance of the 400 kHz switching ripple in the output voltage scope plot. The load current step was used to trigger the horizontal sweep of the oscilloscope.

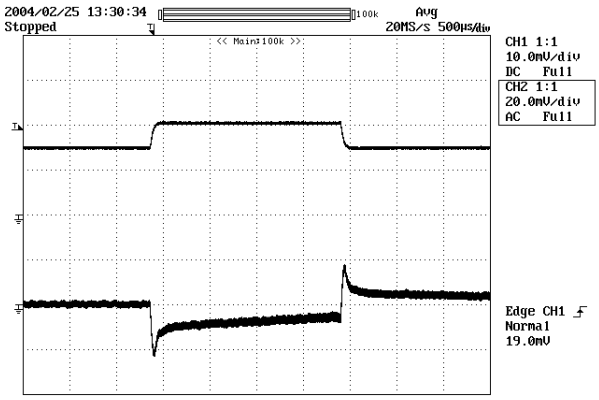

Figure 17 - Transient Response,
36 VDC, 75-100-75% Load Step.
Top: Load Current, 1 A / div.
Bottom: Output Voltage,
20 mV, 500 µs / div.

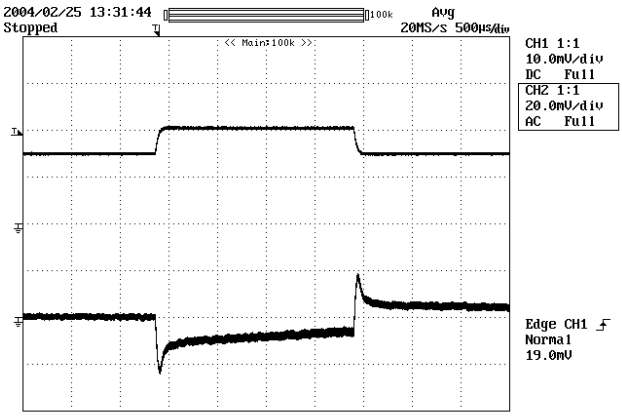

Figure 18 - Transient Response,
57 VDC, 75-100-75% Load Step.
Top: Load Current, 1 A / div.
Bottom: Output Voltage,
20 mV, 500 µs / div.

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10.5 Output Ripple Measurements

10.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figures 19 and 20.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

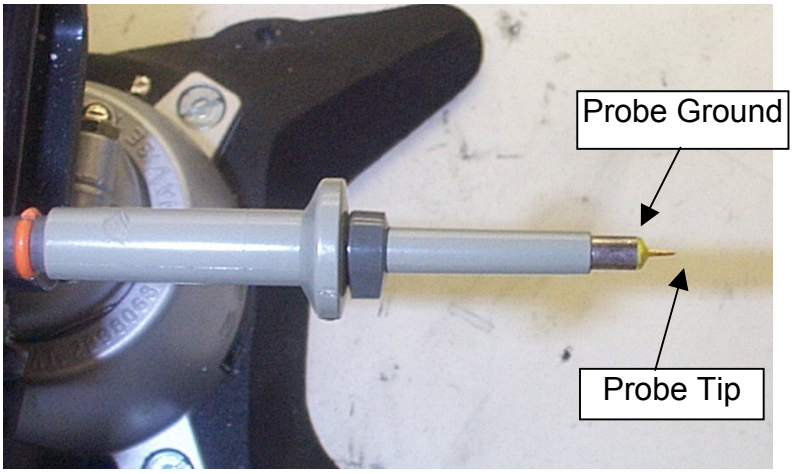

Figure 19 - Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

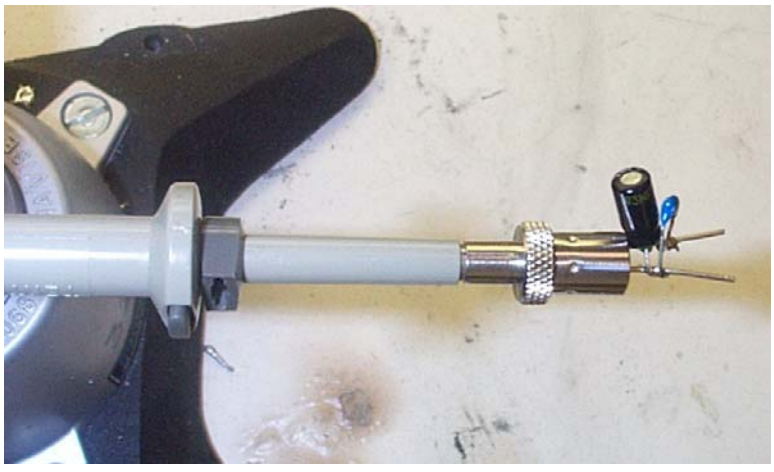

Figure 20 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple Measurement, and Two Parallel Decoupling Capacitors Added).

10.5.2 Output Ripple Measurements

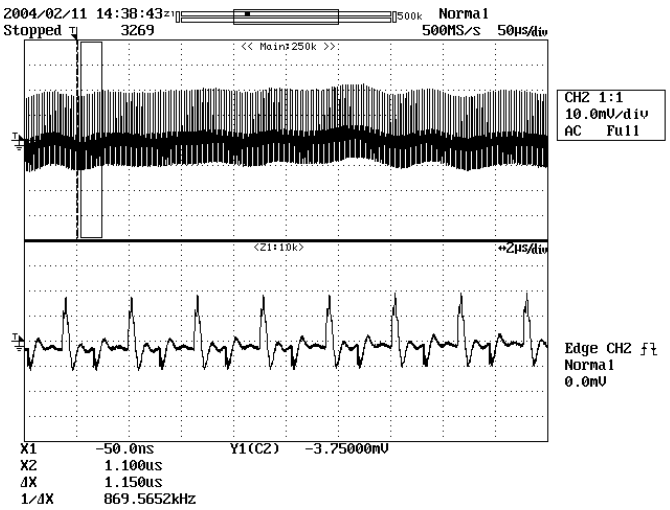

Figure 21 - Ripple, 36 VDC, Full Load.
Top: 10 mV / div, 50 µs / div.
Bottom: 10 mV / div, 2 µs / div.

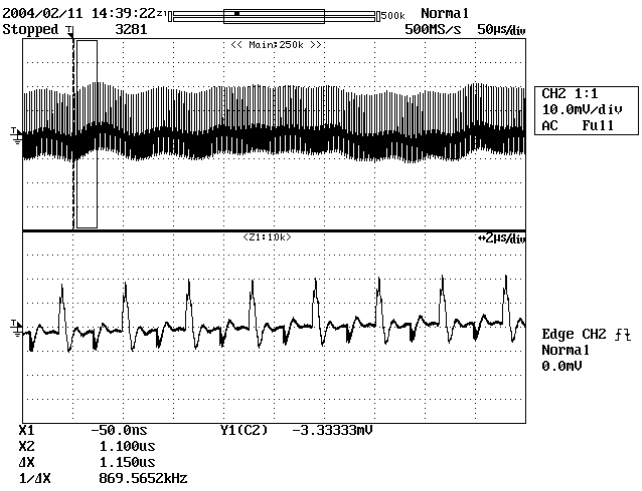

Figure 22 - Ripple, 48 VDC, Full Load.
Top: 10 mV / div, 50 µs / div.
Bottom: 10 mV / div, 2 µs / div.

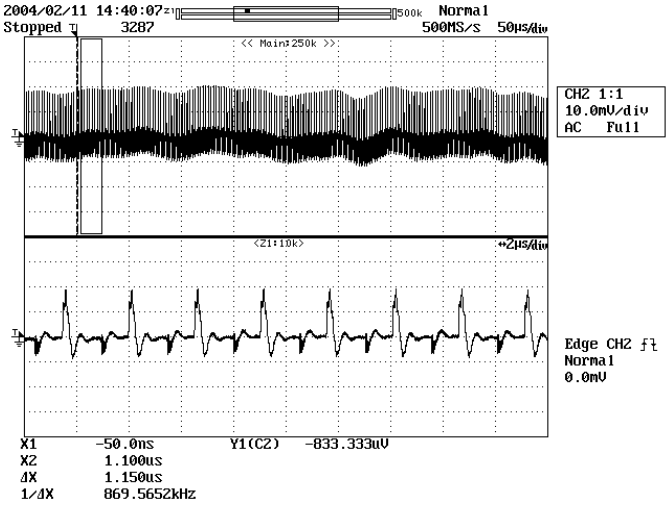

Figure 23 - Ripple, 57 VDC, Full Load.
Top: 10 mV / div, 50 µs / div.
Bottom: 10 mV / div, 2 µs / div.

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11 Thermal Performance

The temperatures of key components were recorded using T-type thermocouples. Two of the four thermocouples were soldered; one directly to a SOURCE pin of the DPA423G (U1) and the other to the cathode of the output rectifier (D1). The other two thermocouples were glued; one to the transformer (T1) core, on the center leg, and the other to the case of the first (of the two) high-ripple output capacitor (C7).

The unit was operated at full load, at 36 VDC, 48 VDC and 57 VDC, in free convection within a small enclosure.

The results show adequate thermal margin, considering an additional ambient rise of +28 °C, equivalent to operating at an ambient of 50 °C. At 36 VDC, full load, within an enclosure at 50 °C ambient, this equates to a DPA423G case temperature of 79 °C. This is well below the recommended maximum case temperature of 100 °C.

Figure 24 is an infrared thermograph taken at nominal-line (48 VDC).

Measured Temperature (°C)			
Item	**36 VDC**	**48 VDC**	**57 VDC**
Ambient	22	22	22
DPA423G (U1)	51	51	53
Transformer core (T1)	75	75	75
Output Rectifier (D1)	63	61	61
Output Capacitor (C7)	45	43	43

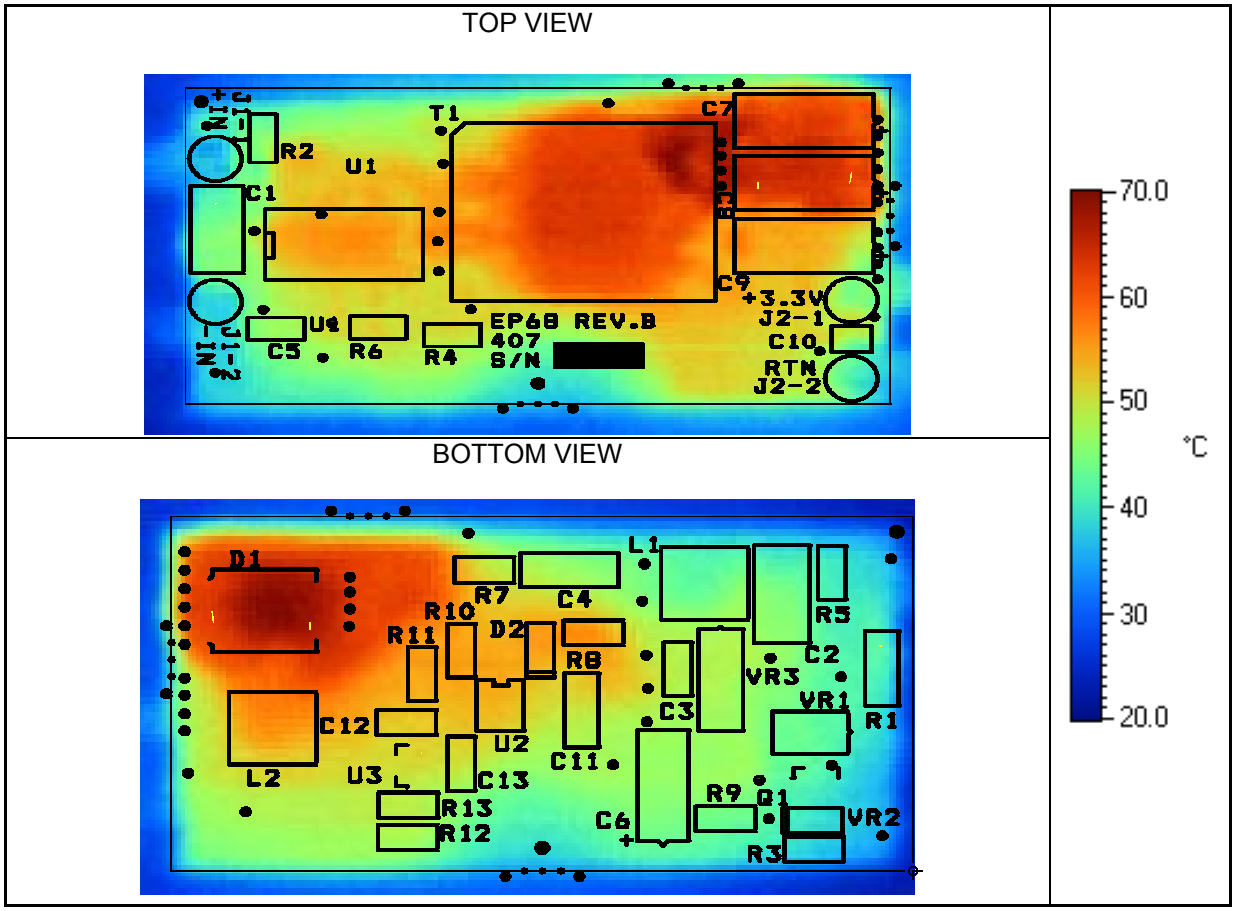

Figure 24- Infrared Thermograph of the EP68 Board, 48 VDC, Full Load, Room Ambient.

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12 Control Loop Measurements

12.1 36 VDC Maximum and Nominal Load

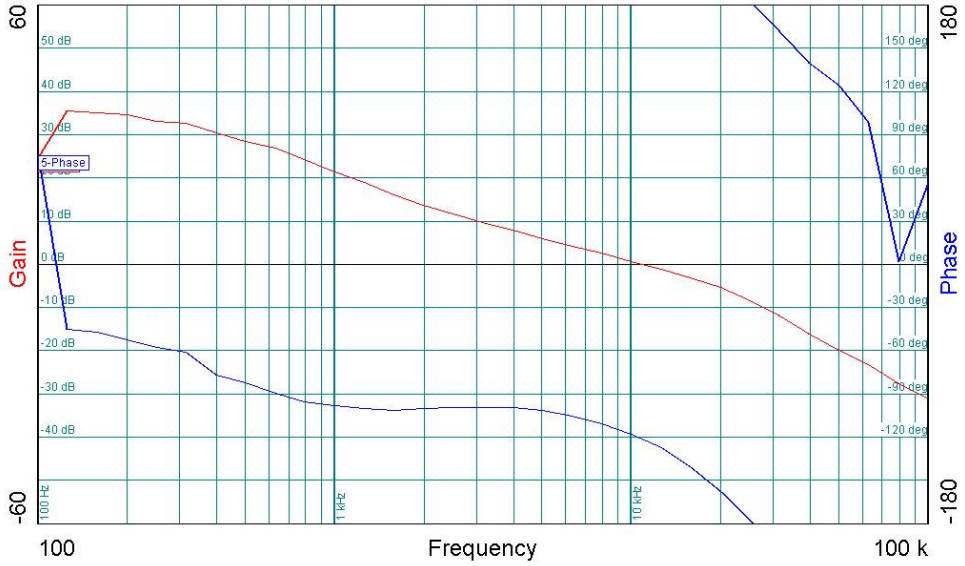

Figure 25 - Gain-Phase Plot, 36 VDC, Maximum Load (2 A).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 10.0 kHz, Phase Margin = 60°

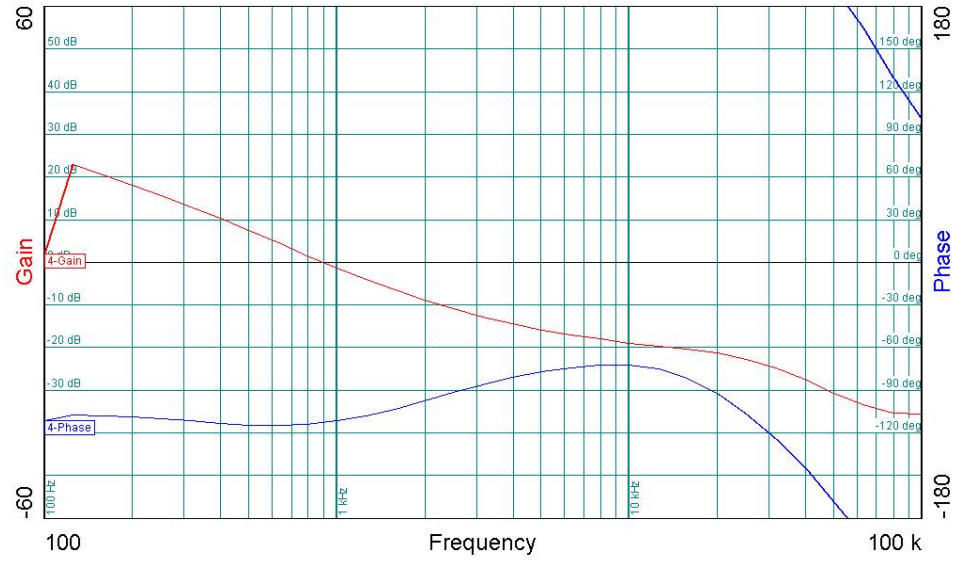

Figure 26 - Gain-Phase Plot, 36 VDC, Light Load (100 mA).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 0.9 kHz, Phase Margin = 65°

12.2 57 VDC Maximum Load

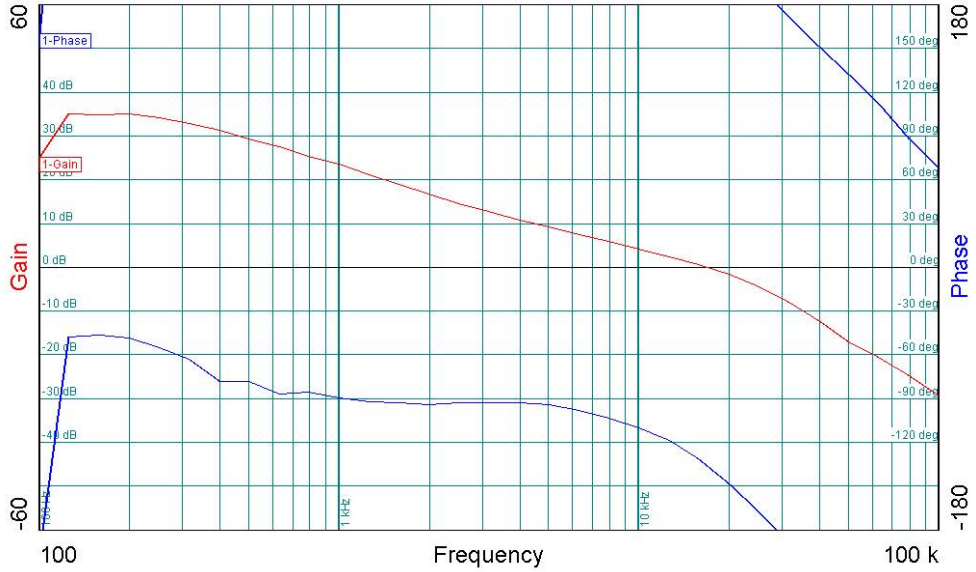

Figure 27 - Gain-Phase Plot, 57 VDC, Light Load (100 mA).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 10.8 kHz, Phase Margin = 40°

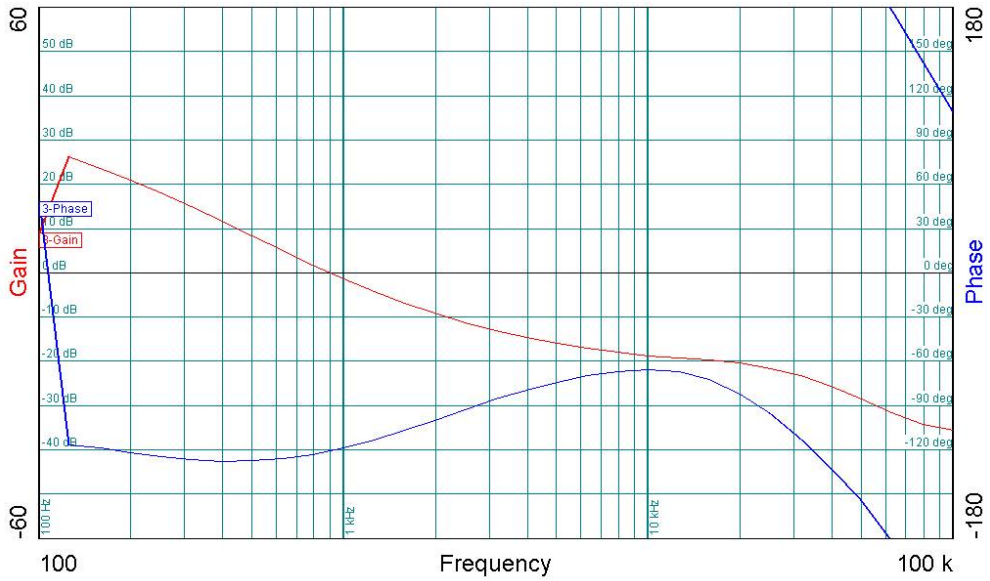

Figure 28 - Gain-Phase Plot, 57 VDC, Light Load (100 mA).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 0.9 kHz, Phase Margin = 60°

The results indicate adequate loop bandwidth and significant gain and phase margin.

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13 Revision History

Date	Author	Revision	Description & changes
25-Feb-04	SH	0.1	First release
02-Mar-04	PV	0.2	Second release after minor edits
15-Mar-04	PV	1.0	Final release
19-Jul-05	PV	1.1	Fixed schematic and bill of materials (BOM)

Notes

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