

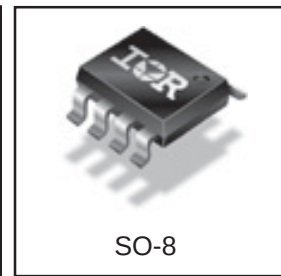
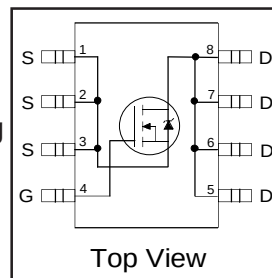
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max (m Ω)	I_D
60V	26@ $V_{GS} = 10V$	4.2A
	30@ $V_{GS} = 4.5V$	3.5A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	7.0	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	5.6	
I_{DM}	Pulsed Drain Current ①	56	
P_D @ $T_A = 25^\circ C$	Power Dissipation④	2.5	W
	Linear Derating Factor	0.02	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ⑥	3.7	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	—	20	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient ④	—	50	

Notes ① through ⑥ are on page 8

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

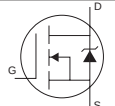
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.065	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	20	26	$m\Omega$	$V_{GS} = 10V, I_D = 4.2A$ ③
		—	23	30		$V_{GS} = 4.5V, I_D = 3.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 48V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	17	—	—	S	$V_{DS} = 50V, I_D = 4.2A$
Q_g	Total Gate Charge	—	21	31	nC	$I_D = 4.2A$
Q_{gs}	Gate-to-Source Charge	—	4.3	—		$V_{DS} = 48V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	9.6	—		$V_{GS} = 4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	7.7	—	ns	$V_{DD} = 30V$
t_r	Rise Time	—	2.6	—		$I_D = 4.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	13	—		$V_{GS} = 10V$ ③
C_{iss}	Input Capacitance	—	1740	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	300	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	37	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	1590	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	220	—		$V_{GS} = 0V, V_{DS} = 48V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	410	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$ ⑤

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	140	mJ
I_{AR}	Avalanche Current①	—	4.2	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	56		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 4.2A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	52	78	ns	$T_J = 25^\circ\text{C}, I_F = 4.2A$
Q_{rr}	Reverse Recovery Charge	—	100	150	nC	$di/dt = 100A/\mu s$ ③

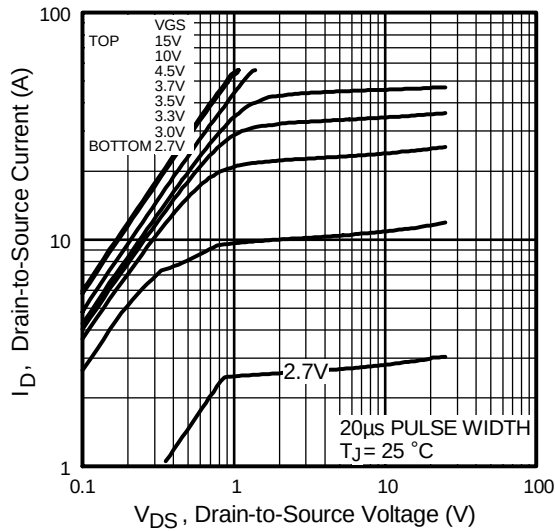


Fig 1. Typical Output Characteristics

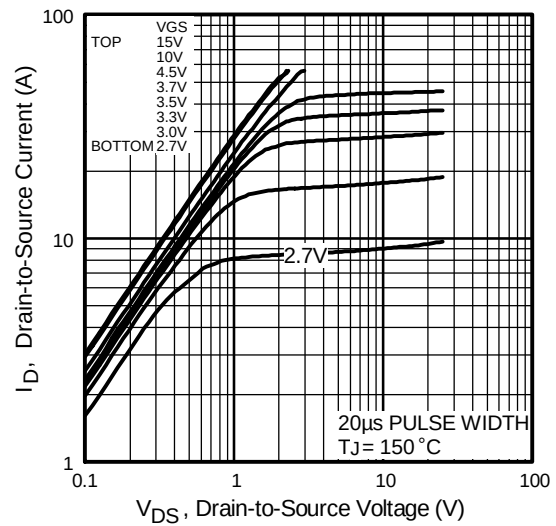


Fig 2. Typical Output Characteristics

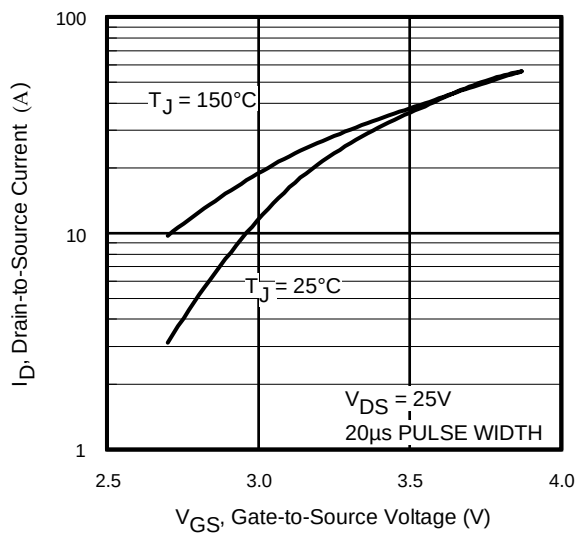


Fig 3. Typical Transfer Characteristics

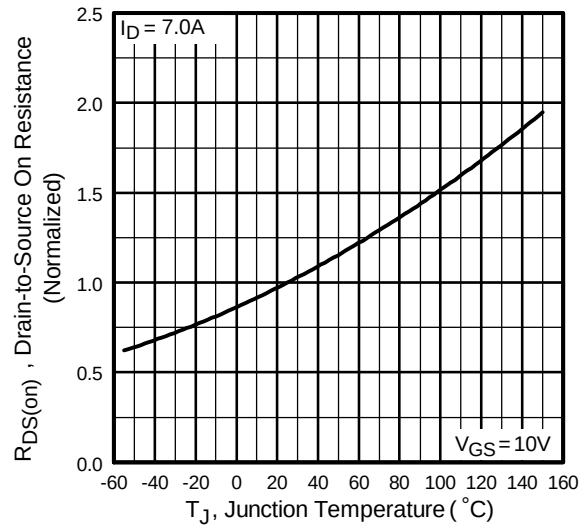
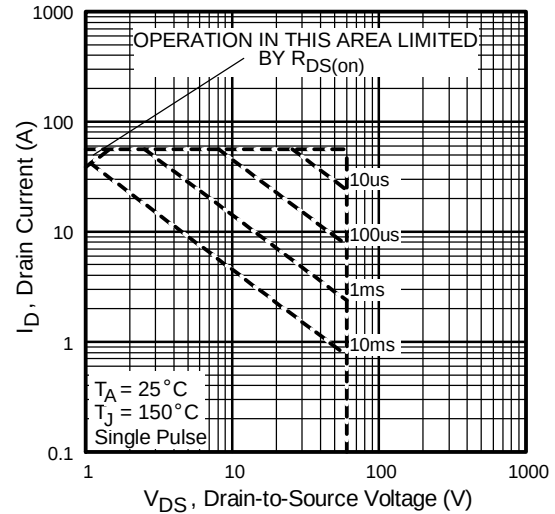
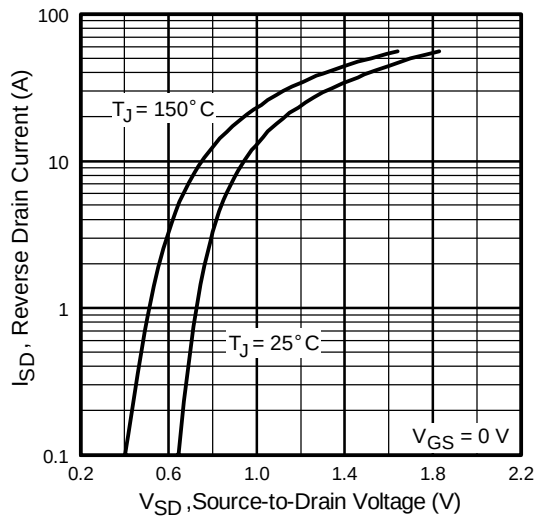
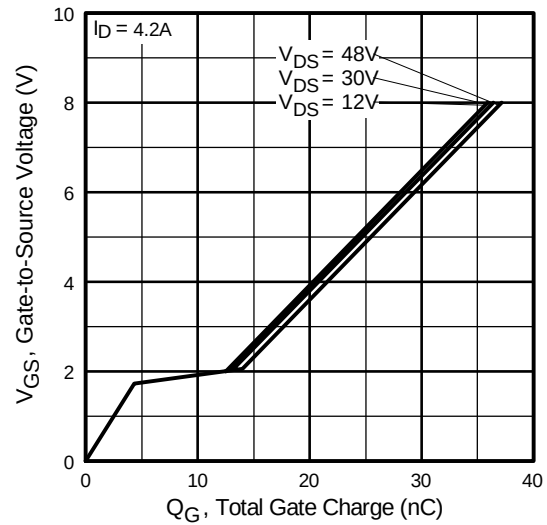
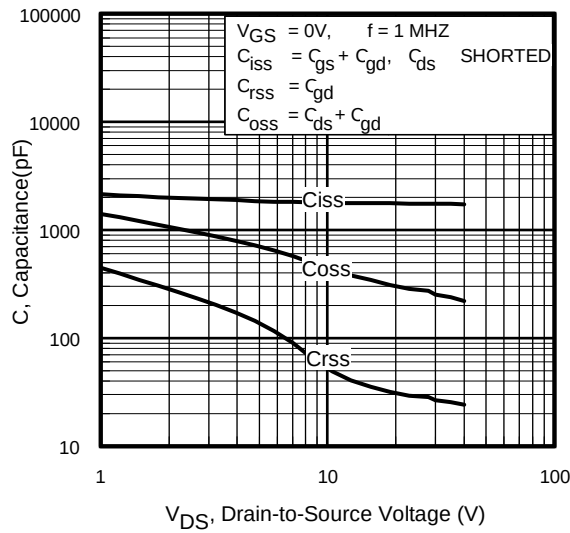


Fig 4. Normalized On-Resistance Vs. Temperature

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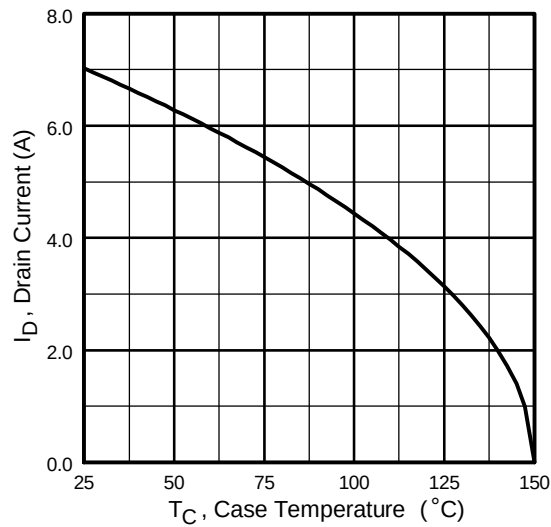


Fig 9. Maximum Drain Current Vs. Ambient Temperature

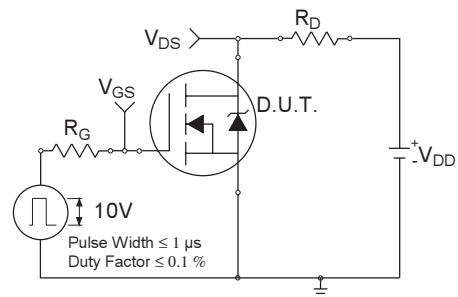


Fig 10a. Switching Time Test Circuit

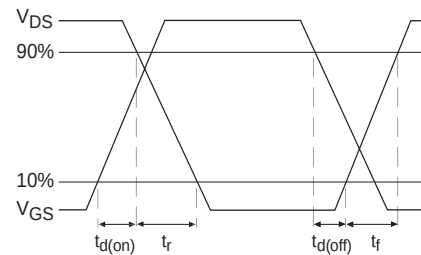


Fig 10b. Switching Time Waveforms

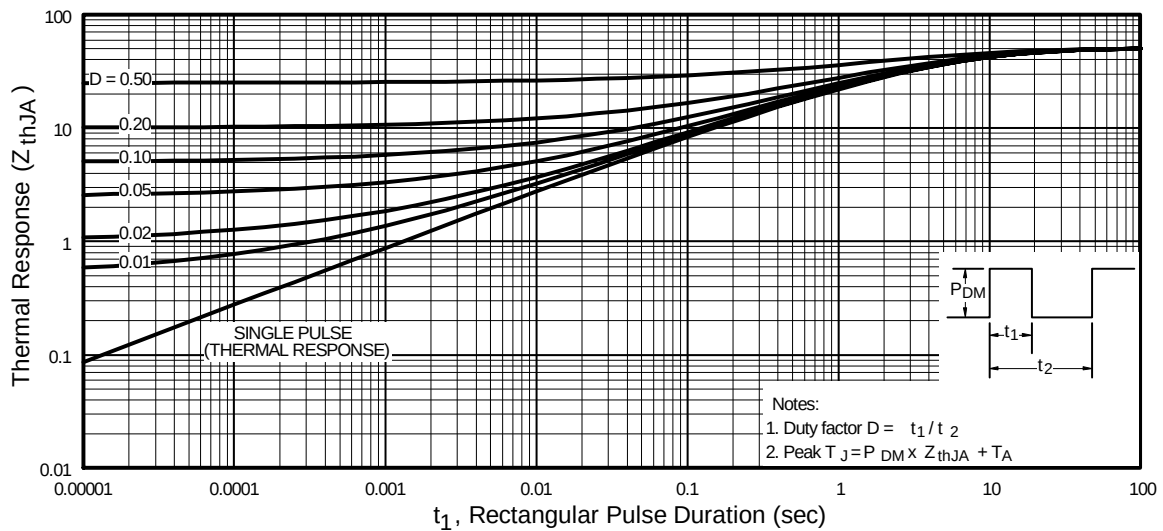


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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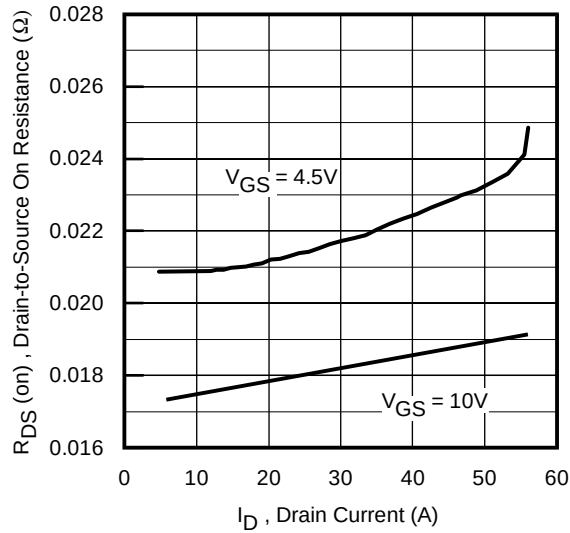


Fig 12. On-Resistance Vs. Drain Current

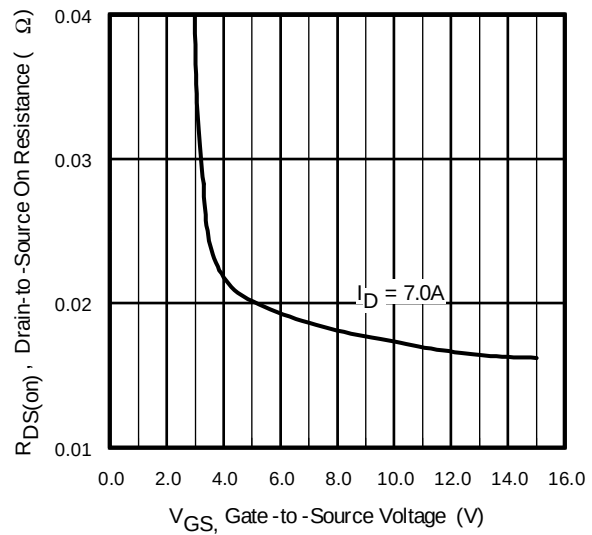


Fig 13. On-Resistance Vs. Gate Voltage

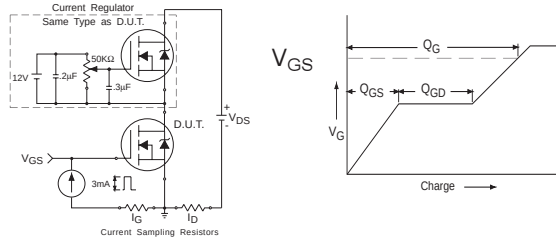


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

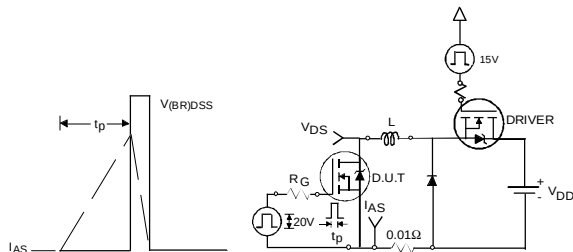


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

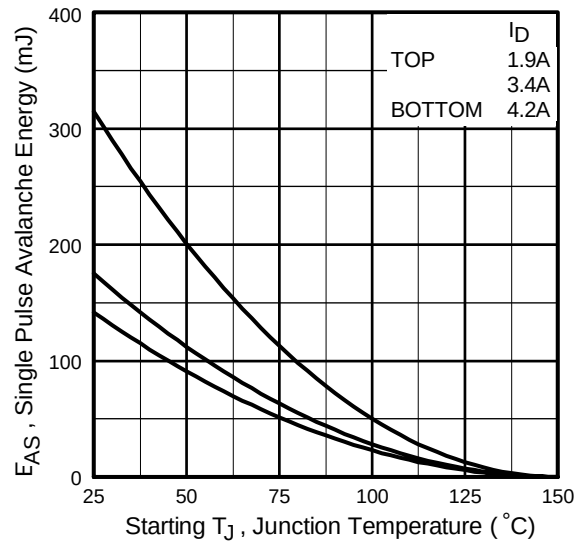
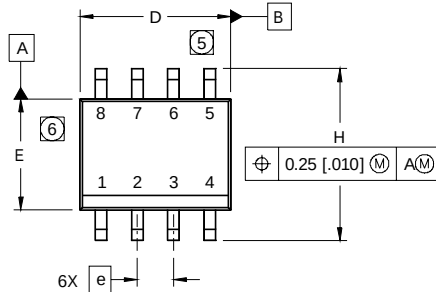


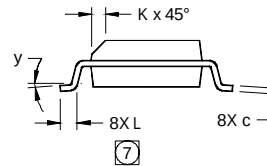
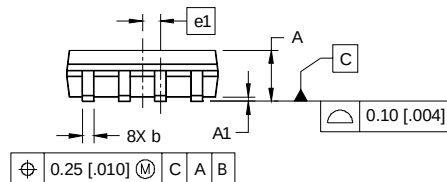
Fig 15c. Maximum Avalanche Energy Vs. Drain Current

SO-8 Package Outline

Dimensions are shown in millimeters (inches)



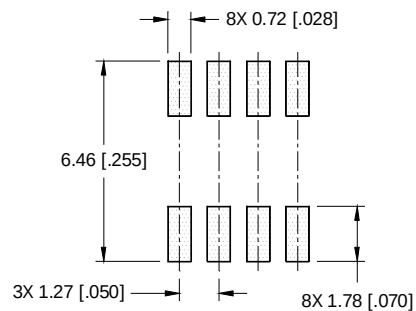
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

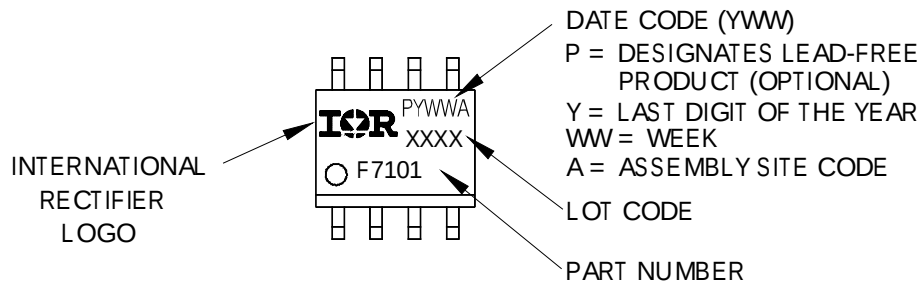
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

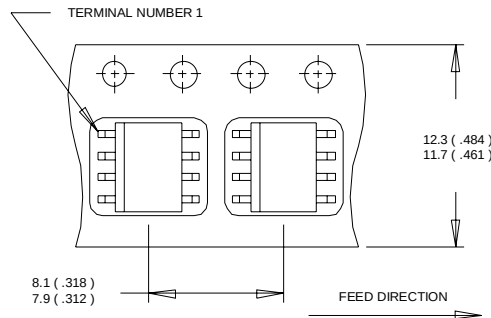


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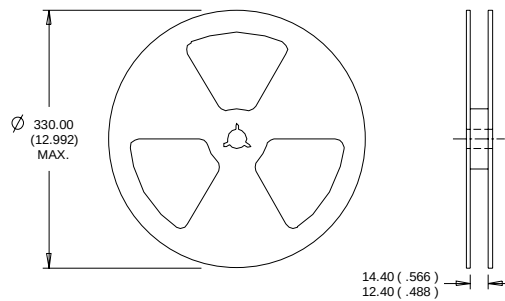
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)

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- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 16\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 4.2\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ $I_{SD} \leq 4.2\text{A}$, $di/dt \leq 160\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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