MOSFET – Power, Dual, N-Channel, for 3-Cells Lithium-ion Battery Protection, WLCSP8

30 V, 2.6 mΩ, 30 A

EFC4C002NL

This N−Channel Power MOSFET is produced using ON Semiconductor's trench technology, which is specifically designed to minimize gate charge and ultra low on resistance.

This device is suitable for applications of Drone or Notebook PC.

Features

- Ultra Low On−Resistance
- Low Gate Charge
- Common−Drain Type
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- 3−Cells Lithium−ion Battery Charging and Discharging Switch

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C (Note 1)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	30	V
Gate to Source Voltage	V_{GSS}	±20	V
Source Current (DC)	I_S	30	A
Source Current (Pulse) PW ≤ 10 μs, Duty Cycle ≤ 1%	I_{SP}	120	A
Total Dissipation (Note 1)	P_T	2.6	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	$R_{\theta JA}$	48	°C/W

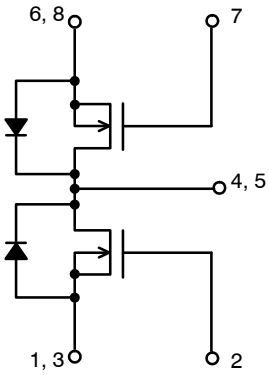
1. Surface mounted on ceramic substrate (5000 $mm^2 \times 0.8$ mm).

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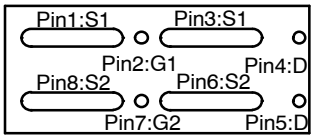
V_{SSS}	$R_{SS(on)}$ Max	I_S Max
30 V	2.6 mΩ @ 10 V	30 A
	3.3 mΩ @ 8 V	
	5.1 mΩ @ 4.5 V	

ELECTRICAL CONNECTION
N−Channel



1. Source 1
2. Gate 1
3. Source 1
4. Drain
5. Drain
6. Source 2
7. Gate 2
8. Source 2

PIN ASSIGNMENT

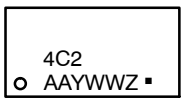


(Bottom View)



WLCSP8
CASE 567MC

MARKING DIAGRAM



4C2 = Specific Device Code
AA = Assembly Location
Y = Year
WW = Work Week
Z = Lot Traceability
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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ELECTRICAL CHARACTERISTICS at T_A = 25°C

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V Test Circuit 1	30			V
Zero−Gate Voltage Source Current	I_{SSS}	V_{SS} = 24 V, V_{GS} = 0 V Test Circuit 1			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{SS} = 0 V Test Circuit 2			200	nA
Gate Threshold Voltage	V_{GS}(th)	V_{SS} = 10 V, I_S = 1 mA Test Circuit 3	1.3		2.2	V
Forward Transconductance	g_{FS}	V_{SS} = 10 V, I_S = 10 A Test Circuit 4		16		S
Static Source to Source On−State Resistance	R_{SS}(on)	V_{GS} = 10 V, I_S = 10 A Test Circuit 5	1.5	2.0	2.6	mΩ
		V_{GS} = 8 V, I_S = 10 A Test Circuit 5	1.6	2.1	3.3	mΩ
		V_{GS} = 4.5 V, I_S = 10 A Test Circuit 5	2.2	2.9	5.1	mΩ
Static Drain to Source On−State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_S = 1 A		10		mΩ
Gate Resistance	R_G			3		Ω
Turn−ON Delay Time	t_d(on)	V_{SS} = 15 V, V_{GS}= 10 V I_S = 10 A Test Circuit 6		40		ns
Rise Time	t_r			750		ns
Turn−OFF Delay Time	t_d(off)			280		ns
Fall Time	t_f			105		ns
Input Capacitance	Ciss	V_{SS} = 15 V, V_{GS}= 0 V, f = 1 MHz		6.200		pF
Total Gate Charge	Qg	V_{SS} = 15 V, V_{GS} = 4.5 V, I_S = 15 A Test Circuit 7		45		nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 10 A, V_{GS} = 0 V Test Circuit 8		0.75	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test circuits are example of measuring FET1 side.

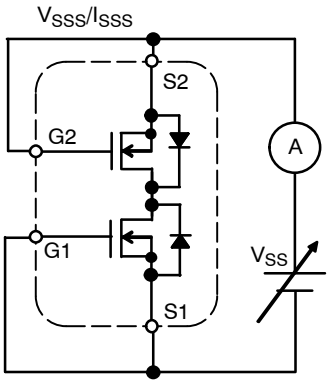
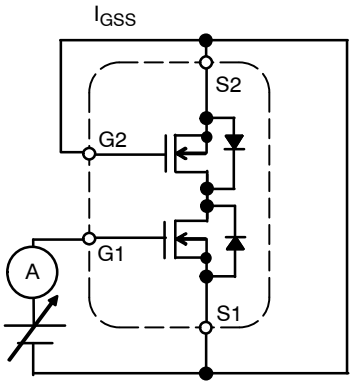
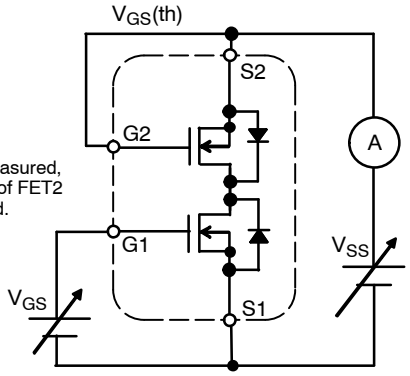


Figure 1. Test Circuit 1



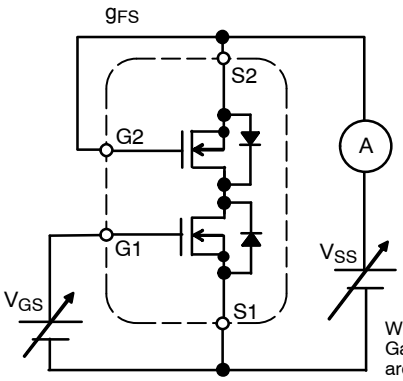
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 2. Test Circuit 2



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 3. Test Circuit 3



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 4. Test Circuit 4

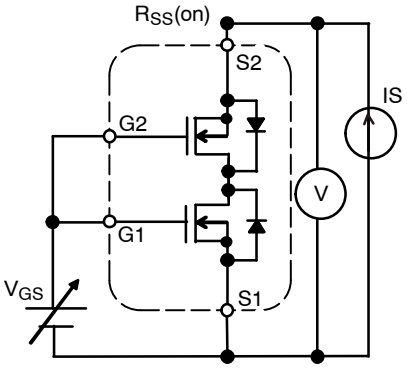
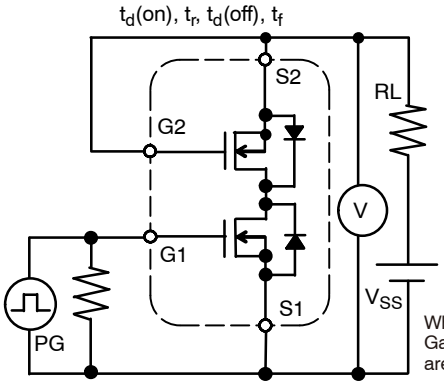
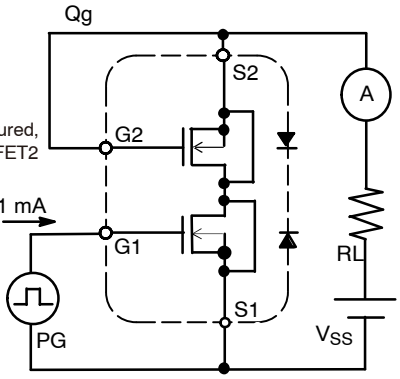


Figure 5. Test Circuit 5



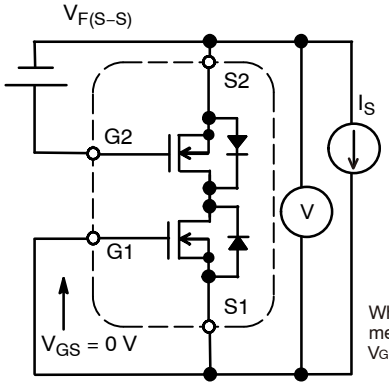
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 6. Test Circuit 6



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 7. Test Circuit 7



When FET1 is measured,+10 V is added to VGS of FET2.

Figure 8. Test Circuit 8

NOTES: When FET2 is measured, the position of FET1 and FET2 is switched.

TYPICAL CHARACTERISTICS

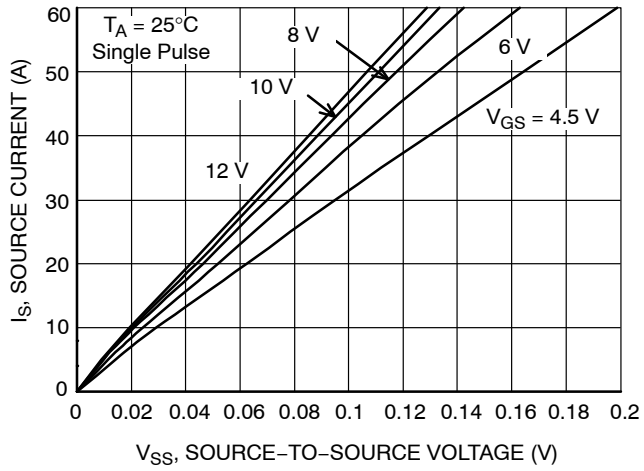


Figure 9. On−Region Characteristics

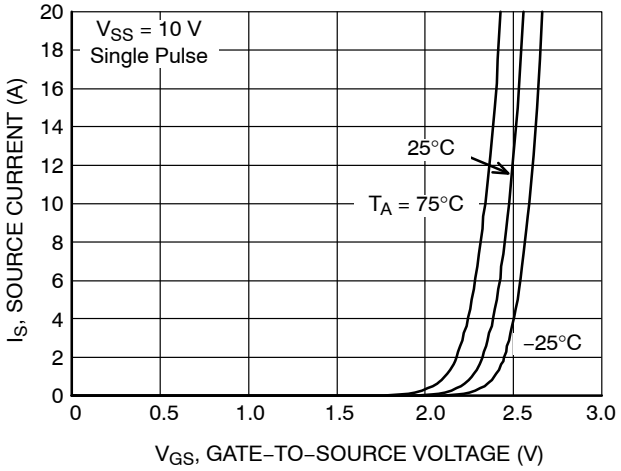


Figure 10. Transfer Characteristics

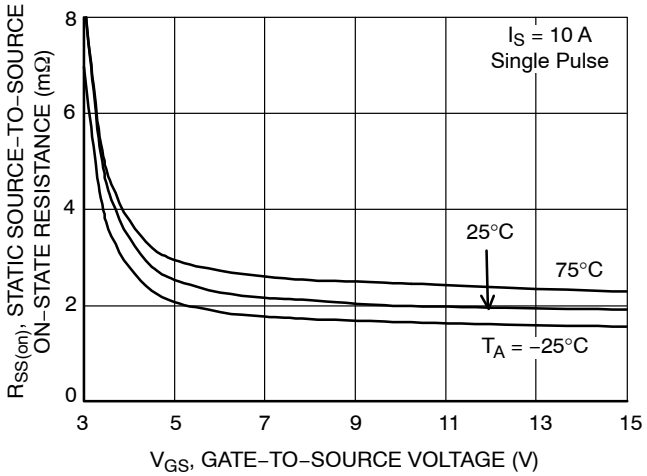


Figure 11. On−Resistance vs. Gate−to−Source Voltage

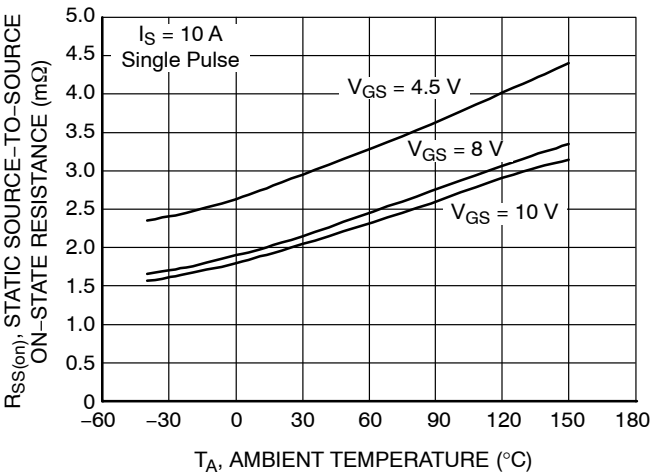


Figure 12. On−Resistance vs. Temperature

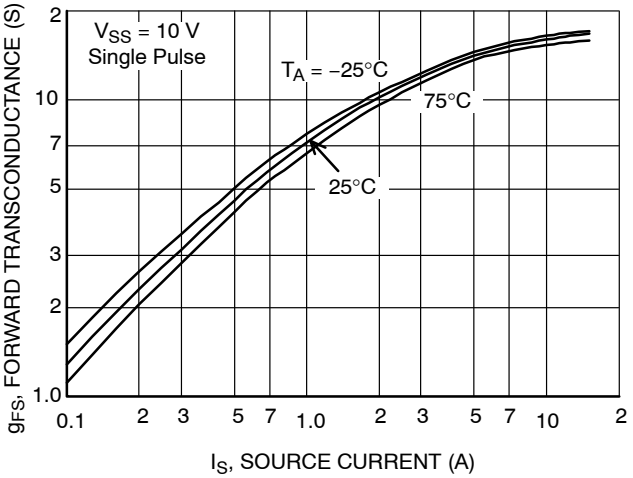


Figure 13. Forward Transconductance vs. Current

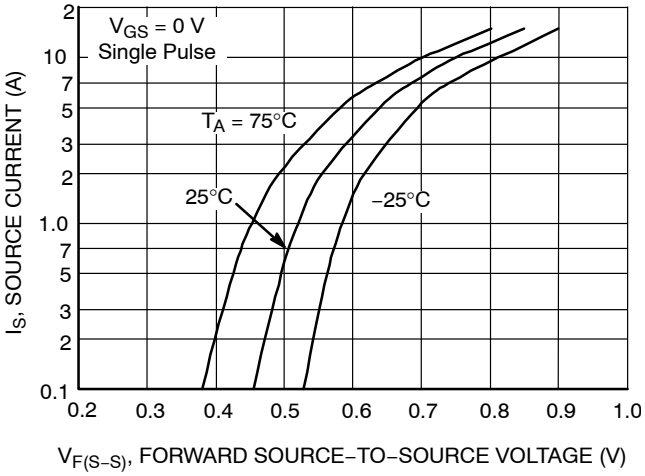


Figure 14. Forward Source−to−Source Voltage vs. Current

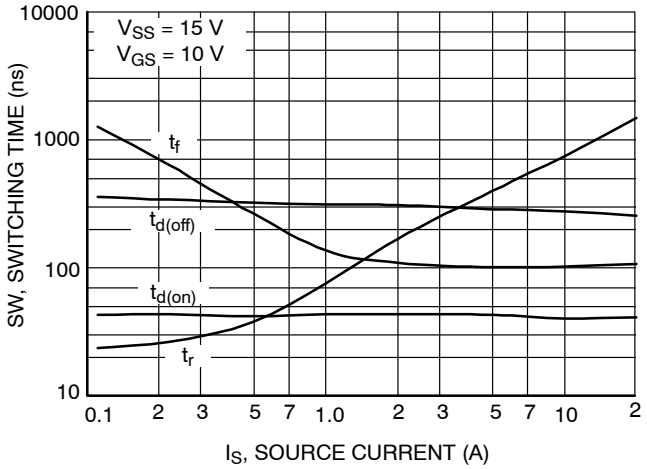


Figure 15. Switching Time vs. Current

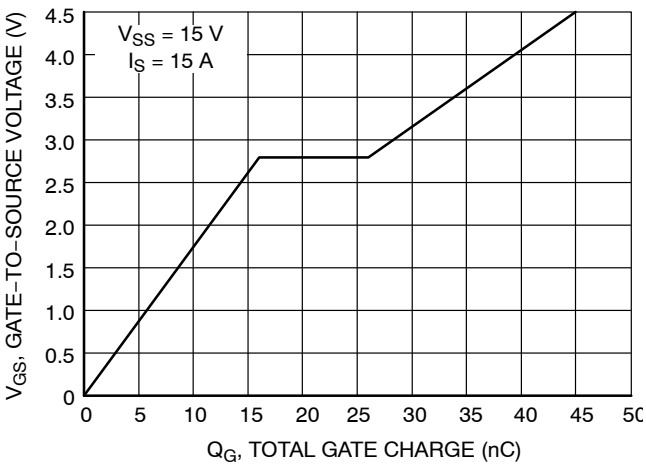


Figure 16. Gate−to−Source Voltage vs. Total Gate Charge

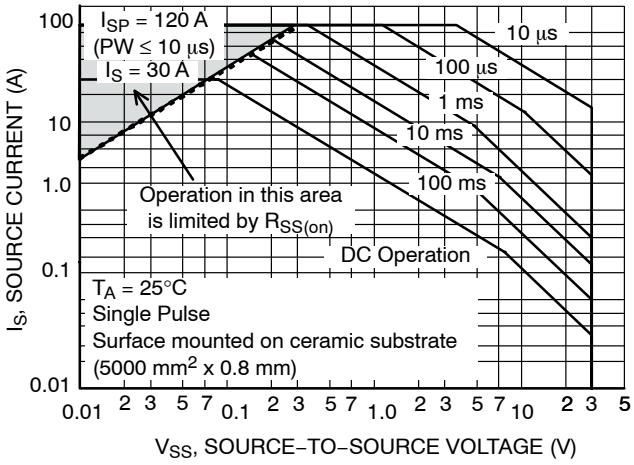


Figure 17. Safe Operating Area

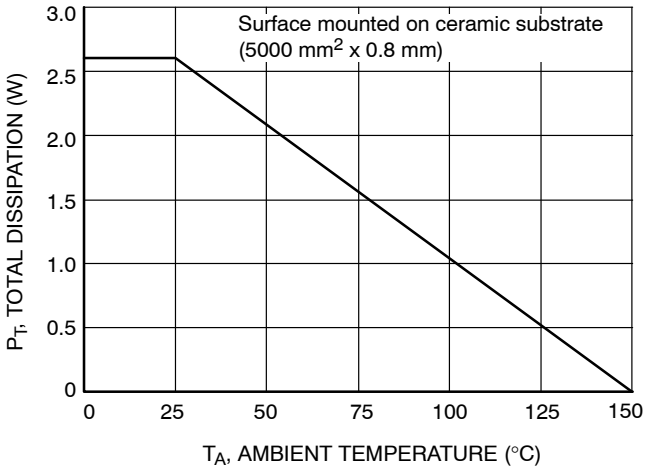


Figure 18. Total Dissipation vs. Temperature

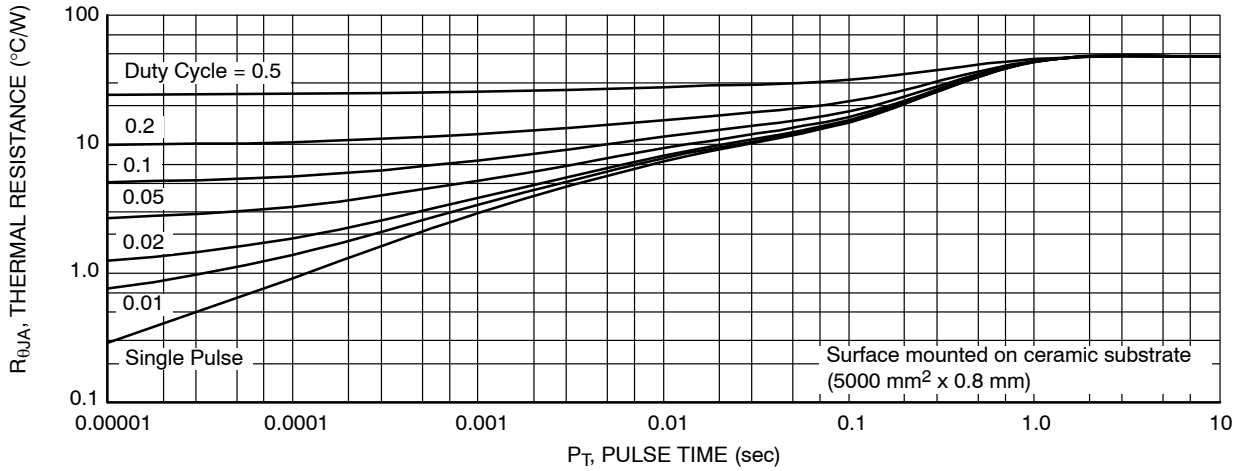


Figure 19. Thermal Response

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)†
EFC4C002NLTDG	NP	WLCSP8 6.00x2.50 (Pb−Free / Halogen Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

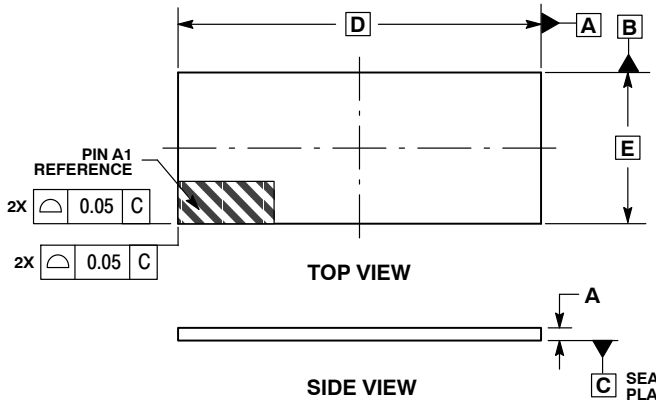
ON Semiconductor®



SCALE 2:1

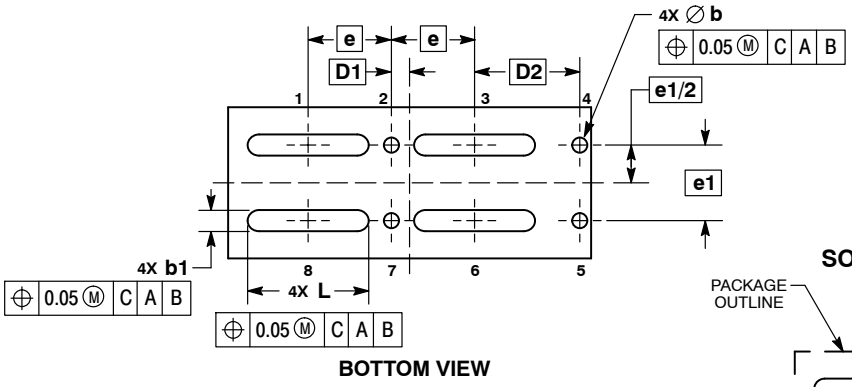
WLCSP8, 6.00x2.50 / EFCP6025−8EGJ−021
CASE 567MC
ISSUE O

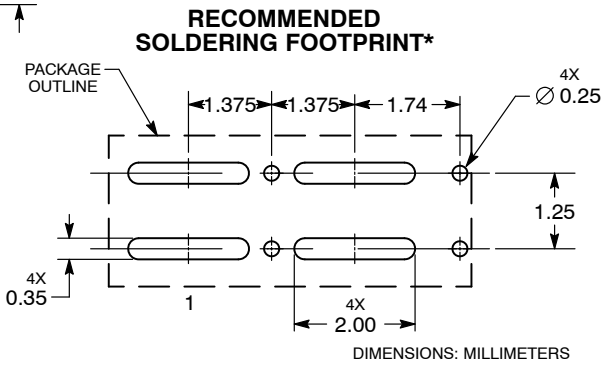
DATE 22 JUL 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.19	0.23
b	0.22	0.28
b1	0.32	0.38
D	5.95	6.05
D1	0.305 BSC	
D2	1.740 BSC	
E	2.45	2.55
e	1.375 BSC	
e1	1.25 BSC	
L	1.97	2.03





*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP8, 6.00X2.50 / EFCP6025−8EGJ−021**		**PAGE 1 OF 1**

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