EBL4600CL-EVALZ: QLx4600-SL30 Evaluation Board User Guide

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Introduction

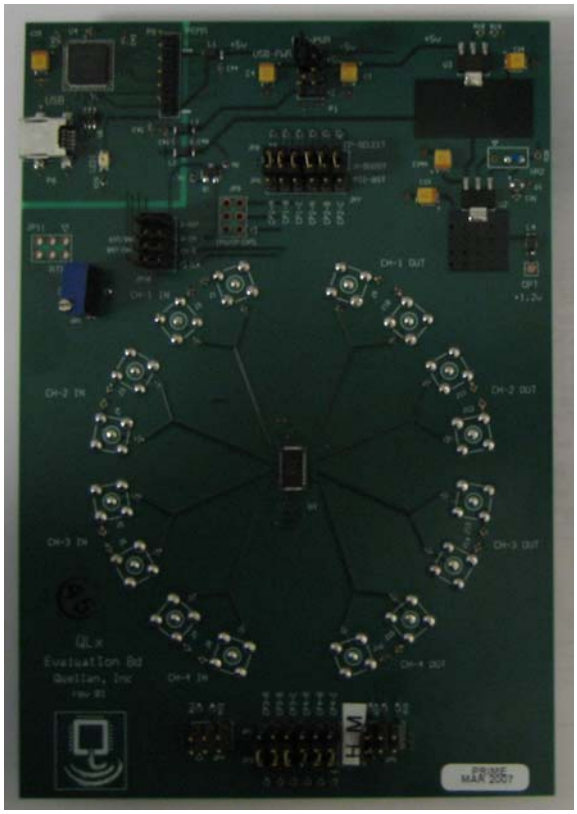
The QLx4600-SL30 Lane Extender Evaluation Board is a versatile stand-alone card developed to evaluate the performance of Intersil QLx4600-SL30 Series Quad Equalizer.

Evaluation Kit Includes:

- EBL4600CL-EVALZ evaluation board
- Power cable

Key Features

- QLx4600-SL30 series IC
- Single 5V external power supply
- On-board regulators provide all voltages required for MCU and IC operation
- On-board DC/DC converter that provides the 1.2V supply to the IC
- Optional on-board boost selection for each channel via two sets of headers
- Adjustable Detection Threshold for quiescent modes
- 8 sets of SMA connectors for high speed signals input and output



Operation of Evaluation Board

After a brief description of the board design and layout, the different features and options to operate the board are highlighted.

- Providing power to the board through an external supply
- The eight high speed differential I/O
- The Loss of Signal (LOS) function
- The variable Detection Threshold
- Controling the equalizer boost via Control Pins

QLx4600-SL30 Evaluation Board

The QLx4600-SL30 Evaluation Board is a 4-layer, 4”(w)x5.6”(h)x0.059”(t) in dimension, and fabricated with (Allied-Signal) FR-408 dielectric material. 100Ω differential signal traces are laid out with 0.0062” width and 0.0058” spacing. 50Ω single-ended traces are 0.009” wide. Figure 1 shows the top view of the board.

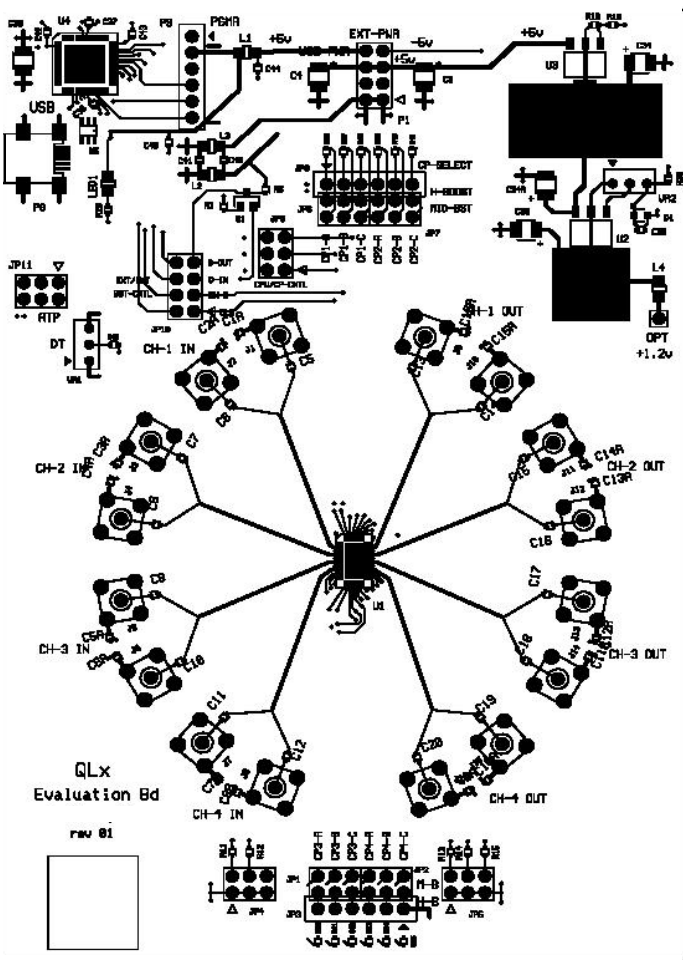


FIGURE 1. QLx4600-SL30 EVALUATION BOARD PCB

Power Supply

Power can be supplied to the board by using an external power supply. On board voltage regulators supply the appropriate 1.2V to the QLx4600-SL30 IC.

PROVIDING POWER FROM EXTERNAL 5V POWER SUPPLY

The evaluation board can also be powered by an independent external 5.0V power supply via header P1 as highlighted on Figure 2. The maximum current consumption for the board including the voltage regulators, microcontroller circuits, and the IC together is approximately 245mA with all channels active.

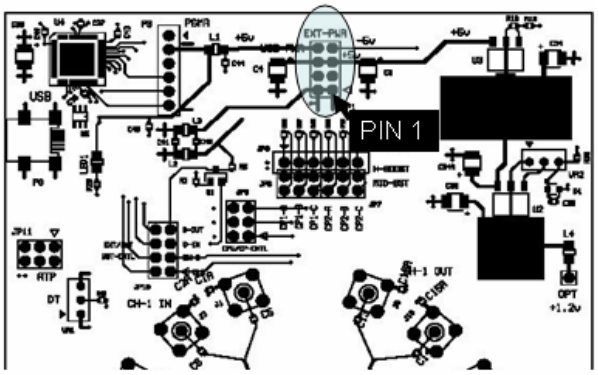


FIGURE 2. QLx4600-SL30 EVALUATION BOARD EXTERNAL POWER SUPPLY POWER CONNECTOR

Table 1 provides description of the connector P1. A power cable is provided with the evaluation kit.

TABLE 1. P1 CONNECTOR DESCRIPTION

8 – NC	7 – NC
6 – 5.0V	5 – 5.0V
4 – NC	3 – NC
2 – GND	1 – GND

High Speed Data_I/O Interface Connectors

There are sixteen SMA connectors on the board, eight for the CML differential inputs and eight for the CML differential outputs. All the connections from the SMA connectors to the QLx4600-SL30 Series chip are AC-coupled with a 220nF broad band capacitor. Figure 3 shows each channel by their name, direction, and their polarities.

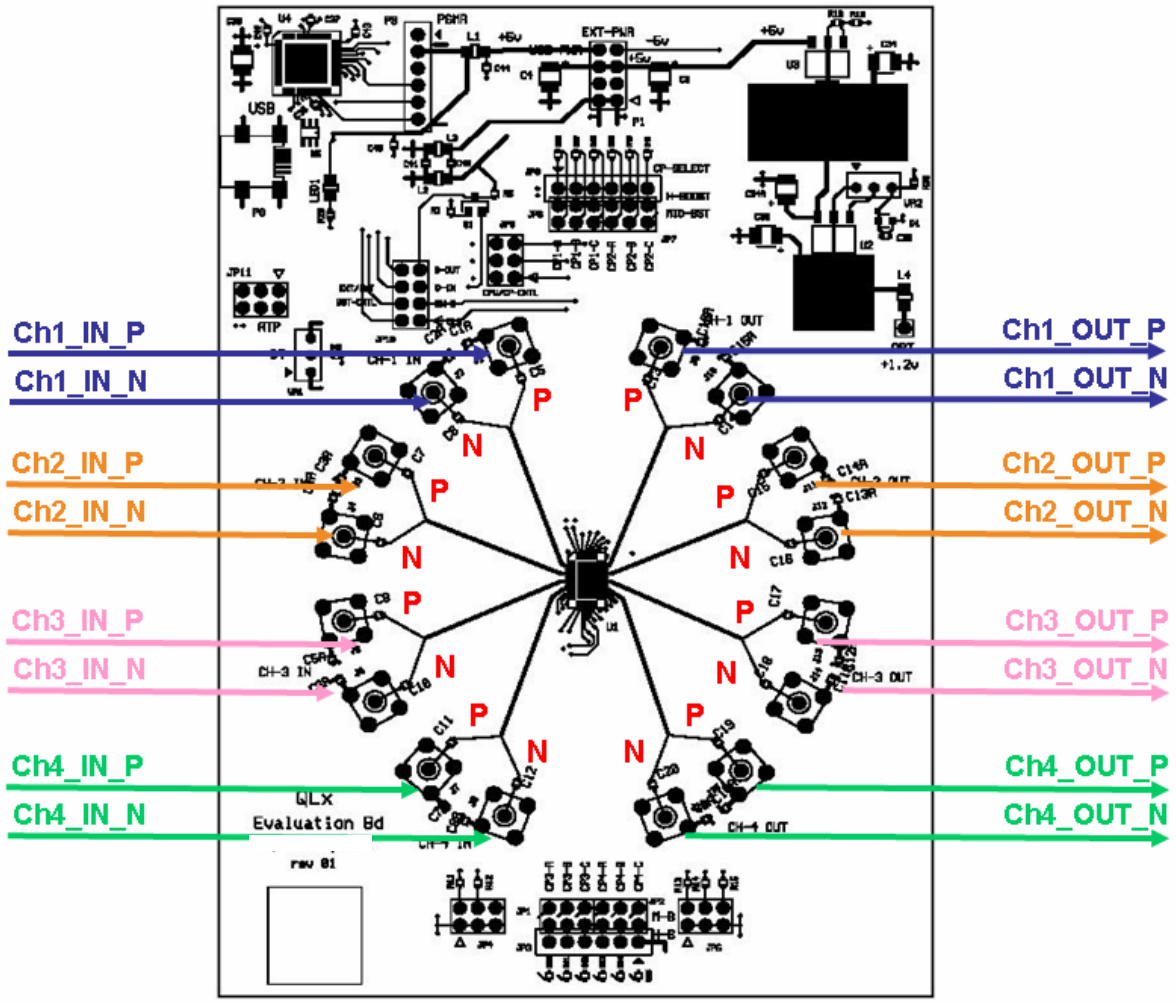


FIGURE 3. QLx4600-SL30 EVALUATION BOARD RF-I/O INTERFACE

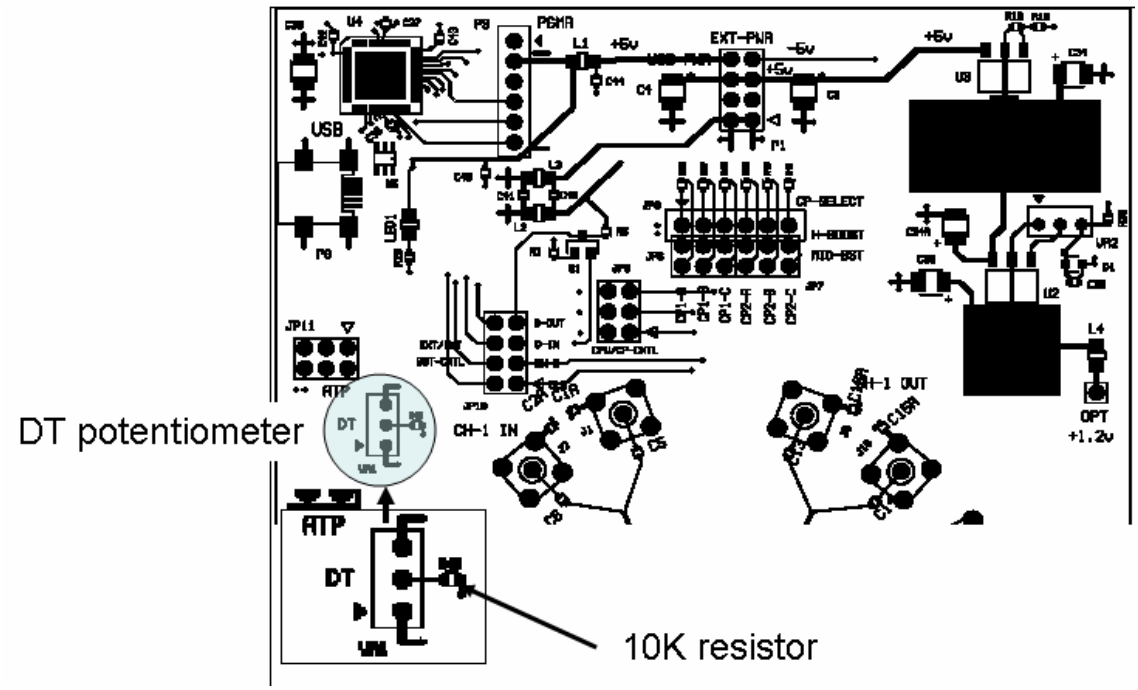


FIGURE 4. QLx4600-SL30 EVALUATION BOARD DT POTENTIOMETER

Detection Threshold (DT)

The DT is another very important feature of the QLx4600-SL30 Series IC. On the evaluation board, the DT can be changed by adjusting the potentiometer VR1 (Figure 4).

In normal operation, the potentiometer should be set so that the voltage across the adjacent 10k resistor is 0V.

For applications that need to adjust this level it can be simply done by changing the potentiometer and reading the voltage across the 10k resistor in order to infer the current coming from the DT pin.

For example, measuring a voltage of -200mV across the 10k resistor indicates a 20µA current from the DT pin.

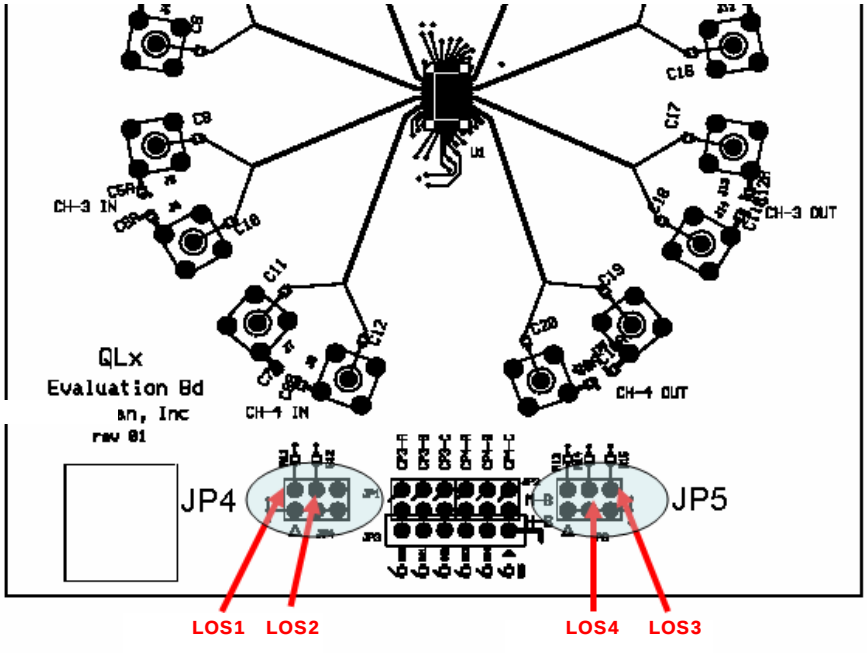


FIGURE 5. QLx4600-SL30 EVALUATION BOARD LOSS OF SIGNAL

Loss of Signal (LOS)

TABLE 2. DESCRIBES JP4 AND JP5 CONNECTIVITY

JP4		
2- LOS1	4- LOS2	6- GND
1- GND	3- GND	5- GND

JP5		
2- Mode	4- LOS4	6- LOS3
1- GND	3- GND	5- GND

Two 3x2 headers, JP4 and JP5, provide interfaces to the Loss Of Signal (LOS) pins of the QLx4600-SL30 IC. With this function the user can know when the output of the equalizer is ON or OFF. When the output is ON the LOS pin is LOW (GND). When the output is OFF the LOS pin is HIGH (1.2V). A separate LOS is accessible for each of the 4 equalizer channels. Figure 5 illustrates where the different LOS signals can be accessed on the evaluation board. Table 2 describes specifically the connectivity of headers JP4 and JP5.

Boost Setting Control Pins

In order to enable boost setting control via Control Pins, JP5-pin2 must be jumpered to ground.

The boost setting configuration (compensation setting) for each individual equalizer channel is done through a 3x3 header. There are four sets of headers, one for each equalizer channel. Figure 6 illustrates the location of the headers.

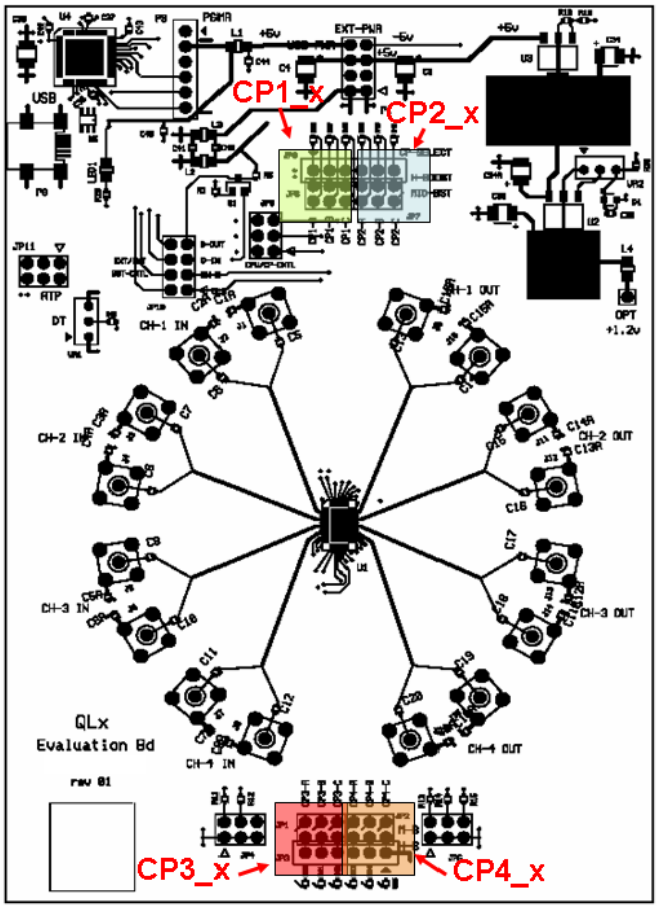


FIGURE 6. EQUALIZER BOOST CONTROL HEADERS

The notation CP[1-4]_[A – C] refers to the QLx4600-SL30 quad equalizer CPs. They are associated with the 4 channels 3-digit number where ‘A’ is the MSB and ‘C’ is the LSB. Table 3 describes the relationship between the CPs and the equalizer boost setting. Bit A can only take one of two values, either Low (L) or High (H), while bit B and C can take one of three values, Low (L), Middle (M) and High (H). Hence eighteen of the thirty-two different boost levels are accessible through the CPs for each equalizer channel.

TABLE 3. CP AND EQUALIZER BOOST SETTING RELATIONSHIP

CP[1-4]_A	CP[1-4]_B	CP[1-4]_C	BOOST
L	L	L	0
L	L	M	2
L	L	H	4
L	M	L	6
L	M	M	8
L	M	H	10
L	H	L	12
L	H	M	14
L	H	H	15
H	L	L	16
H	L	M	17
H	L	H	19
H	M	L	21
H	M	M	23
H	M	H	24
H	H	L	26
H	H	M	28
H	H	H	31

For channels 1 and 2, the headers JP6-8 are used to set the CPs. High state is achieved by placing a jumper between the top two pins of the header and the middle state is achieved by placing a jumper between the bottom two pins. Low state is simply achieved by using no jumper at all. Figure 7 illustrates how one could set the CPs for a QLx4600-SL30 Series IC boost value of 21 (H,M,L) on channel 1 and a boost of 16 (H,L,L) on channel 2.

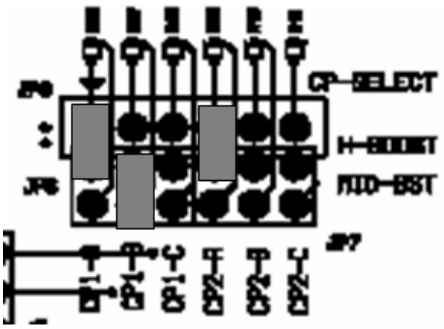


FIGURE 7. ILLUSTRATION OF SETTINGS FOR CP1 = (H,M,L) AND CP2 = (H,L,L)

For channels 3 and 4, we use headers JP1-3 in a similar fashion except High is achieved using the bottom two pins and middle is achieved by using the top two pins. Figure 9 illustrates how one could set the CPs for a boost value of 18 (H,L,M) on channel 3 and a value of 14 (L,H,M) on channel 4.

On Figure 8 please also note how pin 2 on JP5 is jumpered to ground in order to enable the CP control feature.

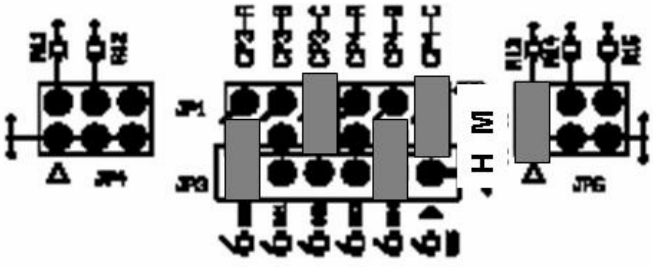


FIGURE 8. ILLUSTRATION OF SETTINGS FOR CP3 = (H,L,M) AND CP4 = (L,H,M)

Evaluation Board Schematic

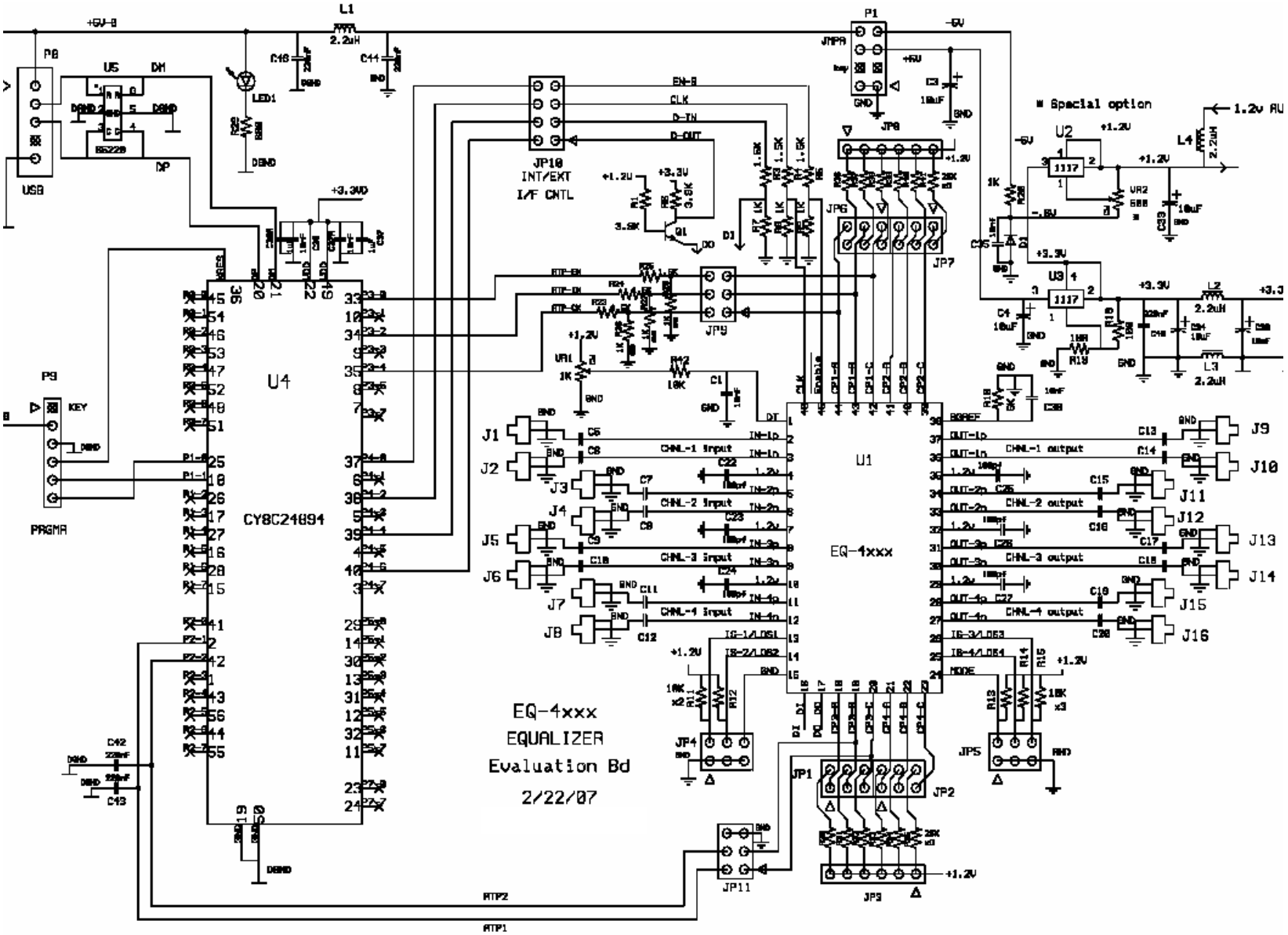


FIGURE 9. SCHEMATIC OF THE QLx4600-SL30 EVALUATION BOARD

QLx4600-SL30 Bill of Materials

Ref Des	Description	Part No. (Digikey)	Qty	25 Brd Qty	Notes
C-1,37,38	10nF	PCC103BQCT-ND	5	125	Do not install C-35
C-35,36	10nf/1uf doublestack	PCC103BQCT-ND / PCC2268CT-ND	2 / 2	50 / 50	
C-22 ~ 27	100pF	PCC101CQCT-ND	6	150	
C-3,4,33,34,34a,39	10uF TANT CAP	478-1673-1-ND	6	150	
C-40,41,42,43,44,46	220nF	PCC2272CT-ND	6	150	
C-5 ~ 20	DLI + 220nF double-stack	P42BN820Z5S (DLI)/ PCC2272CT-ND	16 / 16	400 / 400	
C1A~C16A	10nF	PCC103BQCT-ND	16	400	
D-1	SMD DIODE	Install 0 ohm 0603, P0.0GCT-ND	1	25	Real P/N MAJ11600LCT-ND
J-1 ~ 16	SMA FLUSH MNT	A24691-ND	16	400	
JP-1,2,4,5,6,7,9,11	2x3 HDR	WM26806-ND	6	150	Do not istall JP-9 and JP-11
JP-10, P-1	2x4 HDR	WM26808-ND	2	50	
JP-3, JP-8, P-9	1x6	WM6506-ND	2	50	
L-1,2,3,4	1206 SMD IND	LQH31CN2R2M03L (Murata)	4	100	
L-5,6	BEAD	do not install	2	50	
LED-1	1206 LED	350-1566-1-ND	1	25	
P-8	USB CONN	H2959CT-ND	1	25	
Q1	NPN XSISTOR	2SC248000LCT-ND	1	25	
R-1,6	3.9K	P3.9KJCT-ND	2	50	
R-10	6K	P6.04KLCT-ND	1	25	
R-11 ~ 15	10K	311-10.0KLRCT-ND	5	125	
R-18	100	311-100JRCT-ND	1	25	
R-29	680 ohm	P680JCT-ND	1	25	
R-3,4,5,23,24,25	1.5K	P1.5KJCT-ND	6	150	
R-30 ~ 41	25K	541-25.5KLCT-ND	12	300	
R-42	10K	P10KJCT-ND	1	25	
R-7,8,9,20,26,27,28	1K	RHM1.00KLCT-ND	6	150	Do not install R-20
R-19	180	P180JCT-ND	1	25	
U-1	EQ-4xxx	Quellan Part - do not install	1	25	
U-2,3	LM-1117 VOLT REG	LM1117MP-ADJCT-ND	2	50	
U-4	CY8C24894 MCU	CY8C24894-24LFXI (Cypress)	1	25	
U-5	65220 ESD	296-9694-1-ND	1	25	
VR-1	1K TRIM POT	CT94EW102-ND	1	25	
VR-2	500 TRIM POT	CT94EW501-ND	1	25	Do not install. Short two "outboard pads"

About Q:ACTIVE®

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.