EL8176

Micropower Single Supply Rail-to-Rail Input/Output Precision Op Amp

FN7436
Rev 9.00
January 6, 2015

The EL8176 is a precision low power, operational amplifier. The device is optimized for single supply operation between 2.4V to 5.5V.

The EL8176 draws minimal supply current while meeting excellent DC-accuracy noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micropower supply current.

The EL8176 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

Features

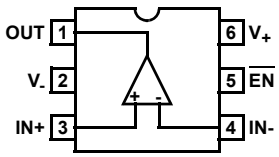
- 55µA supply current
- 100µV max offset voltage (8 Ld SO)
- 2nA input bias current
- 400kHz gain-bandwidth product
- Single supply operation down to 2.4V
- Rail-to-rail input and output
- Output sources 31mA and sinks 26mA load current
- Pb-free (RoHS compliant)

Applications

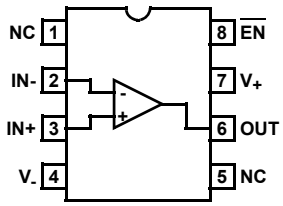
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre amps
- pH probe amplifiers

Pin Configurations

EL8176
(6 LD SOT-23)
TOP VIEW

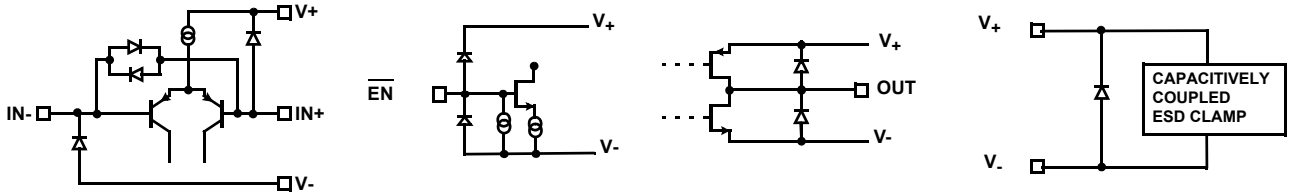


EL8176
(8 LD SO)
TOP VIEW



Pin Descriptions

SO PIN NUMBER	SOT-23 PIN NUMBER	PIN NAME	Equivalent Circuit	DESCRIPTION
1, 5		NC		No internal connection
2	4	IN-	Circuit 1	Amplifier's inverting input
3	3	IN+	Circuit 1	Amplifier's non-inverting input
4	2	V-	Circuit 4	Negative power supply
6	1	OUT	Circuit 3	Amplifier's output
7	6	V+	Circuit 4	Positive power supply
8	5	$\overline{EN}$	Circuit 2	Amplifier's enable pin with internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state.



CIRCUIT 1 CIRCUIT 2 CIRCUIT 3 CIRCUIT 4

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
EL8176FSZ	8176FSZ	8 Ld SO	M8.15E
EL8176FSZ-T7 (Note 1)	8176FSZ	8 Ld SO	M8.15E
EL8176FWZ-T7 (Note 1, 4)	BBVA	6 Ld SOT-23	P6.064A
EL8176FWZ-T7A (Note 1, 4)	BBVA	6 Ld SOT-23	P6.064A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for EL8176. For more information on MSL, please see tech brief TB363.
4. The part marking is located on the bottom of the parts.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S) and Power-up Ramp Rate 5.75V, 1V/µs
Differential Input Voltage 0.5V
Current into IN+, IN-, and $\overline{EN}$ 5mA
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Tolerance
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
6 Ld SOT-23 Package	230
8 Ld SO Package	125

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, V_{EN} = 0V, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage	8 Ld SO	-100	±25	100	µV
			-220		**220**	µV
		6 Ld SOT-23	-350	±80	350	µV
			-350		**350**	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			2.4		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			0.7		µV/°C
I_{OS}	Input Offset Current		-1	±0.4	1	nA
			-4		**4**	nA
I_B	Input Bias Current		-2	±0.5	2	nA
			-5		**5**	nA
CMIR	Input Voltage Range	Guaranteed by CMRR test	0		5	V
CMRR	Common-mode Rejection Ratio	V_{CM} = 0V to 5V	90	110		dB
			90			dB
PSRR	Power Supply Rejection Ratio	V_S = 2.4V to 5.5V	90	110		dB
			90			dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	200	500		V/mV
			200			V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		25		V/mV
V_{OUT}	Maximum Output Voltage Swing	VOL; Output low, R_L = 100kΩ		3	8	mV
					10	mV
		VOL; Output low, R_L = 1kΩ		130	200	mV
					300	mV
		VOH; Output high, R_L = 100kΩ	4.994	4.997		V
			4.992			V
		VOH; Output high, R_L = 1kΩ	4.750	4.867		V
			4.7			V
$I_{S, ON}$	Supply Current, Enabled	V_{EN} = 5V	35	55	75	µA
			30		**90**	µA
$I_{S, OFF}$	Supply Current, Disabled	V_{EN} = 0V		3	10	µA
					10	µA

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, V_{EN} = 0V, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
I_O+	Short Circuit Output Sourcing Current	R_L = 10Ω	18	31		mA
			18			mA
I_O-	Short Circuit Output Sinking Current	R_L = 10Ω	17	26		mA
			15			mA
V_S	Supply Voltage	Guaranteed by PSRR test	2.4		5.5	V
			2.4		**5.5**	V
V_{INH}	Enable Pin High Level		2			V
V_{INL}	Enable Pin Low Level				0.8	V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V	0.25	0.7	2.0	µA
					2.5	µA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V	-0.5	0	+0.5	µA
			-1		**+1**	µA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	A_V = 100, R_f = 100kΩ, R_L = 10kΩ, R_g = 1kΩ to V_{CM}		400		kHz
Unity Gain Bandwidth	-3dB Bandwidth	A_V = 1, R_f = 0Ω, R_L = 100kΩ to V_{CM}, V_{OUT} = 10mV_{P-P}		1		MHz
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz, R_L = 10kΩ to V_{CM}		1.5		µV_{P-P}
	Input Noise Voltage Density	f_O = 1kHz		28		nV/√Hz
i_N	Input Noise Current Density	f_O = 1kHz		0.16		pA/√Hz
ISO	Off-State Input to Output Isolation	V_{EN} = 5V, f_O = 1kHz, A_V = +1, V_{IN} = 1V_{P-P}		-73		dB
CMRR	Input Common Mode Rejection Ratio	f_O = 120Hz; V_{CM} = 1V_{P-P}		-70		dB
PSRR+	Power Supply Rejection Ratio (V_+)	f_O = 120Hz; V_+, V_- = ±2.5V, V_{SOURCE} = 1V_{P-P}		-90		dB
PSRR-	Power Supply Rejection Ratio (V_-)	f_O = 120Hz; V_+, V_- = ±2.5V, V_{SOURCE} = 1V_{P-P}		-70		dB
TRANSIENT RESPONSE						
SR	Slew Rate		**±0.065**	±0.13	**±0.3**	V/µs
t_r, t_f, Large Signal	Rise Time, 10% to 90%, V_{OUT}	A_V = +2, V_{OUT} = 2V_{P-P}, R_g = R_f = R_L = 10kΩ to V_{CM}		18		µs
	Fall Time, 90% to 10%, V_{OUT}	A_V = +2, V_{OUT} = 2V_{P-P}, R_g = R_f = R_L = 10kΩ to V_{CM}		19		µs
t_r, t_f, Small Signal	Rise Time, 10% to 90%, V_{OUT}	A_V = +2, V_{OUT} = 10mV_{P-P}, R_g = R_f = R_L = 10kΩ to V_{CM}		2.4		µs
	Fall Time, 90% to 10%, V_{OUT}	A_V = +2, V_{OUT} = 10mV_{P-P}, R_g = R_f = R_L = 10kΩ to V_{CM}		2.4		µs
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}	$V_{\overline{EN}}$ = 5V to 0V, A_V = +2, R_g = R_f = R_L = 10kΩ to V_{CM}		4		µs
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}	$V_{\overline{EN}}$ = 0V to 5V, A_V = +2, R_g = R_f = R_L = 10kΩ to V_{CM}		0.1		µs

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

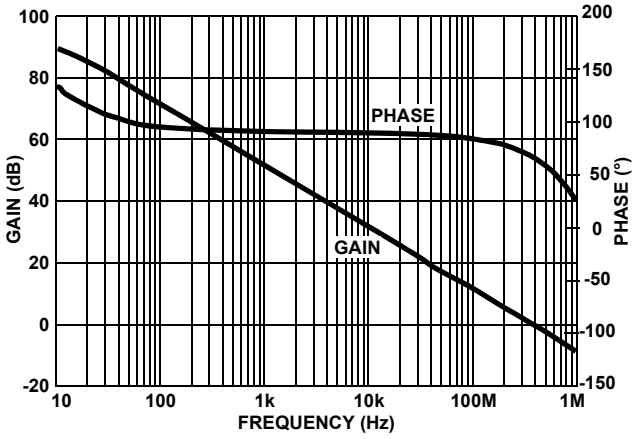


FIGURE 1. A_{VOL} vs FREQUENCY AT 1kΩ LOAD

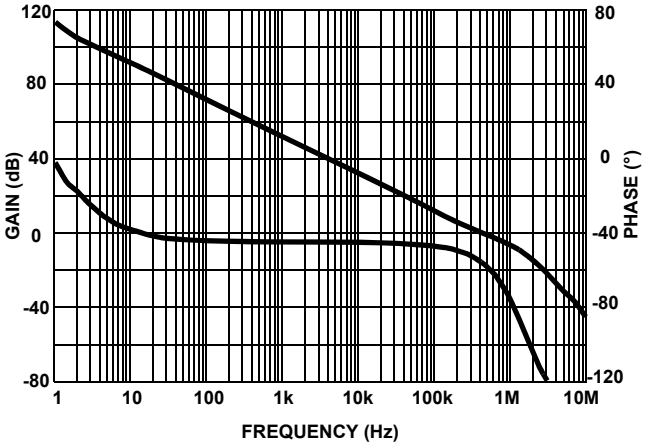


FIGURE 2. A_{VOL} vs FREQUENCY AT 100kΩ LOAD

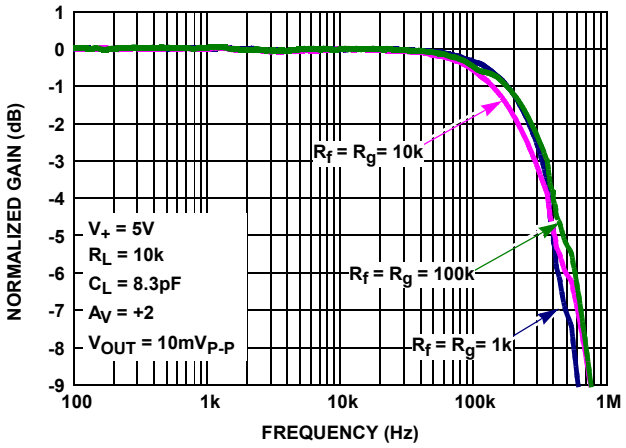


FIGURE 3. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

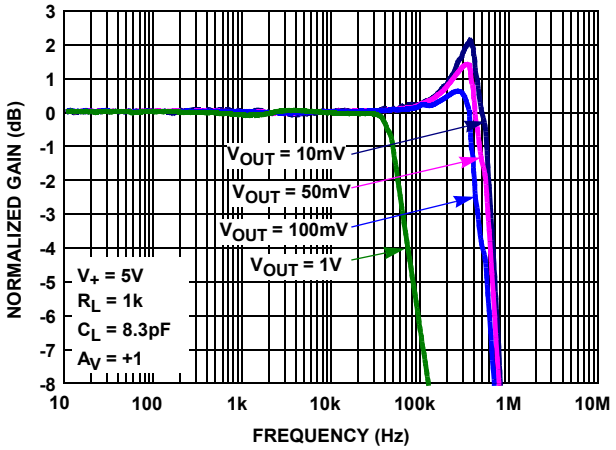


FIGURE 4. GAIN vs FREQUENCY vs V_{OUT}, R_L = 1k

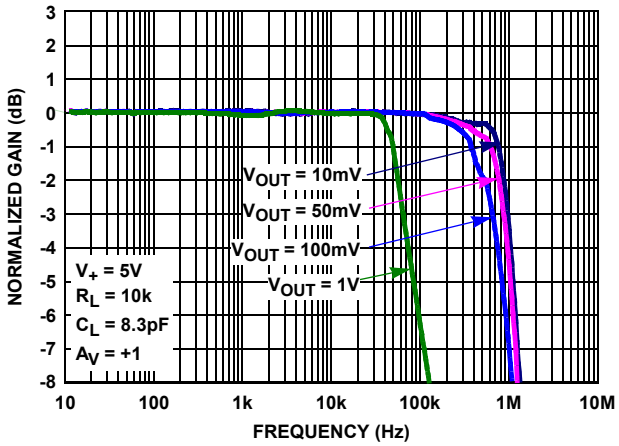


FIGURE 5. GAIN vs FREQUENCY vs V_{OUT}, R_L = 10k

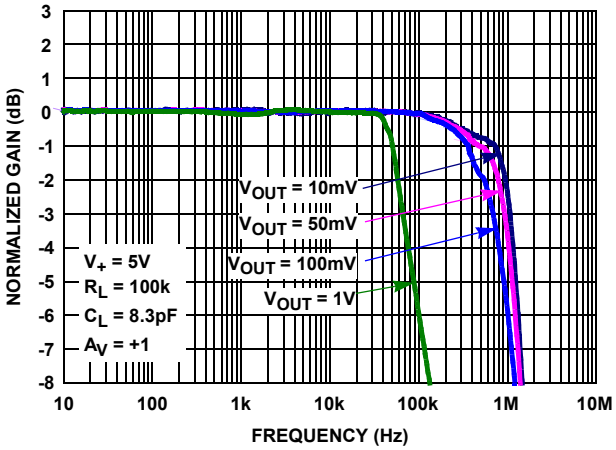


FIGURE 6. GAIN vs FREQUENCY vs V_{OUT}, R_L = 100k

Typical Performance Curves (Continued)

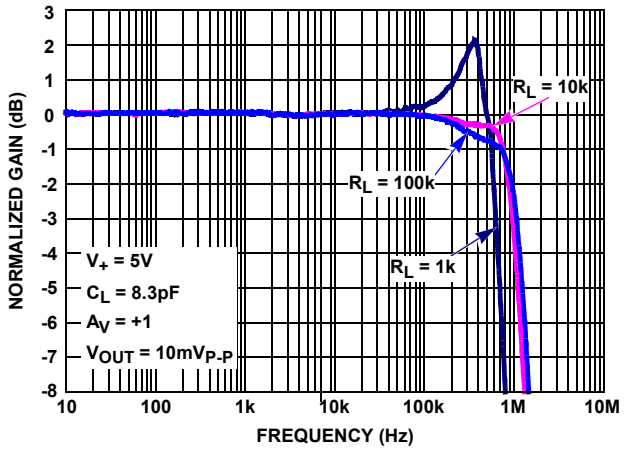


FIGURE 7. GAIN vs FREQUENCY vs R_L

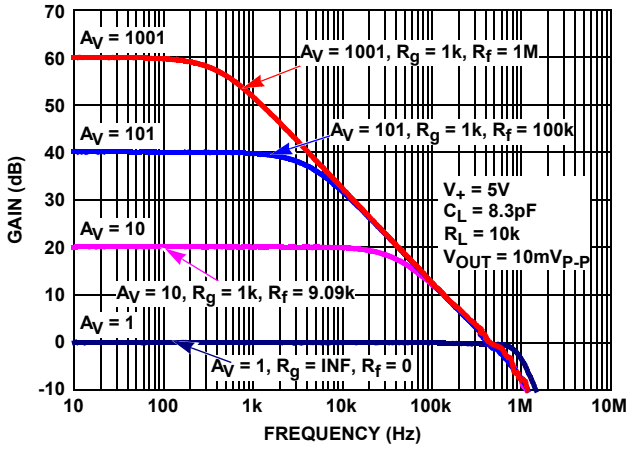


FIGURE 8. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

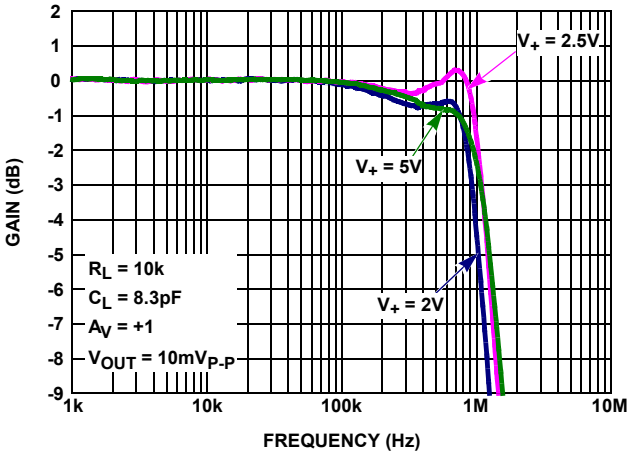


FIGURE 9. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

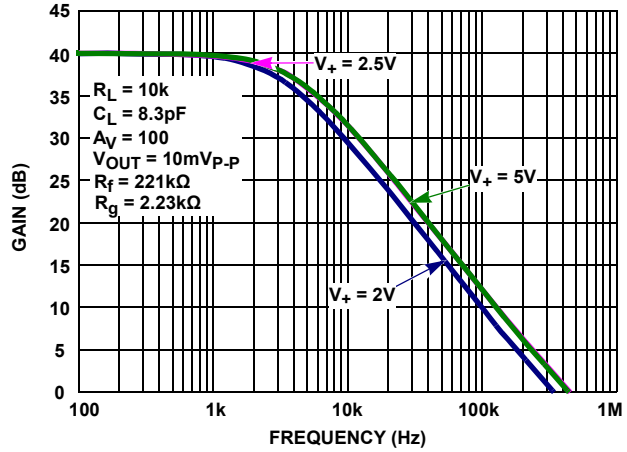


FIGURE 10. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

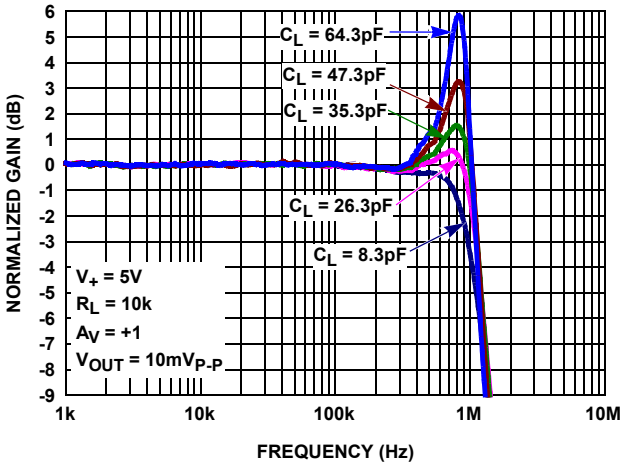


FIGURE 11. GAIN vs FREQUENCY vs C_L

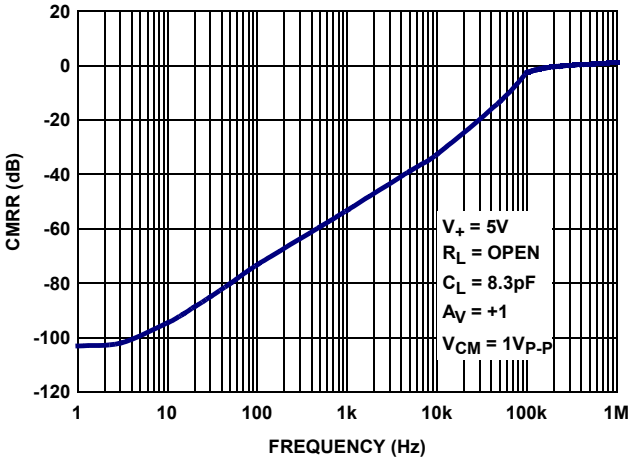


FIGURE 12. CMRR vs FREQUENCY; V_+, V_- = ±2.5V

Typical Performance Curves (Continued)

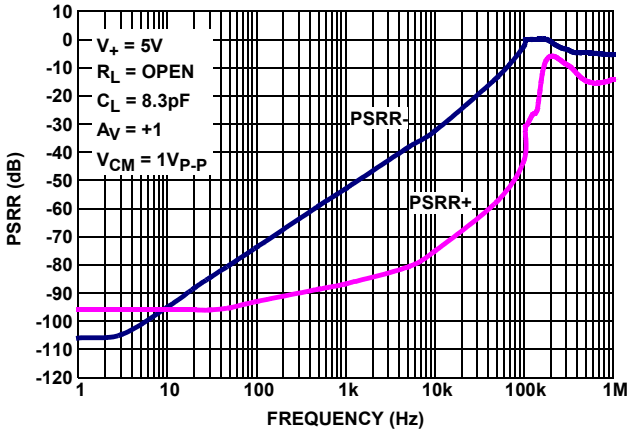


FIGURE 13. PSRR vs FREQUENCY, V_+, V_- = ±2.5V

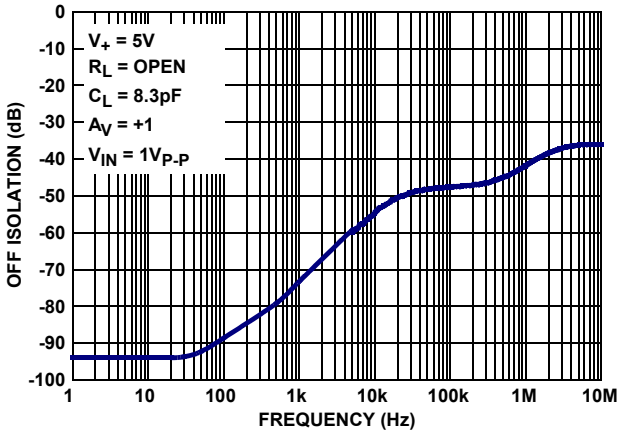


FIGURE 14. OFF ISOLATION vs FREQUENCY; V_+, V_- = ±2.5V

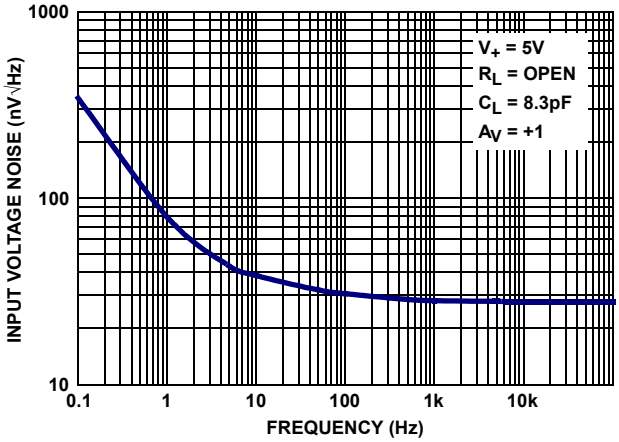


FIGURE 15. INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

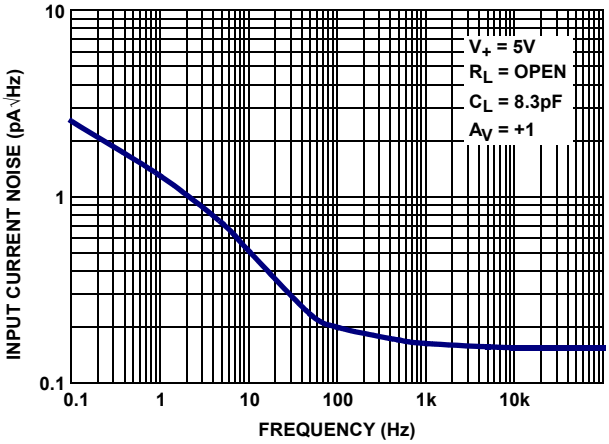


FIGURE 16. INPUT CURRENT NOISE DENSITY vs FREQUENCY

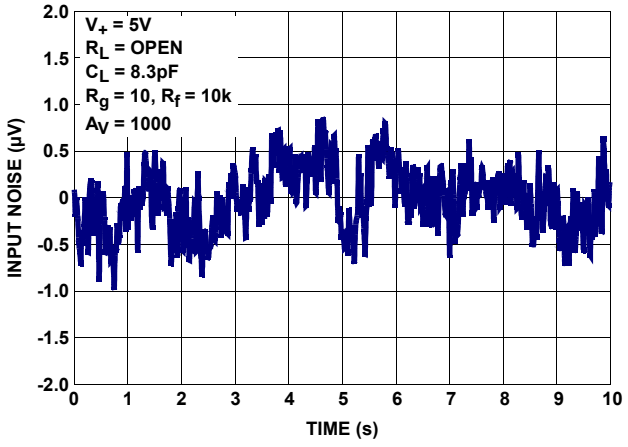


FIGURE 17. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz

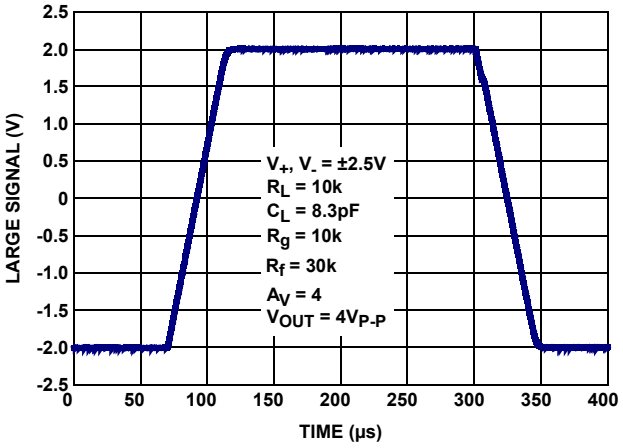


FIGURE 18. LARGE SIGNAL STEP RESPONSE

Typical Performance Curves (Continued)

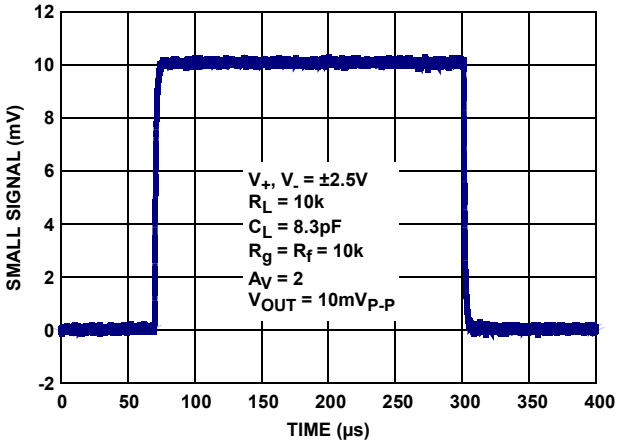


FIGURE 19. SMALL SIGNAL STEP RESPONSE

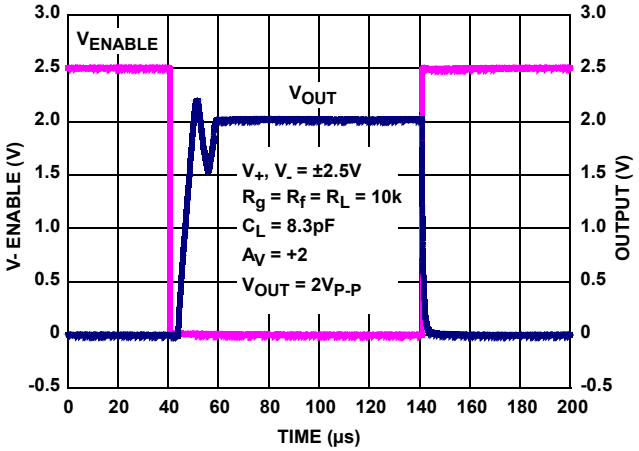


FIGURE 20. ENABLE TO OUTPUT RESPONSE

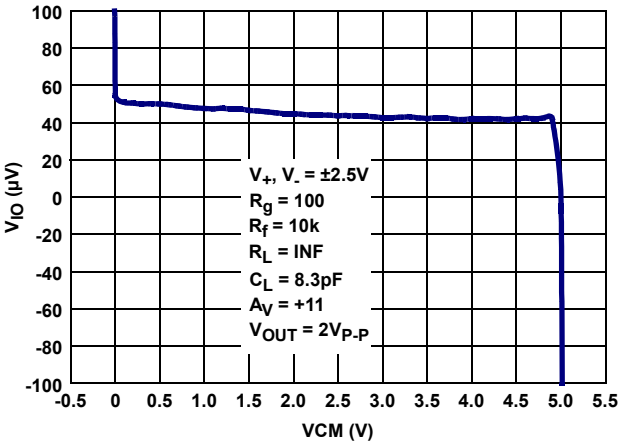


FIGURE 21. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

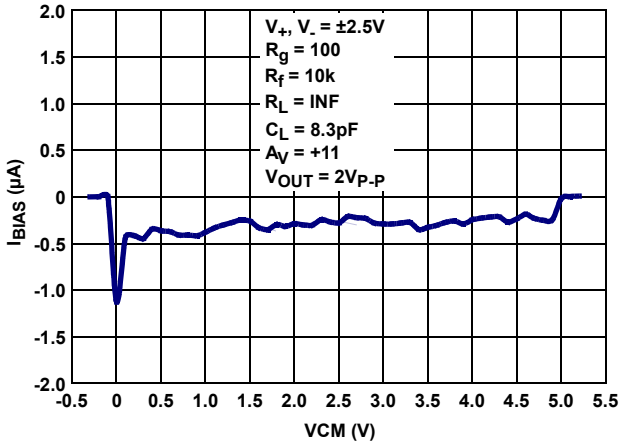


FIGURE 22. INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

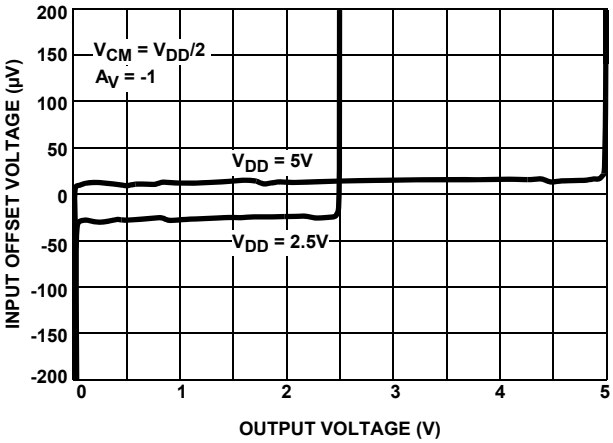


FIGURE 23. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

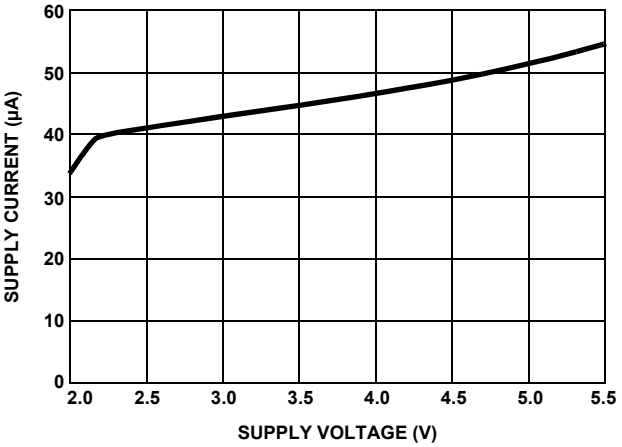


FIGURE 24. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

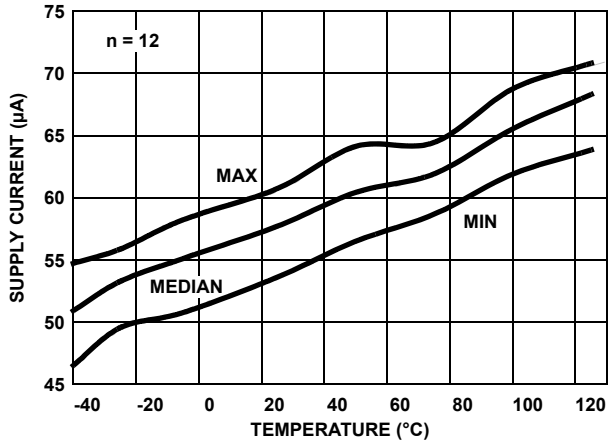


FIGURE 25. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED. R_L = INF

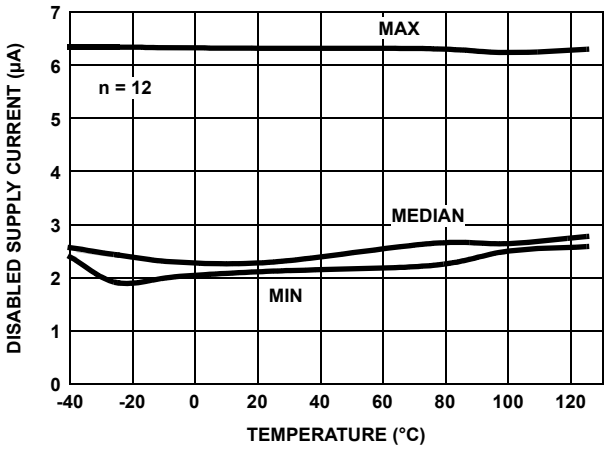


FIGURE 26. DISABLED SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V R_L= INF

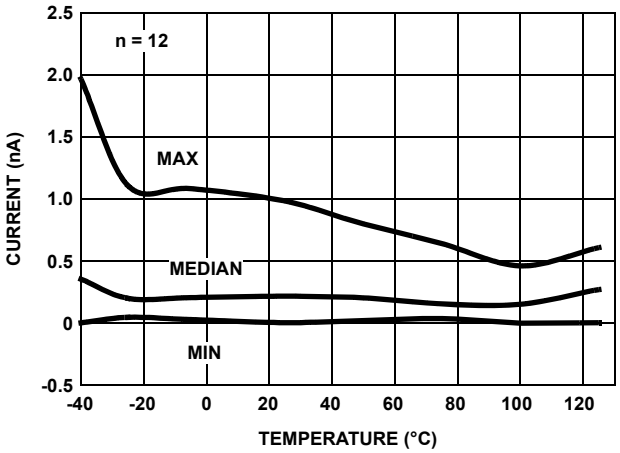


FIGURE 27. I_{BIAS} (+) vs TEMPERATURE V_S = ±2.5V

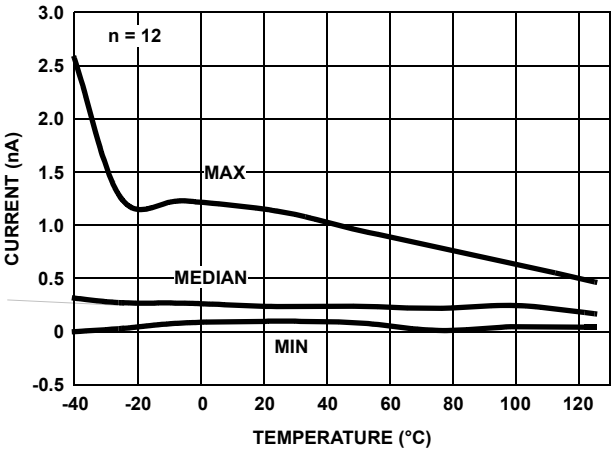


FIGURE 28. I_{BIAS} (+) vs TEMPERATURE V_S = ±1.2V

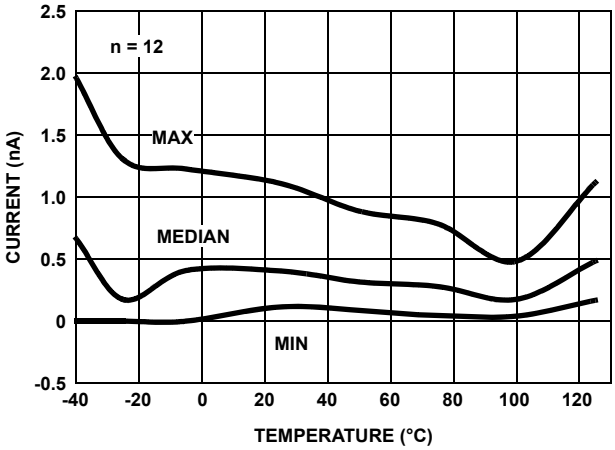


FIGURE 29. I_{BIAS} (-) vs TEMPERATURE V_S = ±2.5V

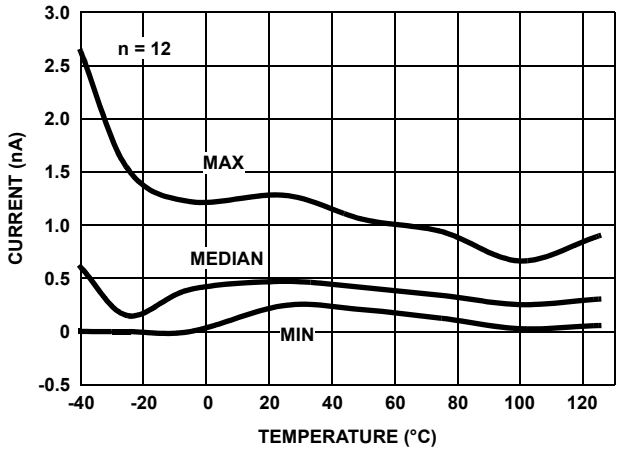


FIGURE 30. I_{BIAS} (-) vs TEMPERATURE V_S = ±1.2V

Typical Performance Curves (Continued)

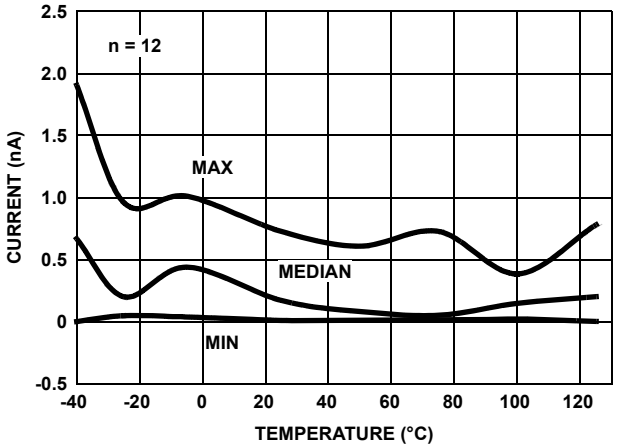


FIGURE 31. INPUT OFFSET CURRENT vs TEMPERATURE
V_S = ±2.5V

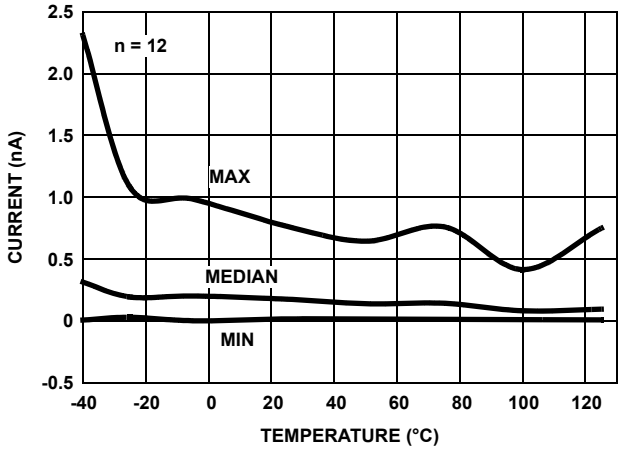


FIGURE 32. INPUT OFFSET CURRENT vs TEMPERATURE
V_S = ±1.2V

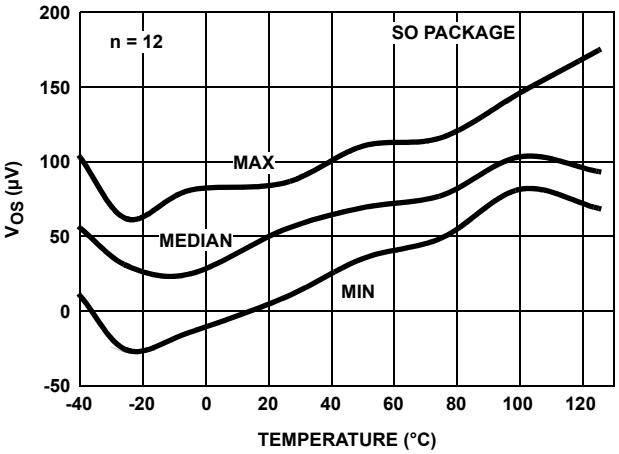


FIGURE 33. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

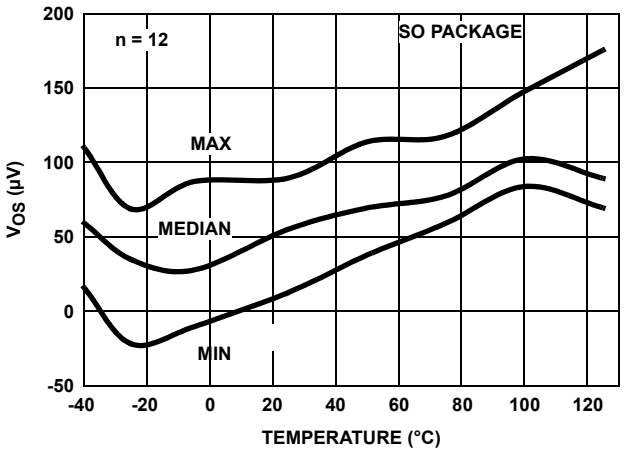


FIGURE 34. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±1.2V

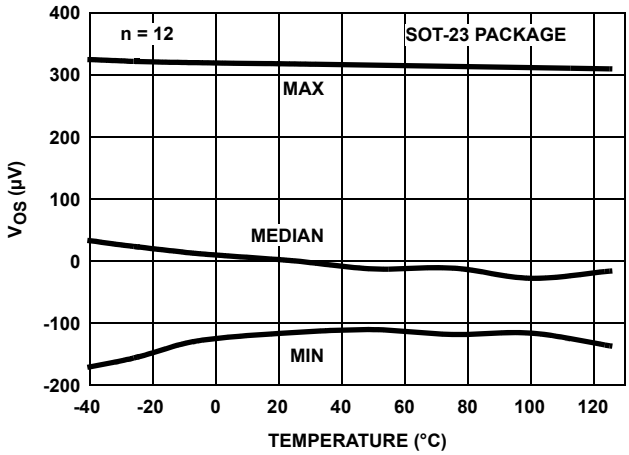


FIGURE 35. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

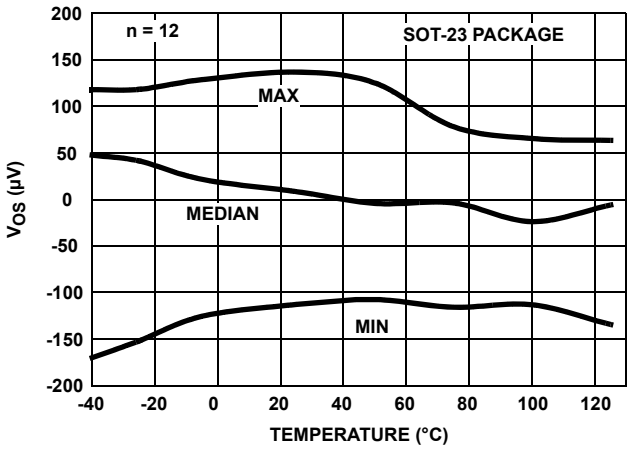


FIGURE 36. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±1.2V

Typical Performance Curves (Continued)

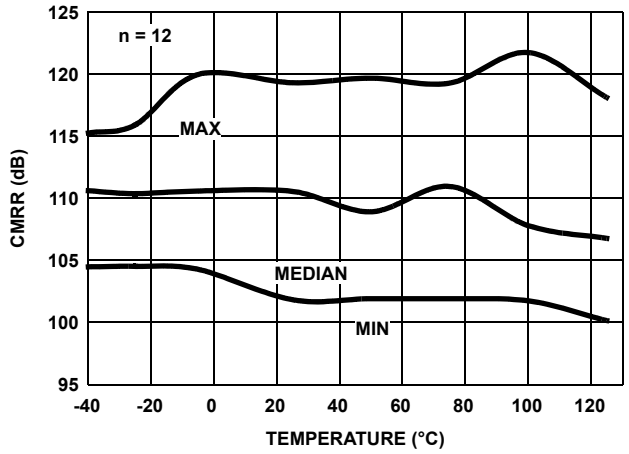


FIGURE 37. CMRR vs TEMPERATURE VCM = +2.5V TO -2.5V

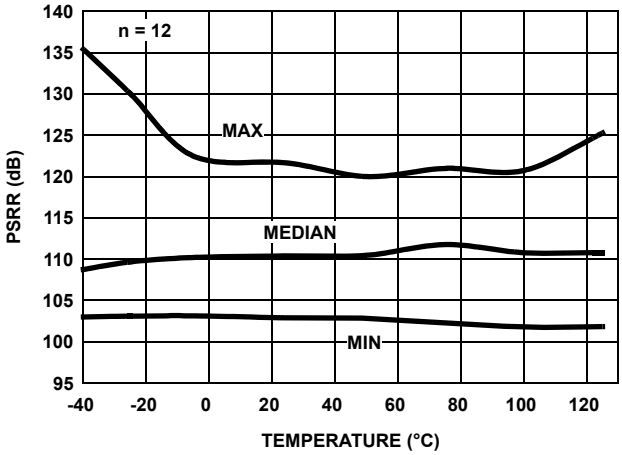


FIGURE 38. PSRR vs TEMPERATURE V_S = ±1.2V TO ±2.5V

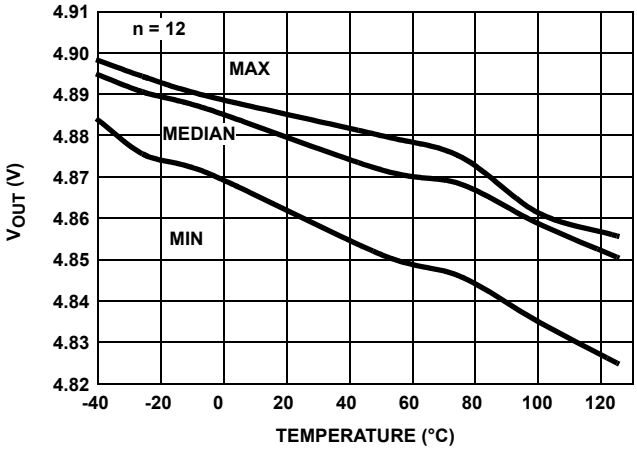


FIGURE 39. POSITIVE V_{OUT} vs TEMPERATURE R_L = 1k
V_S = ±2.5V

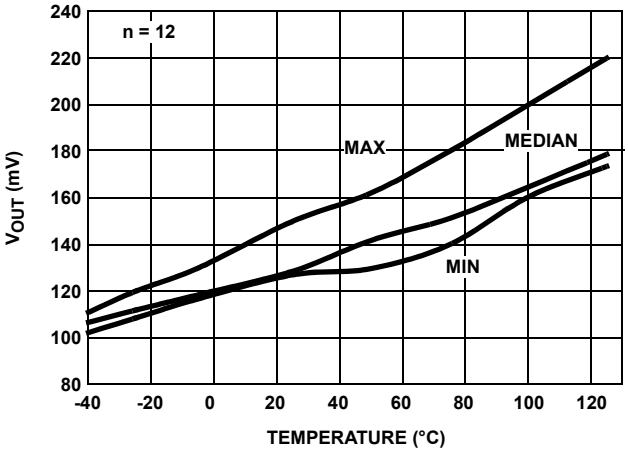


FIGURE 40. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 1k
V_S = ±2.5V

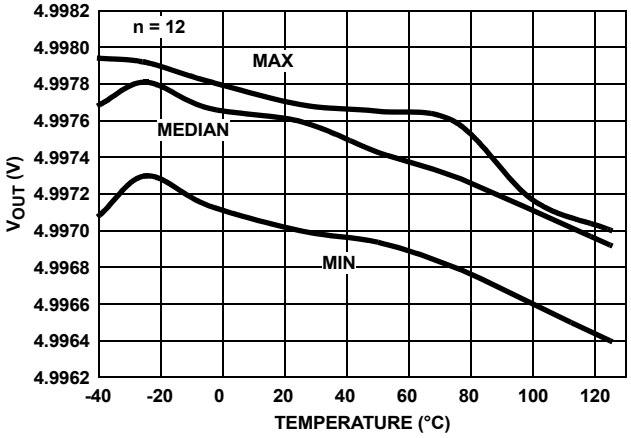


FIGURE 41. POSITIVE V_{OUT} vs TEMPERATURE R_L = 100k
V_S = ±2.5V

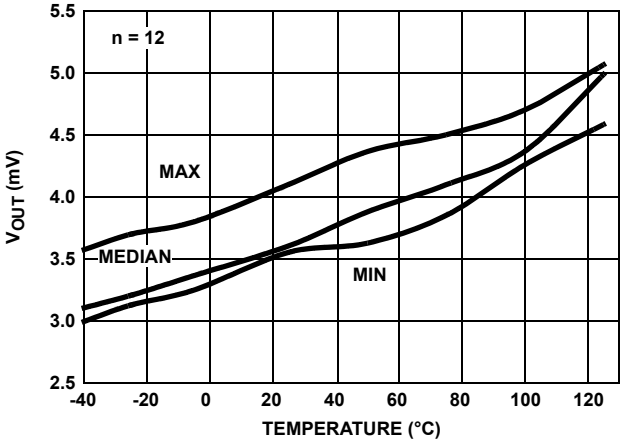


FIGURE 42. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 100k
V_S = ±2.5V

Typical Performance Curves (Continued)

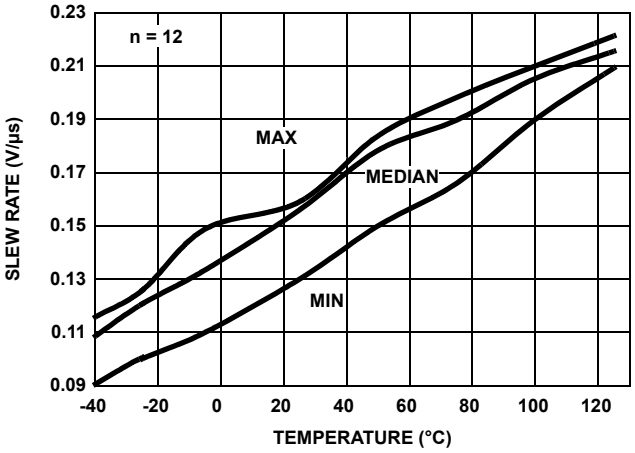


FIGURE 43. ±SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V, A_V = 2

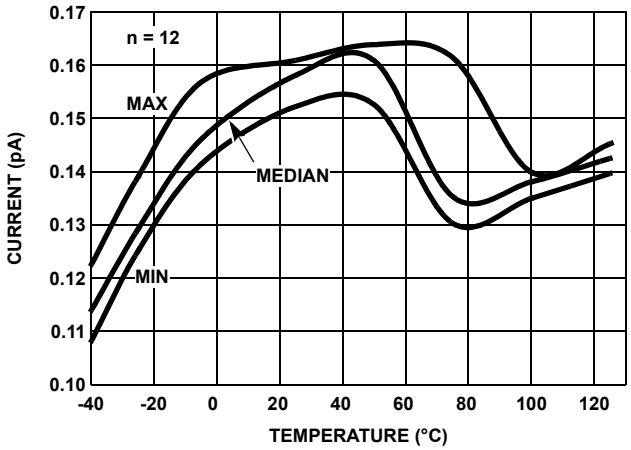


FIGURE 44. ±SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V, A_V = 2

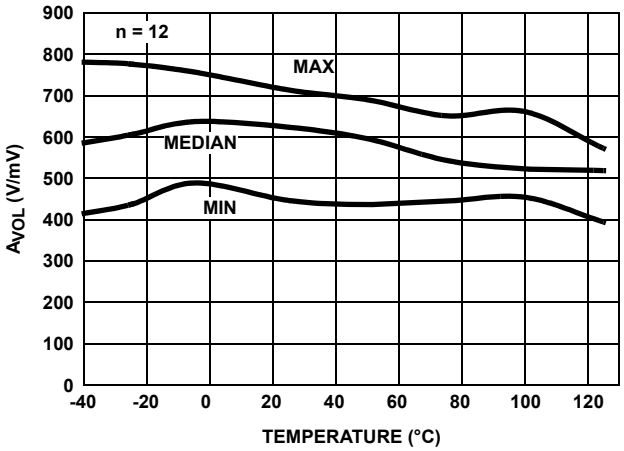


FIGURE 45. A_{VOL}, R_L = 100k, V_S ±2.5V, V_O = ±2V

Applications Information

Introduction

The EL8176 is a rail-to-rail input and output micro-power precision single supply operational amplifier with an enable feature. The device achieves rail-to-rail input and output operation and eliminates the concerns introduced by a conventional rail-to-rail I/O operational amplifier as discussed below.

Rail-to-Rail Input

The input common-mode voltage range of the EL8176 goes from negative supply to positive supply without introducing offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The EL8176 achieves input rail-to-rail without sacrificing important precision specifications and without degrading distortion performance. The EL8176's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range for the EL8176 gives us an undistorted behavior from typically 10mV above the negative rail all the way up to the positive rail.

Input Bias Current Compensation

The input bias currents as low as 500pA are achieved while maintaining an excellent bandwidth for a micro-power operational amplifier. Inside the EL8176 is an input bias canceling circuit. The input stage transistors are still biased with an adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current. The input bias current compensation/cancellation is stable from -40°C to +125°C and operates from typically 10mV to the positive supply rail.

Rail-to-Rail Output

A pair of complementary MOSFET devices achieves rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The EL8176 with a 100kΩ load will swing to within 3mV of the supply rails.

Enable/Disable Feature

The EL8176 offers an $\overline{EN}$ pin. The active low $\overline{EN}$ pin disables the device when pulled up to at least 2.0V. When disabled, the output is in a high impedance state and the part consumes typically 3µA. When disabled, the high impedance output allows multiple parts to be MUXed together. When configured as a MUX, the outputs are tied together in parallel and a channel can be selected by pulling the $\overline{EN}$ pin to 0.8V or lower. The $\overline{EN}$ pin has an internal pull-down. If left open or floating, the $\overline{EN}$ pin will internally be pulled low, enabling the part by default.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage of the EL8176, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 46 shows how the guard ring should be configured and Figure 47 shows the top view of how a surface mount layout can be arranged. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

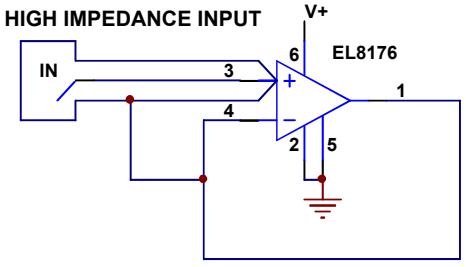


FIGURE 46.

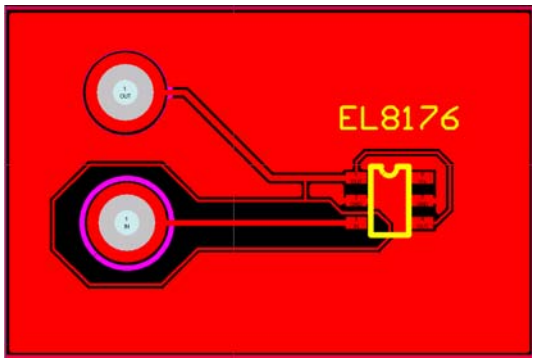


FIGURE 47.

Typical Applications

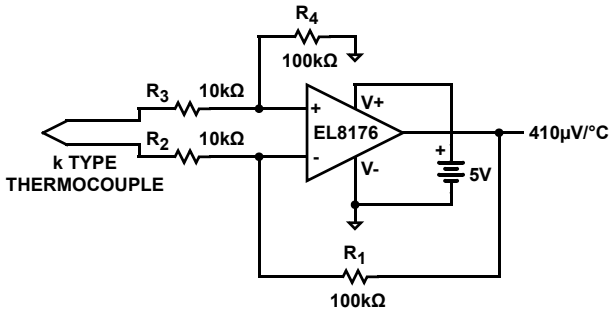


FIGURE 48. THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability and ability to measure a wide range of temperatures. The EL8176 is used to convert the differential thermocouple voltage into single-ended signal with 10x gain. The EL8176's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 6, 2015	FN7436.9	- Updated entire datasheet to Intersil new standard. - Removed WLCSP throughout the document. - Ordering information table on page 2: Added MSL note. - Added revision history and about Intersil verbiage - Updated 8 Ld SO POD from “MDP0027” to “M8.15E”.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

© Copyright Intersil Americas LLC 2004-2015. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

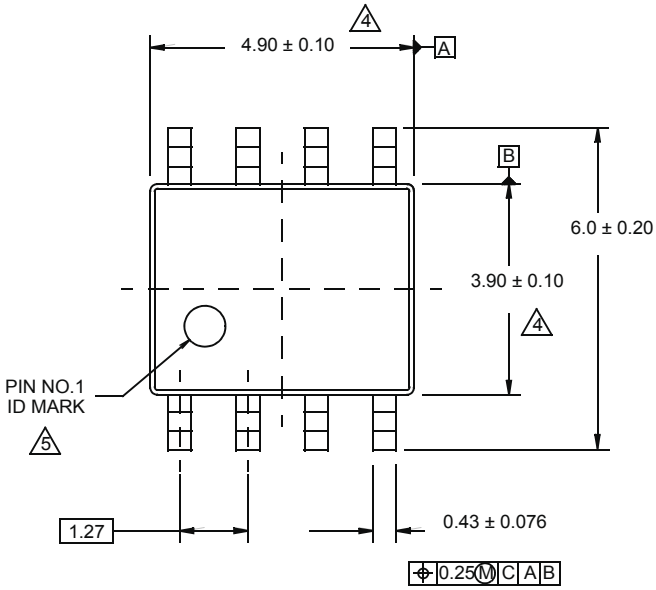
Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

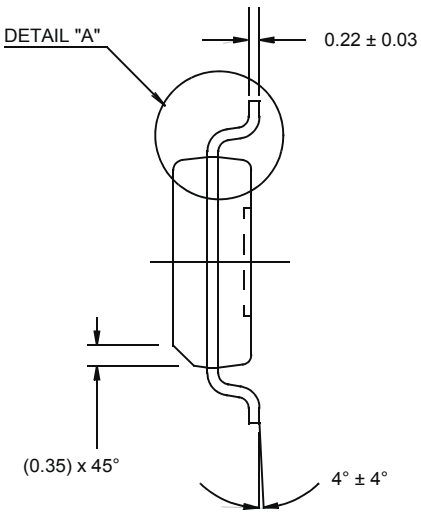
Package Outline Drawing

M8.15E

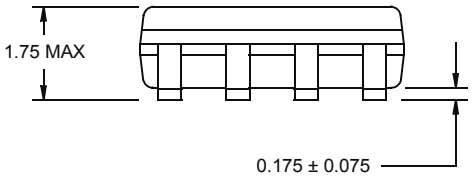
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



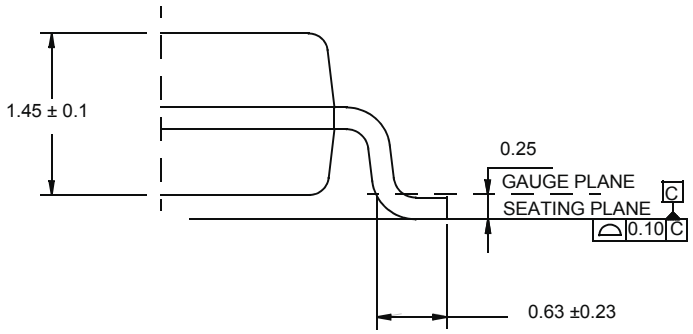
TOP VIEW



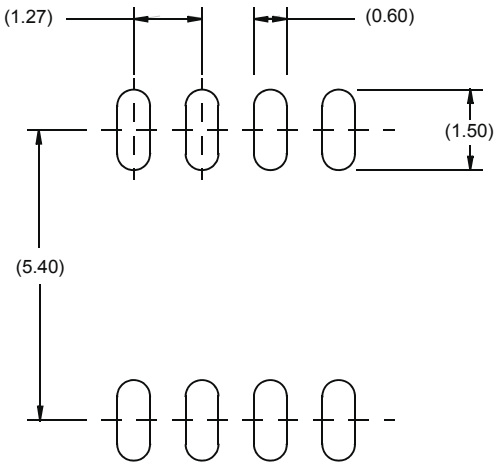
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

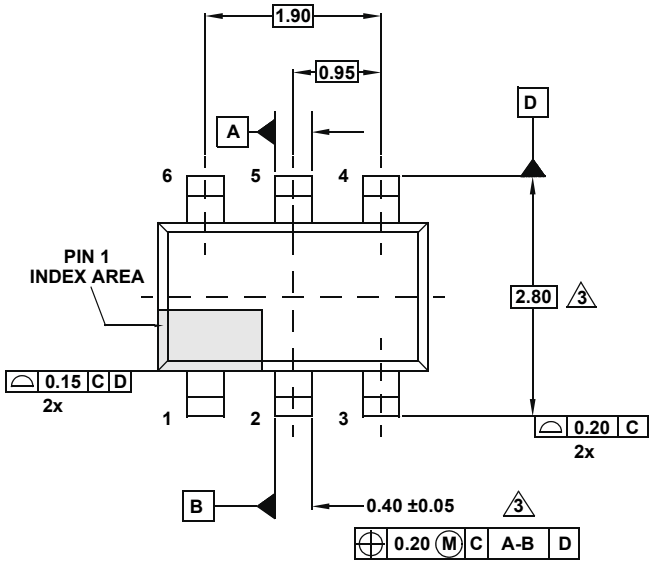
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Package Outline Drawing

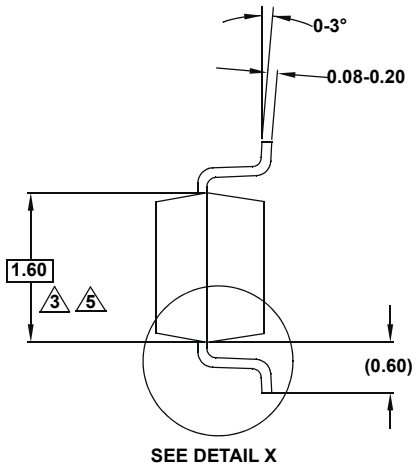
P6.064A

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

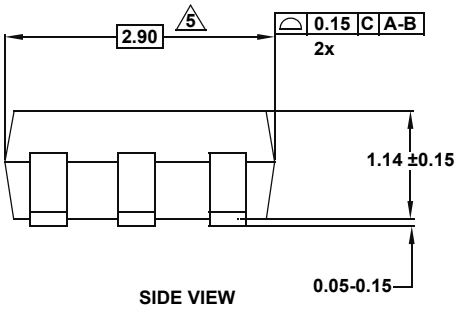
Rev 0, 2/10



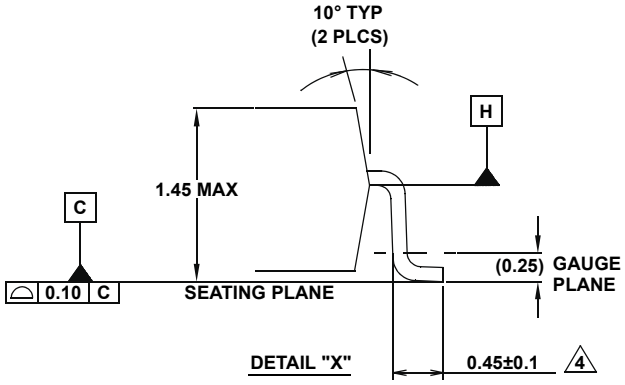
TOP VIEW



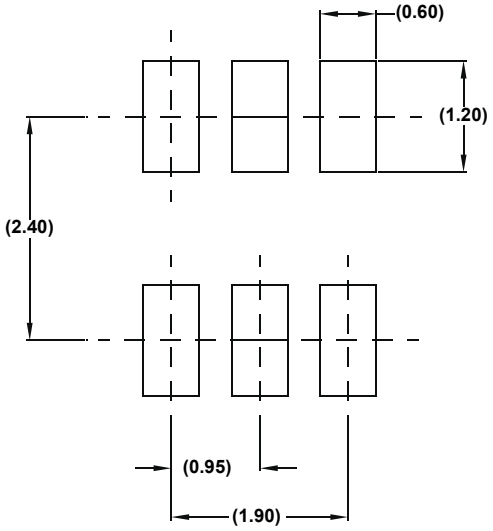
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.