

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

# SSM3J120TU

○ **Power Management Switch Applications**

○ **High-Current Switching Applications**

- 1.5 V drive
- Low on-resistance

$R_{on} = 140 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.5 \text{ V}$ )

$R_{on} = 78 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.8 \text{ V}$ )

$R_{on} = 49 \text{ m}\Omega$  (max) (@ $V_{GS} = -2.5 \text{ V}$ )

$R_{on} = 38 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.0 \text{ V}$ )

**Absolute Maximum Ratings (Ta = 25°C)**

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		$V_{DS}$	-20	V
Gate-Source voltage		$V_{GS}$	$\pm 8$	V
Drain current	DC	$I_D$	-4.0	A
	Pulse	$I_{DP}$	-8.0	
Drain power dissipation	$P_D$ (Note 1)	800	mW	
	$P_D$ (Note 2)	500		
Channel temperature		$T_{ch}$	150	°C
Storage temperature		$T_{stg}$	-55~150	°C

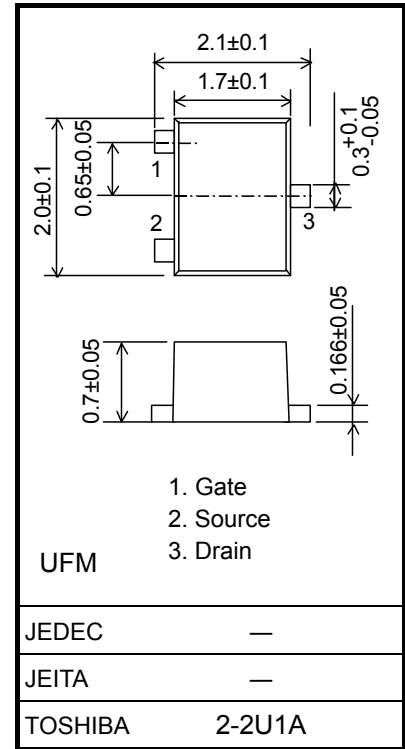
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1 : Mounted on ceramic board  
(25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 mm<sup>2</sup>)

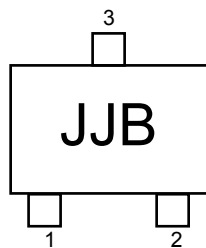
Note 2 : Mounted on FR4 board  
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm<sup>2</sup>)

Unit: mm

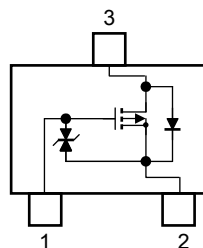


Weight: 6.6mg (typ.)

**Marking**



**Equivalent Circuit (top view)**



Start of commercial production  
2005-11

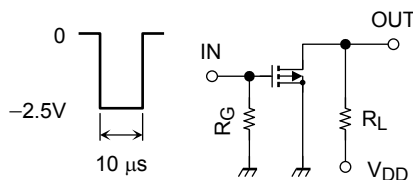
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Drain-Source breakdown voltage	V (BR) DSS	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0	-20	—	—	V	
	V (BR) DSX	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = +8 V	-12	—	—		
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0	—	—	-10	μA	
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0	—	—	±1	μA	
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1 mA	-0.3	—	-1.0	V	
Forward transfer admittance	Y <sub>fs</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -2.0 A (Note 3)	6.1	12.1	—	S	
Drain-Source ON-resistance	R <sub>DS (ON)</sub>	I <sub>D</sub> = -3.0 A, V <sub>GS</sub> = -4.0 V (Note 3)	—	28	38	mΩ	
		I <sub>D</sub> = -2.0 A, V <sub>GS</sub> = -2.5 V (Note 3)	—	34	49		
		I <sub>D</sub> = -1.0 A, V <sub>GS</sub> = -1.8 V (Note 3)	—	47	78		
		I <sub>D</sub> = -0.3 A, V <sub>GS</sub> = -1.5 V (Note 3)	—	60	140		
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 f = 1 MHz	—	1484	—	pF	
Output capacitance	C <sub>oss</sub>		—	185	—	pF	
Reverse transfer capacitance	C <sub>rss</sub>		—	169	—	pF	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -2.0 A V <sub>GS</sub> = 0 to -2.5 V, R <sub>G</sub> = 4.7 Ω	—	67	—	ns
	Turn-off time	t <sub>off</sub>		—	92	—	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = -16 V, I <sub>DS</sub> = -4.0 A, V <sub>GS</sub> = -4.0 V,	—	22.3	—	nC	
Gate-Source charge	Q <sub>gs</sub>		—	14.9	—		
Gate-Drain charge	Q <sub>gd</sub>		—	7.3	—		
Drain-Source forward voltage	V <sub>DSF</sub>	I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 0 (Note 3)	—	0.8	1.2	V	

Note 3: Pulse test

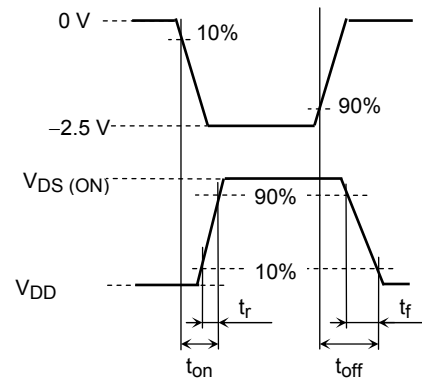
## Switching Time Test Circuit

### (a) Test Circuit



V<sub>DD</sub> = -10 V  
 R<sub>G</sub> = 4.7 Ω  
 Duty ≤ 1%  
 V<sub>IN</sub>: t<sub>r</sub>, t<sub>f</sub> < 5 ns  
 Common Source  
 Ta = 25 °C

### (b) V<sub>IN</sub>



### (c) V<sub>OUT</sub>

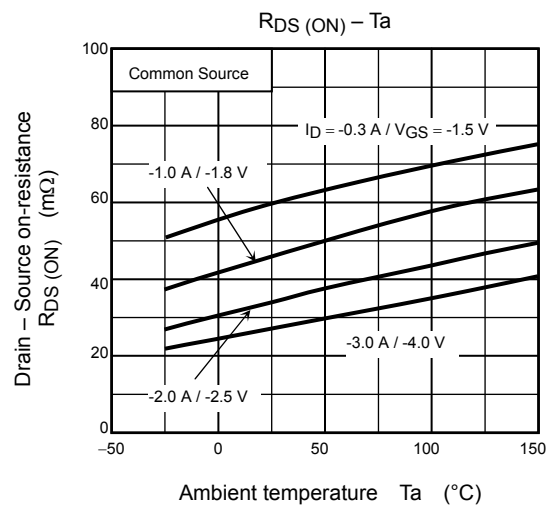
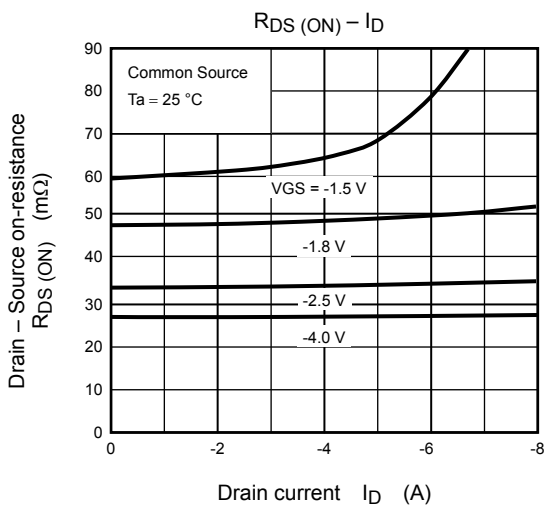
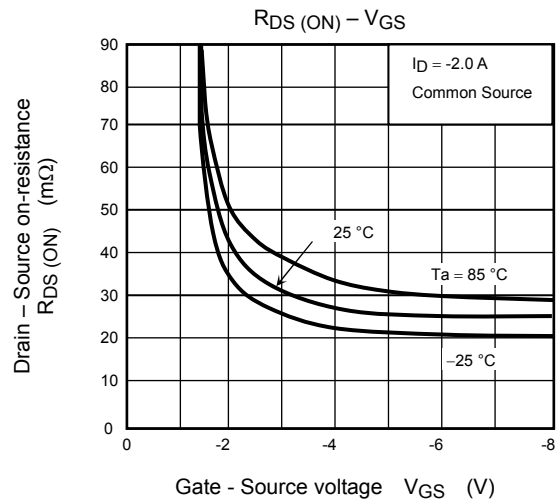
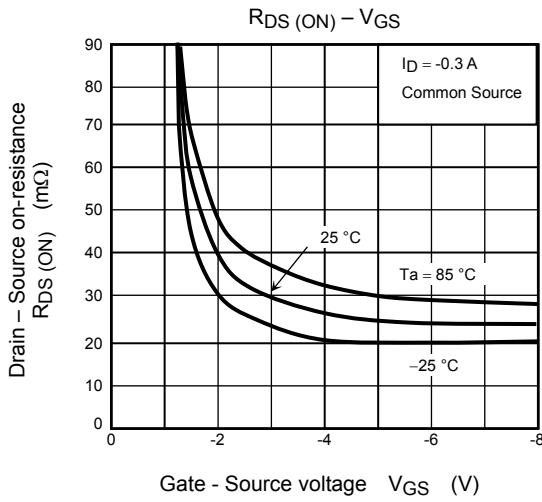
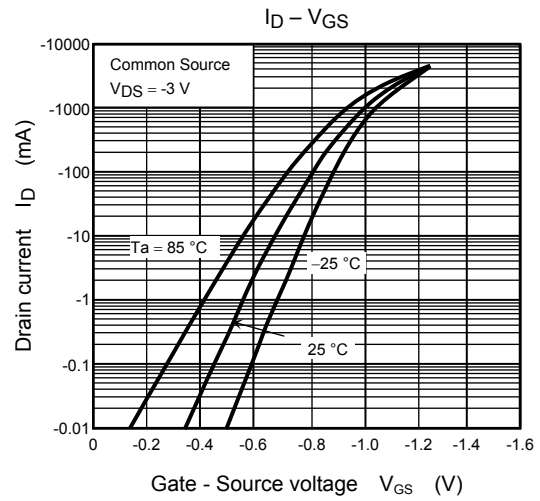
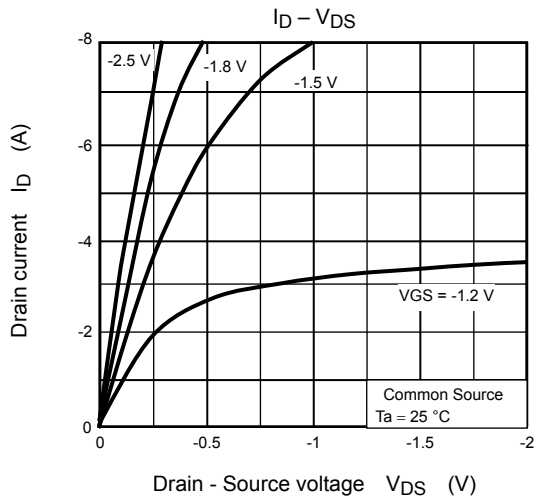
## Precaution

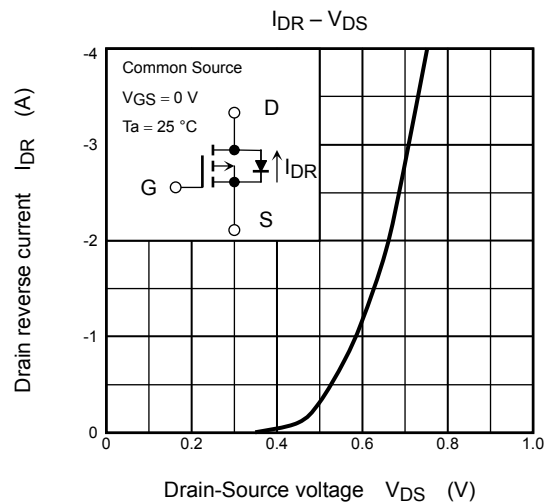
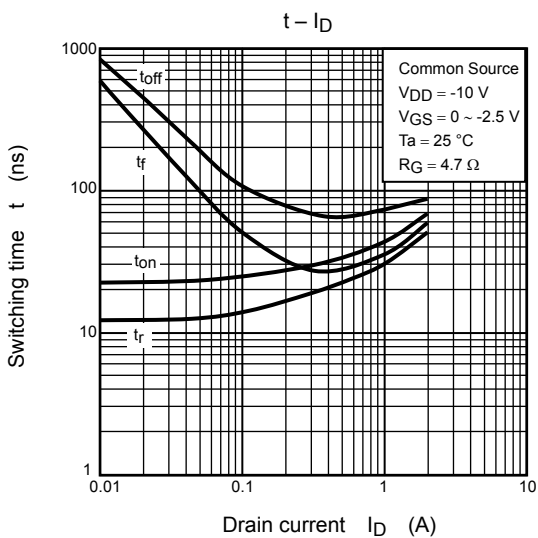
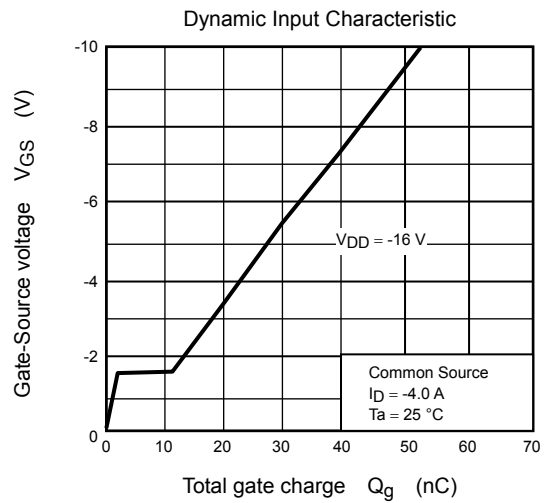
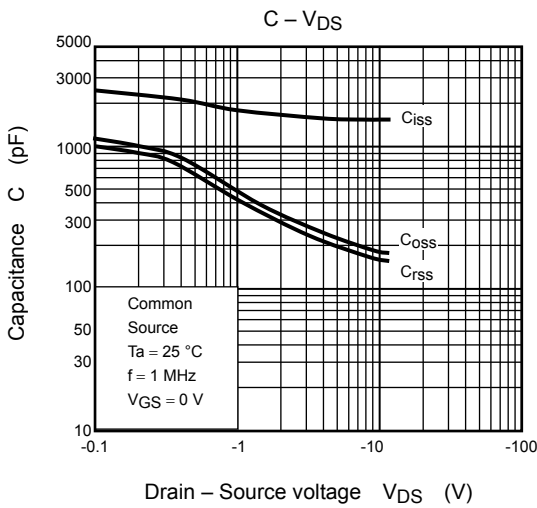
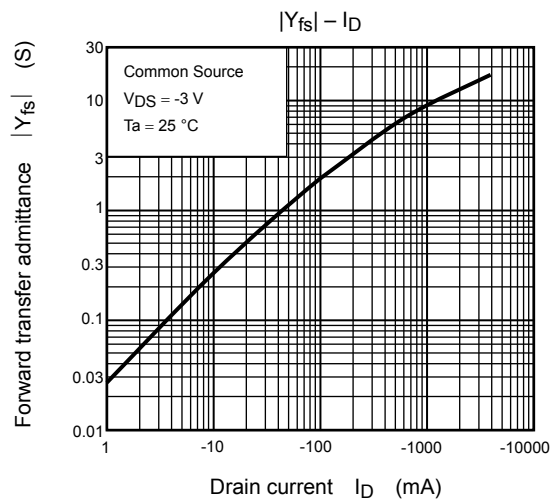
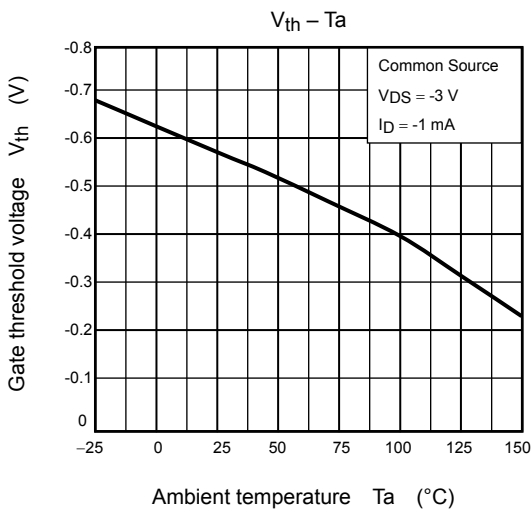
V<sub>th</sub> can be expressed as the voltage between the gate and source when the low operating current value is I<sub>D</sub> = -1mA for this product. For normal switching operation, V<sub>GS (on)</sub> requires a higher voltage than V<sub>th</sub> and V<sub>GS (off)</sub> requires a lower voltage than V<sub>th</sub>. (The relationship can be established as follows: V<sub>GS (off)</sub> < V<sub>th</sub> < V<sub>GS (on)</sub>.)

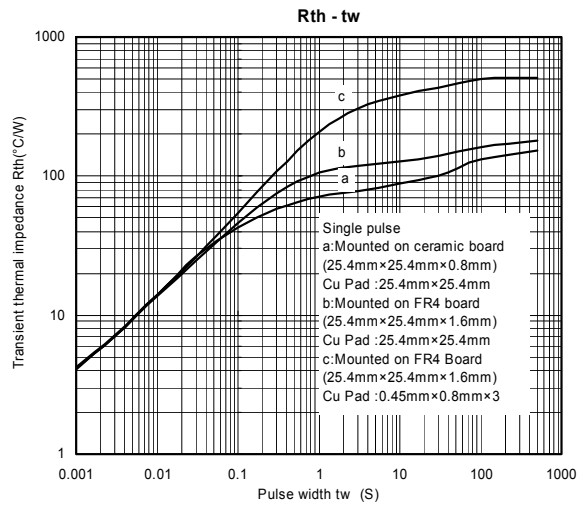
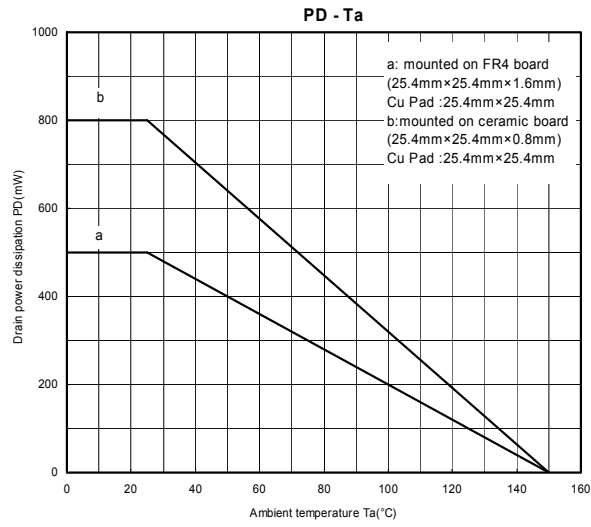
Be sure to take this into consideration when using the device.

## Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.







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