

# ***DAC5675A Evaluation Module***

## *User's Guide*

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It is important to operate this EVM within the input voltage range of 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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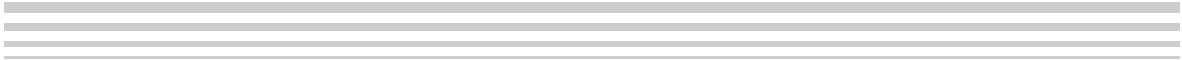
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# Overview



This chapter gives a general overview of the DAC5675A evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

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## 1.1 Purpose

The DAC5675A EVM provides a platform for evaluating the DAC5675A digital-to-analog converter (DAC) under various signal, reference, and supply conditions. This document must be used in combination with the EVM schematic diagram supplied.

## 1.2 EVM Basic Functions

Digital inputs to the DAC can be provided with either LVDS level inputs through a 60 pin header or CMOS inputs through a 40 pin header. This enables the user to provide high-speed digital data to the DAC5675A.

The analog output from the DAC is provided via SMA connectors. Because of its flexible design the analog output of the DAC5675A can be configured to drive a 50  $\Omega$  terminated cable using a 4:1 or 1:1 impedance ratio transformer, or single-ended referred to  $AV_{DD}$ .

The EVM allows for different clock configurations. The user can input a differential ECL/PECL or TTL/CMOS level signal, to be used to generate a single-ended or differential clock source. Refer to the clock section for proper configuration and operation.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog and digital supply.

In addition to the internal bandgap reference provided by the DAC5675A device, options are provided on the EVM to allow external reference to be provided to the DAC.

## 1.3 Power Requirements

The EVM can be powered directly with a single 3.3-V supply. Provision has been made to allow the EVM to be powered with independent 3.3-V analog and digital supplies to provide higher performance.

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**Note: Voltage Limits**

Exceeding the maximum input voltages can damage EVM components. Under voltage may cause improper operation of some or all of the EVM components.

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## 1.4 DAC5675A EVM Operational Procedure

The DAC5675A EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The following setup procedure can be used as a board confidence check:

- 1) Verify all jumper settings against the schematic jumper list in Tables 1–1 and 1–2:

*Table 1–1. Two Pin Jumper List*

| Jumper | Function              | Installed                  | Removed                            | Default   |
|--------|-----------------------|----------------------------|------------------------------------|-----------|
| W4     | Power for LVDS driver | Enables CMOS input circuit | CMOS input circuit is powered down | Installed |

*Table 1–2. Three Pin Jumper List*

| Jumper | Function                | Location: Pins 1– 2 | Location: Pins 2–3 | Default       |
|--------|-------------------------|---------------------|--------------------|---------------|
| W1     | Power down select       | Power down mode     | Operate mode       | 2–3           |
| W2     | N/A                     | N/A                 | N/A                | Not Installed |
| W3     | LVDS line driver enable | Outputs 3-state     | Outputs enabled    | 2–3           |

- 2) Connect supplies to the EVM as follows:
  - 3.3 V analog supply to J1 and return to J2.
  - 3.3 V digital supply to J3 and return to J4.
- 3) Switch power supplies on.
- 4) Use a frequency generator with 50- $\Omega$  output to input a 400 Mhz, 0V offset, 150-mVpp amplitude sine wave signal into J9 to be used as the DAC clock. The frequency of the clock must be within the specification for the device speed grade.
- 5) Use a digital test pattern generator with 50  $\Omega$  outputs to input 3.3-V CMOS logic level inputs to P2. This data must be synchronized and the same frequency as the DAC input clock.
- 6) The analog output on SMA connector J8 can now be monitored using a spectrum analyzer.



# PCB Layout and Parts List

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This chapter shows the PCB layout of the EVM and lists the components used on the module.

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## 2.1 PCB Layout

Figures 4–1 through 4–6 show the PCB layout for the EVM.

Figure 2–1. Top Layer 1

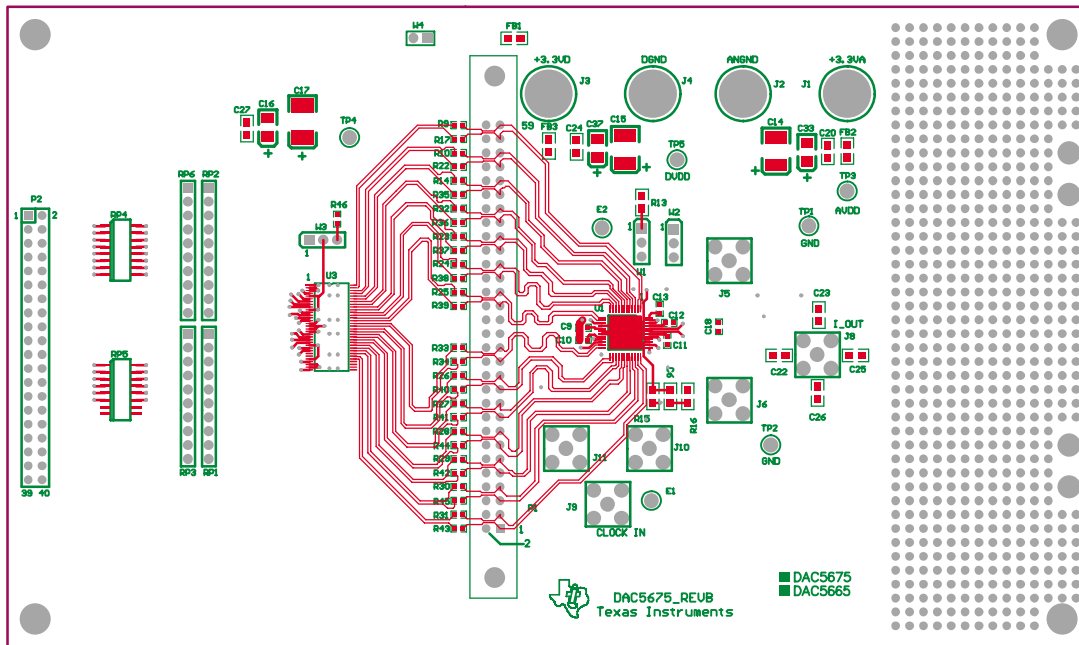


Figure 2–2. Ground Plane 1 Layer 2

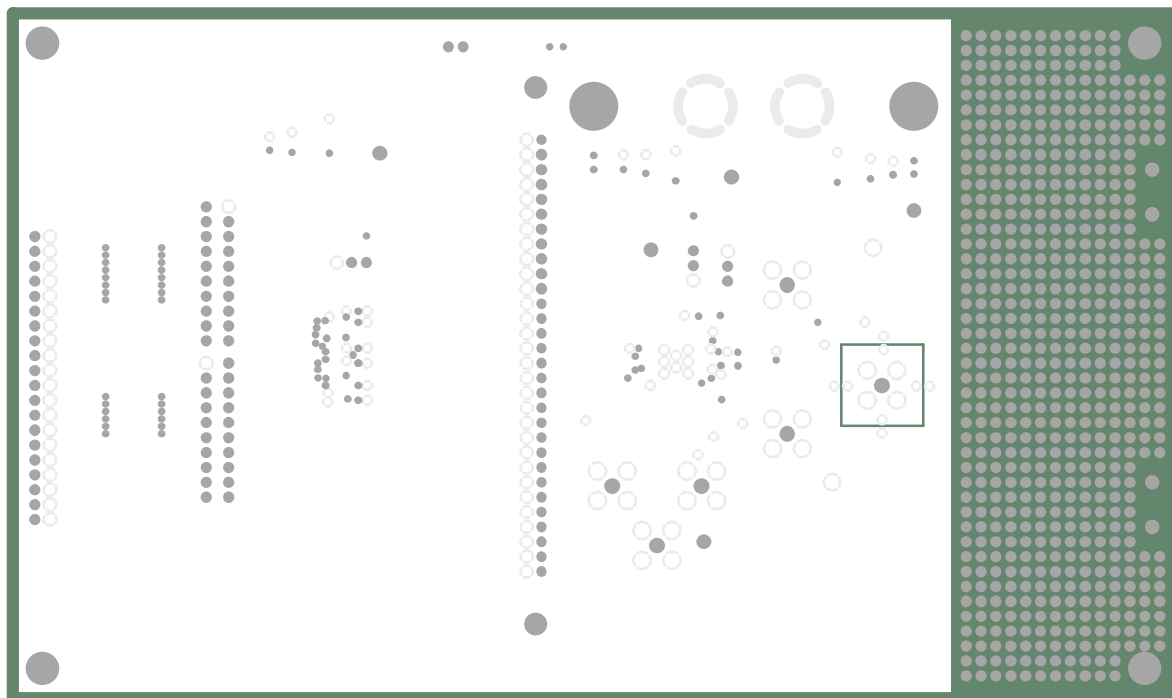


Figure 2–3. AVDD Power Plane Layer 3

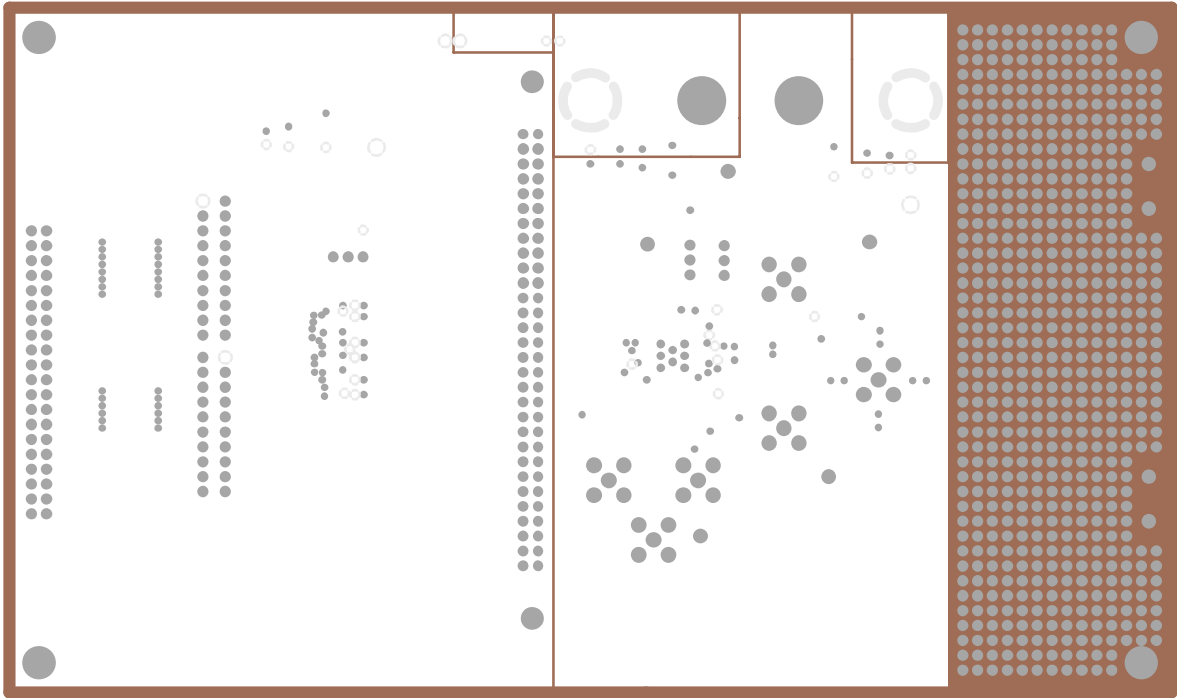


Figure 2–4. DVDD Power Plane Layer 4

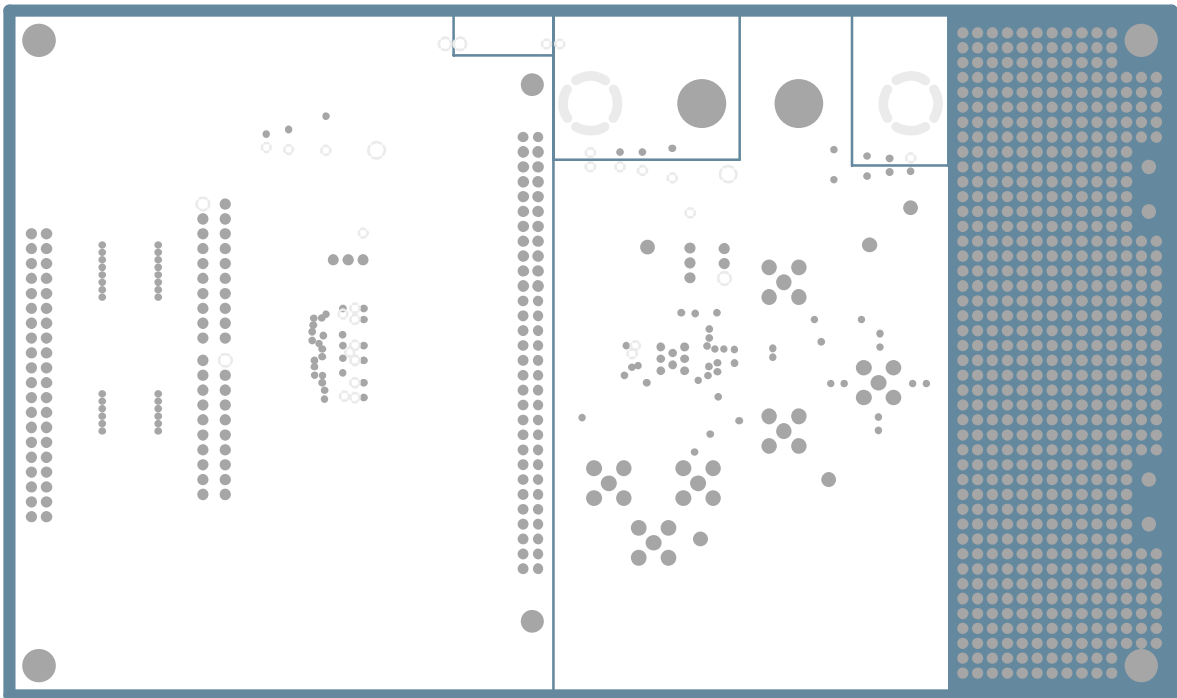


Figure 2–5. Ground Plane 2 Layer 5

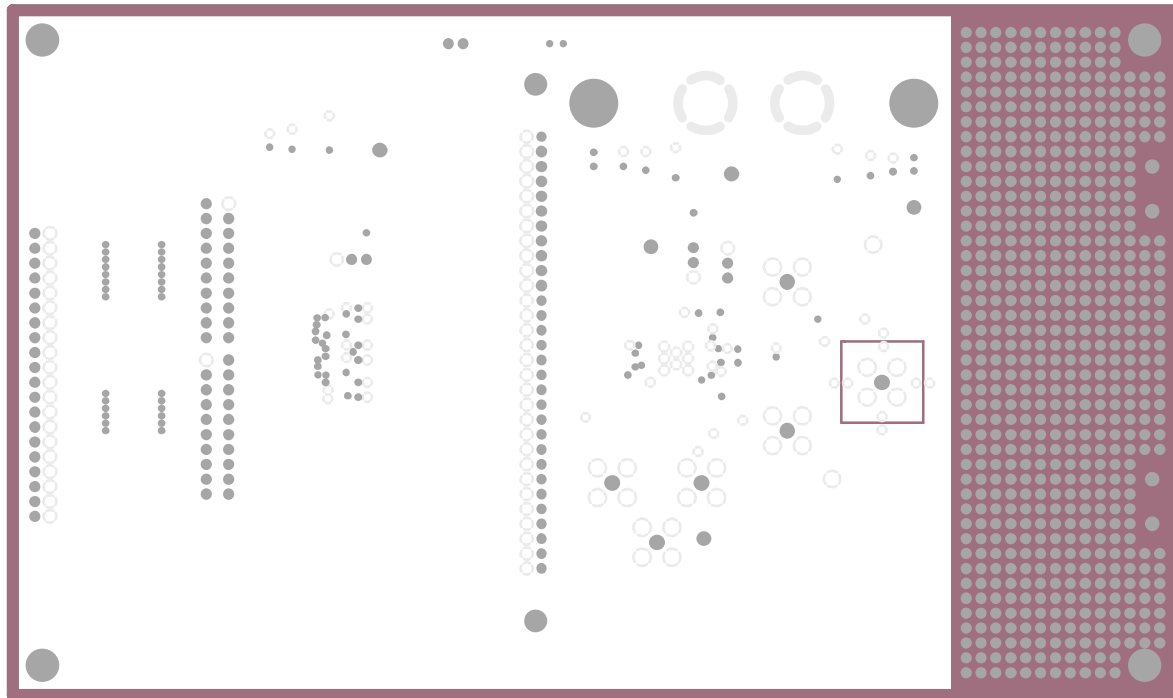
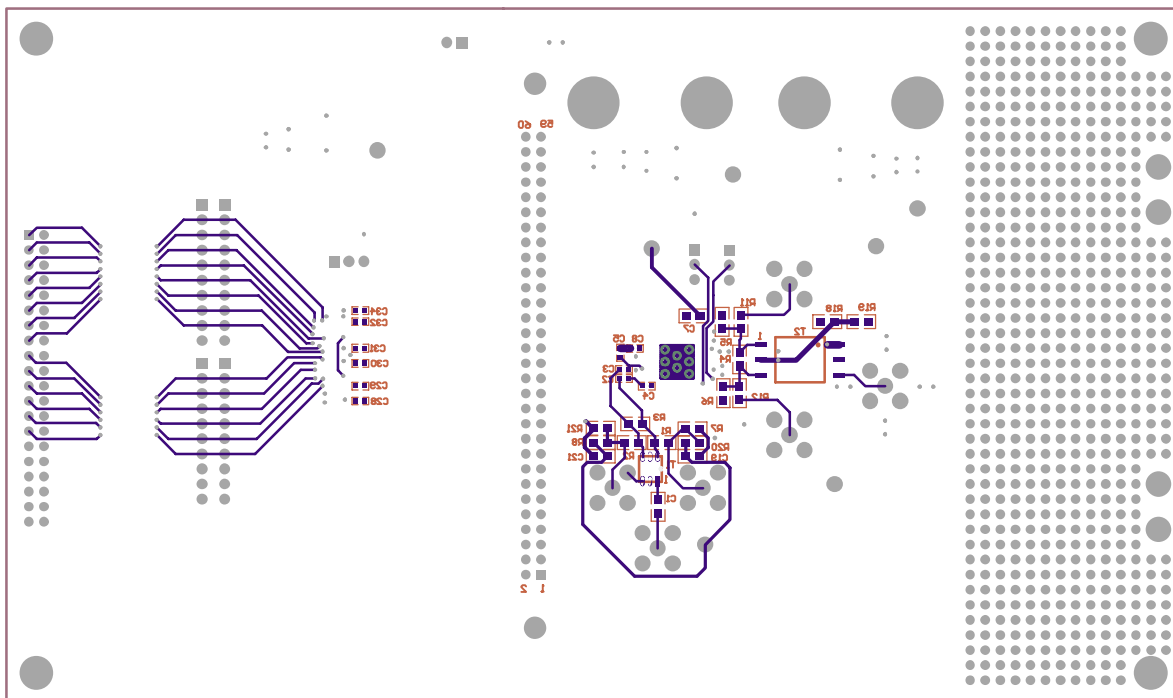


Figure 2–6. Bottom Layer 6



## 2.2 Parts List

Table 2–1 lists the parts used in constructing the EVM.

Table 2–1. DAC5675A EVM Parts List

| Bill Of Material For DAC5675A      |     |                |              |                              |                  |
|------------------------------------|-----|----------------|--------------|------------------------------|------------------|
| Description                        | Qty | Part Number    | Manufacturer | Ref Des                      | Not Installed    |
| 0.01- $\mu$ F, 16 V, 10% capacitor | 12  | ECJ–1VB1C103K  | Panasonic    | C8–C13<br>C28–C32<br>C34     | C4 C5            |
| 0.1- $\mu$ F, 16 V, 10% capacitor  | 1   | ECJ–1VB1C104K  | Panasonic    | C18                          |                  |
| 0.1- $\mu$ F, 16 V, 10% capacitor  | 4   | ECJ–2VB1C104K  | Panasonic    | C7 C20 C24<br>C27            | C19 C21          |
| 0.01- $\mu$ F, 50 V, 10% capacitor | 1   | ECU–V1H103KBG  | Panasonic    | C1                           | C6               |
| 10- $\mu$ F, 10 V, 10% capacitor   | 3   | GRM42X5R106K10 | Murata       | C16 C33<br>C37               |                  |
| 47- $\mu$ F, 10 V, 10% capacitor   | 3   | 10TPA47M       | Sanyo        | C14 C15<br>C17               |                  |
| 0- $\Omega$ resistor               | 30  | ERJ–3EKF0R00V  | Panasonic    | R9 R10 R14<br>R17<br>R22–R45 |                  |
| 0- $\Omega$ resistor               | 5   | ERJ–6GEY0R00V  | Panasonic    | R18 C22<br>C23 C25<br>C26    | R1 R2 R11<br>R12 |
| 10-K $\Omega$ resistor             | 1   | CRCW08051002F  | Dale         | R13                          |                  |
| 49.9- $\Omega$ resistor            | 2   | CRCW080549R9F  | Dale         | R5 R6                        | R7 R8 R20<br>R21 |
| 100- $\Omega$ resistor             | 1   | CRCW08051000F  | Dale         | R4                           |                  |
| 1K- $\Omega$ resistor              | 1   | ERJ–3EKF1001   | Panasonic    | R46                          |                  |
| 1-k $\Omega$ resistor              | 1   | CRCW08051001F  | Dale         | R15                          | R16 R19          |
| 200- $\Omega$ resistor             | 1   | CRCW08052000F  | Dale         | R3                           |                  |
| 22- $\Omega$ resistor pack         | 2   | 4816P–001–220  | Bourns       | RP4 RP5                      |                  |
| 100- $\Omega$ resistor pack        | 0   | EXB–F10E101G   | Panasonic    |                              | RP1 RP6          |
| 51.1- $\Omega$ resistor pack       | 2   | 770–101–R51    | CTS          |                              | RP2 RP3          |
| Ferrite bead                       | 3   | D01608C–472    | Coil Craft   | FB1 FB2<br>FB3               |                  |

Table 2-1. DAC5675A EVM Parts List (Continued)

| Bill Of Material For DAC5675A |     |                |               |                |                  |
|-------------------------------|-----|----------------|---------------|----------------|------------------|
| Description                   | Qty | Part Number    | Manufacturer  | Ref Des        | Not Installed    |
| 2POS_JUMPER                   | 1   | TSW-150-07-L-S | Samtec        | W4             |                  |
| 3POS_JUMPER                   | 3   | TSW-150-07-L-S | Samtec        | W1 W2 W3       |                  |
| 40PIN_IDC                     | 1   | TSW-120-07-L-D | Samtec        | P2             |                  |
| 60PIN_3M                      | 1   | TSW-130-07-L-D | Samtec        | P1             |                  |
| Red Banana Jack               | 2   | ST-351A        | Allied        | J1 J3          |                  |
| Black Banana Jack             | 2   | ST-351B        | Allied        | J2 J4          |                  |
| BLACK TESTPOINT               | 2   | 5001K          | Keystone      | TP1 TP2        |                  |
| RED TESTPOINT                 | 3   | 5000K          | Keystone      | TP3 TP4<br>TP5 |                  |
| DAC5675A                      | 1   | DAC5675AIPHP   | TI            | U1             |                  |
| SN65LVDS387                   | 1   | SN75LVDS387DGG | TI            | U3             |                  |
| Transformer                   | 1   | TCM4-1W        | Mini-Circuits | T1             |                  |
| Transformer                   | 1   | T1-1T-KK8      | Mini-Circuits | T2             |                  |
| SMA connectors                | 2   | 713-4339       | Allied        | J8 J9          | J5 J6 J10<br>J11 |



# **Circuit Description**

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This chapter discusses the various functions on the EVM.

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### 3.1 Circuit Function

The following paragraphs describe the functions of individual circuits. Refer to the relevant data sheet for device operating characteristics.

#### 3.1.1 Input Clock

The DAC5675A EVM default operation setting is with a differential input clock sent to the DAC5675A. An external sinewave clock is applied to SMA connector J9 and converted to a differential clock input to the DAC5675A by transformer T1. This input represents a 50- $\Omega$  load to the source. In order to preserve the specified performance of the DAC5675A converter, the clock source should feature very low jitter. Optimum clock amplitude is 150 mVpp at the J9 input. Using a clock with a 50% duty cycle will give optimum dynamic performance.

##### 3.1.1.1 Differential ECL/PECL Input Clock

The EVM can be configured for differential ECL/ PECL input clock mode by configuring the board per Table 3–1 and applying the appropriate ECL/PECL common mode voltage at terminal E1 (VTT). Use J10 and J11 to input the external differential ECL/PECL clock signals.

##### 3.1.1.2 Single-Ended Input Clock

The EVM can be configured for single-ended input clock mode by configuring the board per Table 3–1. Use J10 SMA to input the external TTL/CMOS clock signal.

Table 3–1. EVM Clock Configuration

| Clock Configuration    | Components Installed†              | Components Not Installed          |
|------------------------|------------------------------------|-----------------------------------|
| Differential (default) | R3, T1, C1, C2 (short), C3 (short) | R1, R2, R7, R8, R20, R21, C4, C5  |
| ECL or PECL            | R1, R2, R20, R8, C2, C3            | R3, R7, R21, T1, C4, C5, C19, C21 |
| Single ended TTL/CMOS  | R1, R7, C5, C2 (short),            | R2, R3, R20, T1, C3, C4           |

† All component values are per the schematic except where shown in parenthesis.

#### 3.1.2 Input Data

The DAC5675A EVM can be configured to accept either 3.3-V CMOS logic level or LVDS logic level input data.

### 3.1.2.1 CMOS Input Data

The DAC5675A EVM can accept 3.3 V CMOS logic level data inputs. With 0 ohm resistors installed for R9, R10, R14, R17, R22–R45, Jumper W4 installed, and Jumper W3 inserted between pins 2 and 3, CMOS level data present at P2 is converted to LVDS levels by the LVDS driver U3. The DAC5675A features internal 100 ohm resistors eliminating the need for external termination resistors. More information on the data inputs can be found in the data sheet. 14-bit CMOS input data is brought in through the 40 pin header P2 per Table 3–2.

Table 3–2. CMOS Input Connector P2

| P2 pin | Description            | P2 pin | Description           |
|--------|------------------------|--------|-----------------------|
| 1      | CMOS data bit 13 (MSB) | 21     | CMOS data bit 3       |
| 2      | GND                    | 22     | GND                   |
| 3      | CMOS data bit 12       | 23     | CMOS data bit 2       |
| 4      | GND                    | 24     | GND                   |
| 5      | CMOS data bit 11       | 25     | CMOS data bit 1       |
| 6      | GND                    | 26     | GND                   |
| 7      | CMOS data bit 10       | 27     | CMOS data bit 0 (LSB) |
| 8      | GND                    | 28     | GND                   |
| 9      | CMOS data bit 9        | 29     |                       |
| 10     | GND                    | 30     | GND                   |
| 11     | CMOS data bit 8        | 31     |                       |
| 12     | GND                    | 32     | GND                   |
| 13     | CMOS data bit 7        | 33     |                       |
| 14     | GND                    | 34     | GND                   |
| 15     | CMOS data bit 6        | 35     |                       |
| 16     | GND                    | 36     | GND                   |
| 17     | CMOS data bit 5        | 37     |                       |
| 18     | GND                    | 38     | GND                   |
| 19     | CMOS data bit 4        | 39     |                       |
| 20     | GND                    | 40     | GND                   |

### 3.1.2.2 LVDS Input Data

The DAC5675A EVM can accept LVDS (low voltage differential signaling) data inputs per TIA/EIA-644 standard compliant electrical interface. For this mode of operation, R9, R10, R14, R17, R22-R45, and Jumper W4 should be removed for optimal operation. 14-bit input data is brought in through the 60 pin header P1 per Table 3-3.

Table 3-3. LVDS Input Connector P2

| P1 Pin | Description                    | P1 Pin | Description                     |
|--------|--------------------------------|--------|---------------------------------|
| 1      | LVDS negative data bit 0 (LSB) | 31     |                                 |
| 2      | GND                            | 32     | GND                             |
| 3      | LVDS positive data bit 0 (LSB) | 33     | LVDS negative data bit 7        |
| 4      | GND                            | 34     | GND                             |
| 5      | LVDS negative data bit 1       | 35     | LVDS positive data bit 7        |
| 6      | GND                            | 36     | GND                             |
| 7      | LVDS positive data bit 1       | 37     | LVDS negative data bit 8        |
| 8      | GND                            | 38     | GND                             |
| 9      | LVDS negative data bit 2       | 39     | LVDS positive data bit 8        |
| 10     | GND                            | 40     | GND                             |
| 11     | LVDS positive data bit 2       | 41     | LVDS negative data bit 9        |
| 12     | GND                            | 42     | GND                             |
| 13     | LVDS negative data bit 3       | 43     | LVDS positive data bit 9        |
| 14     | GND                            | 44     | GND                             |
| 15     | LVDS positive data bit 3       | 45     | LVDS negative data bit 10       |
| 16     | GND                            | 46     | GND                             |
| 17     | LVDS negative data bit 4       | 47     | LVDS positive data bit 10       |
| 18     | GND                            | 48     | GND                             |
| 19     | LVDS positive data bit 4       | 49     | LVDS negative data bit 11       |
| 20     | GND                            | 50     | GND                             |
| 21     | LVDS negative data bit 5       | 51     | LVDS positive data bit 11       |
| 22     | GND                            | 52     | GND                             |
| 23     | LVDS positive data bit 5       | 53     | LVDS negative data bit 12       |
| 24     | GND                            | 54     | GND                             |
| 25     | LVDS negative data bit 6       | 55     | LVDS positive data bit 12       |
| 26     | GND                            | 56     | GND                             |
| 27     | LVDS positive data bit 6       | 57     | LVDS negative data bit 13 (MSB) |
| 28     | GND                            | 58     | GND                             |
| 29     |                                | 59     | LVDS positive data bit 13 (MSB) |
| 30     | GND                            | 60     | GND                             |

### 3.1.3 Output Data

The DAC5675A EVM can be configured to drive a doubly terminated 50-Ω cable or provide unbuffered differential outputs.

#### 3.1.3.1 Transformer Coupled Signal Output

The factory-set configuration of the demonstration board provides the user with a single-ended output signal at SMA connector J8. The DAC5675A is configured to drive a doubly terminated 50-Ω cable using a 1:1 impedance ratio transformer, a 100-Ω terminating resistor R4, and the center tap of T2 connected to  $AV_{DD}$  per Table 3–4. When using a 4:1 impedance ratio transformer, configure the EVM per Table 3–4.

Table 3–4. Transformer Output Configuration

| Configuration                   | Components Installed†                  | Components Not Installed |
|---------------------------------|--|--------------------------|
| 1:1 Impedance ratio transformer | R4, R5, R6, R18, C18 T2 (1:1)          | R11, R12, R19            |
| 4:1 Impedance ratio transformer | R18, R5 (100), R6 (100), C18, T2 (4:1) | R4, R11, R12, R19        |

† All component values are per the schematic except where shown in parenthesis.

#### 3.1.3.2 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows: Remove R4 and T2; Install R11, R12, J5 and J6; Replace R5 and R6 with 25-Ω resistors.

### 3.1.4 Internal Reference Operation

The full-scale output current is set by applying an external resistor (R15) between the BIASJ pin of the DAC5675A and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying R15 or changing the externally applied reference voltage. The full-scale output current,  $I_{OUT_{FS}}$ , is defined as follows:

$$I_{OUT_{FS}} = 16 \times \left( \frac{V_{EXTIO}}{R15} \right)$$

where  $V_{EXTIO}$  is the voltage at pin EXTIO. This voltage is 1.2 V typical when using the internally provided bandgap reference voltage source.

### 3.1.5 External Reference Operation

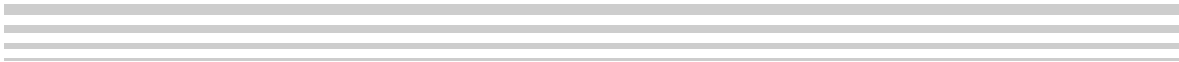
The internal reference can be disabled and overridden by an external reference by connecting a voltage source to terminal E2 (EXT\_I/O). The specified range for external reference voltages should be observed (see the DAC5675A data sheet for details).

### 3.1.6 Sleep Mode

The DAC5675A EVM provides a means of placing the DAC5675A into a power-down mode. This mode is activated by placing Jumper W1 between pins 1 and 2.

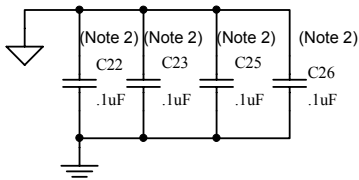
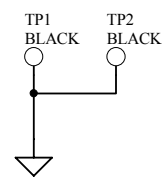
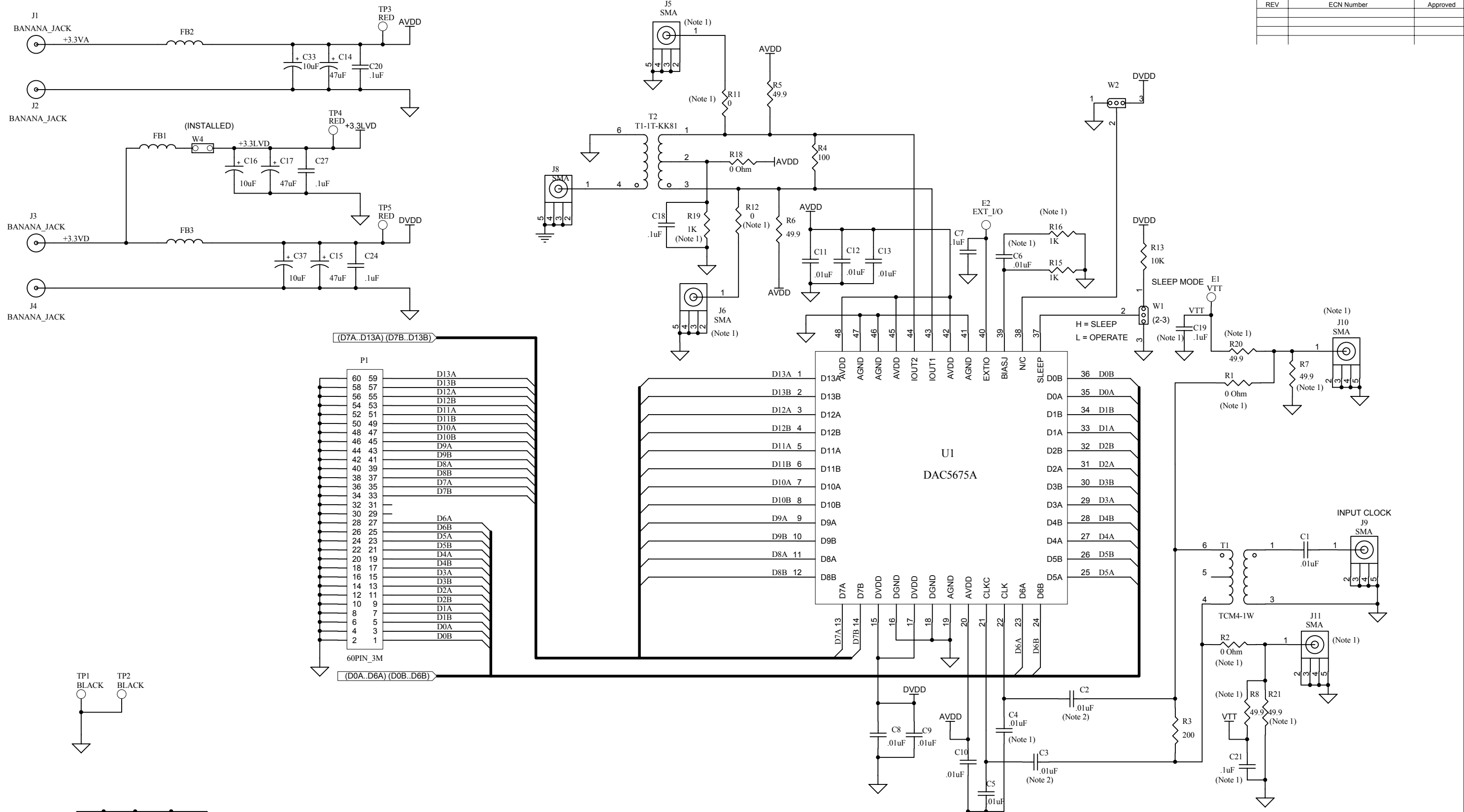


# **Schematics**



This chapter contains the EVM schematic diagrams.

| Revision History |            |          |
|------------------|------------|----------|
| REV              | ECN Number | Approved |
|                  |            |          |
|                  |            |          |
|                  |            |          |



NOTE 1. PART IS NOT INSTALLED  
 NOTE 2. PART IS REPLACED WITH A SHORT



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Title: DAC5675 SCHEMATIC

|                            |                            |                      |
|----------------------------|----------------------------|----------------------|
| Engineer: JIM SETON        | DOCUMENT CONTROL # 6435814 | REV: B               |
| Drawn By: Y. DEWONCK       | DATE: 29-Mar-2005          | SIZE: SHEET: 1 OF: 2 |
| FILE: 6435814 REVB SH1.SCH |                            |                      |



