

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C6 650V

650V CoolMOS™ C6 Power Transistor
IPD65R1K4C6

Data Sheet

Rev. 2.1
Final

Industrial & Multimarket

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ C6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Fully qualified according to JEDEC for Industrial Applications

Applications

Hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and Lighting.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	1.4	Ω
Q_g,typ	10.5	nC
$I_D,pulse$	8.3	A
$E_{oss} @ 400V$	1.15	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPD65R1K4C6	PG-TO 252	65C61K4	see Appendix A

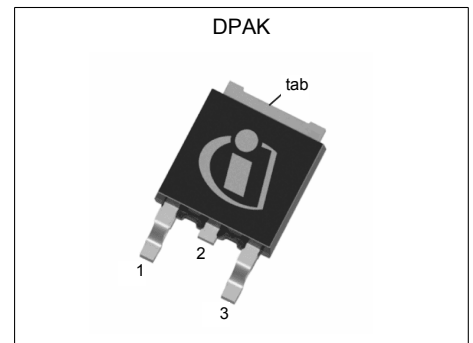
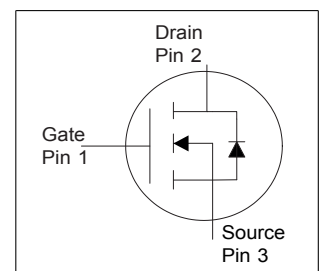


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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			3.2	A	$T_C = 25^\circ\text{C}$
				2.0		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			8.3	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			26	mJ	$I_D = 0.6\text{A}$, $V_{DD} = 50\text{V}$ (see table 10)
Avalanche energy, repetitive	E_{AR}			0.10	mJ	$I_D = 0.6\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			0.6	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 480\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Continuous diode forward current	I_S			2.8	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			8.3	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ (see table 8)
Maximum diode commutation speed	di/dt			500	A/ μs	
Power dissipation	P_{tot}			28	W	$T_C = 25^\circ\text{C}$

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			4.4	°C/W	
Thermal resistance, junction - ambient ¹⁾	R_{thJA}			62	°C/W	leaded
			35			SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

¹⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS} = V_{GS}, I_D = 0.1mA$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
			10			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ C$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		1.260	1.4	Ω	$V_{GS} = 10V, I_D = 1.0A, T_j = 25^\circ C$
			3.280			$V_{GS} = 10V, I_D = 1A, T_j = 150^\circ C$
Gate resistance	R_G		6.5		Ω	$f = 1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		225		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	C_{oss}		18		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		10		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		42		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 480V$
Turn-on delay time	$t_{d(on)}$		7.7		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 1.5A, R_G = 10.2\Omega$ (see table 9)
Rise time	t_r		5.9		ns	
Turn-off delay time	$t_{d(off)}$		33		ns	
Fall time	t_f		18.2		ns	

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		1.3		nC	$V_{DD} = 480V, I_D = 1.5A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		5.8		nC	
Gate charge total	Q_g		10.5		nC	
Gate plateau voltage	$V_{plateau}$		5.4		V	

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 1.5A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		200		ns	$V_R = 400V, I_F = 1.5A,$ $di_F/dt = 100A/\mu s$ (see table 8)
Reverse recovery charge	Q_{rr}		0.9		μC	
Peak reverse recovery current	I_{rrm}		8		A	

5 Electrical characteristics diagrams

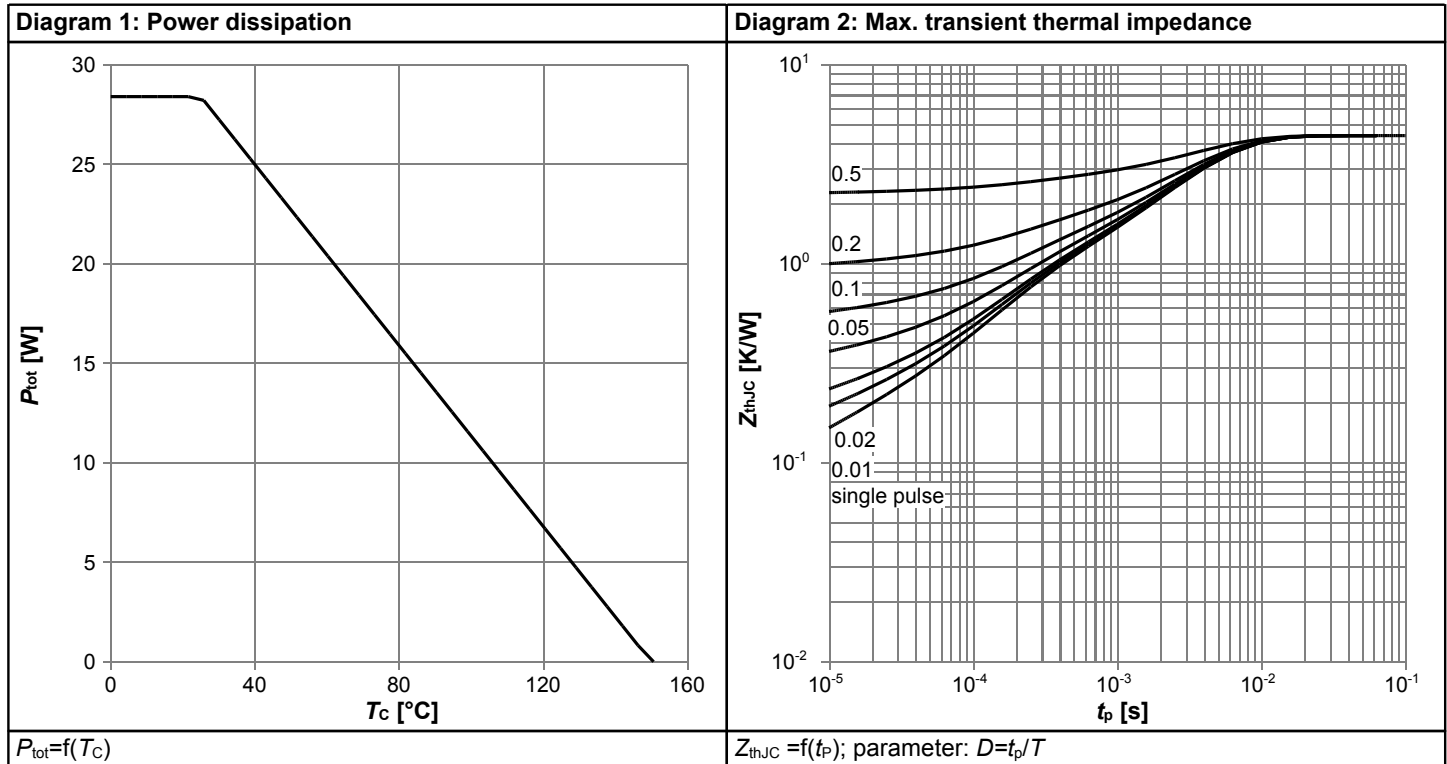
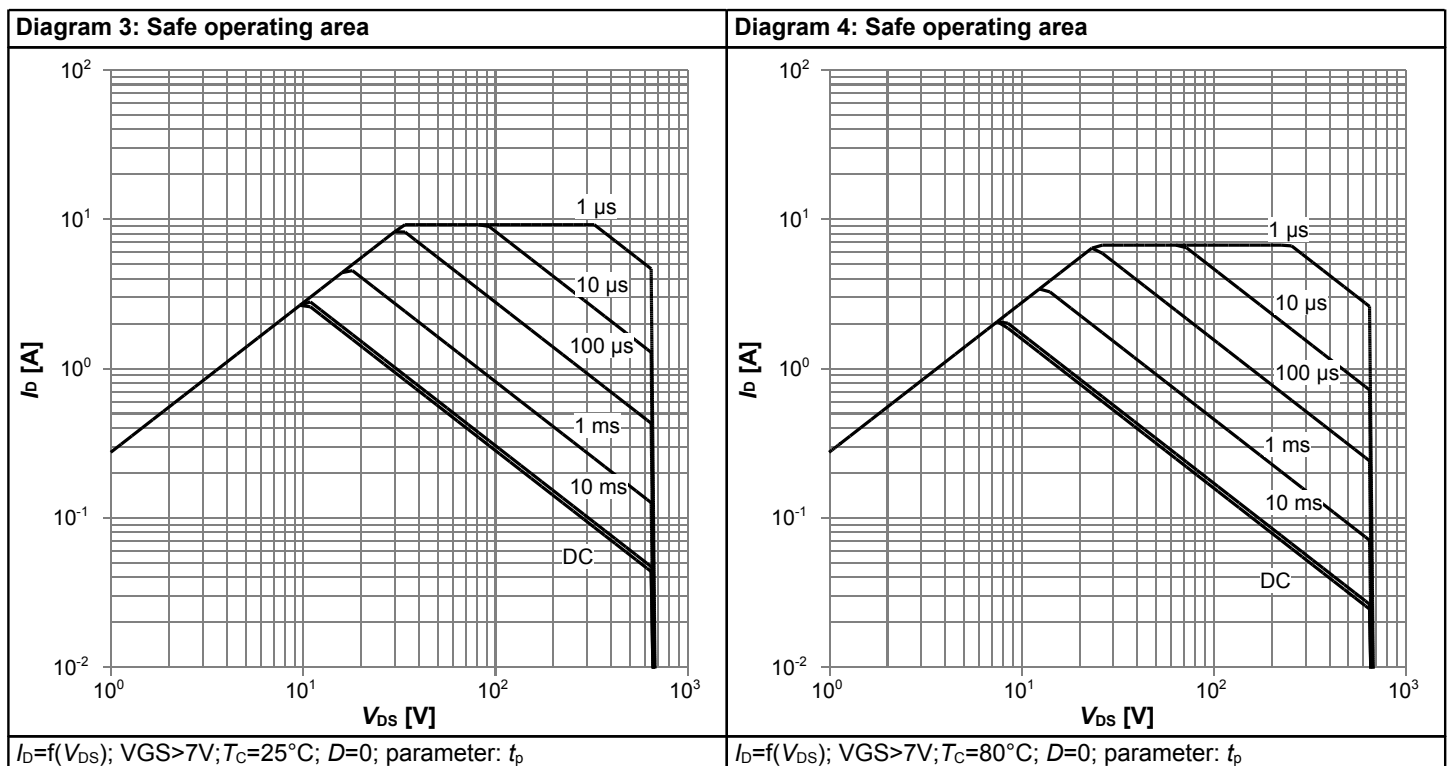


Diagram 5: Typ. output characteristics

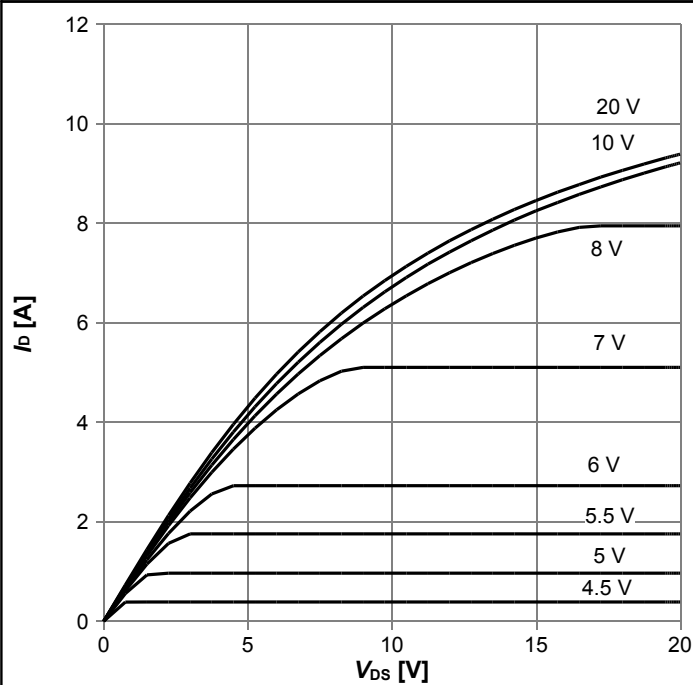

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics

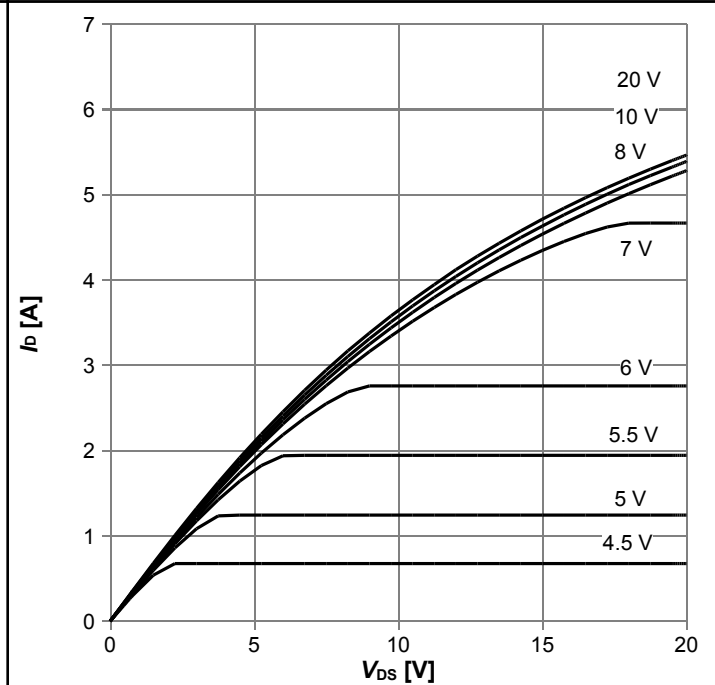

 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance

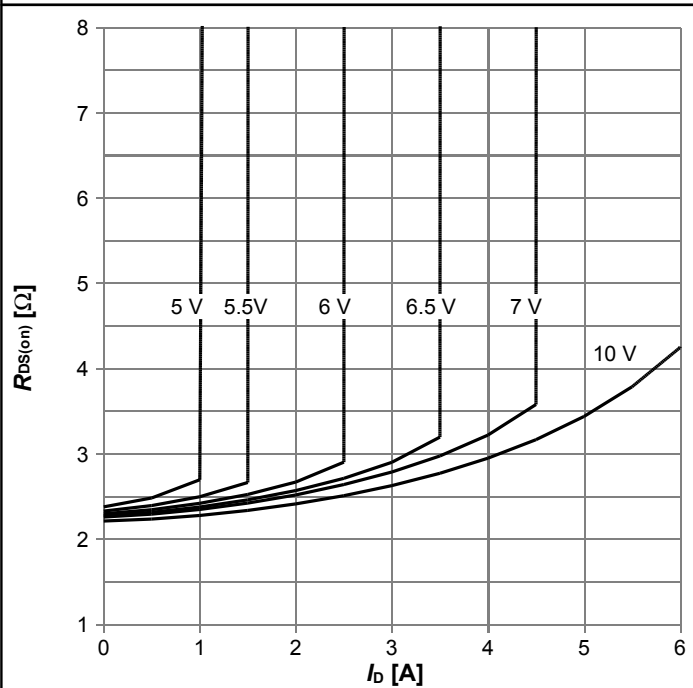

 $R_{DS(on)} = f(I_D); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance

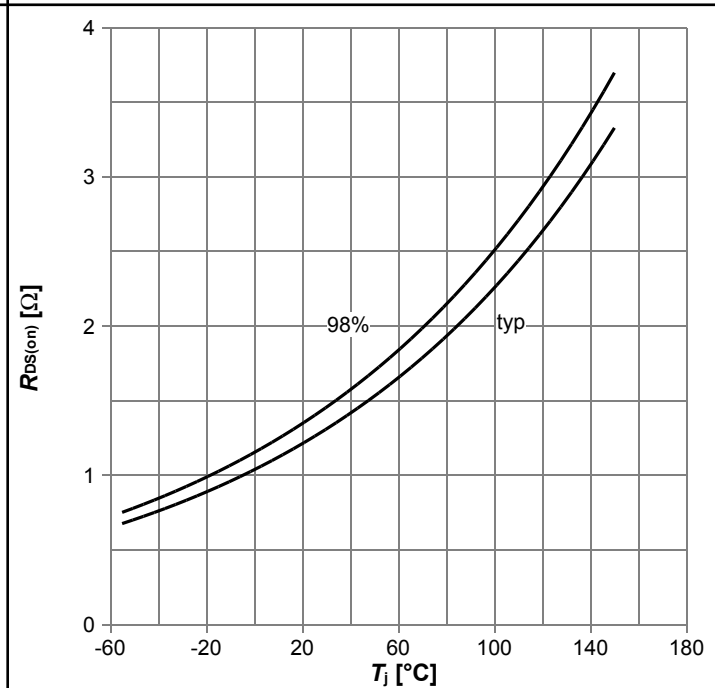

 $R_{DS(on)} = f(T_J); I_D = 1.0\text{ A}; V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics

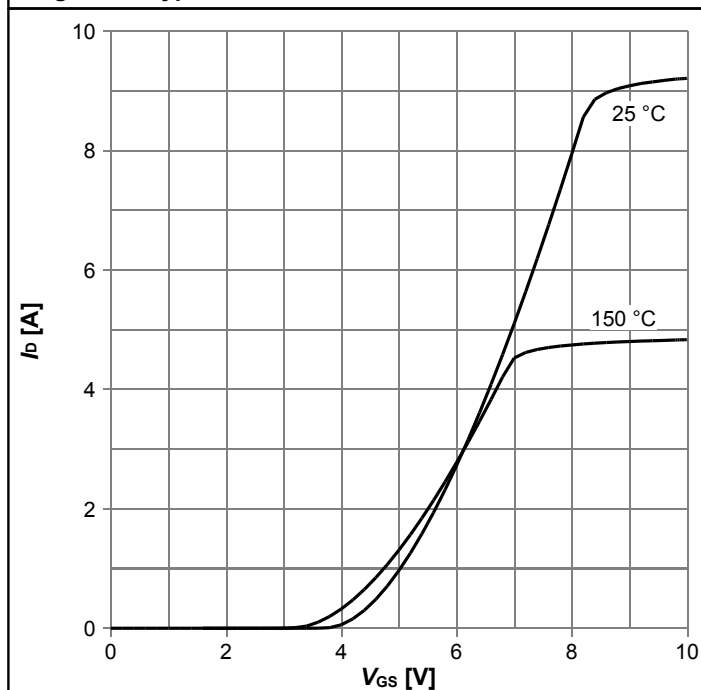

 $I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge

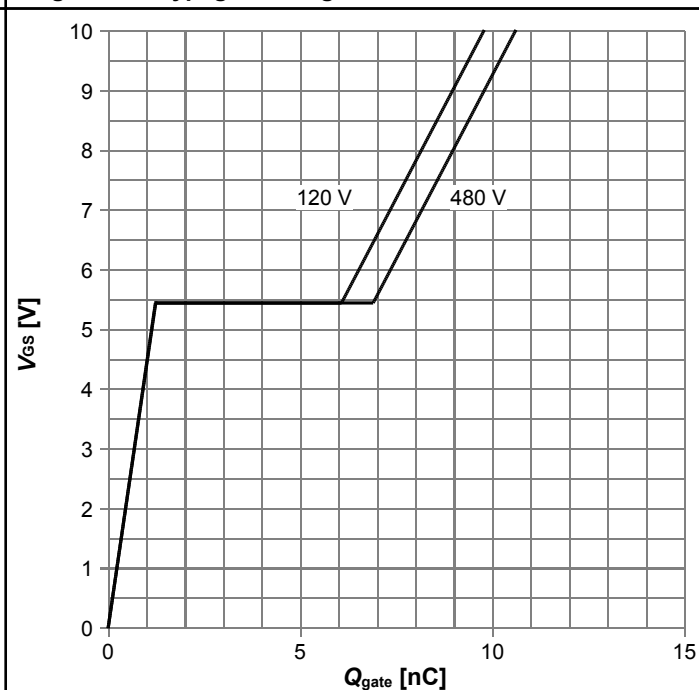

 $V_{GS} = f(Q_{gate}); I_D = 1.5 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Avalanche energy

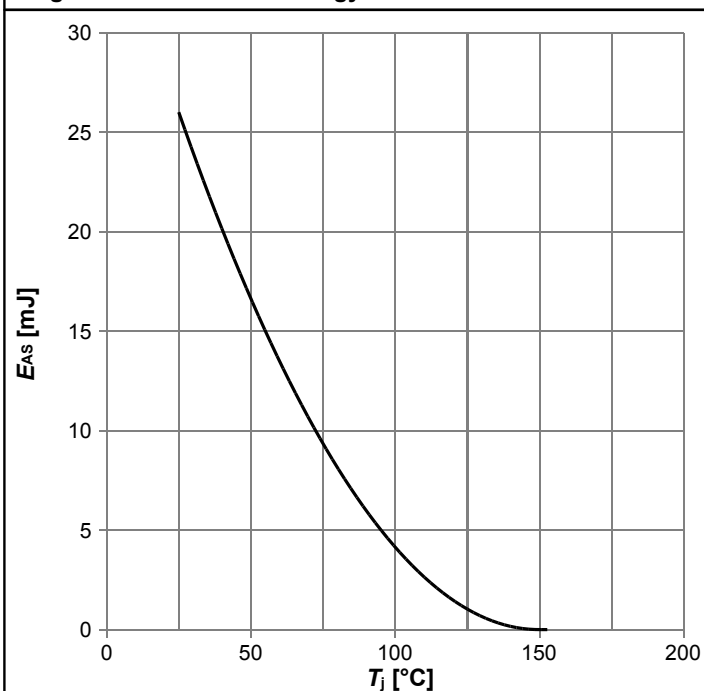

 $E_{AS} = f(T_j); I_D = 0.6 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 12: Drain-source breakdown voltage

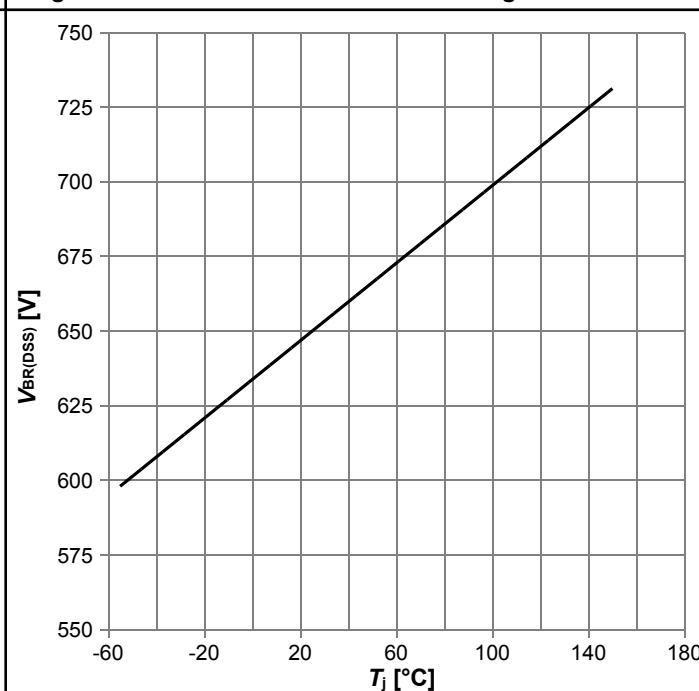
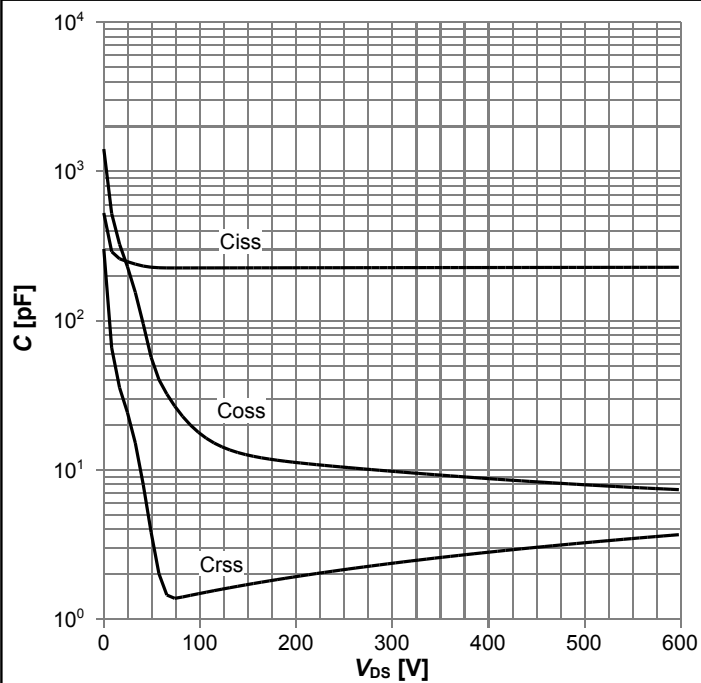
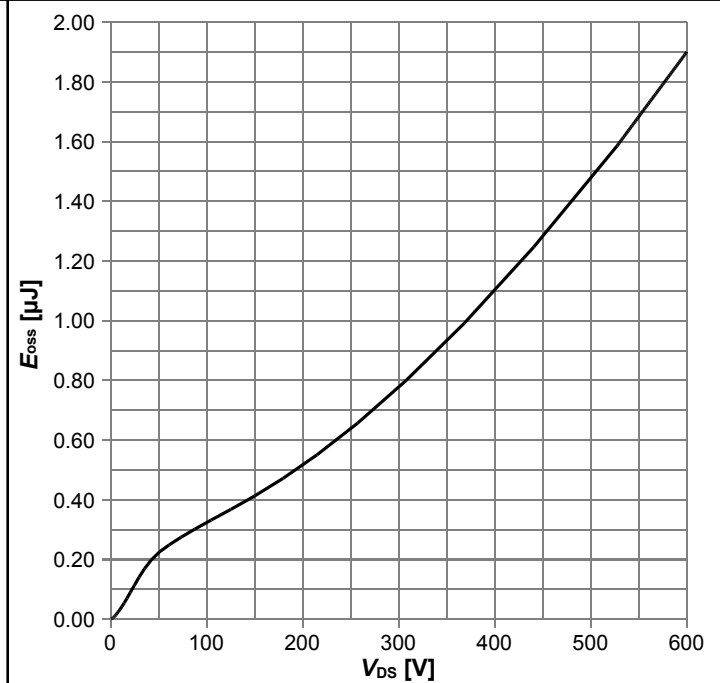

 $V_{BR(DSS)} = f(T_j); I_D = 1.0 \text{ mA}$

Diagram 13: Typ. capacitances



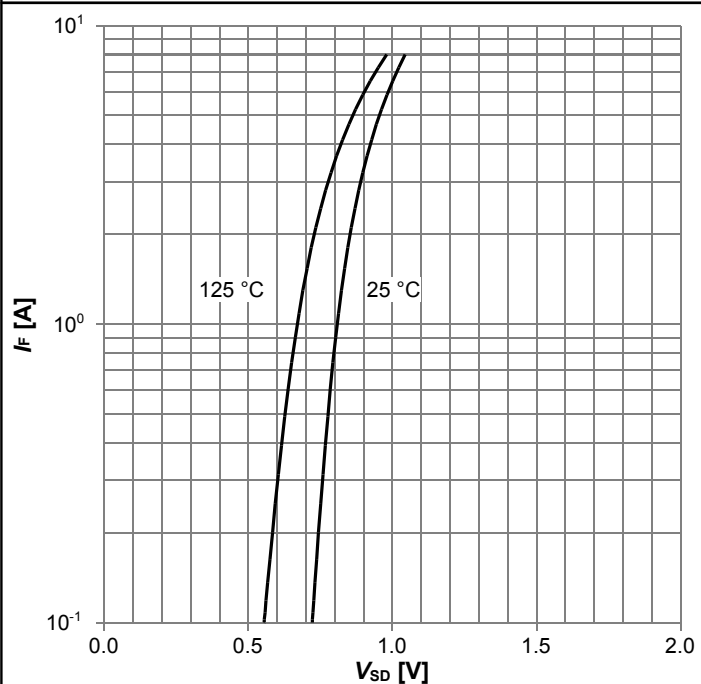
$$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$$

Diagram 14: Typ. Coss stored energy



$$E_{oss}=f(V_{DS})$$

Diagram 15: Forward characteristics of reverse diode



$$I_F=f(V_{SD}); \text{ parameter: } T_j$$

6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics

$R_{g1} = R_{g2}$

Diode recovery waveform

$t_{rr} = t_F + t_S$
 $Q_{rr} = Q_F + Q_S$

Table 9 Switching times

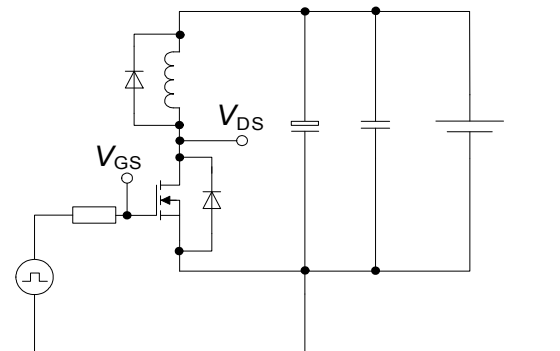
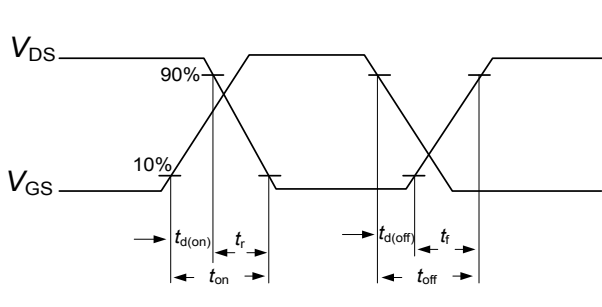
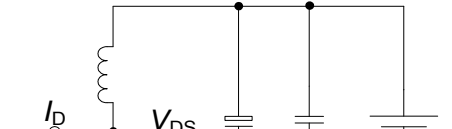
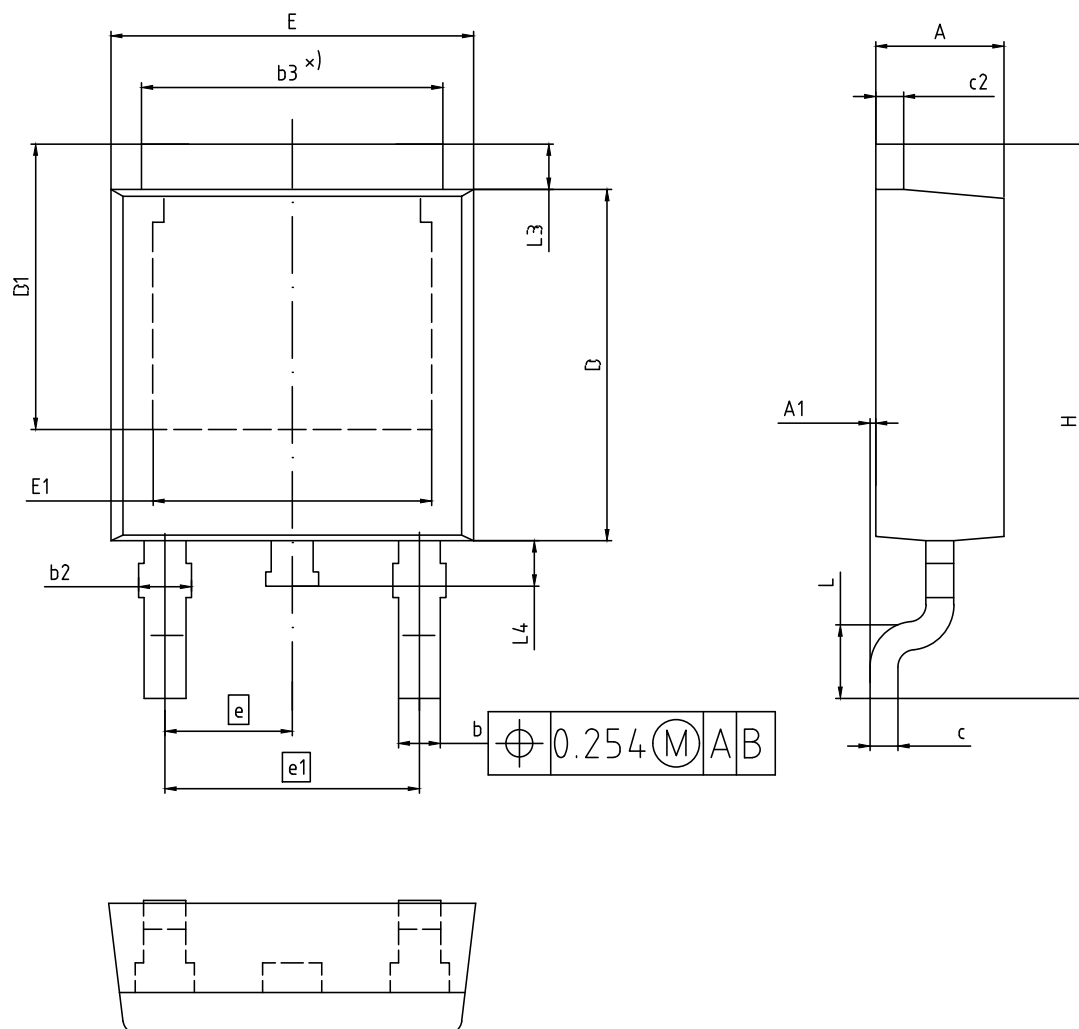
Switching times test circuit for inductive load	Switching times waveform
 <p>The circuit diagram illustrates a switching test setup for an inductive load. A MOSFET is driven by a pulse generator connected to its gate through a resistor. The gate voltage is labeled V_{GS}. The MOSFET's drain is connected to a DC source and an inductive load (represented by an inductor and a diode in parallel). The drain voltage is labeled V_{DS}. The load is connected to ground.</p>	 <p>The timing diagram shows the relationship between the drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}) during switching transitions. The diagram defines the following parameters:</p> <ul style="list-style-type: none"> $t_{d(on)}$: Delay time from the 10% rise of V_{GS} to the 90% rise of V_{DS}. t_r: Rise time of V_{DS} from 90% to 100%. t_{on}: Total turn-on time from the 10% rise of V_{GS} to the steady-state high level of V_{DS}. $t_{d(off)}$: Delay time from the 90% fall of V_{DS} to the 10% fall of V_{GS}. t_f: Fall time of V_{DS} from 90% to 10%. t_{off}: Total turn-off time from the 90% fall of V_{DS} to the steady-state low level of V_{DS}.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

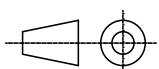
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EUROPEAN PROJECTION 
ISSUE DATE 01.04.2020

Figure 1 Outline PG-TO 252, dimensions in mm

8 Appendix A

Table 11 Related Links

- **IFX C6 Product Brief:** www.infineon.com
- **IFX C6 Portfolio:** www.infineon.com
- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design Tools:** www.infineon.com

Revision History

IPD65R1K4C6

Revision: 2020-05-26, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-07-26	Release of final version
2.1	2020-05-26	Update of the package outlines

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Published by

Infineon Technologies AG

81726 München, Germany

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