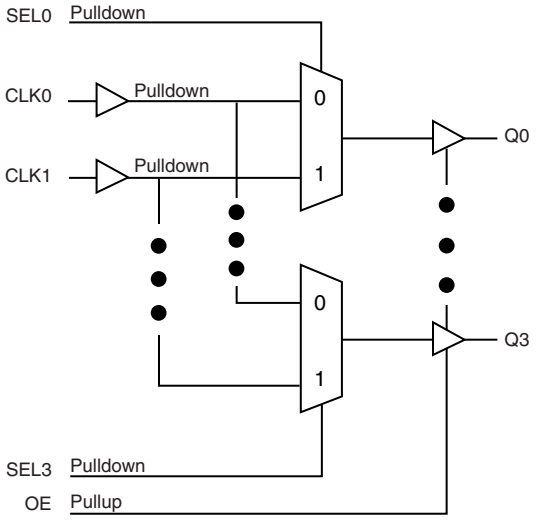
General Description

The 83054I-01 is a 4-bit, 2:1, Single-ended Multiplexer and a member of the family of High Performance Clock Solutions from IDT. The 83054I-01 has two selectable single-ended clock inputs and four single-ended clock outputs. The output has a V_{DDO} pin which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug. Possible applications include systems with up to four transceivers which need to be independently set for different rates. For example, a board may have four transceivers, each of which need to be independently configured for 1 Gigabit Ethernet or 1 Gigabit Fibre Channel rates. Another possible application may require the ports to be independently set for FEC (Forward Error Correction) or non-FEC rates. The device operates up to 250MHz and is packaged in a 16 TSSOP.

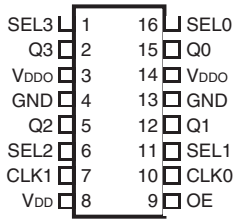
Features

- Four-bit, 2:1 single-ended multiplexer
- Nominal output impedance: 15Ω (V_{DDO} = 3.3V)
- Maximum output frequency: 250MHz
- Propagation delay: 3.2ns (maximum), V_{DD} = V_{DDO} = 3.3V
- Input skew: 170ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Output skew: 90ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Part-to-part skew: 800ps (maximum), V_{DD} = V_{DDO} = 3.3V
- Additive phase jitter, RMS at 155.52MHz, (12kHz – 20MHz): 0.18ps (typical)
- Operating supply modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



83054I-01
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 6 11, 16	SEL3, SEL2, SEL1, SEL0	Input	Pulldown	Clock select inputs. See Control Input Function Table. LVCMOS / LVTTL interface levels.
2, 5, 12, 15	Q3, Q2, Q1, Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
3, 14	V_{DDO}	Power		Output supply pins.
4, 13	GND	Power		Power supply ground.
7, 10	CLK1, CLK0	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin.
9	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V		18		pF
		V_{DDO} = 2.625V		19		pF
		V_{DDO} = 2.0V		19		pF
R_{OUT}	Output Impedance	V_{DDO} = 3.465V		15		Ω
		V_{DDO} = 2.625V		17		Ω
		V_{DDO} = 2.0V		25		Ω

Table 3. Control Input Function Table

Control Inputs	Outputs
SELx	**Qx**
0	CLK0
1	CLK1

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	100.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5%, or 2.5V±5%, or 1.8V±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current				45	mA
I_{DDO}	Output Supply Current	No Load			5	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, V_{DDO} = 2.5V±5%, or 1.8V±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current	No Load			5	mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK1, SEL0:SEL3	V_{DD} = 3.3V or 2.5V ± 5%			150	µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, SEL0:SEL3	V_{DD} = 3.3V or 2.5V ± 5%	-5			µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%	-150			µA
V_{OH}	Output HighVoltage; NOTE 1		V_{DDO} = 3.3V ± 5%	2.6			V
			V_{DDO} = 2.5V ± 5%	1.8			V
			V_{DDO} = 1.8V ± 0.2V	V_{DD} - 0.3			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%			0.5	V
			V_{DDO} = 2.5V ± 5%			0.45	V
			V_{DDO} = 1.8V ± 0.2V			0.35	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, “Load Test Circuit” diagrams.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		1.8	2.5	3.2	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.0	2.6	3.2	ns
*t*sk(o)	Output Skew; NOTE 2, 3			30	90	ps
*t*sk(i)	Input Skew; NOTE 2			40	170	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				800	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52, Integration Range: 12kHz – 20MHz		0.18		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		800	ps
odc	Output Duty Cycle	*f*out ≤ 175MHz	40		60	%
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltags and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 5: Driving only one input clock.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.1	2.6	3.1	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.3	2.7	3.1	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	125	ps
*t*sk(i)	Input Skew; NOTE 2			35	190	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				800	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52, Integration Range: 12kHz – 20MHz		0.14		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		800	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltags and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 5: Driving only one input clock.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.6	3.1	3.6	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.7	3.2	3.7	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	125	ps
*t*sk(i)	Input Skew; NOTE 2			35	195	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				800	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52, Integration Range: 12kHz – 20MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	450		850	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltags and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 5: Driving only one input clock.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		1.5	3.0	4.5	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.2	2.8	3.4	ns
*t*sk(o)	Output Skew; NOTE 2, 3			30	90	ps
*t*sk(i)	Input Skew; NOTE 2			45	190	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				800	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52, Integration Range: 12kHz – 20MHz		0.22		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle	*f*out ≤175MHz	40		60	%
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltags and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 5: Driving only one input clock.

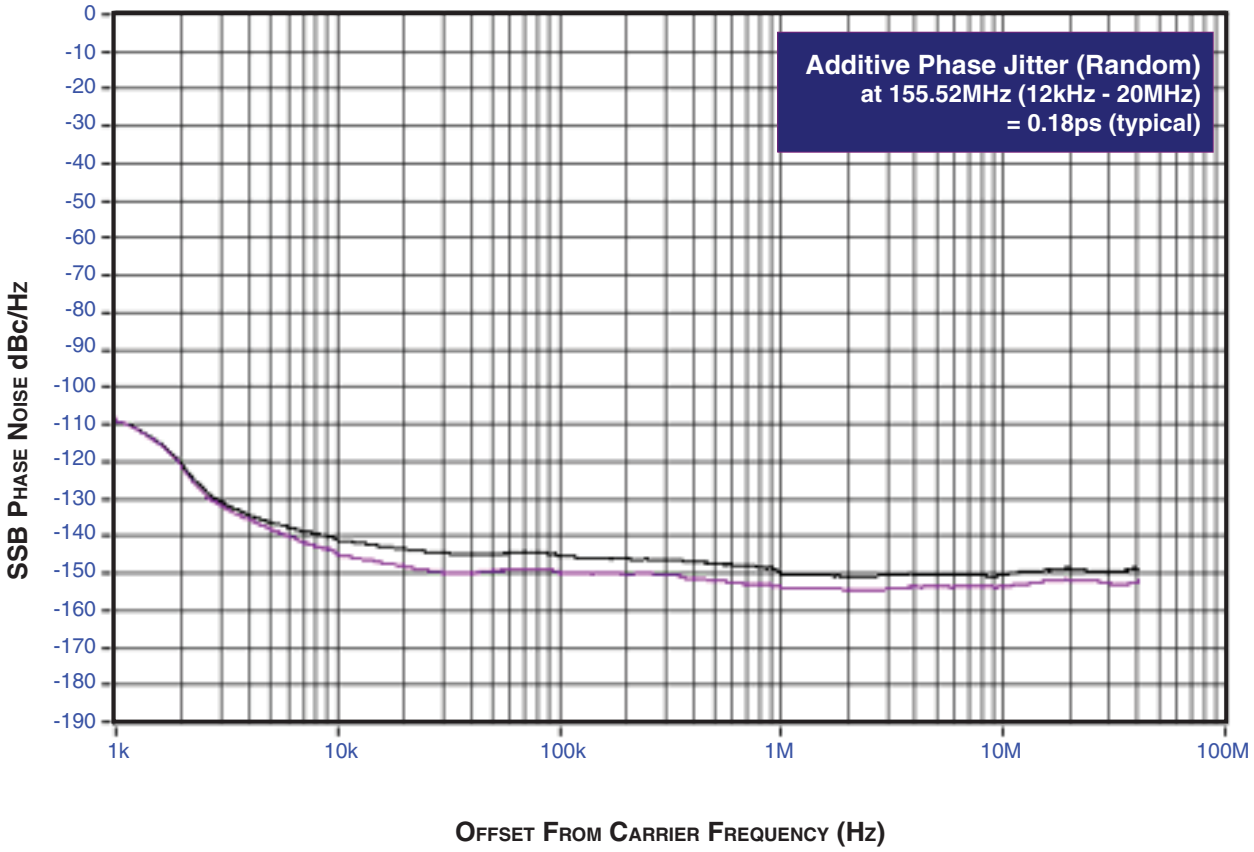
TABLE 5E. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.2	3.2	4.2	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.5	3.2	4.0	ns
*t*sk(o)	Output Skew; NOTE 2, 3			40	125	ps
*t*sk(i)	Input Skew; NOTE 2			30	145	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				800	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52, Integration Range: 12kHz – 20MHz		0.19		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	450		850	ps
odc	Output Duty Cycle	*f*out ≤ 200MHz	40		60	%
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltags and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 5: Driving only one input clock.

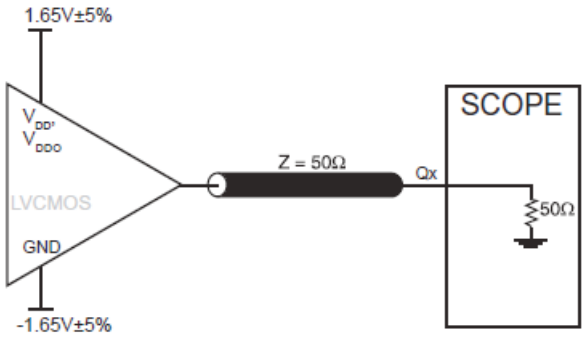
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

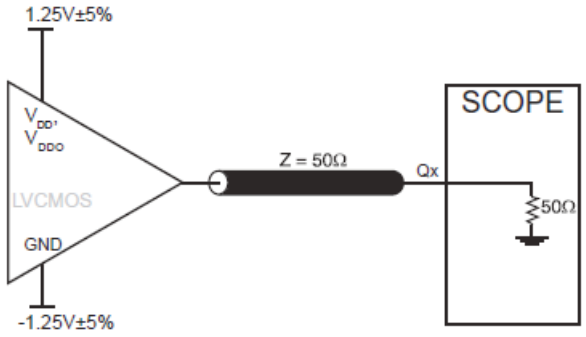


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

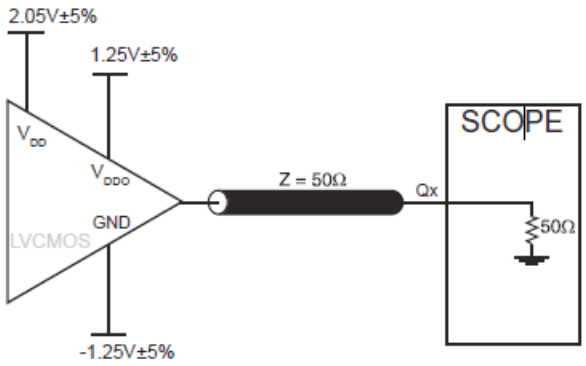
PARAMETER MEASUREMENT INFORMATION



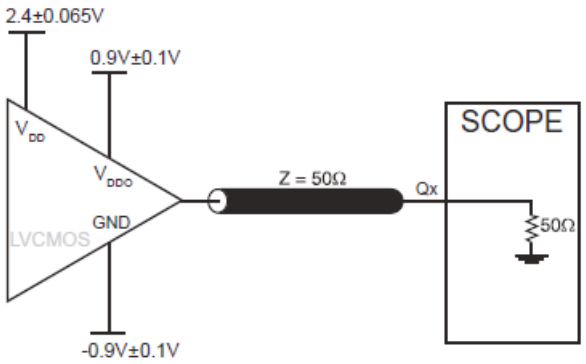
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



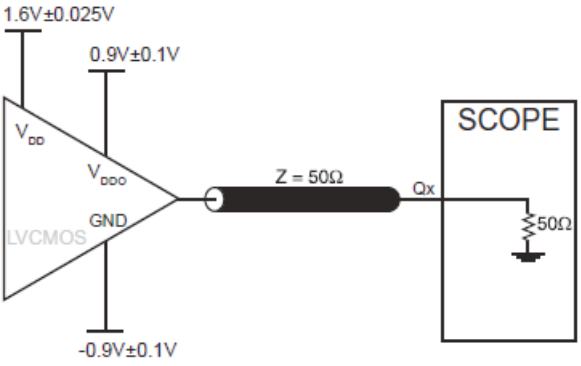
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



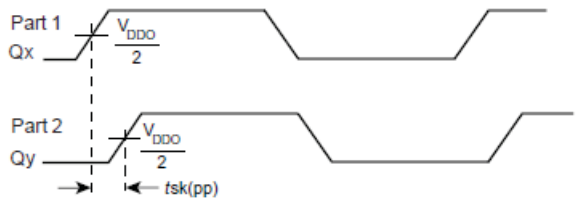
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



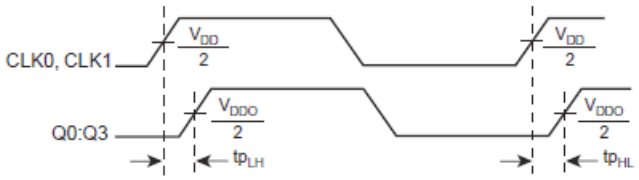
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



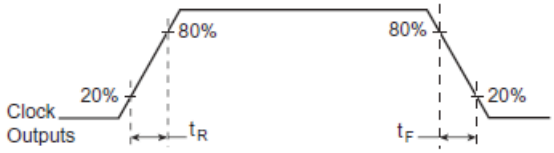
2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



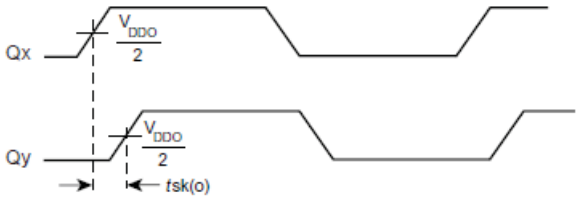
PART-TO-PART SKEW



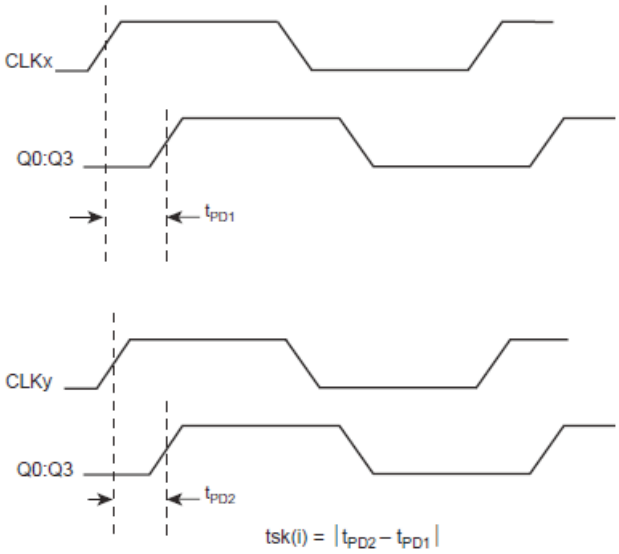
Propagation Delay



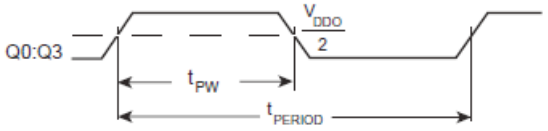
Output Rise/Fall Time



Output Skew



Input Skew



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Transistor Count

The transistor count for 83054I-01 is: 967

Package Outline - G Suffix for 16 Lead TSSOP

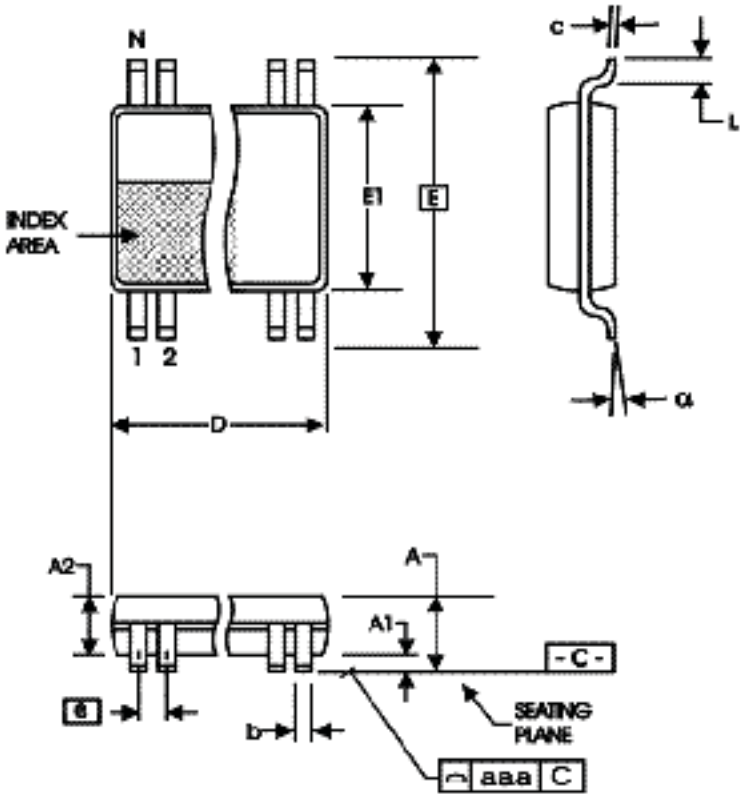


Table 6. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83054AGI-01LF	054AI01L	16 lead “Lead Free” TSSOP	Tray	-40°C to +85°C
83054AGI-01LFT	054AI01L	16 lead “Lead Free” TSSOP	Tape and Reel	-40°C to +85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T7	1 1 12	General Description - removed ICS chip and HiPerClocks. Features Section - removed reference to leaded package. Ordering Information - removed leaded parts and the LF note below the table. Updated header and footer.	12-15-15

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