

UM11665

SC18IS604-EVB evaluation board

Rev. 1.0 — 19 August 2021

User manual

Document information

Information	Content
Keywords	SC18IS604, SC18IS600, SPI to I ² C, I ² C Controller, I ² C bridge, SPI bridge
Abstract	SC18IS604 is designed to serve as an interface between the standard SPI of a host and the serial I ² C-bus. This allows the host to communicate directly with other I ² C-bus devices.



Revision history

Rev	Date	Description
v.1.0	20210819	Initial version

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

SC18IS604 is designed to serve as an interface between the standard SPI of a host (microcontroller, microprocessor, chip set, etc.) and the serial I²C-bus. This allows the host to communicate directly with other I²C-bus devices. SC18IS604 can operate as an I²C-bus master-transmitter or master-receiver. SC18IS604 controls all the I²C-bus specific sequences, protocol, arbitration and timing.

This document is intended to help the users to quickly setup, configure and operate the SC18IS604-EVB evaluation board in the users' hardware platform.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for SC18IS604-EVB evaluation board is at <http://www.nxp.com/SC18IS604-EVB>. The information page provides overview information, documentation, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the SC18IS604-EVB evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <http://community.nxp.com>.

3 Getting ready

Working with the SC18IS604-EVB evaluation board requires the kit contents.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- Quick Start Guide

4 Getting to know the hardware

The SC18IS604-EVB board is designed to be connected to an external SPI master via a 7-pin male (JP1) header. The SC18IS604-EVB evaluation board has an on-board I²C slave serial EEPROM and an I²C slave LED blinker, which can be directly accessed by the external SPI master via SC18IS604. The external SPI master can write, read, and program the serial EEPROM/LED blinker without requiring an I²C slave to be connected to the board.

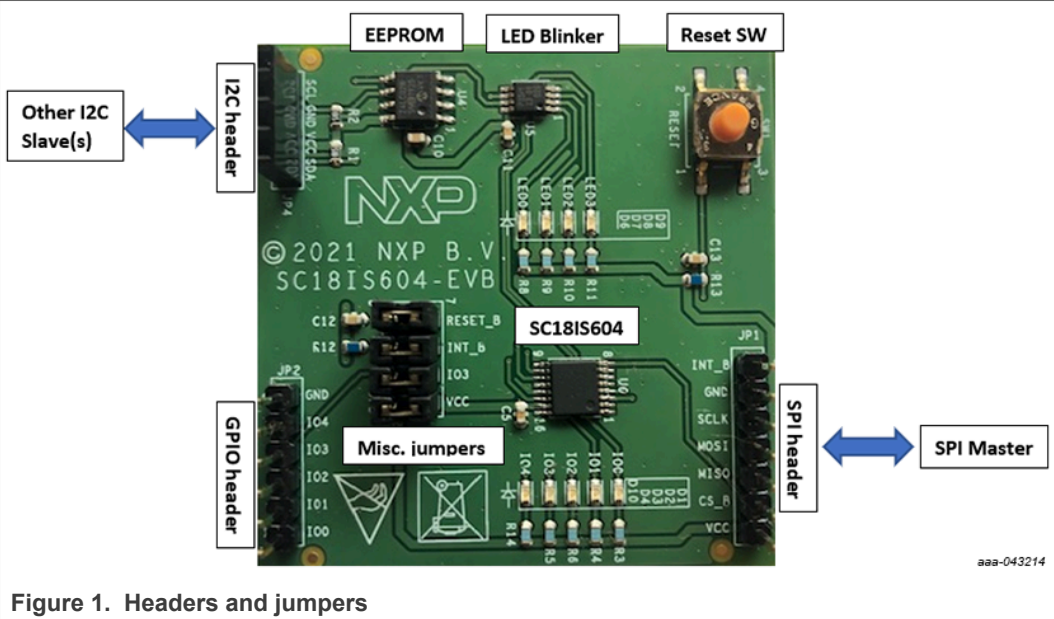
The 3V3 power for the evaluation board should be supplied via this I²C interface header as well.

The SC18IS604-EVB evaluation board also has an I²C interface header (JP4) to allow other I²C slave devices to be connected to the SC18IS604-EVB evaluation board. These

I²C slave devices can be accessed directly by the SPI master via the SC18IS604 SPI to I²C bridge.

4.1 Headers and jumpers

Please refer to [Figure 1](#) to find the location of connectors and jumpers on the SC18IS604-EVB evaluation board.



4.2 Jumper settings

Table 1. Jumper settings

JP5 Misc. Header	Jumper on/off	Comment
1 - 2	ON	Pull out and insert current meter if SC18IS604 current is to be measured
3 - 4	ON	Route GPIO 3 to JP2
5 - 6	ON	Enable pull-up on -INT
7 - 8	ON	Enable pull-up on -RESET

Table 2. JP1 - SPI header

JP1 – SPI Header	Function
1	-INT
2	GROUND
3	SCLK
4	MOSI
5	MISO
6	-CS
7	VCC

Table 3. JP4 - I2C header

JP4 – I2C Header	Function
1	SCL
2	GROUND
3	VCC
4	SDA

Table 4. JP2 - GPIO

JP2 – GPIO	Function
1	GPIO0
2	GPIO1
3	GPIO2
4	GPIO3
5	GPIO4
6	GROUND

4.3 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the SC18IS604-EVB evaluation board are available at <http://www.nxp.com/SC18IS604-EVB>.

4.4 Sample control sequences from SPI master

4.4.1 Register read

```
0x21 0x00 0xFF // Read register 0x00 where 0xFF is an SPI dummy byte
```

4.4.2 Register write

```
0x20 0x00 0xAA // Write register 0x00 with AA
```

4.4.3 GPIO as input

```
0x20 0x00 0x00 // program GPIOs as inputs  
0x21 0x01 0xFF // read IOState register
```

4.4.4 GPIO as output

```
0x20 0x00 0xAA // program GPIOs as output (push-pull) 0x21 0x01  
0x20 0x01 0xFF // write to IOState register to set GPIO pins
```

4.4.5 I²C clock configuration

```
0x20 0x02 0x05 // Set I2C clock to 375KHz
```

4.4.6 Device ID read

```
0x50 0xFE // Read device ID into buffer
0x06 0xFF 0xFF ..... 0xFF // read 16 bytes from buffer, return data 0x53
                                // 0x43 0x31 0x38 0x49 0x53.. 0x2E 0x30 0x2E 0x32
```

4.4.7 On-board EEPROM write and read

```
0x00 0x04 0xA0 0x00 0xAA 0x77 0xCC // write AA 77 CC to EEPROM
0x00 0x01 0xA0 0x00
0x01 0x03 0xA1 // read 3 bytes from EEPROM
0x06 0xFF 0xFF 0xFF 0xFF // read 4 bytes from buffer, the last three bytes should be AA, 77, CC
```

4.4.8 Blinking on-board LEDs

```
0x00 0x06 0xC4 0x11 0x97 0x80 0x00 0x00 0xAA // write 6 control bytes to I2C blinker at address 0xC4
```

5 Errata list

Table 5. Errata list

Date	Errata Description	Demo Impact	Solution
-	None	None	None

6 Legal information

6.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or

the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Jumper settings	5	Tab. 4.	JP2 - GPIO	6
Tab. 2.	JP1 - SPI header	5	Tab. 5.	Errata list	7
Tab. 3.	JP4 - I2C header	6			

Figures

Fig. 1.	Headers and jumpers	5
---------	---------------------------	---

Contents

1	Introduction	4
2	Finding kit resources and information on the NXP web site	4
2.1	Collaborate in the NXP community	4
3	Getting ready	4
3.1	Kit contents	4
4	Getting to know the hardware	4
4.1	Headers and jumpers	5
4.2	Jumper settings	5
4.3	Schematic, board layout and bill of materials	6
4.4	Sample control sequences from SPI master	6
4.4.1	Register read	6
4.4.2	Register write	6
4.4.3	GPIO as input	6
4.4.4	GPIO as output	6
4.4.5	I2C clock configuration	7
4.4.6	Device ID read	7
4.4.7	On-board EEPROM write and read	7
4.4.8	Blinking on-board LEDs	7
5	Errata list	7
6	Legal information	8

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 19 August 2021
Document identifier: UM11665