HDG204-WiFi 802.11b+g System in Package

Data Sheet

HDG204

WiFi SIP component

H&D Wireless

Revision History

Revision	Revision date	Description
PA1	2009-08-22	First issue
PA2	2011-01-11	Revised pin out
PA3	2011-02-18	Added landpattern
PA4	2011-03-11	Updated reference design
PA5	2011-11-24	Added measurements in landpattern

CONTENTS

1 INTRODUCTION

1.1 Overview

HDG204 is a complete WLAN System In Package, SIP, solution specifically designed to address the proliferation of Wi-Fi technology into embedded devices. HDG204 enables a cost efficient ultra low power, high performance and feature rich client solution. It provides up to 54 Mbit/s data rate when operating in the OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.
HDG204 integrates RF IC, baseband/MAC IC, EEPROM and RF filters into a highly integrated and optimized SIP (System In Package) solution with high quality and reliability. This minimizes the need of external components, simplifying assembly and test.
The integrated circuits are implemented in state of the art processes like SiGe in 0.35um for the radio and 0.13um 1.2V CMOS for the baseband/MAC. This highly integrated solution is optimized for customer applications running on a host CPU.
The host interface supports SDIO/SPI and UART. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces. Baseband firmware, FW, is stored on the host and downloaded at start up. MAC address, trimming values etc are stored in the on board EEPROM.

1.2 Key Features

- Data Rates: 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54Mbps
- Modulation: QPSK, 16QAM, 64QAM DBPSK, DQPSK, CCK, OFDM with BPSK
- WEP and AES hardware encryption accelerator up to 128 bits
- Adjustable output power. Max +18dBm (CCK).
- Advanced on-chip RF filter
- Selection (DFS) for spectrum management and Transmit Power Control (TPC).
- Low power consumption due to efficient class AB PA design
- LDO:s for RF-VCO and crystal oscillator for lower pushing
- Support for an external 32kHz real time clock
- Extensive DMA hardware support for data flow to reduce CPU load.
- External clock 40MHz supported, internal trimming capacitors allows the use of low cost crystal
- Internal Boot-ROM. This allows firmware to be downloaded into SRAM from the host
- Advanced power management for optimum power consumption at varying load.
- External interfaces SDIO/SPI
- Power Supplies 3.3 V and 1.2 V
- Small footprint 8 x 8 mm (64 mm2), height 1.4 mm max
- RoHS Compliant

2 HARDWARE ARCHITECTURE

2.1 Block Diagram

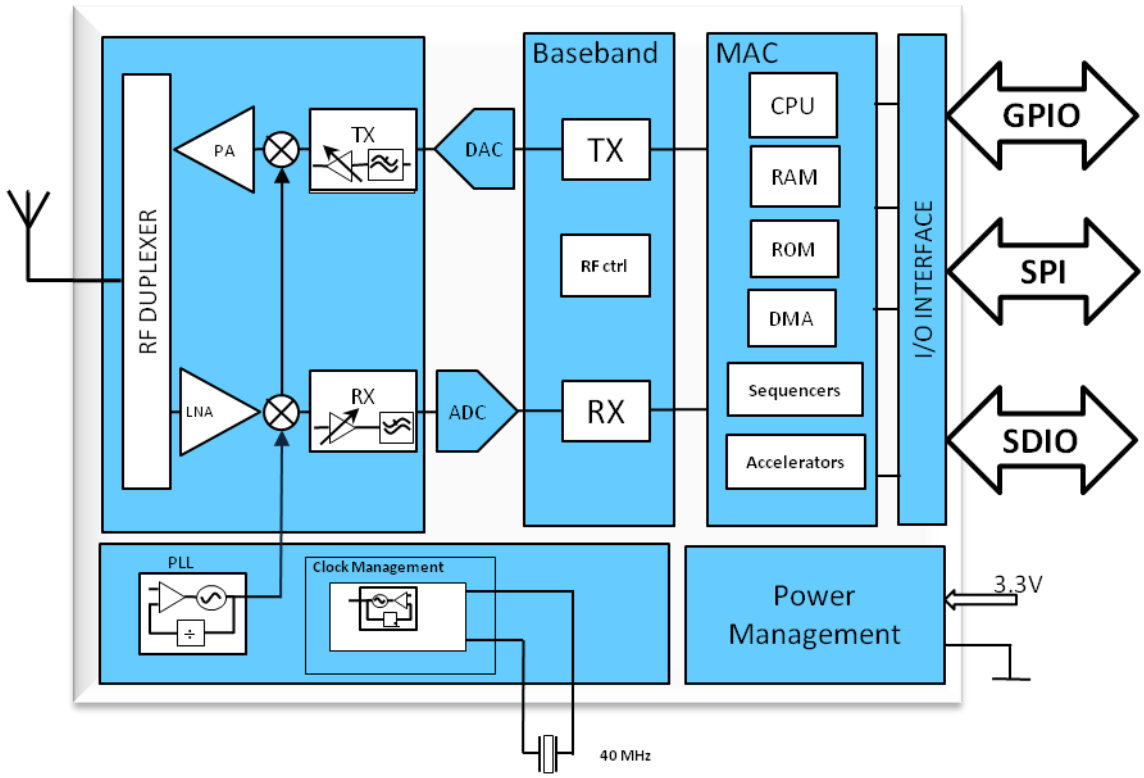

Figure 2.1: Block diagram.

2.2 Order information

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Part No.	Clock option	Package	Shipment package
HDG204-DN-2	External clock support	QFN 44+4 pins, 8.0 x 8.0 mm	Tape & Reel
HDG204-DN-3	External clock support	QFN 44+4 pins, 8.0 x 8.0mm	Tray

Table 2-1: Order information.

3 ELECTRICAL DATA

3.1 Absolute maximum ratings

Rating	Min	Max	Unit
Supply voltage	0	4	V
Supply voltage I/O	0	4	V
Input RF level		10	dBm
Storage temperature	-50	+125	°C
Lead temperature (No Pb), solder 40sek*)		260	°C

Table 3-1:Absolute maximum ratings. Exceeding any of the maximum ratings, even briefly lead to deterioration in performance or even destruction. Values indicates condition applied one at the time.

*Ref. IPC/JEDEC J-STD-020C, July 2004

3.2 Electro Static Discharge

HDG204 withstands ESD voltages up to 2000 V tested with HBM (Human Body Model) according to JESD22-A114 and up to 300 V tested with MM (Machine Model) according to JESD22-A115.

3.3 Recommended operating conditions

Rating	Min	Typ.	Max	Unit
Supply Voltage VCC	2.75	3.3	3.6	V
Supply Voltage VBAT_P	2.7	3.3	3.6	V
Supply Voltage VBAT_32K	VBAT_P-0.6	3.3	3.6	V
Supply Voltage VPA	2.7	3.3	3.6	V
Supply Voltage, DVDD	1.15	1.20	1.25	V
Supply Voltage VDD_IO, VDD_SDIO	1.7	3.3	3.6	V
Operating temperature	-40	+25	+85	°C

Table 3-2: Recommended operating conditions

3.4 Power Consumption

3.4.1 Current Consumption

Mode	Conditions	Supply Pin	Voltage	Min	Typ.	Max	Unit
All modes		VBAT_P+VCC+ VPA+VBAT_32K	3.6 V			250	mA
All modes		VPA	3.6 V			150	mA
All modes		VBAT_P+VCC	3.6 V			150	mA
All modes		DVDD	1.2 V			100	mA
All modes	25ºC	VBAT_32K	3.3 V		10		µA
Tx	25ºC	DVDD	1.2 V		15		mA
Rx	25ºC	DVDD	1.2 V		60		mA
Sleep	25ºC	VBAT_P+VCC+ VPA+VBAT_32K	3.3 V		30		µA
Sleep	25ºC	DVDD	1.2 V		110		µA
Shutdown	25ºC DVDD OFF	VBAT_P+VCC+ VPA+VBAT_32K	3.3 V		15		µA

Table 3-3: Current consumption in different modes

3.4.2 Power Consumption

T_{amb}=25°C, VCC=VBAT_P=VBAT_32K=VPA=3.3 V, DVDD =1.2 V

Mode	Output Power	Power Consumption	Comments
TX 802.11b	+17 dBm	725 mW	1, 2, 5.5, 11 Mbit/s
TX 802.11g	+14 dBm	590 mW	6, 9, 12, 18, 24, 36, 48, 54 Mbit/s
RX 802.11b	N/A	220 mW	
RX 802.11g	N/A	230 mW	
Power Save	N/A	0,4 mW	Receive only, 2s RX beacons
Sleep	N/A	0,2 mW	No receive, FW loaded, only LFC running
Shutdown	N/A	0,05 mW	No FW loaded, DVDD OFF

Table 3-4: Power consumption in different modes.

3.5 RF Performance

VCC=VPA= 2.75 – 3.6V, DVDD=1.15 - 1.25V External supply, Tamb= -40 – +85°C

Parameter	Conditions	Min	Typical	Max	Units
Frequency range		2400		2500	MHz
RF impedance			50		ohm
TRANSMITTER PERFORMANCE					
Output power	QPSK	+16,5	+17	+17,5	dBm
Output power	OFDM 54Mbit/s	+13,5	+14	+14,5	dBm
EVM at +15dBm	QPSK		30	35	%
EVM at +11dBm	OFDM 54MBit/s		3.5	5	%
RECEIVER PERFORMANCE					
Receiver sensitivity	DPSK 1Mbit/s		-96		dBm
Receiver sensitivity	QDPSK 2Mbit/s		-92		dBm
Receiver sensitivity	CCK/DPSK 5.5Mbit/s		-91		dBm
Receiver sensitivity	CCK/BPSKK 11Mbit/s		-88		dBm
Receiver sensitivity	OFDM 6Mbit/s		-91		dBm
Receiver sensitivity	OFDM 9Mbit/s		-90		dBm
Receiver sensitivity	OFDM 12Mbit/s		-88		dBm
Receiver sensitivity	OFDM 18Mbit/s		-86		dBm
Receiver sensitivity	OFDM 24Mbit/s		-83		dBm
Receiver sensitivity	OFDM 36Mbit/s		-80		dBm
Receiver sensitivity	OFDM 48Mbit/s		-76		dBm
Receiver sensitivity	OFDM 54Mbit/s		-74		dBm

Table 3-5: RF performance

3.6 Digital pin characteristics

3.6.1 SDIO timing characteristics

The SDIO/SPI-interface can run in two different modes, Default mode and High speed mode. SDIO 1-bit default mode is selected at Power On Reset. The default mode is showed in Fig. 3.6.1 and table: 3.6. For the high speed mode see Fig. 3.2 and table: 3.7. Condition: VDDIO= 1.7 – 3.6 V, TA= -40 – +85°C

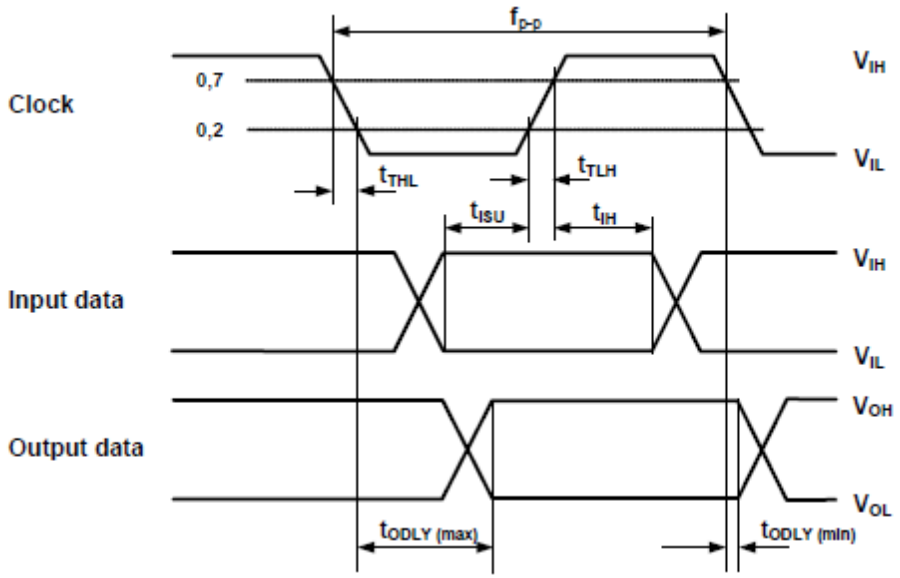

Figure 3-1: SDIO/SPI timing diagram (default mode)

Parameter	Symbol	Min	Max	Unit	Comments
Input set-up time	tISU	5		ns	
Input hold time	tIH	5		ns	
Clock fall time	tTHL		10	ns	
Clock rise time	tTLH		10	ns	
Output delay time	tODLY	0	14	ns	

Table 3-6: SDIO timing parameter values (default mode)

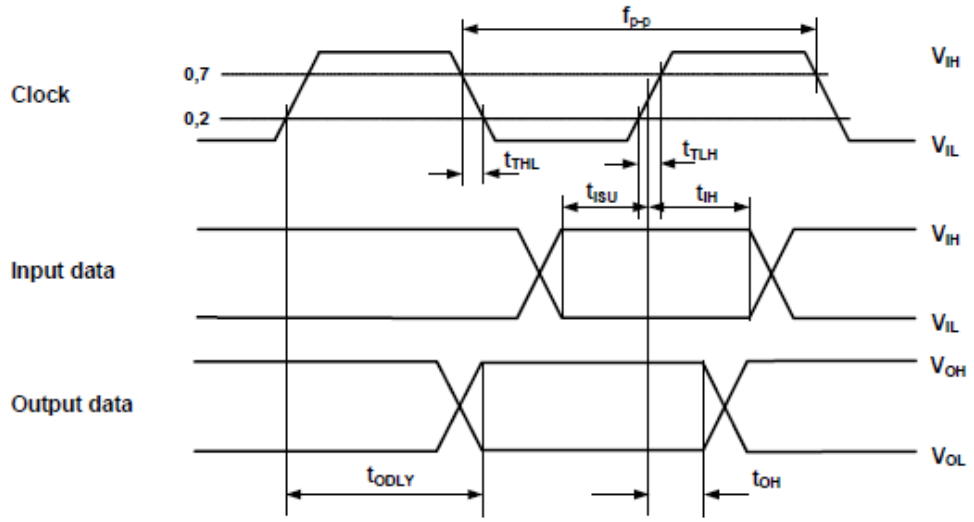

Figure 3-2: SDIO timing diagram (high speed mode)

Parameter	Symbol	Min	Max	Unit	Comments
Clock fall time	tTHL		3	ns	
Clock rise time	tTLH		3	ns	
Output delay time	tODLY	2,5	14	ns	
Output hold time	tOH	2.5		ns	

Table 3-7: SDIO timing parameter values (high speed mode)

3.6.2 Digital input IPU and IPD

IPU (Input pin with pull-up) Input with internal pull-up includes a high impedance input buffer. The input has pull-up that ensures that the pad is detected as high if it is left open.
IPD (Input pin with pull-down) Input with an internal pull-down includes a high impedance input buffer. The input has a pull-down that ensures that the pad is detected as high if it is left open.
Both configurations are also protected against over-voltages and ESD with a protection circuitry, see Figure 3-3. The pins configured according to this are stated IPU and IPD under Type in Table 4-1.

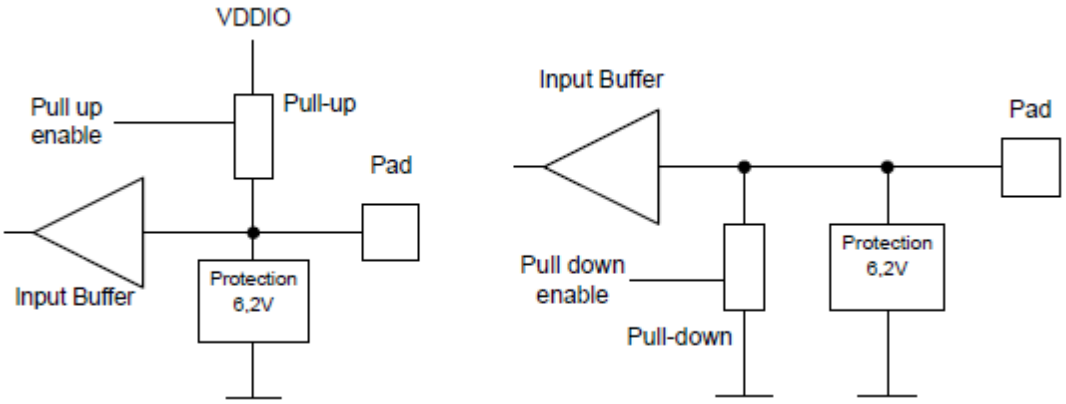

Figure 3-3: Function schematics of the IPU and IPD input pad configurations.

Parameter	Symbol	Min	Typ.	Max	Units	Comments
Input low voltage	VIL	-0.3		0.25*VIO	V	
Input high voltage	VIH	0.625*VIO		VIO+0.3	V	
Input leakage current	IIL	-1		1	µA	
Input pin capacitance	CIP		2,5		pF	
VDDIO, VDD_SDIO	VIO	1.7		3,6	V	

Table 3-8: IPU and IPD pin DC characteristics.

3.6.3 Digital input/output pad (I/O)

The I/O pin functional schematic is stated in Fig. 3.4. It includes an input buffer and an output buffer with an enable/disable bit. No pull-up or pull-down is available on this type of pad.

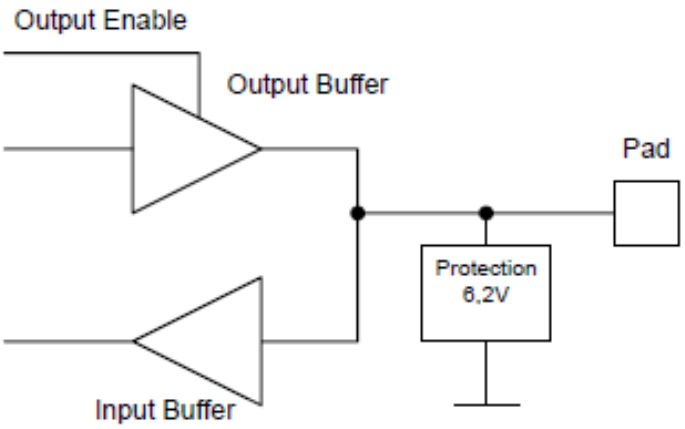

Figure 3-4: Function schematics of the I/O input pad configuration.

Parameter	Symbol	Min	Typ.	Max	Units	Comments
Input low voltage	vIL	-0.3		0.25*V_{IO}	V	
Input high voltage	vIH	0.625*V_{IO}		V_{IO}+0.3	V	
Input leakage current	iIL	-1		1	µA	
Output low voltage	vOL			0.125*V_{IO}	V	I_{out}<1mA
Output high voltage	vOH	0.75*V_{IO}			V	I_{out}>-1mA
Input pin capacitance	cIP		2.5		pF	
VDDIO, VDD_SDIO	vIO	1.7		3.6	V	

Table 3-9: I/O pin DC characteristics

3.6.4 Protection digital pins

All digital pins are protected against over-voltage with a “snap-back” circuit connected between the pad and GND. The “snap-back” voltage is 6.2 V and the holding voltage is 6 V. This provides a satisfying protection against over voltages and ESD. Also there is a diode included to protect against reversed voltages.

3.6.5 Analogue input A1 and A2

There are two different analogue input pad types. One (A1) for I/O using higher voltages than 1.8 V and another (A2) for I/O using voltages below 1.8 V (i.e. supplied from the 1.2 V supply), see schematic in Figure 3-5. The A1 is protected with a diode to the supply voltage.
The A2 is protected from voltages above 3 x V_{diode} (about 2 V at Ta=25°C)

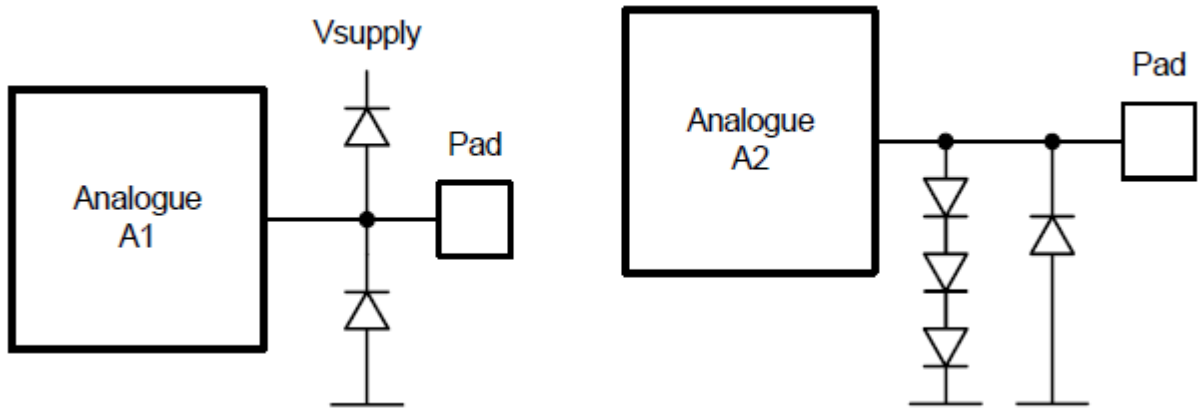

Figure 3-5: Schematics of analogue inputs A1 and A2

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One digital input, SHUTDOWN uses the analog pad A1.
SHUTDOWN is a dedicated pin used for controlling the shutdown function.
For pin data see Table 4-1

Parameter	Symbol	Min	Typ.	Max	Units	Comments
Input low voltage	vIL	-0.3		0.2	V	
Input high voltage	vIH	1.5		VBAT_32K+0.3	V	
Input leakage current	iIL	-1		+1	µA	
Input current	iIN			2	mA	During low to high transition

Table 3-10: SHUTDOWN pin DC characteristics.

4 PIN CONFIGURATIONS

4.1 Pin Configuration

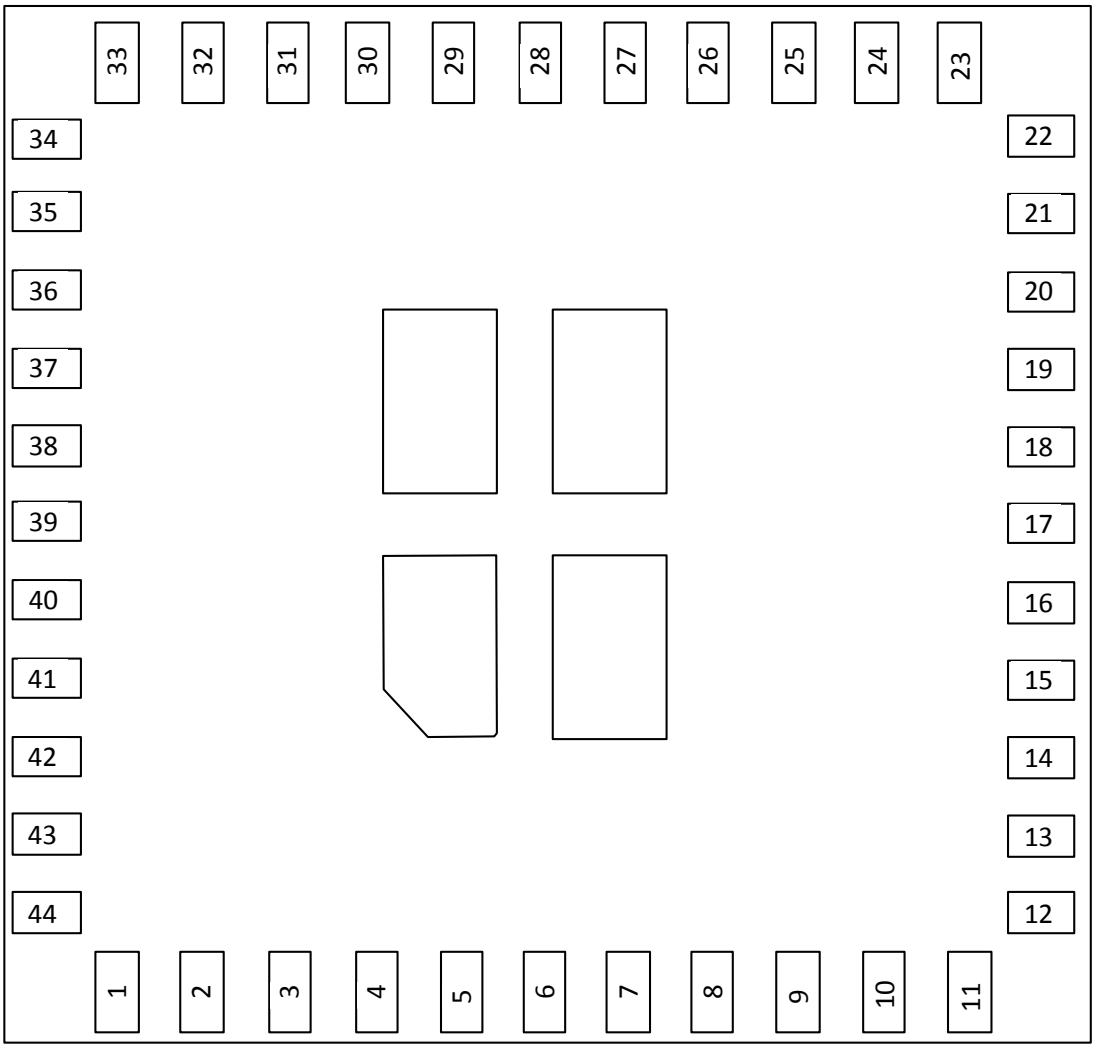


Figure 4-1: Package pin out. Top view

4.2 Pin assignments

Pin	Function	Type	Description
1	SDIO CLK	IPU	SDIO Clock, SDIO/SPI CLK
2	SDIO DAT0	I/O	SDIO Data 0, SDIO/SPI MISO
3	SDIO DAT1	I/O	SDIO Data 1, SDIO/SPI IRQ
4	GND	S	Ground
5	ANT_WLAN	RF	Antenna Port (50 Ohm) for WLAN

6	GND	S	Ground
7	ICE_TDI	IPU	ICE Test Data Input, do not connect
8	ICE_TRST	IPU	ICE Test Reset, do not connect
9	ICE_TCK	IPU	ICE Test Clock, do not connect
10	NO CONNECTION	-	Do not connect
11	ICE_TMS	IPU	ICE Test Mode Select, do not connect
12	VPA	S	Power supply for RF Power Amplifier
13	ICE_TDO	I/O	ICE Test Data output, do not connect
14	NO CONNECTION	-	Do not connect
15	NO CONNECTION	-	Do not connect
16	NO CONNECTION	-	Do not connect
17	NO CONNECTION	-	Do not connect
18	DVDD	S	DIGITAL VDD 1.2V, de-couple with a 1uF capacitor to GND
19	NO CONNECTION	-	Do not connect
20	VCC_REG_VCO	S	LDO Decoupling. Connect a 27pF capacitor to GND
21	VCC	S	Radio supply 3.3V, de-couple with a 1uF capacitor to GND
22	NO CONNECTION	-	Do not connect
23	VCC_REG_PLL	S	LDO Decoupling. Connect a 27pF capacitor to GND
24	SHUTDOWN	A1	Shutdown pin. Active Low
25	40MHz IN/EXT_REF_IN	I	HFC Oscillator IN
26	40MHz OUT/ EXT_REF_OP	O	HFC Oscillator OUT
27	DCDC_ENABLE	A1	Connect to GND. Internal DC/DC not used
28	VDD_CKL_12	S	HFC X-tal driver decoupling. Connect a 100nF capacitor to GND
29	VDD_CKL_26	S	HFC PLL decoupling. Connect a 1uF capacitor to GND
30	VBAT_32K	S	32 kHz clock supply. Connect a 100nF capacitor to GND
31	TEST_EN	IPD	Test Enable with internal pull down, connect to GND
32	DCO	S	DC/DC Converter out. Leave open
33	NO CONNECTION	-	Do not connect
34	VBAT_P	S	Main supply 3.3V. De-couple with a 1uF capacitor to GND
35	RESET_N	IPU	Digital Reset with internal pull up. Active Low

36	EXT_PWR_EN	I/O	External Power Control. Connect 100k resistor to GND
37	LFC	I/O	32KHz external clock
38	VDD_IO	S	VDD_IO Supply for digital I/Os except SDIO domain
39	NO CONNECTION	-	Do not connect
40	SDIO DAT3	I/O	SDIO Data 3, SDIO/SPI CARD_SELECT active low
41	SDIO CMD	I/O	SDIO Command, SDIO/SPI MOSI
42	VDD_MAC_BB	S	Internal 1.2V Decoupling, connect a 330nF capacitor to GND
43	VDD_SDIO	S	SDIO domain I/O Supply 3.3V
44	SDIO DAT2	I/O	SDIO Data 2
45	GND	S	Ground
45	GND	S	Ground
45	GND	S	Ground
45	GND	S	Ground

Table 4-1: Pin Description for the package.

5 APPLICATION INFORMATION

5.1 Power Supply

HDG204 should be powered by dual supplies 3.3V and 1.2V (typical).

5.1.1 Main supply

The main power is connected to the VCC, VBAT_P, VPA and VBAT_32K pins. The ripple on VCC should be less than 10mV p-p. External decoupling capacitors should be connected, min 1uF on VCC, VBAT_P and DVDD, min 100nF on VBAT_32K.
The 1.2V supply should be fed externally. Leave the DCO pin open.

5.1.2 Interface Supply

HDG204 has two IO-Supply voltage pins. VDD_SDIO is for the SDIO-bus.
All other I/O-pins are supplied by VDD_IO.
All IO-Supply voltage pins shall be connected to a supply voltage even if some interfaces are not used

5.1.3 Ground pins

The HDG204 is an RF device and requires as such a good RF grounding. Connect pin 3 and the four pads in the bottom center, pins 45-48, to GND.

5.2 Clocks

5.2.1 High Frequency Clock, HFC

The circuit has an internal oscillator driver that only needs a 40 MHz external crystal and one capacitor to generate the clock signal. The crystal is connected between the pins 40MHz_IN and 40MHz_OUT. A 0.5 pF capacitor should be connected between the 40MHz_IN and 40MHz_OUT pins. The crystal should be placed as close as possible to the circuit pins. Stray capacitances to GND for crystal interconnect traces should be as small as possible. See Figure 5-1

Parameter	Condition	Min	Typ.	Max	Unit
Frequency			40		MHz
CL			8		pF
Cm		3.5		6.0	fF
C0 (shunt cap)		0.5		2.0	pF
Equiv Rs		0		60	ohm
Frequency tolerance	Ta=25 °C	-15		15	ppm
Freq vs temp	Ta= -40 – +85 °C	-15		15	ppm

Table 5-1: Recommended crystal parameters

Condition Min Max Unit

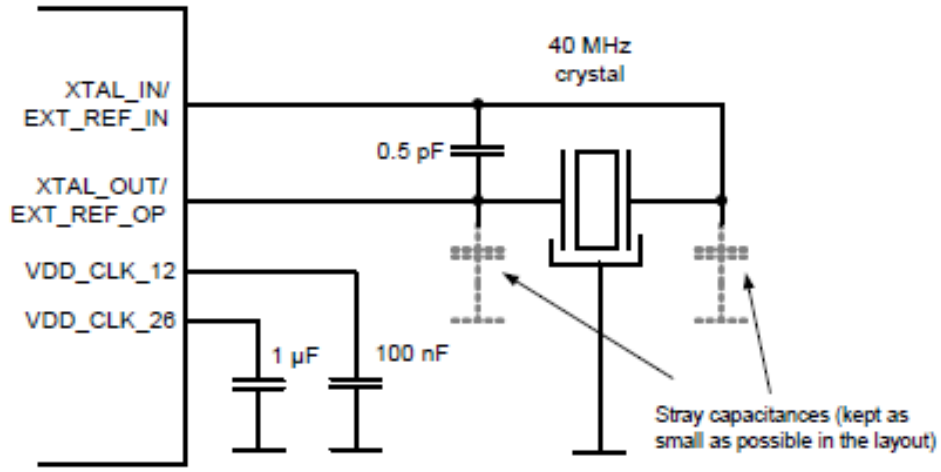


Figure 5-1: Reference clock setup

5.2.2 Low frequency clock, LFC

HDG204 utilize an external 32 kHz clock for keeping Real Time. It is connected to the LFC_IN pin. Internal Real Time is kept by FW, calibrating the LFC against the more accurate HFC in runtime. Thus a fairly wide LFC frequency range can be used.

Parameter	Min	Typ.	Max	Unit	Note
LFC frequency	30	32	34	kHz	
Clock accuracy	-2000		2000	ppm	
Duty cycle	30	50	70	%	

Table 5-2: External LFC requirements

5.3 Reset Pin

The RESET_N pin is active low. It has an internal pull-up, can be left unconnected. Pulling the RESET_N pin low resets all digital logic.
Note: An internal RESET is generated at Power On with the same function as pulling the RESET_N pin low. All VBAT power supply pins must be discharged close to GND, typically below 0.2 Volt, for this Power On Reset to be generated at a following Power On.

5.4 Shutdown

The SHUTDOWN pin shall be set high during normal operation. Pulling the SHUTDOWN pin low, sets HDG204 in Shutdown mode. This turns OFF most parts of the circuit and minimizes the current consumption. All I/O interface pins are set to predefined states (high, low or high-z) when in Shutdown mode. For minimum power consumption keep VBAT_P and VCC ON but turn DVDD, external 1.2 V, OFF while the SHUTDOWN pin is low.
To end Shutdown mode set SHUTDOWN pin high and reload FW.

For more information regarding the use of SHUTDOWN refer to Power On sequence and Shutdown sequence.
Note: During Power ON, with SHUTDOWN low, before loading of FW, pin EXT_PWR_EN is high and all other I/O-pins are high-z. With SDHUTDOWN high, load FW and let it start, then when SHUTDOWN is set low all I/O-pins will be set according to their FW defaults.
Application Information

5.5 Power save

Power save is an energy saving mode where HDG204 is only listening at regular intervals for the beacons transmitted from an access point and is set in sleep mode in between. During this sleep mode, FW is kept in RAM but all not needed functions are turned off. Since the receive time is very short compared to the listening interval the average current consumption is reduced significantly.
The timing of the listening interval is based on the LFC (32 kHz) clock. See Low frequency clock, LFC.
Pin EXT_PWR_EN is set high at initial Power ON, independent of pins RESET and SHUTDOWN, before FW is loaded. FW then sets it low. This pin is not further used in the present FW. During HW Shutdown this pin is in-determent, set to output low or to high z. Thus if HW Shutdown is used, connected it to a 100K pull down resistor.

5.6 Power On sequence

The HDG204 Power On sequence is described in timing diagram Figure 5-2 and Table 5-3 berlow.

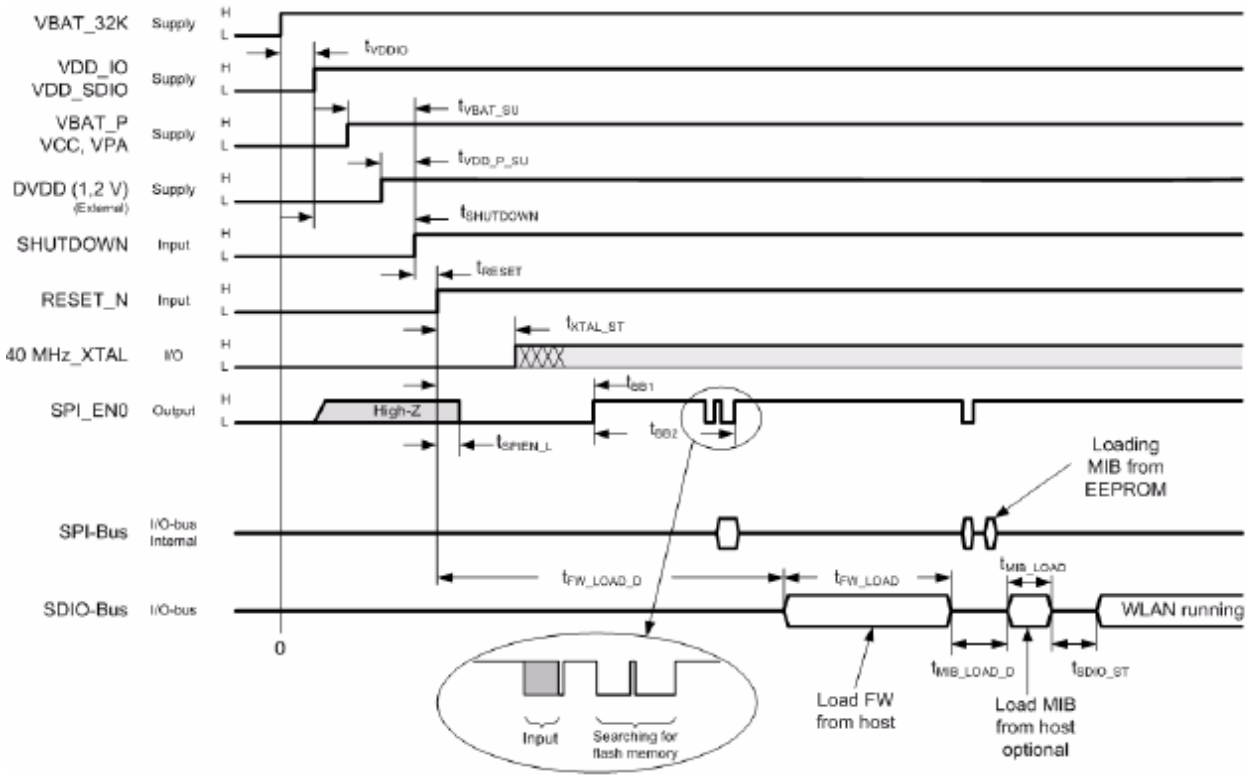


Figure 5-2: Start up sequence with 40 MHz crystal and FW loaded from host via SDIO.

Parameter	Symbol	Min	Typ.	Max	Unit	Comment
VDDIO turn on time	tVDDIO	0			ms	
Shut down disable time	tSHUTDOWN	0			ms	
VBAT set up time	tVBAT_SU	-0.2 *		tSHUTDOWN	ms	
DVDD set up time	tVDD_P_SU	-0.2 *		tSHUTDOWN	ms	External 1.2 V supply
Reset time	tRESET		2		ms	
SPI_EN0 turn low time	tSPIEN_L		0.02		ms	
40 MHz OSC start up time	tXTAL_ST		2.5		ms	
BB1 HW start up time 1	tBB1		3		ms	At 32.768 kHz
BB2 HW start up time 2	tBB2		7		ms	At HFC 40 MHz
Firmware loading Delay time	tFW_LOAD_D	20			ms	At HFC 40 MHz
Firmware loading time	tFW_LOAD		100		ms	SDIO clock and host SW dependent

Table 5-3: Start up timing using 40 MHz crystal and FW load from host

**. SHUTDOWN-pin can be set high slightly before VBAT_P, VCC or DVDD, this makes it possible to use the SHUTDOWN signal as enable for external LDO:s for these supplies*

5.7 Shut Down sequence

The following shutdown procedure shall be used for a shutdown and start up sequence of the HDG204, when a 40MHz crystal is used. FW are reloaded from the host when restarting from SHUTDOWN. Note that all supply voltages are ON during shutdown except DVDD which must be tuned OFF. VPA can optionally be turned OFF. See timing diagram Fig. 5.4 and Table 5.6

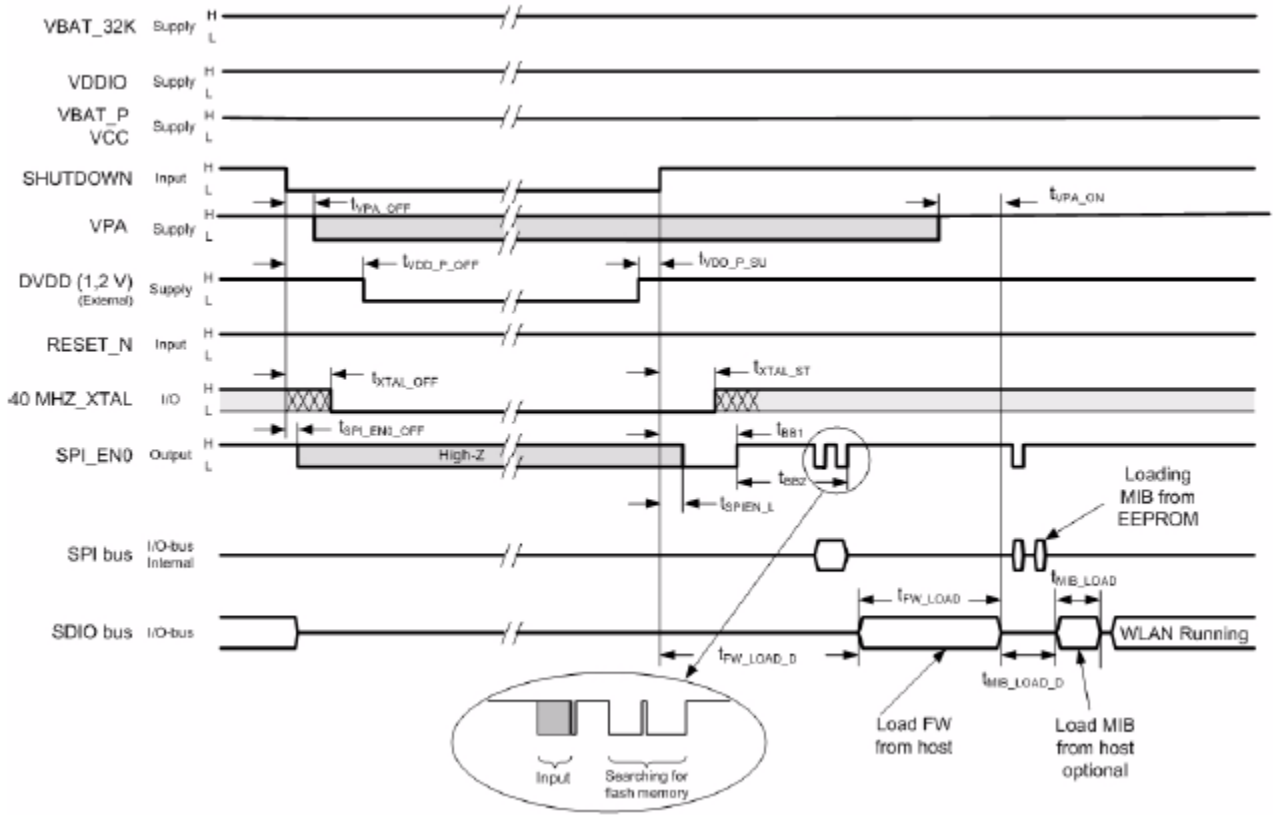


Figure 5-3: Shut down and start up sequence with 40 MHz crystal osc. and FW loaded from host.

Parameter	Symbol	Min	Typ.	Max	Unit	Comment
FW loading delay time	tFW_LOAD_D	20			ms	
FW loading time	tFW_LOAD		100		ms	SDIO clock and host SW dependent.

Table 5-4: Shutdown timing with external 1.2 V supply, crystal and FW load from host.

5.8 Power OFF Sequence

All power supplies can be turned OFF at the same time.
If not turned OFF simultaneously the sequence in Figure 5.5 below should be followed.

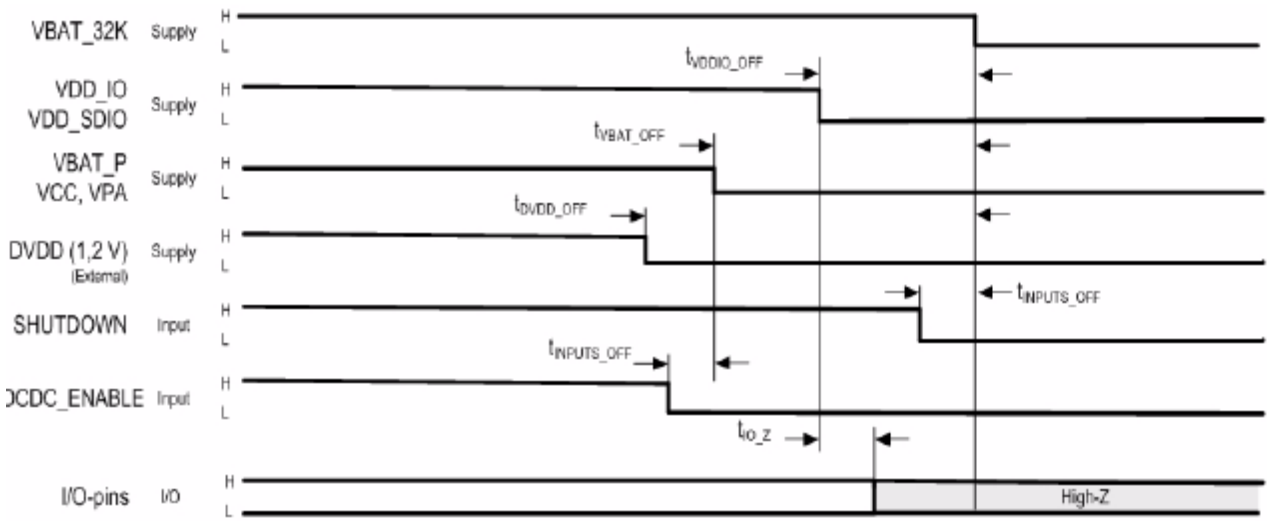


Figure 5-4: Power OFF Sequence

Parameter	Symbol	Min	Typ.	Max	Unit	Comment
VDDIO turn off time	tVDDIO_OFF	0			µs	
VBAT_P , VCC, VPA turn off times	tVBAT_OFF	tVDDIO_OFF			µs	
DVDD turn OFF time	tDVDD_OFF	tVBAT_OFF			µs	
SHUTDOWN, DCDC_ENABLE turn OFF time	tINPUTS_OFF	0			ms	
IO-pins to High-Z time	tIO_Z	0				

Table 5-5: Power OFF timing

5.9 Interfaces

The HDG204 is equipped with a number of interfaces that can be set up in various ways.

5.9.1 Host Interface SDIO/SPI

The SDIO-bus pins can be used as SDIO or SPI
Default at Power On Reset is SDIO 1-bit mode. Host Software must send the appropriate command in SDIO 1-bit mode to change to SDIO 4-bit mode or to SDIO SPI-mode.
All unused interface pins shall be left open. For timing characteristics and trigger level see
Figure 3-1: SDIO/SPI timing diagram (default mode)Figure 3-1and Table 3-6 or Figure 3-2 and Table 3-7

5.9.2 Host Wake Up

To wake up the host if the HDG204 detects an event it can wake up the host via SDIO DAT1 (pin2) of the SDIO interface. This is the normal wake up and is implemented in the FW.

5.10 RF interface

The RF output pin impedance is 50 ohm and shall be connected to an antenna with VSWR much better than 2:1.

5.11 General application information

5.11.1 Design directions

The design using the HDG204 must be performed according to good RF design considerations. All the leads shall be as short as possible between the circuit pins and the external components. Highest priority has the RF-port to antenna strip line, the 40MHz x-tal connections and the VBAT_P decoupling capacitor.

5.11.2 Soldering

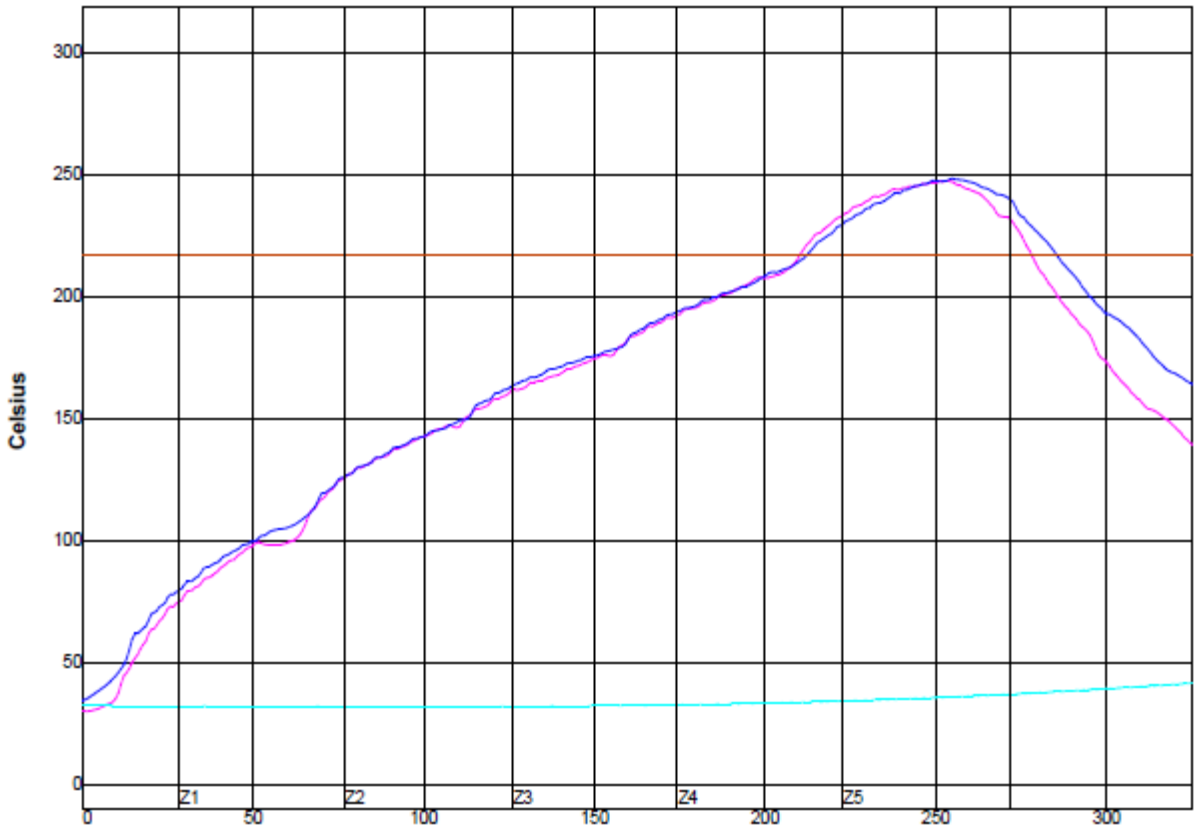
The HDG204 uses a QFN package. The recommended solder profile is pictured in Figure 5.6.
To lower the moister content bake the packages for 192 hours at 40–45°C and <5%RH, or 24 hours at 120–130°C, depending on the maximum temperature rating of the packaging.
HDG204
Pin I/O Signal
CSR

Seconds

PWI= 51%	Max Rising Slope		Max Falling Slope		Peak Temp		Tot Time /217C	
Fram right	2.11	41%	-2.13	-13%	247.73	-51%	68.05	27%
bak left	1.93	29%	-1.72	28%	248.67	11%	73.50	45%
Delta	0.18		0.41		0.94		5.45	

Process Window:

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=1.5) (Calculate Slope over 20 Seconds)	0	3	Degrees/Second
Max Falling Slope (Calculate Slope over 20 Seconds)	-3	-1	Degrees/Second
Peak Temperature	247	250	Degrees Celsius
Total Time Above - 217C	30	90	Seconds



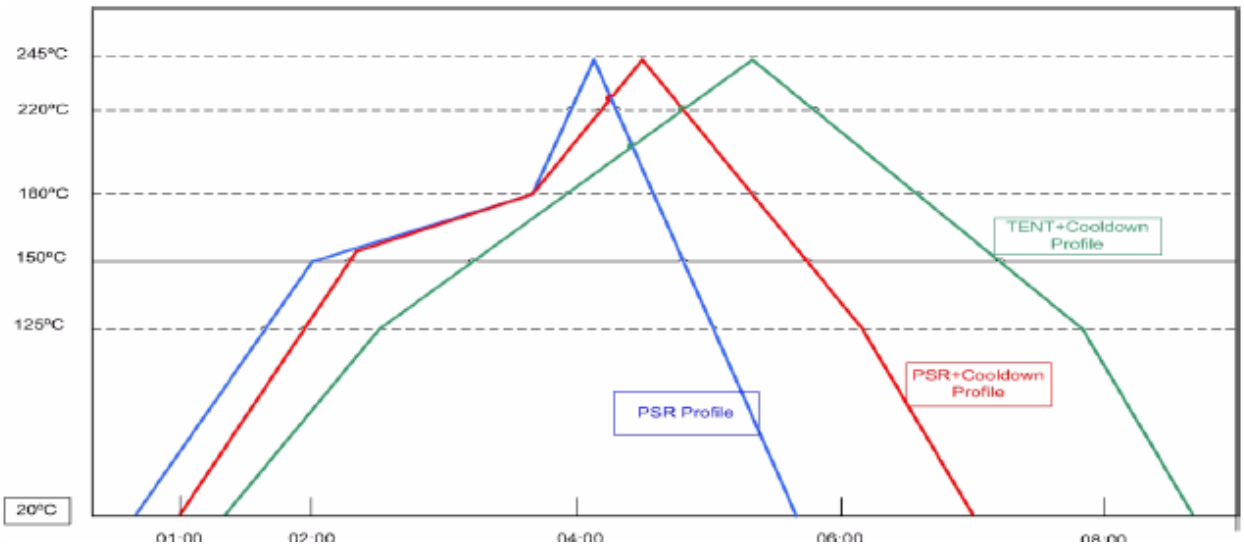


Figure 5-5: Reflow Temperature Profile.

Type	Rising Zone	Preheat Zone	Reflow Zone	Peak Zone	Cool Down Zone	Comment
PSR	125ºC-Peak No	150-180ºC 60-120 s	>220ºC 30-60 s	240-255ºC	Peak-125ºC No	O_2< 500ppm
PSR + Cool Down	125ºC-Peak No	150-180ºC 60-120 s	>220ºC 30-60 s	240-255ºC	Peak-125ºC < 1ºC/s	
TENT + cool down	125-217ºC < 1ºC/s	125-217ºC 150-210 s	>217ºC 60-90 s	240-255ºC	Peak-125ºC < 1ºC/s	

Table 5-6: Reflow Zones

5.11.3 Environmental statement

The HDG204 is designed and manufactured to comply with the RoHS and Green directives.

5.12 Reference design schematic HDG204

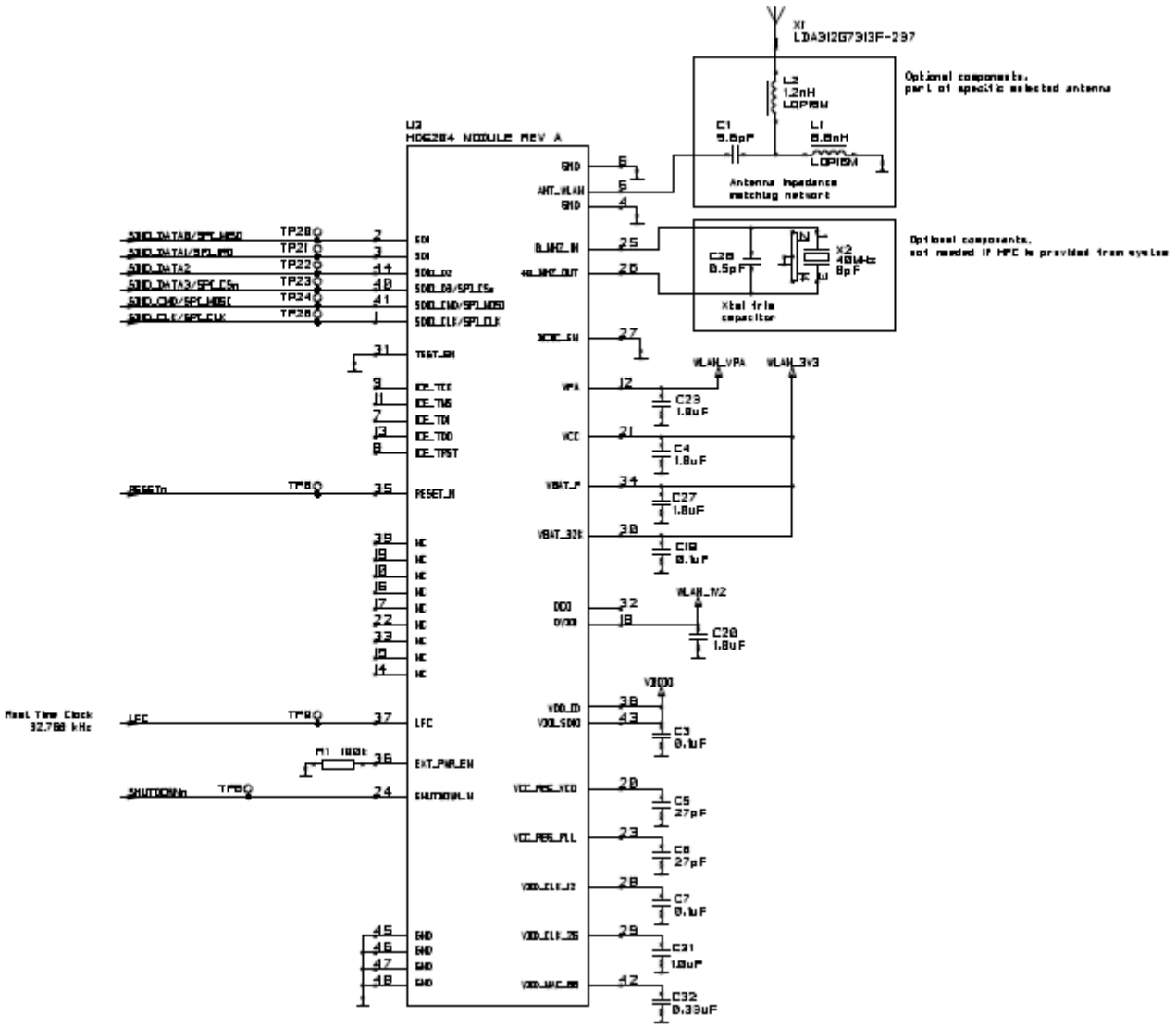
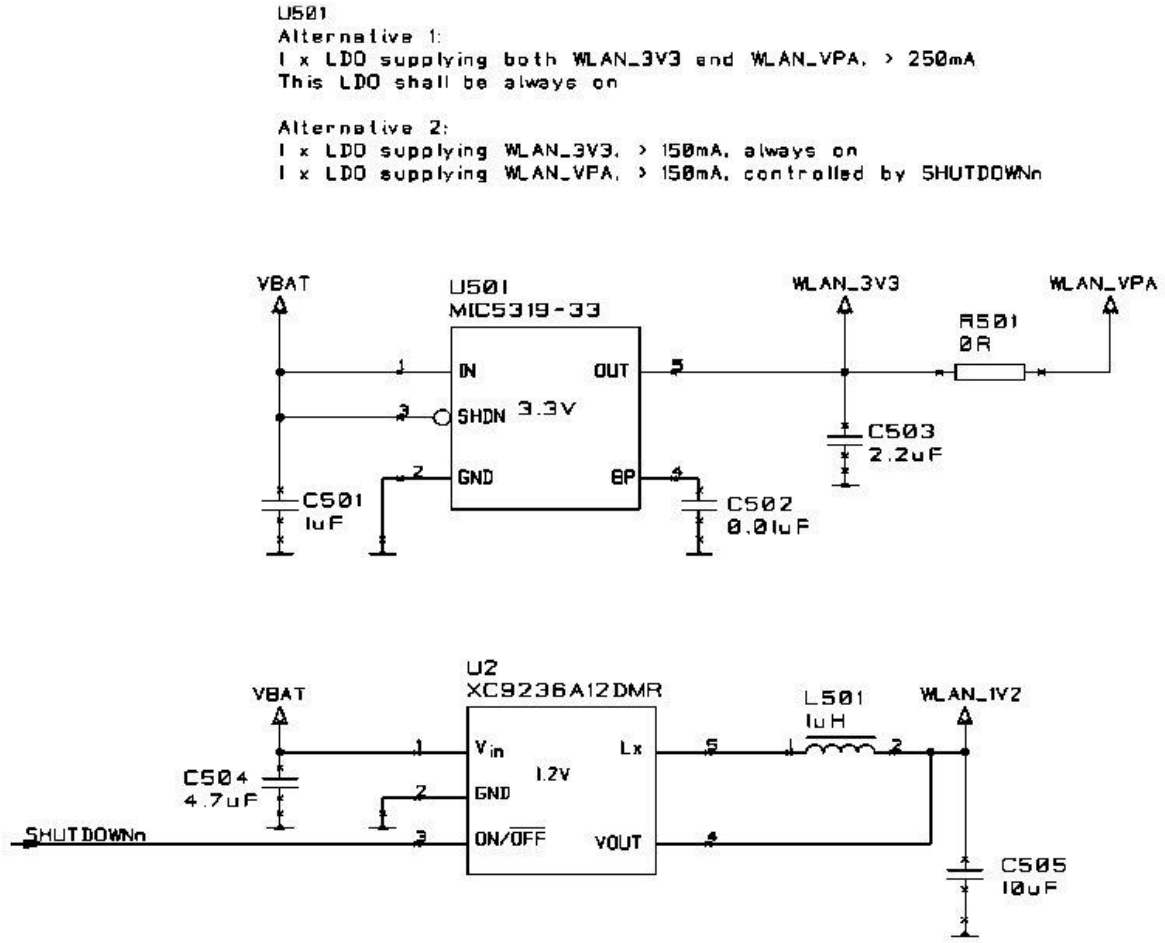


Figure 5-6: Reference design schematic.

5.12.1 Reference Design power supplies



Requirements with SHUTDOWN pin Low	
HDG204 pin	**State**
VPA	ON or OFF
VCC, VBAT_P	ON
VBAT_32K	ON
DVDD	OFF
VDDIO	ON
SDIO DAT0, SDIO DAT1, SDIO DAT2, SDIO DAT3	Output High

Figure 5-7: Reference Design power supplies

6 Package Specifications

6.1 Mechanical outline QFN 44pin

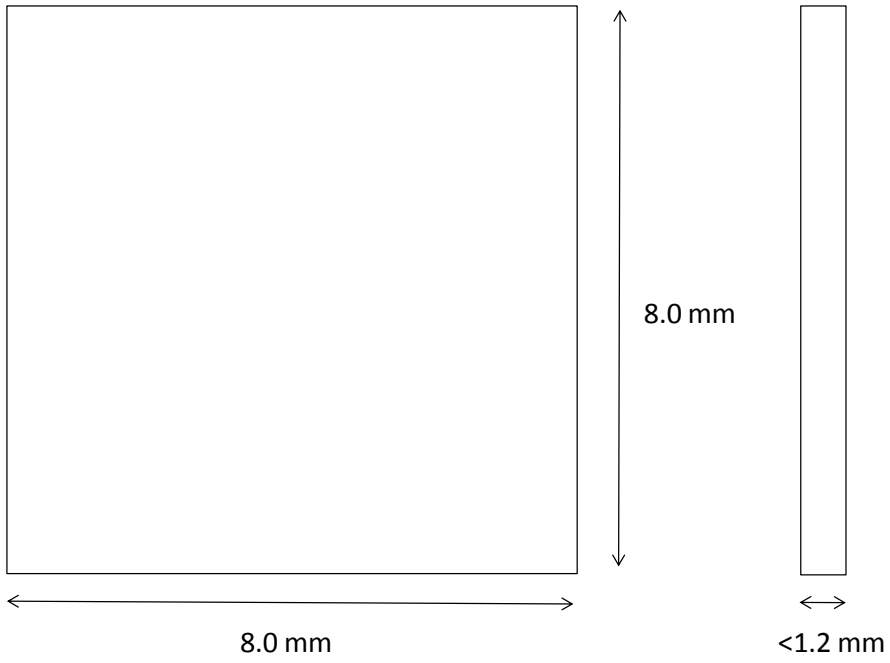


Figure 6.1: Mechanical drawing, 44 pin Quad Flat No-Lead (QFN) package.

6.2 Marking HDG204 QFN

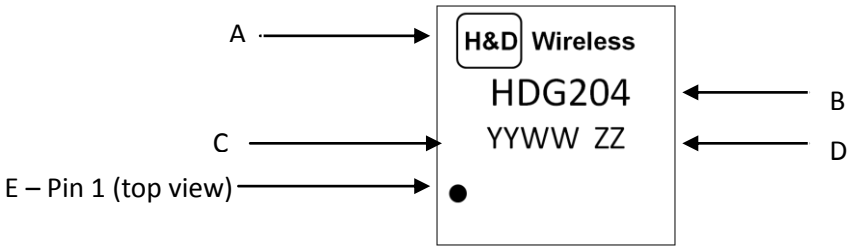


Figure 6.2: HDG204 QFN package marking.

Ref	Marking	Description
A	H&D Wireless	Company Logo
B	HDG204	Product name
C	YYWW	Production date. YY= year, WW=week
D	ZZ	Production lot
E	Dot	Defines pin 1 (Top view)

Table 6-1:QFN package marking description

6.3 Package pad dimension

HDG204 pad placement and sizes, top view. Units in mm.

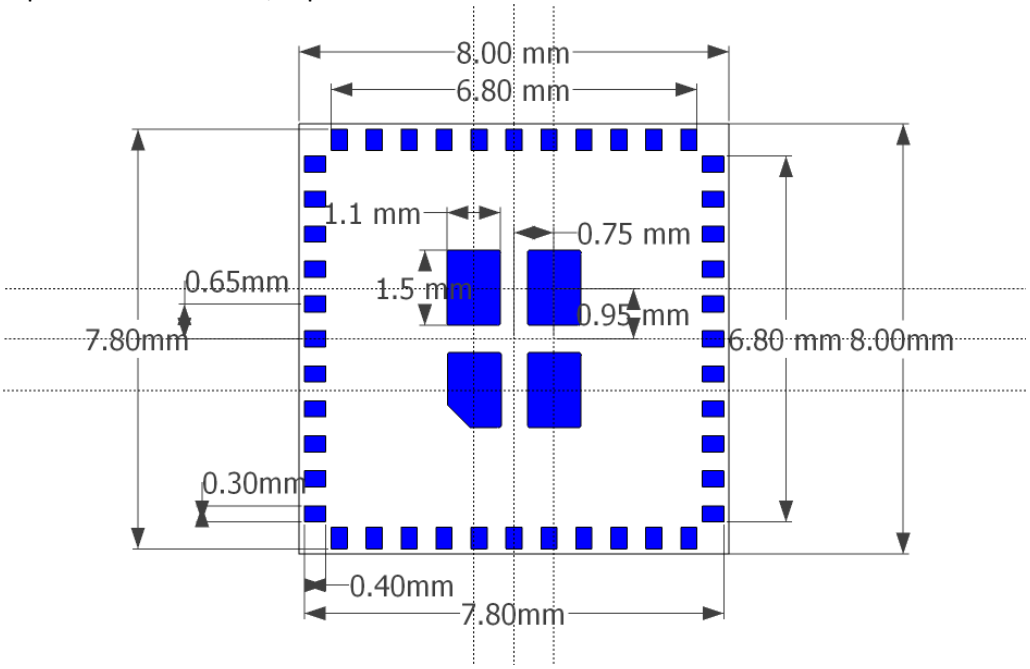


Figure 6.3: HDG204 Pad pattern, top view, units in mm

6.4 Mounting information

Recommended land pattern on the PCB

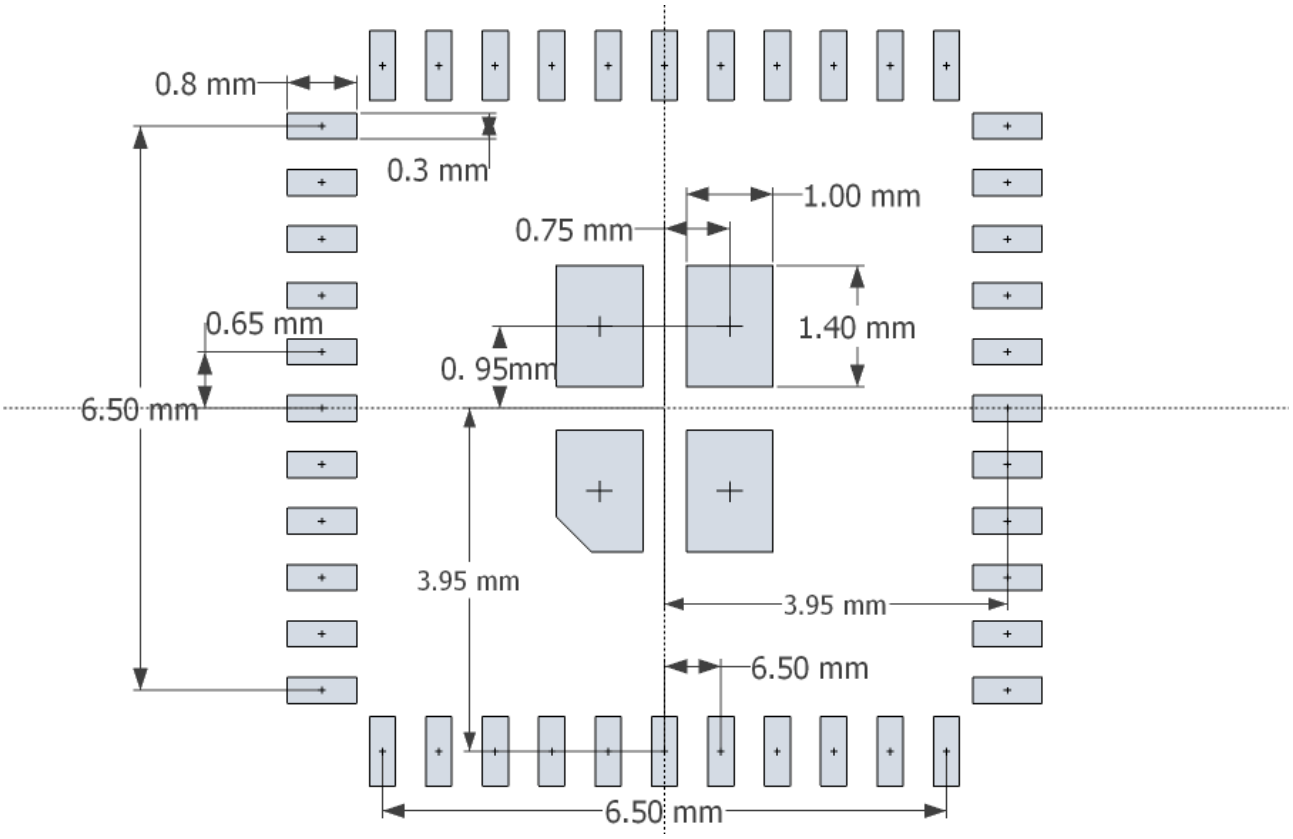
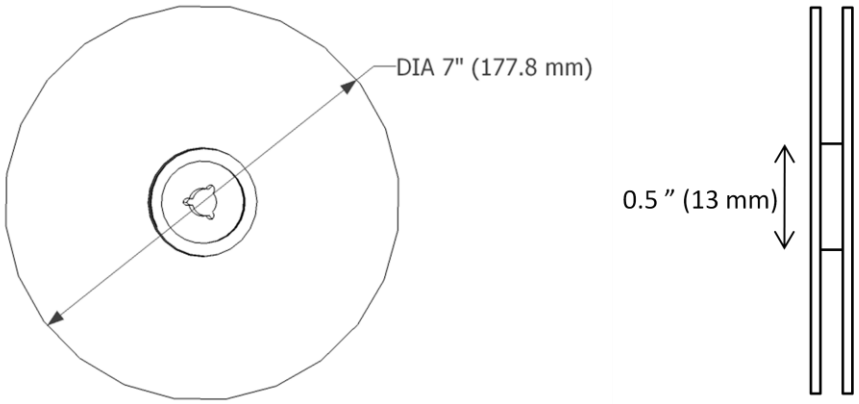


Figure 6.4: Recommended land pattern on the PCB, top view

7 Tape and Reel Information

TBA

Figure 7-1: Tape dimensions



7-2: Reel dimensions

8 STANDARDS COMPLIANCE

8.1 IEEE/IETF

Standard	Revision	Description
802.11	802.11 R2003	WLAN MAC& PHY
802.11b	802.11 R2003	High rate DSSS (5,5/11Mbit/s)
802.11d	802.11 R2003	Operation in different regulatory domains
802.11e	D9,0 Aug. 2004	QoS enhancements
802.11g	-2003	Extended rate PHY (ERP-PBCC, DSS-OFDM)
802.11i	-2004	Security enhancements
802.11k	Draft 11.0, 2008	Wireless network management
802.11r	Draft 9.0, 2008	Fast BSS transition
802.11h	1997 edition	Bridge tunneling
RFC1023	Inherent	Frame encapsulation
802.15.2		Bluetooth coexistence

Table 7.1: applicable IEEE standards

8.2 WiFi standards

Specification	Description	Revision
Wi-Fi 802.11b with WPA system interoperability test plan for IEEE 802.11b devices	802.11b devices with WPA	2.1
WiFi 802.11g with WPA system inter operability test plan	802.11g devices with WPA	2.0
WMM (including WMM Power Save)		Ver 1.1

Table 7.2: Applicable WiFi standards

8.3 Regulatory

Country	Approval authority	Regulatory	Frequency band
USA	FCC	FCC	2.4 GHz -2.4835 GHz
Canada	IC	RSS	2.4 GHz -2.4835 GHz
Europe	National	ETSI	2.4 GHz -2.4835 GHz

Table 7.3: Regulatory standards

8.3.1 FCC (United States of America)

This equipment complies with Part 15 of the FCC rules and regulations as a Limited modular approval.
To fulfill FCC Certification requirements, an OEM manufacturer must If the HDG204 module are incorporated into a product, ensure compliance of the final end-user product.
The modular transmitter must be labeled with its own FCC ID number, and, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module.

WARNING: The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment.

IMPORTANT: This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19).

The internal / external antenna(s) used for this mobile transmitter must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance. This device is approved as a mobile device with respect to RF exposure compliance, and may only be marketed to OEM installers. Use in portable exposure conditions (FCC 2.1093) requires separate equipment authorization.

IMPORTANT: Modifications not expressly approved by this company could void the user's uthority to operate this equipment (FCC section 15.21).

IMPORTANT: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense (FCC section 15.105).

8.3.2 IC (Canada)

Equipment is subject to certification under the applicable RSSs, shall be permanently labeled on each item, or as an inseparable combination. To fulfill RSS Certification requirements, an OEM manufacturer must if the HDG204 module is incorporated into a product, ensure compliance of the final end-user product**.**

IMPORTANT: This equipment for which a certificate has been issued is not considered certified if it is not properly labeled. The information on the Canadian label can be combined with the manufacturer's other labeling requirements

IMPORTANT: Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT: To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

IMPORTANT: The installer of this radio equipment must ensure that the antenna is located or pointed such that it does not emit RF field in excess of Health Canada limits for the general population. Consult Safety Code 6, obtainable from Health Canada's website www.hc-sc.gc.ca/rpb.

8.3.3 ETSI (Europe)

The HGD104 module has been certified for use in European union countries according to ETSI EN 300 328 (Electromagnetic compatibility and Radio spectrum matters for equipment operating in the 2,4 GHz ISM band using spread spectrum modulation techniques). This standard is harmonized within the European Union and covering essential requirements under article 3.2 of the R&TTE-directive.

If the HGD104 module are incorporated into a product, the manufacturer must ensure compliance of the final end-user product to the European harmonized EMC and low voltage/safety standards. A declaration of conformity must be issued for the product including compliance references to these standards. Underlying the declaration of conformity a technical construction file (TCF), including all relevant test reports and technical documentation, must be issued and kept on file as described in Annex II of the R&TTE-directive.

Furthermore, the manufacturer must maintain a copy of the HGD104 module documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a complete re-test must be made in order to comply with all relevant standards as basis for CE-marking. A submission to notified body must be used only if deviations from standards have been found or if non-harmonized standards have been used.

9 SALES OFFICES

Global Sales Office Sweden

H&D Wireless AB
H&D Wireless AB
Norgegatan 1
164 32 Kista
Sweden

E-mail: info@hd-wireless.se
Support: support@hd-wireless.se
Home page: www.hd-wireless.se

Local sales offices and distributors see **www.hd-wireless.se**

10 Reference designs

10.1 Reference design using HDG204

This document describes how to use the HDG204 SIP component in a customer application.
See www.hd-wireless.se for the complete list of reference designs and other support documents.