ECLSOIC8EVB

Evaluation Board User's Manual for High Frequency SOIC 8

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

INTRODUCTION

ON Semiconductor has developed an evaluation board for the devices in 8−lead SOIC package. These evaluation boards are offered as a convenience for the customers interested in performing their own engineering assessment on the general performance of the 8−lead SOIC device samples. The board provides a high bandwidth 50 Ω controlled impedance environment. The pictures in Figure 1 show the top and bottom view of the evaluation board, which can be configured in several different ways, depending on device under test (See Table 1. Configuration List).

This evaluation board manual contains:

- Information on 8−lead SOIC Evaluation Board
- Assembly Instructions
- Appropriate Lab Setup
- Bill of Materials

This manual should be used in conjunction with the device data sheet, which contains full technical details on the device specifications and operation.

Board Lay−Up

The 8−lead SOIC evaluation board is implemented in four layers with split (dual) power supplies (Figure 2. Evaluation Board Lay−up). For standard ECL lab setup and test, a split (dual) power supply is essential to enable the 50 Ω internal impedance in the oscilloscope as a termination for ECL devices. The first layer or primary trace layer is 0.008″ thick Rogers RO4003 material, which is designed to have equal electrical length on all signal traces from the device under the test (DUT) to the sense output. The second layer is the 1.0 oz copper ground plane and a portion of the plane is the V_{EE} power plane. The FR4 dielectric material is placed between second and third layer and between third and fourth layer. The third layer is also 1.0 oz copper ground plane and a portion of this layer is V_{CC} power plane. The fourth layer is the secondary trace layer.

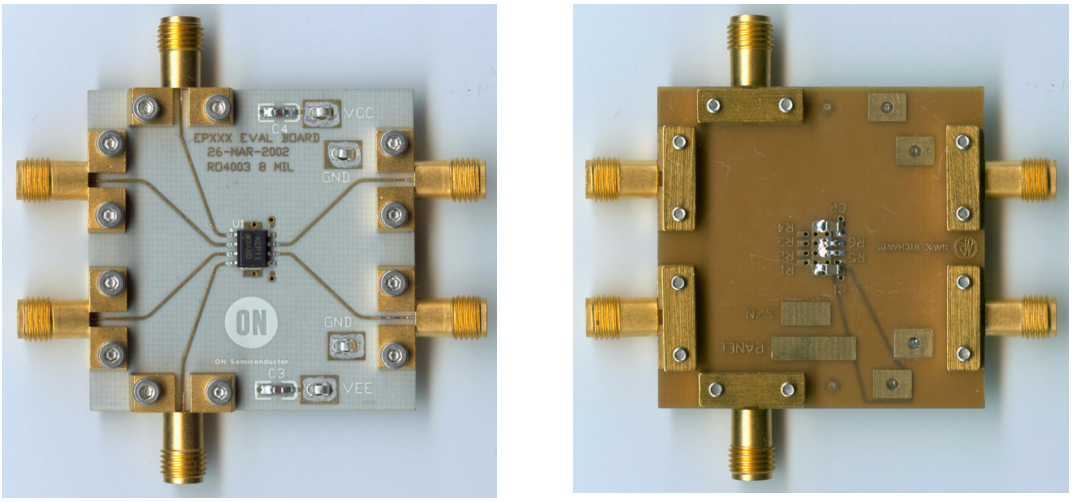


Figure 1. Top and Bottom View of the 8−lead SOIC Evaluation Board

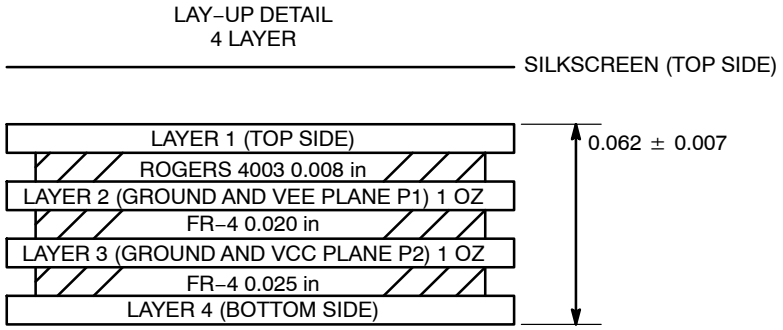


Figure 2. Evaluation Board Lay−up

Board Layout

The 8−lead SOIC evaluation board was designed to be versatile and accommodate several different configurations. The input, output, and power pin layout of the evaluation board is shown in Figure 3. The evaluation board has at least eleven possible configurable options. Table 1. list the devices and the relevant configuration that utilizes this PCB board. List of components and simple schematics are located in Figures 4 through 14. Place SMA connectors on J1 through J7, 50 Ω chip resistors on R1 through R7, and chip capacitors C1 through C4 according to configuration figures. (C1 and C2 are 0.01 μF and C3 and C4 are 0.1 μF).

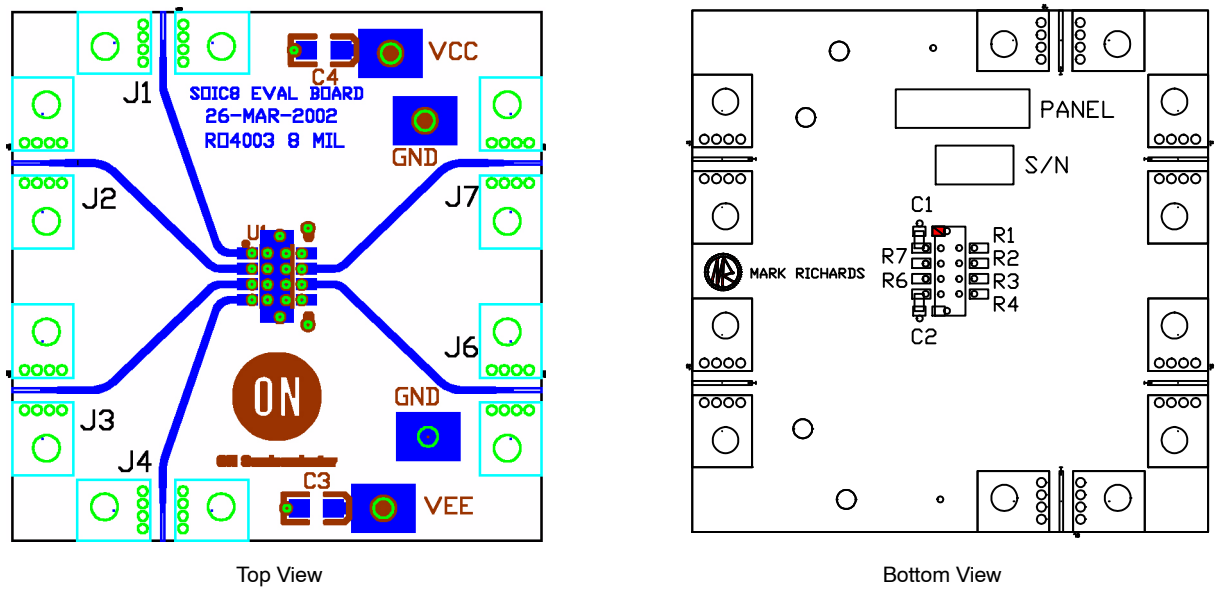


Figure 3. Evaluation Board Layout

Table 1. Configuration List

ECLinPS Lite™		
Device	**Comments**	**Configuration**
MC10EL01D/MC100EL01D	See Figure 4	1
MC10EL04D/MC100EL04D	See Figure 5	2
MC10EL05D/MC100EL05D	See Figure 4	1
MC10EL07D/MC100EL07D	See Figure 5	2
MC10EL11D/MC100EL11D	See Figure 6	3
MC10EL12D/MC100EL12D	See Figure 6	3
MC10EL16D/MC100EL16D*	See Figure 5	2
MC10EL31D/MC100EL31D	See Figure 4	1
MC10EL32D/MC100EL32D	See Figure 7	4
MC10EL33D/MC100EL33D	See Figure 7	4
MC10EL35D/MC100EL35D	See Figure 4	1
MC10EL51D/MC100EL51D	See Figure 4	1
MC10EL52D/MC100EL52D	See Figure 4	1
MC10EL58D/MC100EL58D	See Figure 8	5
MC10EL89D/MC100EL89D	See Figure 6	3
MC10ELT20D/ MC100ELT20D	See Figure 9	6
MC10ELT21D/ MC100ELT21D	See Figure 10	7
MC10ELT22D/ MC100ELT22D	See Figure 11	8
MC100ELT23D	See Figure 12	9
MC10ELT26D/ MC100ELT26D	See Figure 13	10
MC10ELT28D/ MC100ELT28D	See Figure 14	11

Low Voltage ECLinPS™		
Device	**Comments**	**Configuration**
MC100LVEL01D	See Figure 4	1
MC100LVEL05D	See Figure 4	1
MC100LVEL11D	See Figure 6	3
MC100LVEL12D	See Figure 6	3
MC100LVEL16D*	See Figure 5	2
MC100LVEL31D	See Figure 4	1
MC100LVEL32D	See Figure 7	4
MC100LVEL33D	See Figure 7	4
MC100LVEL51D	See Figure 4	1
MC100LVEL58D	See Figure 8	5
MC100LVELT22D	See Figure 11	8
MC100LVELT23D	See Figure 12	9

ECLinPS Plus™		
Device	**Comments**	**Configuration**
MC10EP01D/MC100EP01D	See Figure 4	1
MC10EP05D/MC100EP05D	See Figure 4	1
MC10EP08D/MC100EP08D	See Figure 4	1
MC10EP11D/MC100EP11D	See Figure 6	3
MC10EP16D/ MC100EP16D*	See Figure 5	2
MC100EP16FD*	See Figure 5	2
MC10EP16TD/ MC100EP16TD*	See Figure 5	2
MC100EP16VAD*	See Figure 5	2
MC100EP16VBD*	See Figure 5	2
MC100EP16VCD*	See Figure 8	5
MC100EP16VSD*	See Figure 5	2
MC100EP16VTD*	See Figure 5	2
MC10EP31D/MC100EP31D	See Figure 4	1
MC10EP32D/MC100EP32D	See Figure 7	4
MC10EP33D/MC100EP33D	See Figure 7	4
MC10EP35D/MC100EP35D	See Figure 4	1
MC10EP51D/MC100EP51D	See Figure 4	1
MC10EP52D/MC100EP52D	See Figure 4	1
MC10EP58D/MC100EP58D	See Figure 8	5
MC100EP89D	See Figure 6	3
MC10EPT20D/ MC100EPT20D	See Figure 9	6
MC100EPT21D*	See Figure 10	7
MC100EPT22D	See Figure 11	8
MC100EPT23D*	See Figure 12	9
MC100EPT26D*	See Figure 13	10

Low Voltage ECLinPS Plus		
Device	**Comments**	**Configuration**
MC100LVEP11D	See Figure 6	3
MC100LVEP16D*	See Figure 5	2

*See Appendix for additions or modifications to the current configuration.

ECLinPS MAX™		
Device	**Comments**	**Configuration**
NB6L11D	See Figure 6	3
NB6L16D	See Figure 5	2

Evaluation Board Assembly Instructions

The 8−lead SOIC evaluation board is designed for characterizing devices in a 50 Ω laboratory environment using high bandwidth equipment. Each signal trace on the board has a via, which has an option of termination resistor or bypassing capacitor depending on the input/output configuration (see Table 1. Configuration List). Table 17 contains the Bill of Materials for this evaluation board.

Solder the Device on the Evaluation Board

The soldering can be accomplished by hand soldering or soldering re−flow techniques. Make sure pin 1 of the device is located next the white dotted mark U1 and all the pins are aligned to the footprint pads. Solder the 8−lead SOIC device to the evaluation board.

Connecting Power and Ground Planes

For standard ECL lab setup and test, a split (dual) power supply is required enabling the 50 Ω internal impedance in the oscilloscope to be used as a termination of the ECL signals ($V_{TT} = V_{CC} - 2.0$ V, in split power supply setup, V_{TT} is the system ground, V_{CC} is 2.0 V, and V_{EE} is –3.0 V or –1.3 V; see Table 2: Power Supply Levels).

Table 2. Power Supply Levels

Power Supply	V_{CC}	V_{EE}	GND
5.0 V	2.0 V	−3.0 V	0.0 V
3.3 V	2.0 V	−1.3 V	0.0 V
2.5 V	2.0 V	−0.5 V	0.0 V

The power supply for voltage level translating device need slight modification as indicated in Table 3. Power Supply Levels for Translators.

Table 3. Power Supply Levels for Translators

	V_{CC}	V_{EE}	GND
PECL Translators	3.3 V / 5.0 V	0.0 V	0.0 V

On the top side of the evaluation board solder the four surface mount test point clips to the pads labeled V_{CC}, V_{EE}, and GND. The V_{CC} clip connects directly to pin 8 of the device. The V_{EE} clip connects directly to pin 5 of the device. There are two GND clip footprints which can be connected to the ground plane of the evaluation board depending on the setup configuration.

It is recommended to solder 0.01 μF capacitors to C1 and C2 to reduce the unwanted noise from the power supplies. C3 and C4 pads are provided for 0.1 μF capacitor to further diminish the noise from the power supplies. Adding capacitors can improve edge rates, reduce overshoot and undershoot.

Termination

All ECL outputs need to be terminated to V_{TT} ($V_{TT} = V_{CC}$ –2.0 V = GND) via a 50 Ω resistor in a split power supply lab set−up. 0603 chip resistor pads are provided on the bottom side of the evaluation board to terminate the ECL driver (More information on termination is provided in AN8020). Solder the chip resistors to the bottom side of the board on the appropriate input of the device pins labeled R1, R2, R3, R4, R6, and R7, depending on the specific device.

Installing the SMA Connectors

Each configuration indicates the number of SMA connectors needed to populate an evaluation board for a given configuration. Each input and output requires one SMA connector. Attach all the required SMA connectors onto the board and solder the connectors to the board. Please note that alignment of the signal connector pin of the SMA can influence the lab results. The reflection and launch of the signals are largely influenced by imperfect alignment and soldering of the SMA connector.

Validating the Assembled Board

After assembling the evaluation board, it is recommended to perform continuity checks on all soldered areas before commencing with the evaluation process. Time Domain Reflectometry (TDR) is another highly recommended validation test.

CONFIGURATIONS

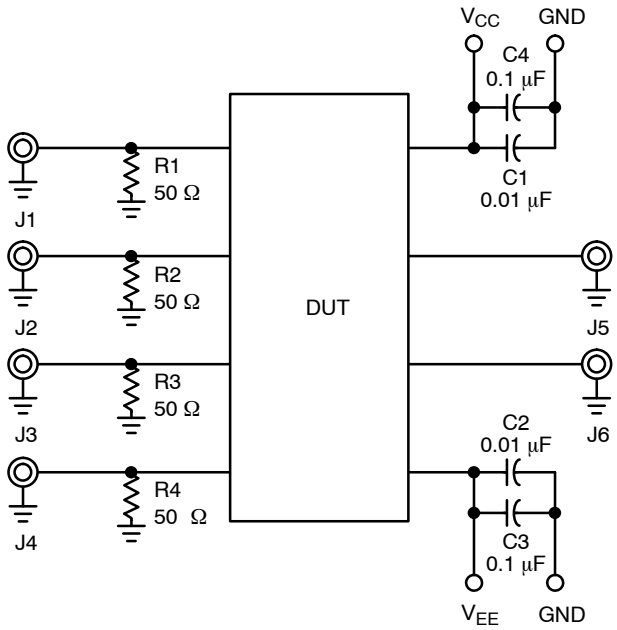


Figure 4. Configuration 1 Schematic

Table 4. Configuration 1

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC10EL01D/MC100EL01D	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes
MC10EL05D/MC100EL05D																
MC10EL31D/MC100EL31D																
MC10EL35D/MC100EL35D																
MC10EL51D/MC100EL51D																
MC10EL52D/MC100EL52D																
MC100LVEL01D																
MC100LVEL05D																
MC100LVEL31D																
MC100LVEL51D																
MC10EP01D/MC100EP01D																
MC10EP05D/MC100EP05D																
MC10EP08D/MC100EP08D																
MC10EP31D/MC100EP31D																
MC10EP35D/MC100EP35D																
MC10EP51D/MC100EP51D																
MC10EP52D/MC100EP52D																

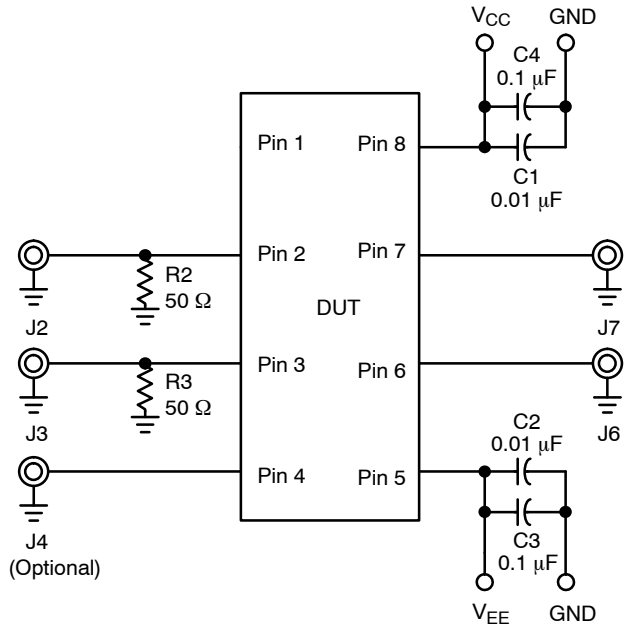


Figure 5. Configuration 2 Schematic

Table 5. Configuration 2

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC10EL04D/MC100EL04D	No	No	Yes	Yes	Yes	Yes	No	No	Yes	Yes	Yes	No	Yes	No	Yes	Yes
MC10EL07D/MC100EL07D																
MC10EL16D/MC100EL16D*																
MC100LVEL16D*																
MC10EP16D/MC100EP16D*																
MC100EP16FD*																
MC100LVEP160*																
MC10EP16TD/MC100EP16TD*																
MC100EP16VAD*																
MC100EP16VBD*																
MC100EP16VSD*																
MC100EP16VTD*																
NB6L160D																

*See Appendix for additional or modification to the current configuration

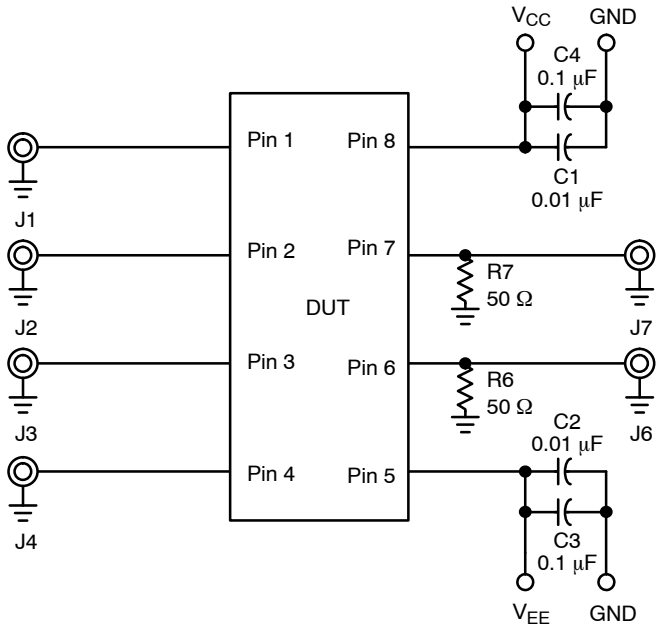


Figure 6. Configuration 3 Schematic

Table 6. Configuration 3

	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
Device	**J1**	**R1**	**J2**	**R2**	**J3**	**R3**	**J4**	**R4**	**C2**	**C3**	**J6**	**R6**	**J7**	**R7**	**C1**	**C4**
MC10EL11D/MC100EL11D	Yes	No	Yes	No	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MC10EL12D/MC100EL12D																
MC10EL89D/MC100EL89D																
MC100LVEL11D																
MC100LVEL12D																
MC10EP11D/MC100EP11D																
MC100EP89D																
MC100LVEP11D																
NB6L11D																

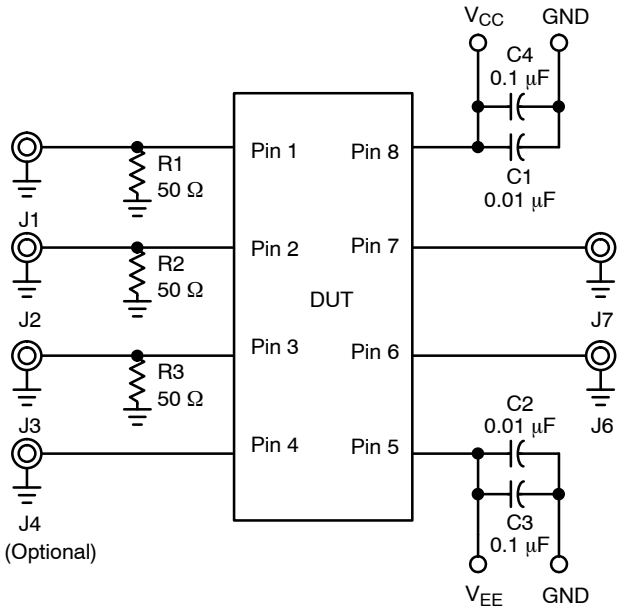


Figure 7. Configuration 4 Schematic

Table 7. Configuration 4

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC10EL32D/MC100EL32D	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes	Yes	No	Yes	No	Yes	Yes
MC10EL33D/MC100EL33D																
MC100LVEL32D																
MC100LVEL33D																
MC10EP32D/MC100EP32D																
MC10EP33D/MC100EP33D																

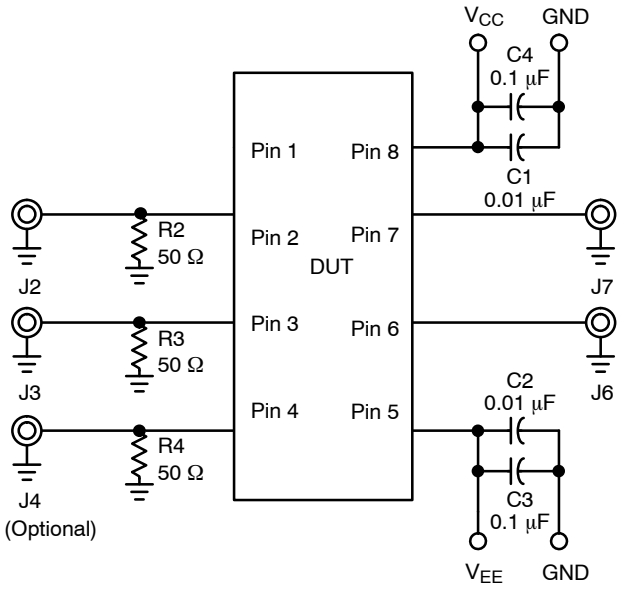


Figure 8. Configuration 5 Schematic

Table 8. Configuration 5

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC100EP16VCD*	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes
MC10EL58D/MC100EL58D																
MC100LVEL58D																
MC10EP58D/MC100EP58D																

*See Appendix for addition or modification to the current configuration

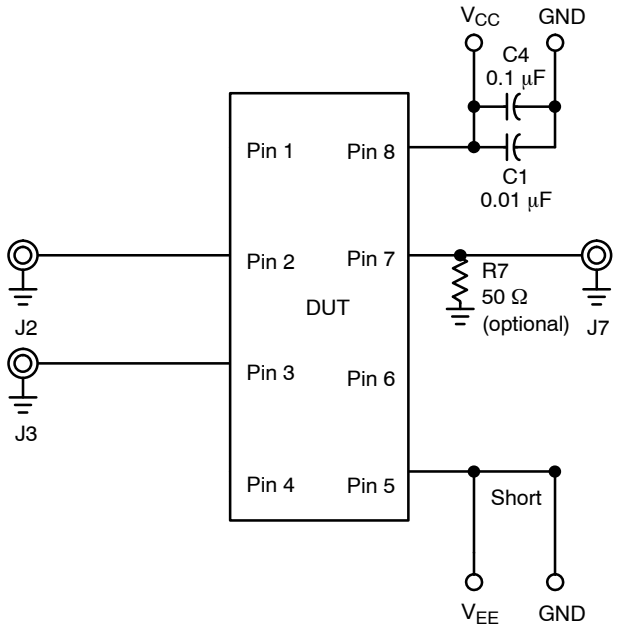


Figure 9. Configuration 6 – Translator Schematic

Table 9. Configuration 6

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC10ELT20D/MC100EL20D	No	No	Yes	No	Yes	No	No	No	No	No	No	No	Yes	Optional	Yes	Yes
MC10EPT20D/MC100EPT20D																

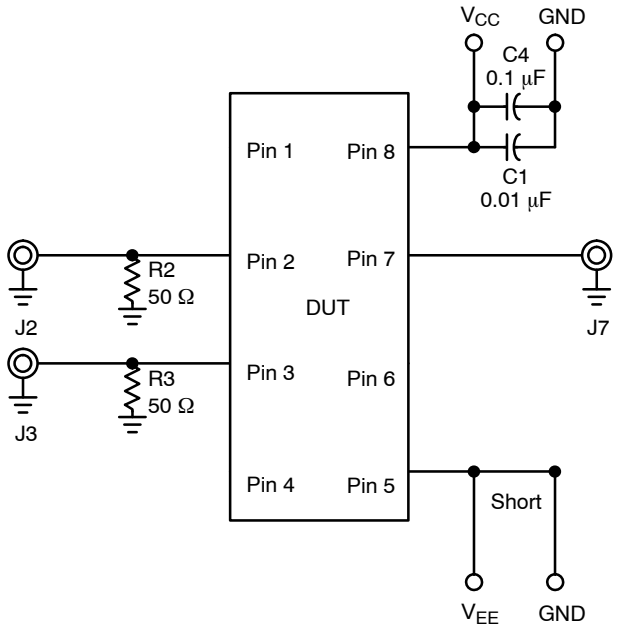


Figure 10. Configuration 7 – Translator Schematic (Unloaded Testing Condition)

Table 10. Configuration 7

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC10ELT21D/MC100EL21D	No	No	Yes	Yes	Yes	Yes	No	No	No	No	No	No	Yes	No	Yes	Yes
MC100EPT21D																

*See Appendix for loaded testing condition.

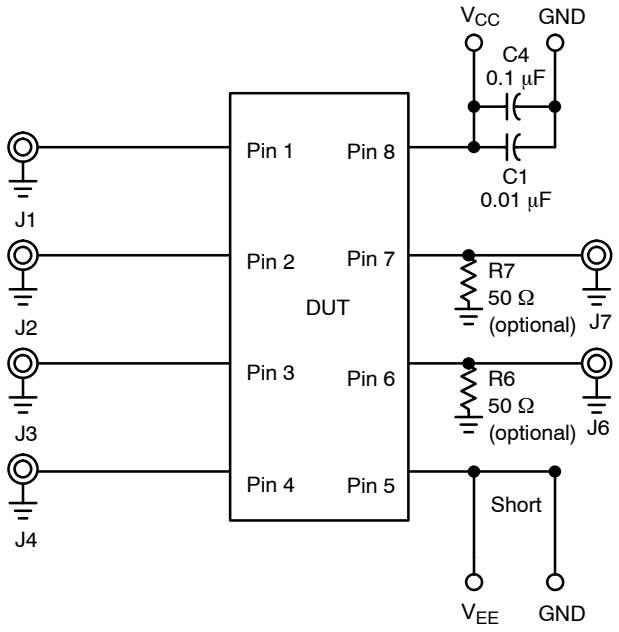


Figure 11. Configuration 8 – Translator Schematic

Table 11. Configuration 8

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J57	R7	C1	C4
MC10ELT22D/ MC100EL22D	Yes	No	Yes	No	Yes	No	Yes	No	No	No	Yes	Optional	Yes	Optional	Yes	Yes
MC100LVELT22D																
MC100EPT22D																

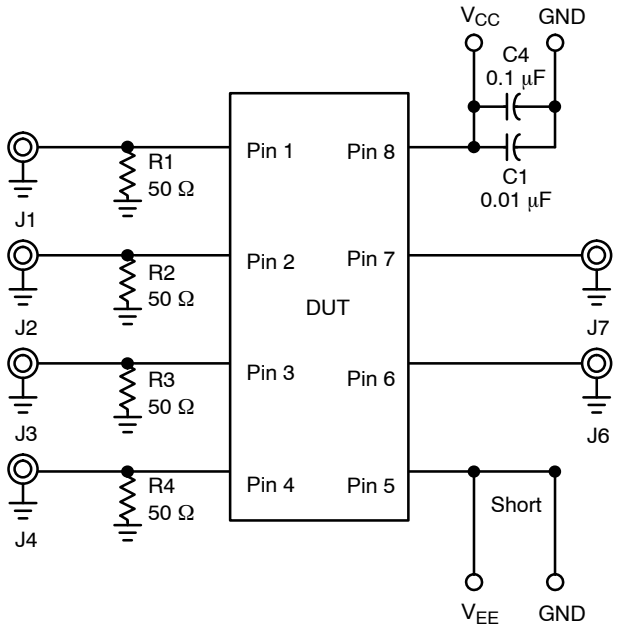


Figure 12. Configuration 9 – Translator Schematic (Unloaded Testing Condition)

Table 12. Configuration 9

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC100EL23D	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes	No	Yes	No	Yes	Yes
MC100LVELT23D																
MC100EPT23D																

*See Appendix for loaded testing condition.

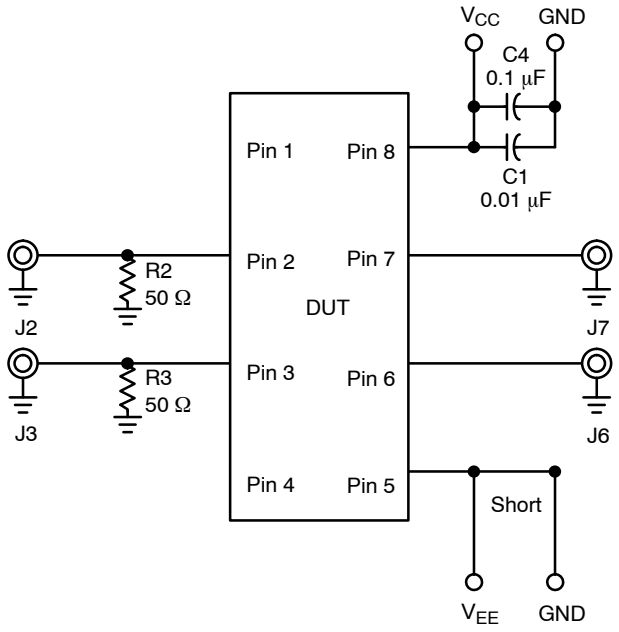


Figure 13. Configuration 10 – Translator Schematic (Unloaded Testing Condition)

Table 13. Configuration 10

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC10ELT26D/MC100ELT26D	No	No	Yes	Yes	Yes	Yes	No	No	No	No	Yes	Yes	Yes	No	Yes	Yes
MC100EPT26D																

*See Appendix for loaded testing condition.

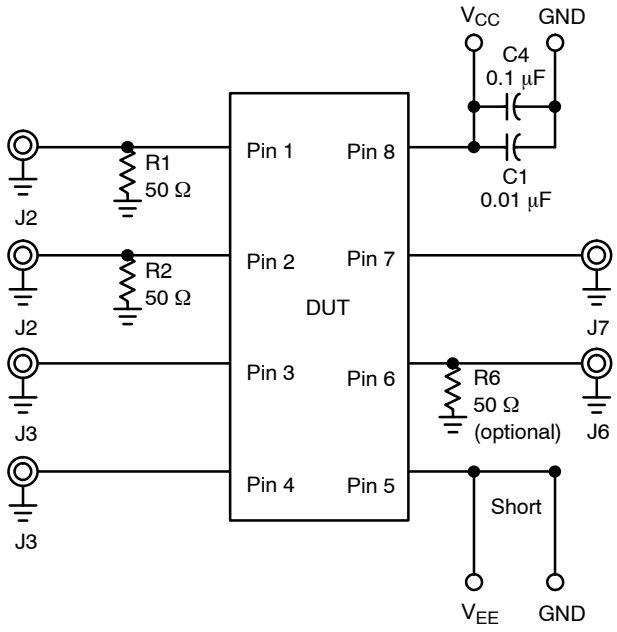


Figure 14. Configuration 11 − Translator Schematic

Table 14. Configuration 11

Device	Pin 1		Pin 2		Pin 3		Pin 4		Pin 5		Pin 6		Pin 7		Pin 8	
	J1	R1	J2	R2	J3	R3	J4	R4	C2	C3	J6	R6	J7	R7	C1	C4
MC10ELT28D/MC100ELT28D	Yes	Yes	Yes	Yes	Yes	No	Yes	No	No	No	Yes	Optional	Yes	No	Yes	Yes

LAB SETUP

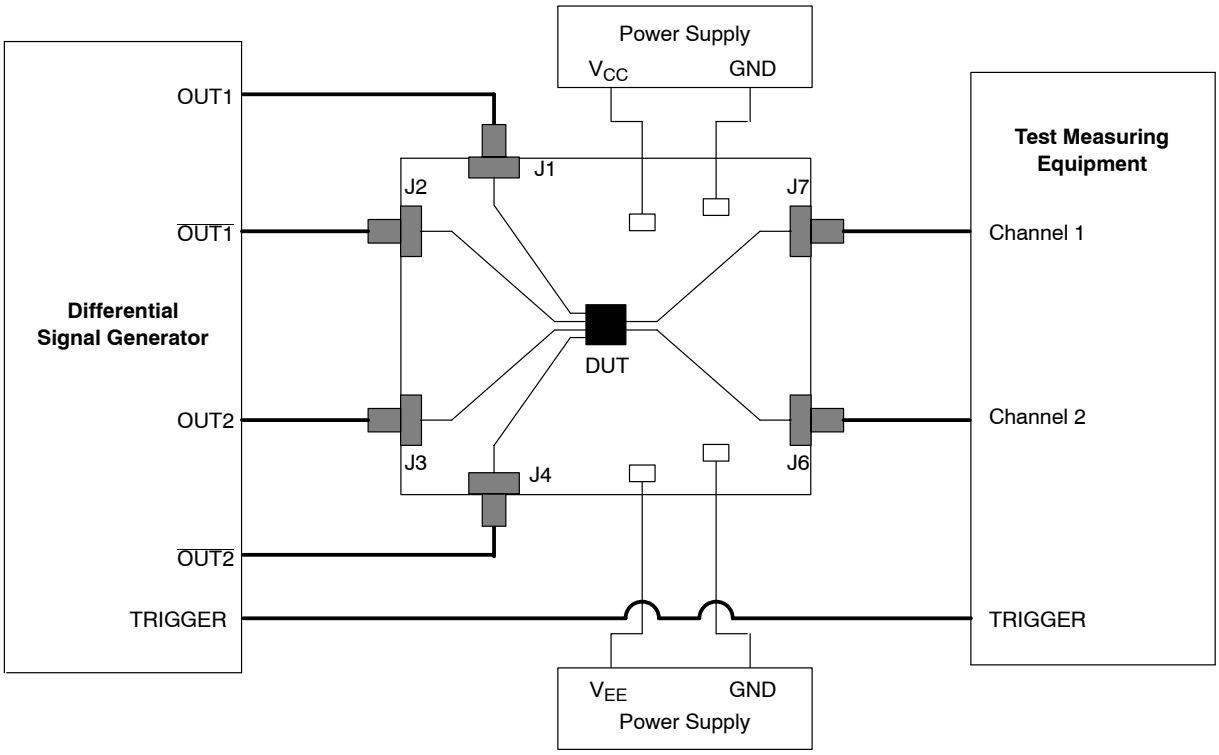


Figure 15. Example of Standard Lab Setup (Configuration 1)

1. Connect appropriate power supplies to V_{CC}, V_{EE}, and GND.
   For standard ECL lab setup and test, a split (dual) power supply is required enabling the 50 Ω internal impedance in the oscilloscope to be used as a termination of the ECL signals (V_{TT} = V_{CC} – 2.0 V, in split power supply setup, V_{TT} is the system ground, V_{CC} is 2.0 V, and V_{EE} is –3.0 V or –1.3 V; see Table 15).

Table 15. Power Supply Levels

Power Supply	V_{CC}	V_{EE}	GND
5.0 V	2.0 V	–3.0 V	0.0 V
3.3 V	2.0 V	–1.3 V	0.0 V
2.5 V	2.0 V	–0.5 V	0.0 V

The power supply for voltage level translating device need slight modification as indicated in Table 16.

Table 16. Power Supply Levels for Translators

	V_{CC}	V_{EE}	GND
PECL Translators	3.3 V / 5.0 V	0.0 V	0.0 V

2. Connect a signal generator to the input SMA connectors. Setup input signal according to the device data sheet.
3. Connect a test measurement device on the device output SMA connectors.

NOTE: The test measurement device must contain 50 Ω termination.

Table 17. Bill of Materials

Components	Manufacturer	Description	Part Number	Web Site
SMA Connector	Rosenberger	SMA Connector, Side Launch, Gold Plated	32K243−40ME3	http://www.rosenberger.de http://www.rosenbergerna.com
	Johnson Components*	SMA Connector, Side Launch, Gold Plated	142−0701−851	http://www.johnsoncomponents.com
Surface Mount Test Points	Keystone*	SMT Miniature Test Point	5015	http://www.keyelco.com
		SMT Compact Test Point	5016	
		Thru−Hole Mount Compact Test Point	5005−5009	
Chip Capacitor	AVC Corporation*	0603 0.01 μF ±10%	06035C103KAT2A	http://www.avxcorp.com
		0603 0.1 μF ±10%	06035C104KAT2A	
Chip Resistor	Vishay Dale*	0603 50 Ω ± 1% Thick Film Resistor	CRCW060351R1J	http://www.vishay.com
Evaluation Board	ON Semiconductor	SOIC 8 Evaluation Board	ECLSOIC8EVB	http://www.onsemi.com
Device Samples	ON Semiconductor	SOIC 8 Package Device	Various	http://www.onsemi.com

*Components are available through most distributors, i.e. www.newark.com, www.digikey.com

Appendix A (Modified Configurations)

MC10EL16D/MC100EL16D
MC100LVEL16D
MC10EP16D/MC100EP16D
MC10EP16DF/MC100EP16DF
MC100EP16VAD
MC100LVEP16D

The devices listed above have the option of being driven single−endedly by using the provided V_{BB} pin of the device. In order to drive it single−endedly, Configuration 2 needs to be modified.

1. Remove the 50 Ω chip resistor from R3.
2. Short pin 3 and pin 4 together.
   - Option A) Short R3 and R4 trace pads.
     Or
   - Option B) Place a SMA connector on J4 and use a cable with SMA connectors to short J3 and J4 connectors.

MC10EP16D/MC100EP16DT

This device has an option of being 50 Ω terminated internally. To evaluate the internal 50 Ω resistor of the device, Configuration 2 needs to be modified.

1. Remove the 50 Ω chip resistors from R2 and R3.
2. Short R1 and R4 to V_{TT} (GND).
   - Option A) Short R1 and R4 to V_{TT} (GND).
     Or
   - Option B) Place SMA connectors on J1 and J4. Place shorting barrels on J1 and J4 SMA connector.

MC100EP16VBD

This device has an option of single−ended feedback output and being driven single−endedly using the V_{BB}. To utilize the feedback option and drive it single−endedly, Configuration 2 needs to be modified.

Feedback option

1. Connect a SMA connector on J1

Drive single−endedly

2. Remove the 50 Ω chip resistor from R3.
3. Short pin 3 and pin 4 together.
   - Option A) Short R3 and R4.
     Or
   - Option B) Place a SMA connector on J4 and use a cable with SMA connectors to short J3 and J4 connectors.

MC100EP16VCD

This device has an option of single−ended feedback output with an enable pin. To utilize the feedback option and enable option, Configuration 5 needs to be modified.

1. Connect a SMA connector on J1.
2. Remove the 50 Ω chip resistor from R3.

MC100EP16VSD

This device has an option of varying the output swing amplitude and being driven single−endedly. In order to utilize these options, Configuration 2 needs to be modified.

Output Swing Control

1. Connect a SMA connector on J1
2. Add a decoupling capacitor between J1 and V_{CC} (0.01 μF)

Drive Single−Endedly

1. Remove the 50 Ω chip resistor from R3.
2. Short pin 3 and pin 4 together.
   - Option A) Short R3 and R4.
     Or
   - Option B) Place a SMA connector on J4 and use a cable with SMA connectors to short J3 and J4 connectors.

MC100EP16VTD

This device has an option of varying the output swing amplitude and internal termination. In order to utilize these options, Configuration 2 needs to be modified.

Output Swing Control

1. Connect a SMA connector on J1
2. Add a decoupling capacitor between J1 and V_{CC} (0.0 1 μF)

Internal Termination

1. Remove the 50 Ω chip resistors from R2 and R3.
2. Short R1 and R4 to V_{TT} (GND)
   - Option A) Short R1 and R4 to V_{TT} (GND).
     Or
   - Option B) Place SMA connectors on J1 and J4. Place shorting barrels on J1 and J4 SMA connector.

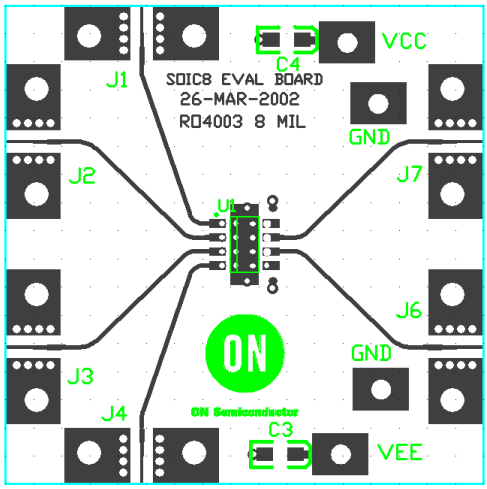
MC10ELT21D/MC100EL21D
MC100EL23D
MC10ELT26D/MC100ELT26D
MC100EPT21D
MC100EPT23D
MC100EPT26D
MC100LVELT23

The TTL output data presented in the data sheet are obtained under 500 Ω load resistor in parallel with 20 pF fixture capacitance. In order to obtain comparable data as in the data sheet, the evaluation board needs to be modified.

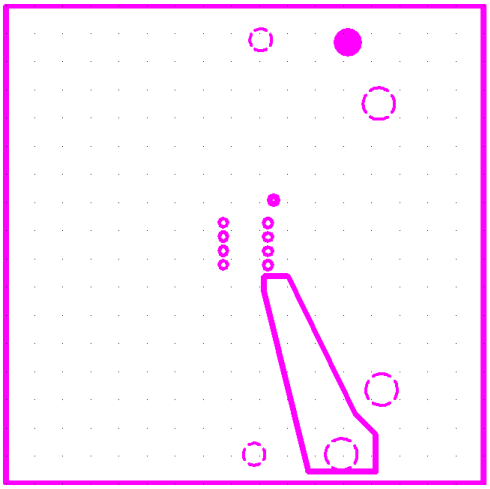
1. Cut the output trace so that the 0402* size chip resistor can be placed over the cut out trace.
2. Solder a 450 Ω chip resistor across the cut out trace.

*Any size chip resistor can be used. The recommended size of the chip resistor is 0402, to reduce the effect of parasitic with a 17 mil trace width. 450 Ω in series with 50 Ω instrument resistance add up to 500 Ω loaded condition.

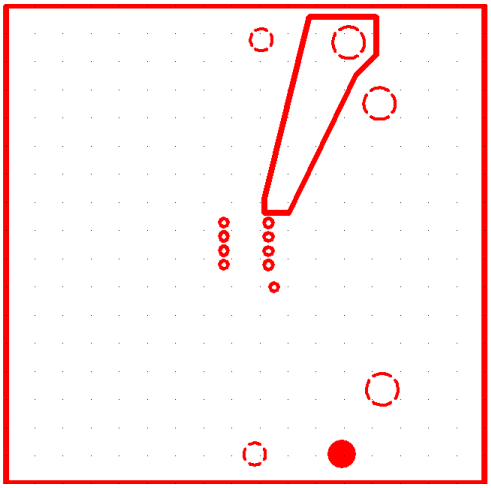
Appendix B (Gerber Files)



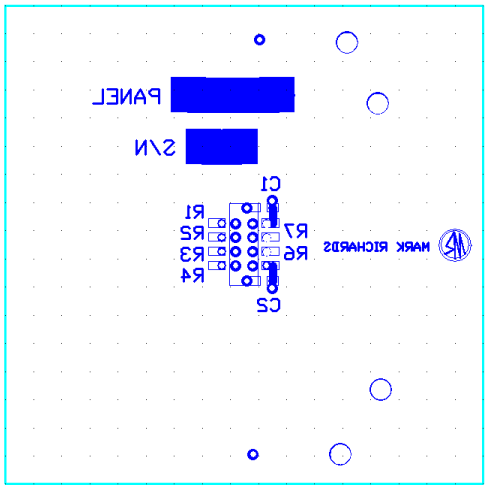
Top Layer



Second Layer (V_{EE} and Ground Plane



Third Layer (V_{CC} and Ground Plane)



Bottom Layer

Figure 16. Gerber Files

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