Using the UCC3895 in a Direct Control Driven Synchronous Rectifier Applications

User's Guide



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1 Introduction

The UCC3895EVM-001 evaluation module (EVM) is an isolated 48-V input phase-shifted full-bridge converter providing an output of 3.3 V at 15 A. The AB outputs of the UCC3895, in this application are used for direct control driven synchronous rectification. No demodulation of the AB phase shift clock signals is necessary to produce fully operational synchronous rectification gate drive signals yielding a significant overall efficiency increase.

Operating in peak current-mode control, this EVM highlights the many benefits of using the UCC3895 advanced phase-shift PWM controller for direct control of synchronous rectification. This user's guide provides the schematic, component list, assembly drawing, artwork and test setup necessary to evaluate the UCC3895 in a typical control-driven synchronous rectification application.

2 Features

- 48-V typical input (36 V < VIN < 72 V), 2:1 input range
- 3.3-V output at 15 A_{DC}
- Control driven synchronous rectifier current doubler output
- 1500-V input to output isolation
- Compact size, low profile (3.5" x 2.5" x 0.5")
- Peak current-mode control
- 400-kHz oscillator frequency (200-kHz operating frequency)
- Fixed-frequency operation
- 87% efficiency
- Single side OTS surface-mount components
- Short circuit protection

3 Description

The UCC3895EVM-001 EVM highlights the benefits of using the UCC3895 to implement direct control of a synchronous rectifier current-doubler output in a phase-shifted full bridge topology. The UCC3895 provides four 100-mA complementary outputs, labeled OUTA-OUTD, optimized to drive FET driver circuits. Two of the complementary outputs, OUTA and OUTB, are used to generate the drive signals necessary to switch the synchronous rectifiers. Since the UCC3895 controller is referenced to primary side ground, the OUTA and OUTB signals must first transition through a signal transformer before being fed into the secondary-side referenced UCC27424 dual 4-A MOSFET driver. This technique provides the proper gating and timing signals necessary to accurately synchronize the output switching to the primary-side bridge switching.

In addition to implementing synchronous rectification, designing a highly efficient phase shifted full bridge power converter is greatly dependant upon understanding the parasitic elements within the converter. This is necessary to optimize the resonant circuit responsible for achieving ZVS. The UCC3895 offers the added feature of adaptive delay set (ADS) and delay programming between complementary outputs. The ADS function serves to vary the delay time necessary, during the resonant transition period, as a function of load current. When more current is available to fully charge the equivalent resonant capacitance, less delay time is required, resulting in a longer effective duty cycle available for power transfer.

Further information regarding the details of ZVS resonant requirements and optimizing the UCC3895 PWM in a current doubler phase-shifted full-bridge topology are fully explained in references [1] - [3] and are not repeated here. As such, the scope of the following documentation shall focus primarily on configuring the UCC3895 for direct control driven synchronous rectification applications.

3.1 Schematic

A schematic of the UCC3895EVM-001 board is shown in Figure 1. Terminal block J2 is the DC input voltage source connector. Terminal block J3 is the DC primary-side bias voltage, while terminal block J1 is the secondary output and return for the 3.3-V output.

The primary-side full-bridge power section is comprised of MOSFET's Q1-Q4. Because the converter switches at zero voltage, 8-pin SOIC packages were selected forgoing the use of large heatsinks typically found at this power level. Control of the full bridge is provided by U1, the UCC3895 and its accompanying circuitry. The four outputs of the UCC3895 are fed into two Texas Instruments UCC27200. The UCC27200 is a 3-A, 120-V high frequency high-diode/low-side driver which was chosen primarily because of the low impedance drive of 4 Ω. Primary power is efficiently transferred to the secondary across T1, a low profile planar transformer available from Payton.

Q5 and Q6 are the secondary-side synchronous rectifier MOSFET's shown with associated local gate discharge circuitry made up of D16, Q9, and D17, Q8. As mentioned previously, the control signals for Q5 and Q6 are derived directly from OUTA and OUTB of the UCC3895, greatly simplifying any timing issues typically met when designing isolated control driven synchronous power converters. To maintain isolation, OUTA and OUTB are fed through T3, a signal transformer. The output of T3 is then used as the input to U4, a UCC27424 dual 4-A MOSFET driver that directly drives the gates of Q5 and Q6. Passing OUTA and OUTB through T3 before U4 minimizes any leakage inductance current spike based on the fact that very little power is actually transferred through T3. In addition, a secondary side referenced bias voltage is generated from T3 and used to power U4, pin 6 (VDD).

The secondary to primary feedback path of the UCC3895EVM-001 is optically isolated via U3. The compensation network is located on the secondary side and is built around U5, a TL431 adjustable shunt regulator. This provides a low cost, simplified secondary referenced feedback solution with good noise immunity. Designing the UCC3895 for peak current mode control, allows a single pole (R33, C10), single zero (R33, C11) compensation network to be used. R41 and C14 are present to compensate for the inherent pole of the optocoupler. The feedback divider circuitry is set by R32 and R34, while the UCC3895 error amp (U1, pins 1 and 2) is set up in a voltage follower configuration.

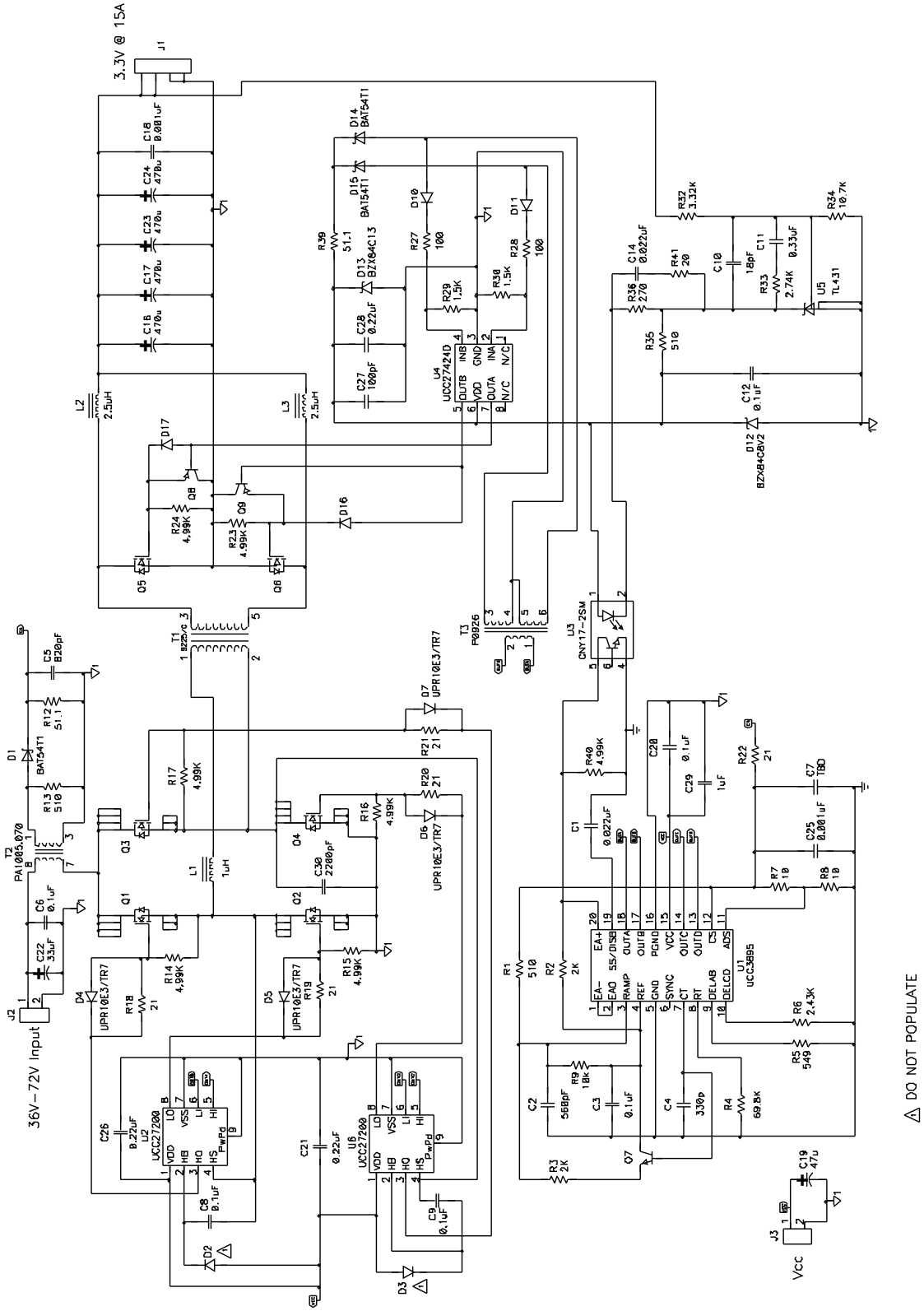


Figure 1. UCC3985EVM-001 Schematic

3.2 Circuit Performance

The schematic shown in Figure 1 was built and tested upon the printed circuit board (PCB) design shown in Figure 10 through Figure 14. For a detailed description of the list of materials used, refer to Table 1.

3.3 UCC3895EVM-001 ZVS Measured Data

In addition to a significant increase in overall efficiency, one of the primary benefits of using synchronous rectifiers in a phase-shifted full bridge topology is to extend the useful load range for ZVS operation. While there is always the argument that ZVS may not be a concern at light load, due to the reduction in power dissipation, the objective of this design is to extend ZVS operation down to some minimum load less than that of the DM3895. One benefit of doing so would perhaps become more apparent from a systems point of view where electromagnetic interference (EMI) would be a concern. At the point where the converter crosses over from ZVS to traditional hard switching, a noticeable change in the EMI signature would be expected, which in the worst case might possibly result in a noncompliant system.

Figure 2 and Figure 3 show the MOSFET drain-to-source and gate-to-source waveforms of Q2 and Q4 for an input voltage of 48 V. Since Q2 and Q4 each have primary ground-referenced sources, they are convenient test points for obtaining ZVS waveforms. Q2 is the bottom MOSFET of the AB leg while Q4 corresponds to the CD leg. At an output load of 15 A, the drain voltage of each MOSFET completely falls to zero before the gate voltage starts to rise, clearly illustrating that each leg is switching at zero voltage.

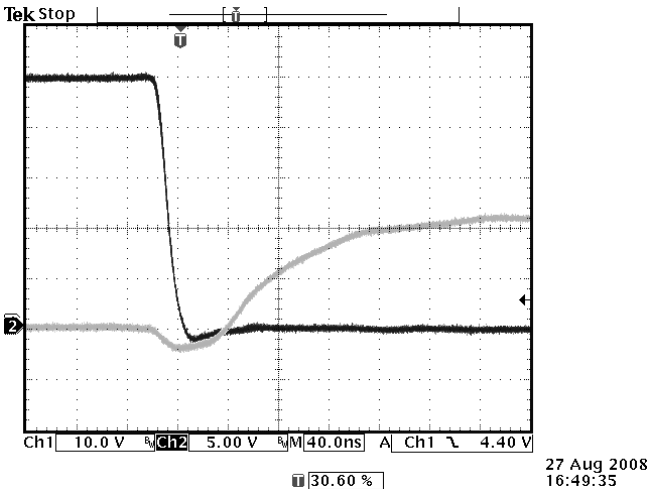


Figure 2. Q2 (AB Leg) at 15-A Load

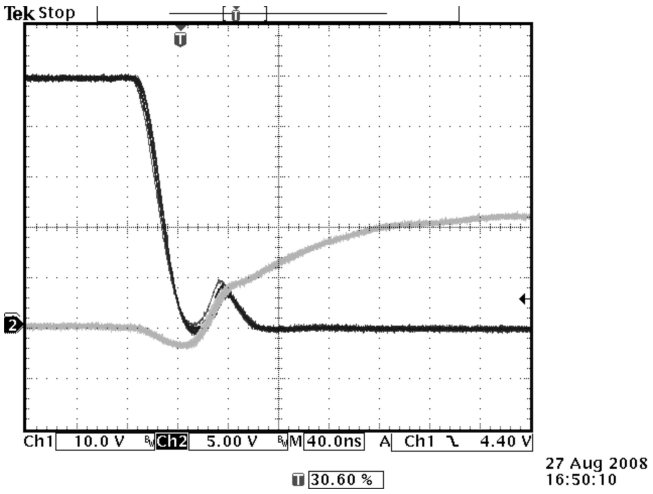


Figure 3. Q4 (CD Leg) at 15-A Load

More importantly, Figure 4 and Figure 5 show the same waveforms of Q2 and Q4, switching during an output load of 5.5 A. Figure 4 shows that the drain voltage of Q2 still falls to zero, prior to the gate voltage starting to rise. However, the upward cusp shown on the drain voltage signal suggests that the stored resonant inductive energy is almost insufficient to drive the total resonant capacitance. ZVS is retained down to a minimum output load of 5.5 A in the AB leg, where the start of hard switching begins. Conversely, Figure 5 illustrates that the CD leg is still switching at zero voltage at the same output load where ZVS is nearly lost in the AB leg.

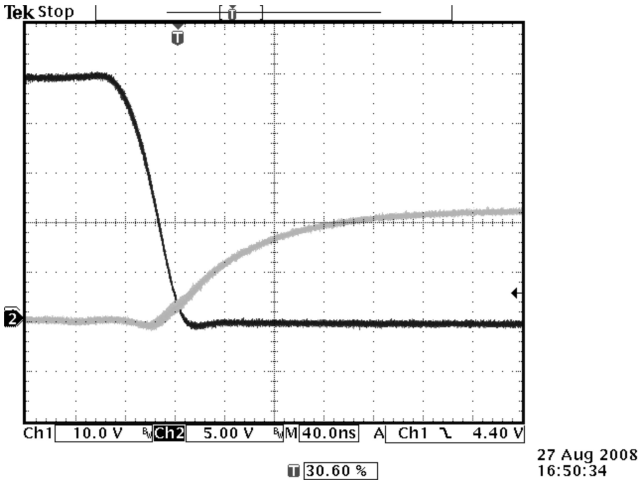


Figure 4. Q2 (AB Leg) at 5.5-A Load

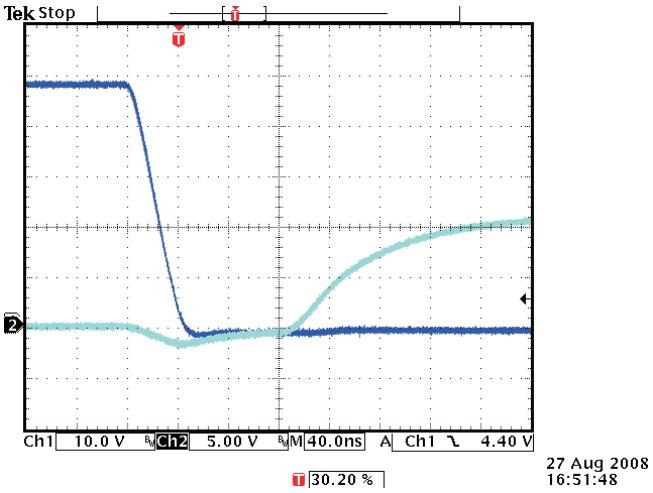


Figure 5. Q4 (CD Leg) at 5.5-A Load

At output loads less than 5.5 A, the UCC3895EVM-001 loses the benefits of ZVS in the AB leg, as the converter moves deeper into hard switching. The worst case of this is shown below in Figure 6 where the gate of Q2 moves beyond VGS(th) while there is still significant voltage present on the drain when operating with no output load current. From Figure 7 however, notice that the ZVS of the CD leg is retained all the way down to zero output load current. The switching details of how this is possible are fully explained in reference [1].

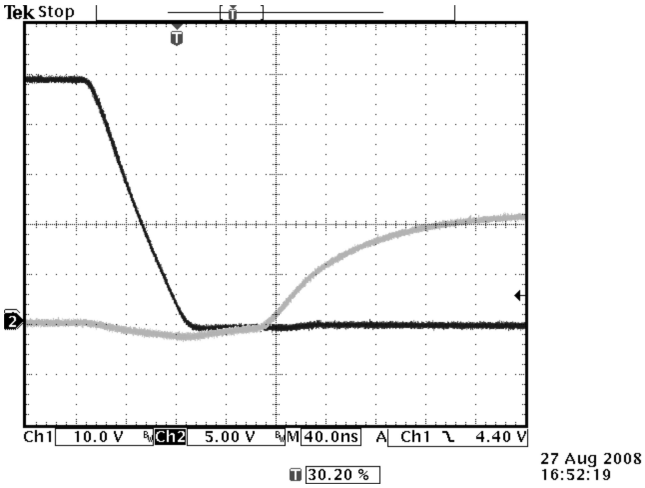


Figure 6. Q2 (AB Leg) at 0-A Load

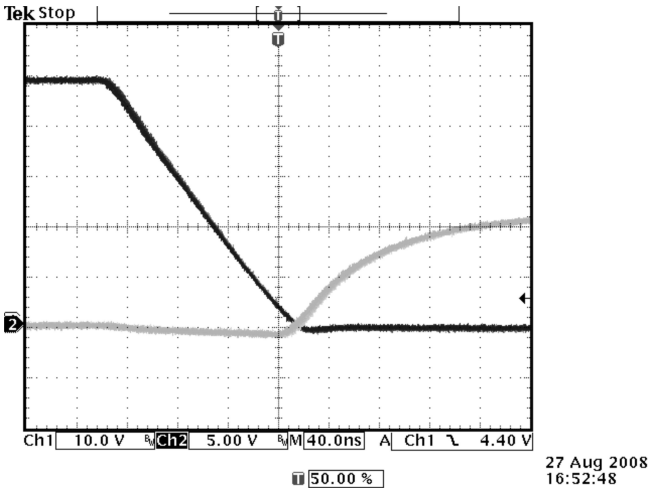


Figure 7. Q4 (CD Leg) at 0-A Load

At an output load current of 15 A, the UCC3895EVM-001 has an efficiency of approximately 85%, while the peak efficiency of just over 87% occurs between a load current of 7 A to 10 A. A plot of efficiency versus output power for an input voltage of 48 V is shown below in Figure 8.

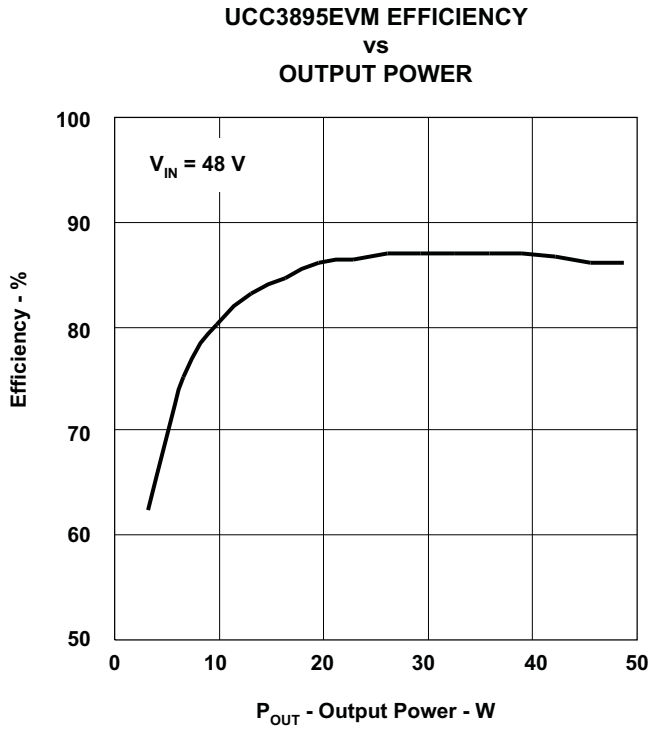


Figure 8.

4 Test Set Up

Shown below in Figure 9 is the basic test setup needed to evaluate the UCC3895EVM-001. Please note the secondary ground (J1) is isolated from primary ground (J2, J3).

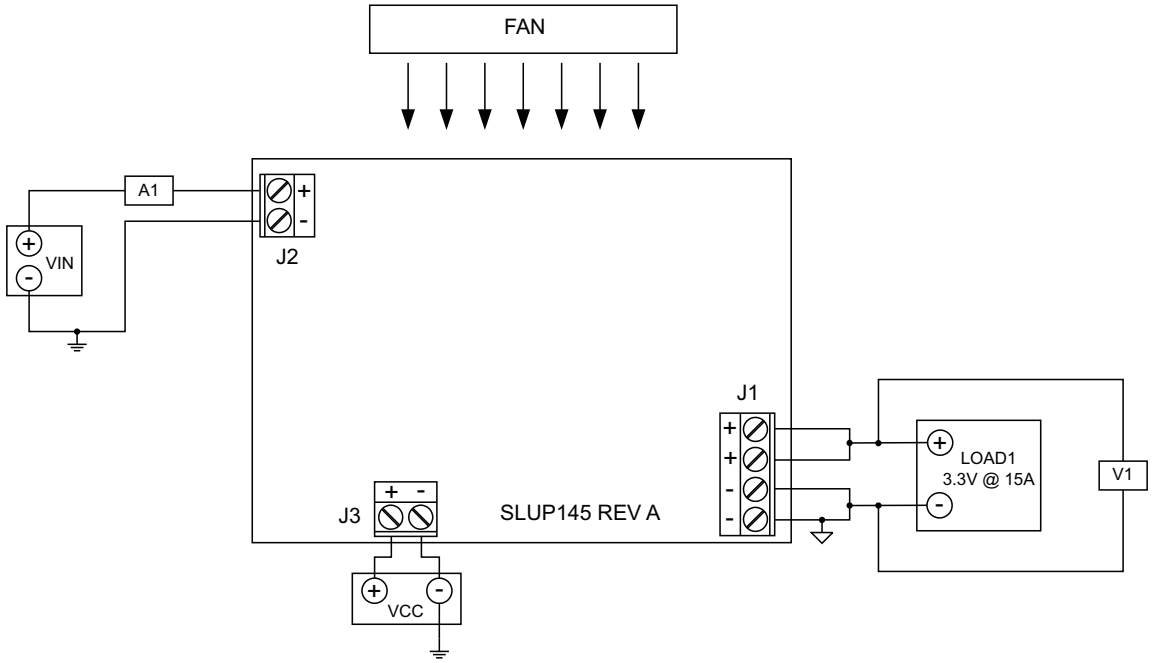


Figure 9. Recomended EVM Test Configuration

4.1 Output Load (LOAD1)

For the output load to VOUT, a programmable electronic load set to constant current mode and capable of sinking 0 -15 A_{DC}, is used. The UCC3895EVM-001 is ground isolated between the input and output. VIN and VCC are referenced to the primary side while VOUT is secondary side referenced. Refer to the EVM schematic of Figure 1 and the test setup of Figure 9. Using a DC voltmeter, V1, it is also advised to make all output voltage measurements directly at J1 terminals in order to minimize any voltage error experienced due to drops between J1 and the electronic load.

4.2 VCC DC Bias Supply (VCC)

The bias voltage supply is a variable DC source capable of supplying between 0 V_{DC} and 12 V_{DC} at no less than 0.25 A_{DC} and connected to J3 as shown in Figure 9.

4.3 DC Input Source (VIN)

The input voltage should be a variable DC source capable of supplying between 0 V_{DC} and 72 V_{DC} at no less than 2 A_{DC}, and connected to J2 as shown in Figure 9. For fault protection to the EVM, good common practice is to limit the source current to no more then 1.75 A_{DC}. A DC ammeter, A1 should also be inserted between VIN and J2 as shown in Figure 9.

4.4 Fan

Most power converters include components that can get hot to the touch when approaching temperatures of 60°C. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 20-30 cfm is recommended to reduce component temperatures when operating at full output load.

5 Power Up/Down Test Procedure

The following test procedure is recommended primarily for power up and shutting down the EVM. Whenever the EVM is running above an output load of 10 A, the fan should be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Connect VCC to J3 as shown in Figure 9. Make sure that VCC is initially set to 0 V.
3. Prior to connecting the DC input source, VIN, it is advisable to limit the source current from VIN to 1.75 A maximum. Connect the ammeter A1 (0-1.5 A range) between VIN and J2 as shown in Figure 9. Make sure VIN is initially set to 0 V.
4. Connect LOAD1 and the voltmeter, V1 to J1 as shown in Figure 9. Set LOAD1 to constant current mode to sink 0 A_{DC} before VIN and VCC are applied.
5. Increase VCC from 0 V_{DC} to 12 V_{DC} (overcome UVLO threshold) and then set to 10.5 V_{DC}. With VCC applied, the control and switching circuitry can now be checked from the UCC3895 outputs to the gates of the bridge MOSFETS, Q1-Q4 and synchronous MOSFETS, Q5 and Q6.
6. Increase VIN from 0 V to 48 V_{DC}, while monitoring the output voltage on V1.
7. Vary LOAD1 anywhere between 0 A to 15 A_{DC}, making sure to turn on fan blowing air directly on the EVM for loads above 10 A.
8. Vary the input voltage between 36 V and 72 V.
9. Shut down the electronic load.
10. Shut down VIN.
11. Shut down VCC.

6 EVM Assembly Drawing and Layout

Figure 10 shows the top-side component placement for the EVM, as well as pin numbers and component polarity where necessary. A four layer PCB was designed using the top and bottom layers for signal traces and an internal split ground plane tied to a single point at C22. The PCB dimensions are 3.5" x 2.5" with a design goal of maintaining all components to less than 0.5" high measured from the top layer surface. All components are standard OTS surface-mount components placed on the top side of the PCB only. The copper etch, looking through the top of the PCB, for each layer is also shown in Figure 11 through Figure 14.

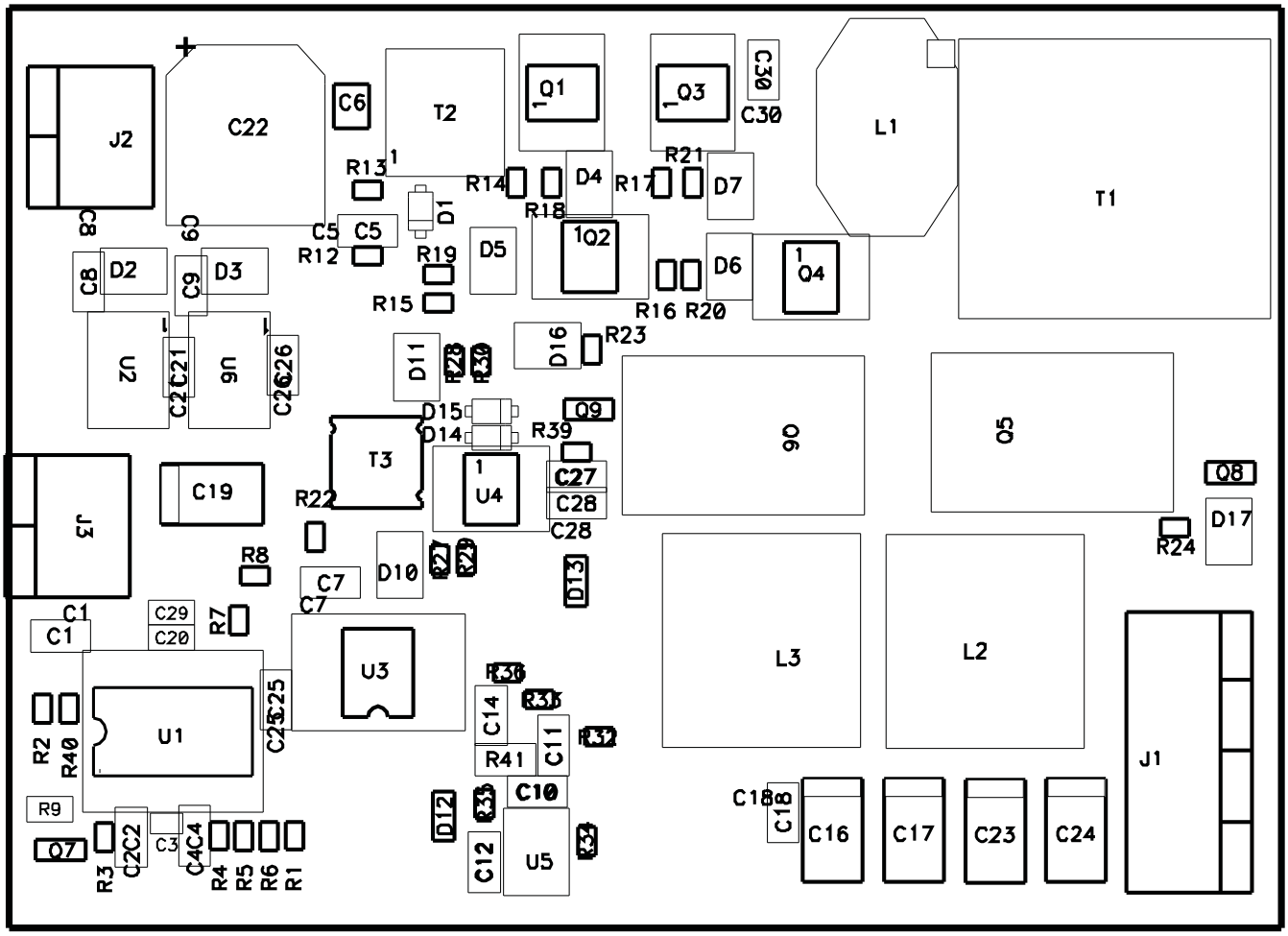


Figure 10. Top-Side Component Assembly

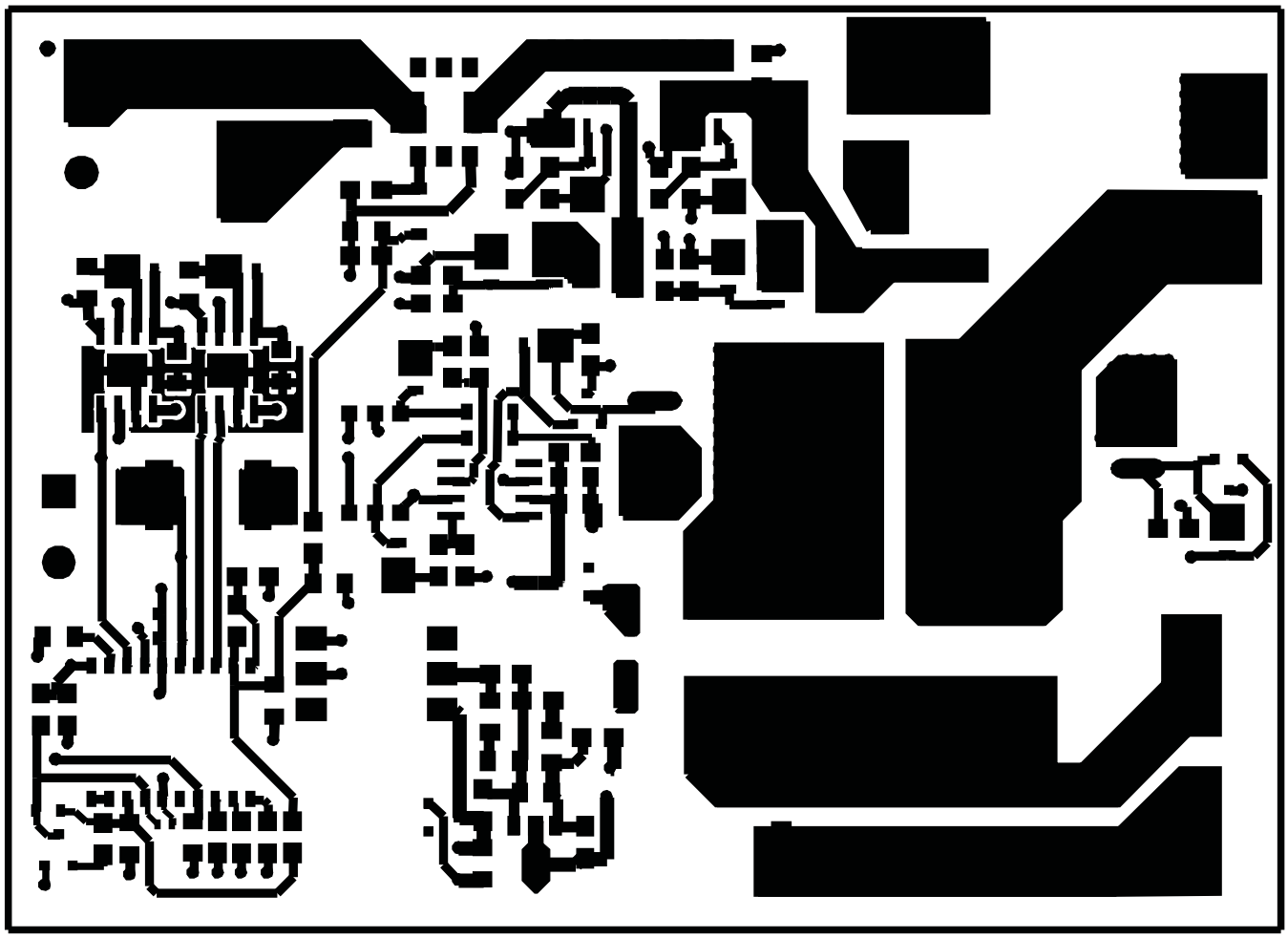


Figure 11. Top Signal Trace Layer

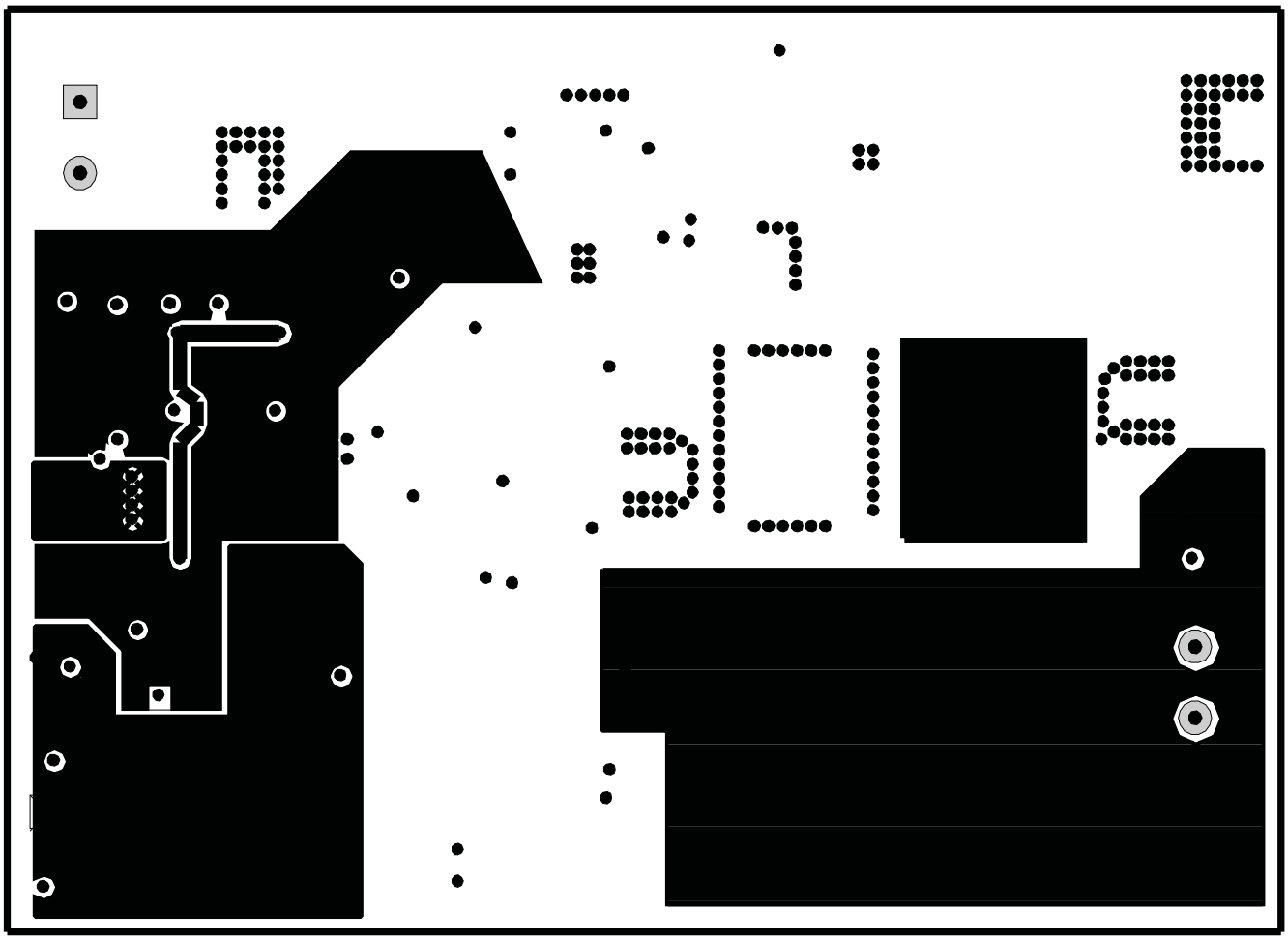


Figure 12. Internal Signal Trace Layer

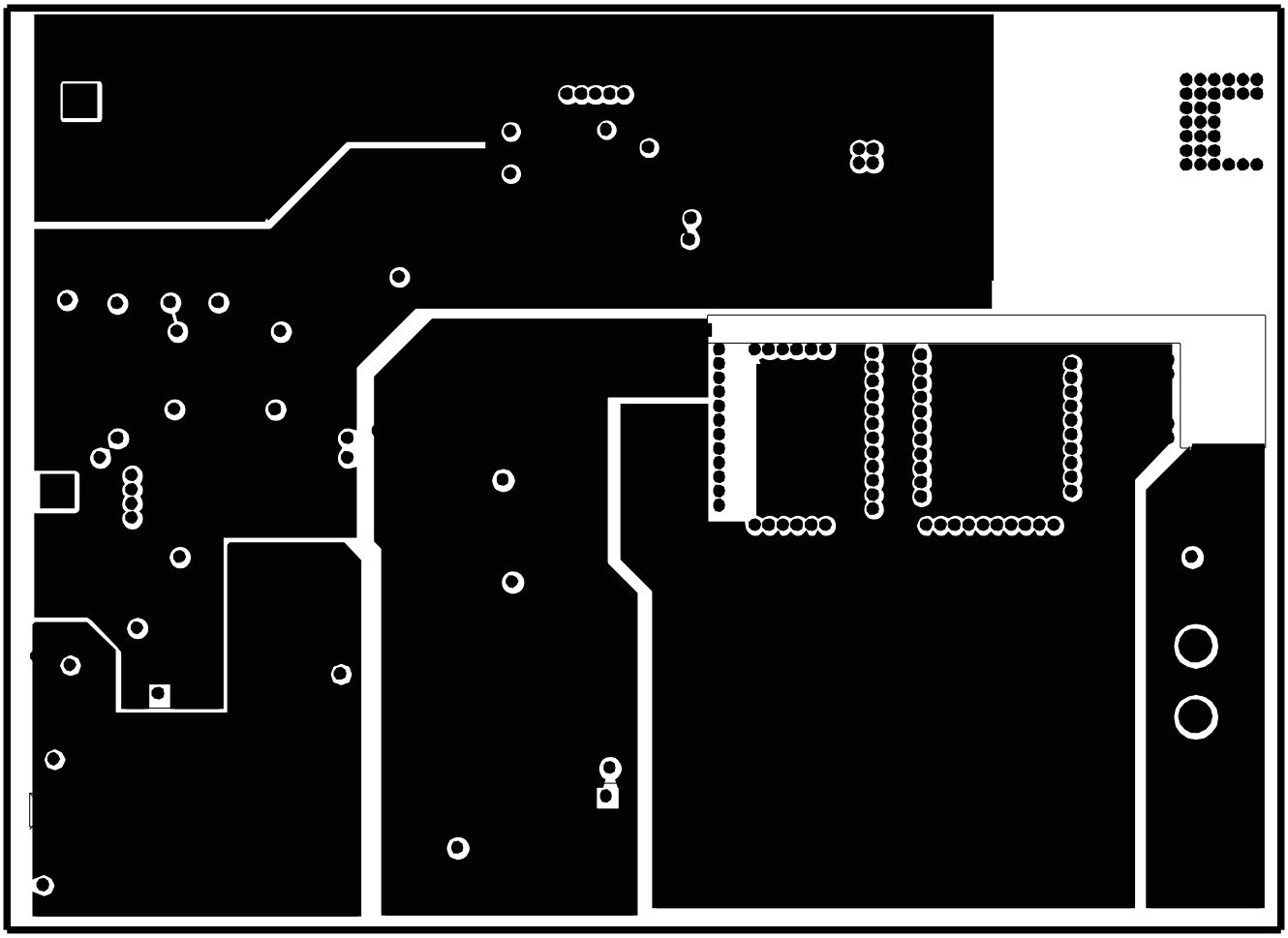


Figure 13. Internal Split Ground Plane

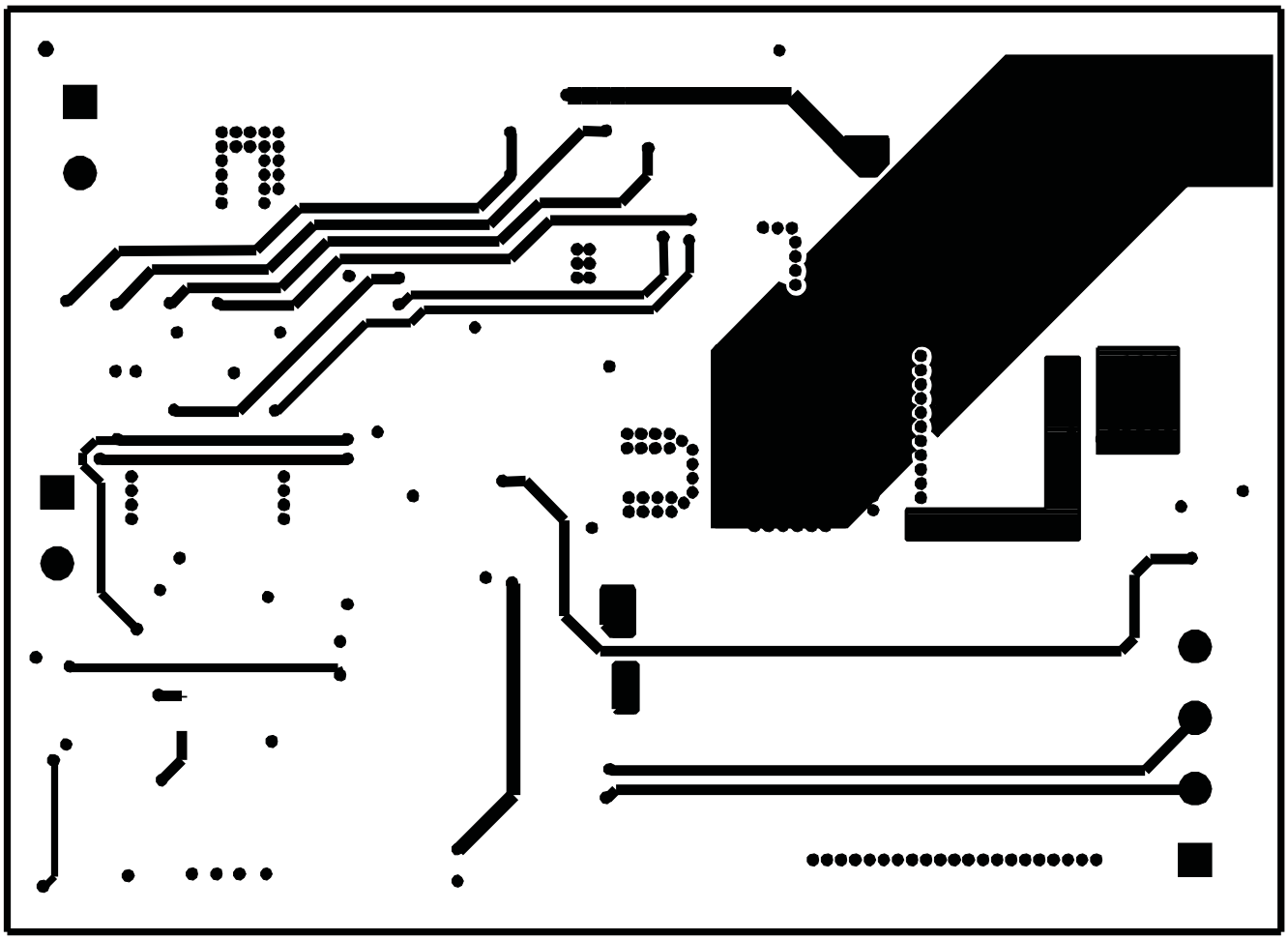


Figure 14. Bottom Signal Trace Layer

7 List of Materials

Table 1 below lists the EVM components as configured corresponding to the schematic shown in Figure 1. Part types and manufacturers can be modified according to specific application requirements.

Table 1. List of Materials(1)(2)(3)(4)

REF DES	COUNT	DESCRIPTION	MFR	PART NUMBER
C1, C14	2	Capacitor, ceramic, 0.022 µF, 50 V, X7R, 10%, 0805	Std	Std
C10	1	Capacitor, ceramic, 18 pF, 50 V, NPO, 10%, 0805	Std	Std
C11	1	Capacitor, ceramic, 0.33 µF, 16 V, X7R, 10%, 0805	Std	Std
C16, C17, C23, C24	4	Capacitor, tantalum, 470 µF, 6.3 V, 50.0 mΩ, 20%, 7343 (D)	AVX	TPSE477M006R0050
C18, C25	2	Capacitor, ceramic, 1000 pF, 50 V, X7R, 10%, 0805	Std	Std
C19	1	Capacitor, tantalum, 47 µF, 20 V, 125.0 mΩ, 10%, 7343 (D)	AVX	TPSE476K020R0125
C2	1	Capacitor, ceramic, 560 pF, 50 V, X7R, 10%, 0805	Std	Std
C20	1	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%, 0603	Std	Std
C21, C26, C28	3	Capacitor, ceramic, 0.22 µF, 25 V, X7R, 10%, 0805	Std	Std
C22	1	Capacitor, aluminum, SM, 33 µF, 100 V, VS series, 10x12mm	Panasonic	EEE-2AA330P
C27	1	Capacitor, ceramic, 100 pF, 50 V, X7R, 10%, 0805	Std	Std
C29	1	Capacitor, ceramic, 1 µF, 25 V, X5R, 10%, 0603	Std	Std
C3	1	Capacitor, ceramic, 0.1 µF, 10 V, X5R, 10%, 0402	Std	Std
C30	1	Capacitor, ceramic, 2200 pF, 50 V, X7R, 10%, 0805	Std	Std
C4	1	Capacitor, ceramic, 330 pF, 50 V, X7R, 10%, 0805	Std	Std
C5	1	Capacitor, ceramic, 820 pF, 50 V, X7R, 10%, 0805	Std	Std
C6	1	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%, 1210	Std	Std
C7	1	Capacitor, ceramic, 0805	Std	Std
C8, C9, C12	3	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%, 0805	Std	Std
D1, D14, D15	3	Diode, Schottky, 200 mA, 30 V, SOD123	On Semi	STD
D12	1	Diode, Zener, 8.2 V, 25 mA, 225 mW, SOT23	Onsemi	BZX84C8V2LT1G
D13	1	Diode, Zener, 13 V, 20 mA, 225 mW, SOT23	Onsemi	BZX84C13LT1G
D4, D5, D6, D7, D10, D11, D16, D17	8	Diode, 2.5 A, 25 ns, 100 V, powermite, 75 x 148	Microsemi	UPR10E3/TR7
J1	1	Terminal block, 4 pin, 15 A, 5.1 mm, 0.80 x 0.35""	OST	ED2227
J2, J3	2	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 x 0.35""	OST	ED1609
L1	1	Inductor, SMT, 1 µH, 4.0 A, 25 mΩ, 0.510 x 0.370	Coilcraft	DT3316P-102
L2, L3	2	Inductor, 2.5 µH, 11.4 A smd, 500 x 500	Coilcraft	MLC1550-252ML
Q1, Q2, Q3, Q4	4	MOSFET, N-channel, 100 V, 7.3 A, 22 mΩ, SO8	IR	IRF7495
Q5, Q6	2	Transistor, NFET, 80 A, 60 V, 35 mΩ, TO-263AB	Fairchild	FDB035AN06A0
Q7	1	Bipolar, NPN, 80 V, 600 mA, SOT23	Diodes Inc	MMBTA06-7-F
Q8, Q9	2	Bipolar, PNP, 60 V, 600 mA, SOT23	Diodes Inc	MMBT2907ALT1G
R1, R13, R35	3	Resistor, chip, 510 Ω, 1/10 W, 1%, 0805	Std	Std
R12	1	Resistor, chip, 51.1 Ω, 1/10 W, 1%, 0805	Std	Std
R14, R15, R16, R17, R23, R24, R40	7	Resistor, chip, 4.99 kΩ, 1/10 W, 1%, 0805	Std	Std
R18, R19, R20, R21, R22	5	Resistor, chip, 21 Ω, 1/10 W, 1%, 0805	Std	Std
R2, R3	2	Resistor, chip, 2 kΩ, 1/10 W, 1%, 0805	Std	Std

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

Table 1. List of Materials (continued)

REF DES	COUNT	DESCRIPTION	MFR	PART NUMBER
R39	1	Resistor, chip, 51.1 Ω, 1/10 W, 1%, 0805	Std	Std
R27, R28	2	Resistor, chip, 100 Ω, 1/10 W, 1%, 0805	Std	Std
R29, R30	2	Resistor, chip, 1.5 kΩ, 1/10 W, 1%, 0805	Std	Std
R32	1	Resistor, chip, 3.32 kΩ, 1/10 W, 1%, 0805	Std	Std
R33	1	Resistor, chip, 2.74 kΩ, 1/10 W, 1%, 0805	Std	Std
R34	1	Resistor, chip, 10.7 kΩ, 1/10 W, 1%, 0805	Std	Std
R36	1	Resistor, chip, 270 Ω, 1/10 W, 1%, 0805	Std	Std
R4	1	Resistor, chip, 69.8 kΩ, 1/10 W, 1%, 0805	Std	Std
R41	1	Resistor, chip, 20 Ω, 1/10 W, 1%, 0805	Std	Std
R5	1	Resistor, chip, 549 Ω, 1/10 W, 1%, 0805	Std	Std
R6	1	Resistor, chip, 2.43 kΩ, 1/10 W, 1%, 0805	Std	Std
R7, R8	2	Resistor, chip, 10 Ω, 1/10 W, 1%, 0805	Std	Std
R9	1	Resistor, chip, 1/16 W, 0.1%, 0603	Std	Std
T1	1	Xfmr, planer,100 W, 6:2, smd, 760x850	Payton	9225, RevC
T2	1	XFMR, current sense, 20 A, 1:70, 0.284 x 0.330 inch	Pulse	PA1005.070
T3	1	Transformer, dDriver, 330 µH Ip, 1500 V isolation, 0.210 x 0.210	Pulse	P0926
U1	1	BiCMOS Advanced Phase Shift PWM Controller, TSSOP 20 pin	Texas Instruments	UCC3895
U2, U6	2	120-V Boot, 2.5-A Peak, High-Freq. High-Side Low-Side Driver, SO8[DDA]	Texas Instruments	UCC27200
U3	1	Opto coupler, 6-pin DIP, modified	Isocom	CNY17-2SM
U4	1	Dual 3 A MOSFET driver, SOIC-8	Texas Instruments	UCC27424D
U5	1	Adjustable precision shunt regulator, SOT-89	Texas Instruments	TL431CPKR

8 References

1. Balogh, L. Design Review: *100-W, 400-kHz, DC/DC Converter With Current Doubler Synchronous Rectification Achieves 92% Efficiency*, Topic 2, SEM-1100 Power Supply Design Seminar Manual, Unitrode Corporation
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3. Balogh, L. The Current Doubler Rectifier: A*n Alternative Rectification Technique For Push-Pull and Bridge Converters*, Texas Instruments Literature No. SLUA121
4. Dennis, M. *UCC3895 Phase Shift PWM Controller EVM Kit Setup and Usage*, Texas Instruments Literature No. SLUU069A

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 36 V to 72 V and the output voltage range of 0V to 3.3 V as supplied.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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