User's Manual

RTKA2108702H00000BU

User's Manual: Evaluation Board

Industrial Analog and Power

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1. Overview

The RAA210870 is a pin-strap configurable 70A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally enhanced HDA packaging technology, the module can deliver up to 70A of continuous output current without the need for airflow or additional heat sinking. The RAA210870 uses ChargeMode™ control (ASCR) architecture, which responds to a transient load within a single switching cycle.

The RTKA2108702H00000BU evaluation board is a 4.7in x 4.8in 8-layer FR4 board with 2oz. copper on all layers. This evaluation board comes with placeholders for pin-strap resistor population to adjust output voltage, switching frequency, soft-start/stop timing, input UVLO threshold, ASCR gain and residual parameters, and device PMBus address. Fault limits can be easily programmed or changed using a PMBus-compliant serial bus interface.

The optional ZLUSBEVAL3Z (USB to PMBus adapter) is provided with this evaluation board, which connects the evaluation board to a PC to activate the PMBus communication interface. The PMBus command set is accessed by using the PowerNavigator™ evaluation software from a PC running Microsoft Windows. The RTKA2108702H00000BU can operate in Pin-Strap mode without needing the ZLUSBEVAL3Z adapter or PMBus communication.

1.1 Key Features

- V_{IN} range of 4.5V to 14V, V_{OUT} adjustable from 0.6V to 2.5V
- Programmable V_{OUT}, input and output UVP/OVP, OTP/UTP, soft-start/stop, and external synchronization
- Monitor: V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, switching frequency, and faults
- ChargeMode control tunable with PMBus
- Mechanical switch for enable and power-good LED indicator

1.2 Specifications

This board is configured for the following operating conditions by default:

- V_{IN} = 4.5V to 12V
- V_{OUT} = 0.93V
- I_{MAX} = 70A
- f_{SW} = 320kHz
- Peak efficiency: >91% at 70% load
- ASCR gain = 200, ASCR residual = 90
- On/off delay = 5ms; On/off ramp time = 5ms

1.3 Ordering Information

Part Number	Description
RTKA2108702H00000BU	RAA210870 evaluation board, ZLUSBEVAL3Z adapter, USB cable

1.4 Related Literature

For a full list of related documents, visit our website

- RAA210870 product page

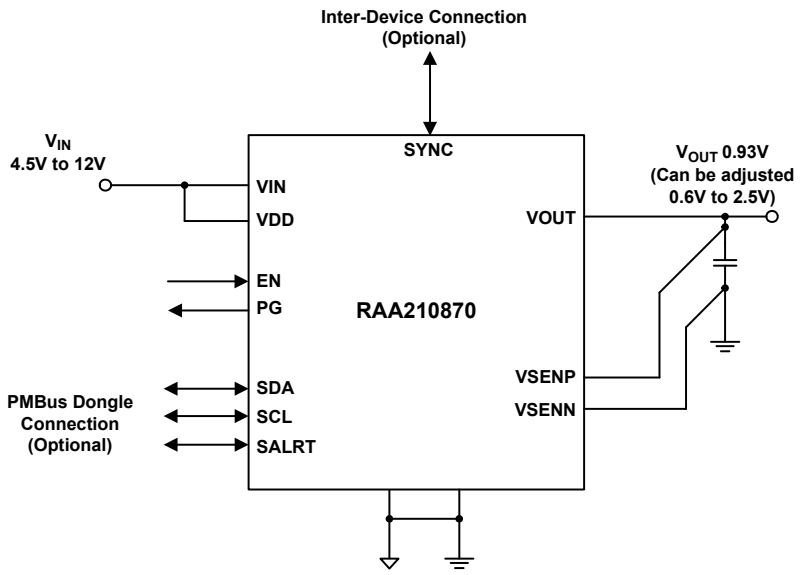

Figure 1. Block Diagram

1.5 Recommended Equipment

- DC power supply with minimum 15V/40A sourcing capacity
- Electronic load capable of sinking current up to 70A
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

2. Functional Description

The RTKA2108702H00000BU provides all circuitry required to evaluate the features of the RAA210870. A majority of the features of the RAA210870, such as compensation-free ChargeMode control, soft-start delay and ramp times are available on this evaluation board. For interleave functionality evaluation, the board can be connected to another Renesas digital module evaluation board.

Figures 5 and 6 show the board images of the RTKA2108702H00000BU evaluation board.

2.1 Operating Range

By default, the RTKA2108702H00000BU is configured to operate at V_{OUT} = 0.93V, f_{SW} = 320kHz. V_{IN} ranges from 4.5V to 12V. The board can also support a wider operating range to meet the requirements of specific applications. The V_{OUT} can be adjusted from 0.6V to 2.5V. Load current range is 0A to 70A. Note that airflow across the board may be needed for continuous operation at 70A (at elevated ambient temperatures). The f_{SW} and output voltage can also be tuned. However, to ensure sufficient stability margins, switching frequency and output capacitors can only be selected using the "RAA210870 Design Guide Matrix and Output Voltage Response" table in the RAA210870 datasheet. If input voltage is less than 5V, tie the VDRV/VCC test point directly to V_{IN} or to a separate 5V power supply for normal operation and best efficiency.

If external synchronization is used, connect the SYNC test point to the external clock. Note that the external clock signal should be active before the module is enabled.

2.2 Quick Start Guide

2.2.1 Pin-Strap Option

RTKA2108702H00000BU can be configured in Pin-Strap mode with standard 1% 0603 resistors. The PMBus interface is not required to evaluate the RAA210870 in Pin-Strap mode. Output voltage (V_{OUT}), switching frequency (f_{SW}), soft-start/stop delay and ramp times, input Undervoltage Protection (UVLO) threshold, interleave, ASCR gain and residual, and device PMBus address can be changed by populating recommended resistors at placeholders provided on the evaluation board. By default, the evaluation board operates in Pin-Strap mode and regulates at V_{OUT} = 0.93V, f_{SW} = 320kHz, soft-start/stop delay time = 5ms, soft-start/stop ramp time = 5ms, UVLO = 4.2V, ASCR gain = 200, ASCR residual = 90, and PMBus address = 28h. Complete the following steps to evaluate the RAA210870 in Pin-Strap mode.

(1) Set ENABLE switch to "DISABLE".

(2) Connect load to the VOUT lug connectors (J_7-J_{10}).

(3) Connect a power supply to the VIN connectors (J_5 and J_6). Make sure the power supply is not enabled when making connection.

(4) Turn the power supply on.

(5) Set the ENABLE switch to "ENABLE".

(6) Measure 0.93V V_{OUT} at probe point labeled "VOUT REGULATION MONITOR" (J_{11}).

(7) Observe switching frequency of 320kHz at probe points labeled "PHASE1" (TP_{10}) and "PHASE2" (TP_{11}).

(8) To measure the module efficiency, connect the multimeter voltage probes at probe points labeled "VIN" (TP_1), "GND" (TP_2), and "VOUT" (TP_{12}).

(9) To change $V_{OUT,}$ disconnect the board from the setup and populate a 1% standard 0603 resistor at the RVSET_CRS placeholder location on the bottom layer. If additional output voltage fine-tuning is required, populate a resistor at the RVSET_FINE placeholder. Refer to "Output Voltage Selection" in the RAA210870 datasheet to determine the correct selection of resistors for programming the output voltage. By default, VOUT_MAX is set to 110% of V_{OUT} set by the pin-strap resistor.

(10) To change switching frequency, disconnect the board from the setup and populate a 1% standard 0603 resistor at the RFSET placeholder location on the bottom layer. Refer to "Switching Frequency and PLL" in RAA210870 datasheet for recommended resistor values.

(11) To change soft-start/stop delay and ramp time, disconnect the board from the setup and populate a 1% standard 0603 resistor at the R_6 placeholder location on the bottom layer. Refer to "Soft-Start, Stop Delay, and Ramp Times" in the RAA210870 datasheet for the recommended resistor values.

(12) To change UVLO, disconnect board from the setup and populate a 1% standard 0603 resistor at the R_6 placeholder location on the bottom layer. Refer to "Input Undervoltage Lockout (UVLO)" in the RAA210870 datasheet for the recommended resistor values. Notice that the UVLO programming shares the same pin with soft-start/stop programming.

(13) To change ASCR gain and residual, disconnect the board from the setup and populate a 1% standard 0603 resistor at the R_7 placeholder location on the bottom layer. Refer to "Loop Compensation" and the design guide matrix in the RAA210870 datasheet for the recommended resistor values.

2.2.2 PMBus Option

The RTKA2108702H00000BU can be evaluated for all features using the provided ZLUSBEVAL3Z dongle and PowerNavigator software. Follow these steps to evaluate the RAA210870 with PMBus option.

(1) Install PowerNavigator from the website.

(2) Set the ENABLE switch to "DISABLE".

(3) Connect the load to the VOUT lug connectors (J_7-J_{10}).

(4) Connect the power supply to the VIN connectors (J_5 and J_6). Make sure the power supply is not enabled when making connection.

(5) Connect the ZLUSBEVAL3Z dongle (USB to PMBus adapter) to the RTKA2108702H00000BU board using the 6-pin male connector labeled "PMBus DONGLE IN".

(6) Turn the power supply on.

(7) Connect the supplied USB cable from the computer USB to the ZLUSBEVAL3Z dongle.

(8) Launch PowerNavigator.

(9) The RAA210870 device on the board operates in Pin-Strap mode from factory default, but the user can modify the operating parameters using PowerNavigator. The default pin-strap configurations are overwritten if PowerNavigator is used.

(10) Set the ENABLE switch to "ENABLE". Alternatively, the PMBus ON_OFF_CONFIG and OPERATION commands may be used from PowerNavigator to allow PMBus Enable.

(11) Monitor and configure the RTKA2108702H00000BU board using the PMBus commands in PowerNavigator.

(12) PowerNavigator tutorial videos are available on the website.

(13) For evaluating interleave functionality for multiple Renesas digital power products using a single ZLUSBEVAL3Z dongle, the RAA210870 can be daisy chained with other digital power evaluation boards. The PMBus address can be changed by placing a 1% standard 0603 resistor at the R_4 placeholder location on the bottom layer. Refer to the "SMBus Module Address Selection" table in the RAA210870 datasheet for recommended values.

3. Evaluation Board Information

If the input voltage is less than 5.3V, tie the VCC test point directly to the VIN, or for operational efficiency, tie the VCC test point to a separate 5V power supply. For external synchronization, connect the SYNC test point to the external clock.

Note: The external clock signal should be active before the module is enabled.

3.1 External Clock Synchronization

The RAA210870 can synchronize to an external clock. External clock synchronization allows the user to operate multiple converters at the same switching frequency and can lead to improved EMI characteristics. The RTKA2108702H00000BU evaluation board can assess this functionality. A function generator is required. Complete the following steps to operate the RAA210870 with an external clock frequency of 593kHz:

(1) Set the Enable switch to the “DISABLE” position.

(2) Solder a 17.8kΩ resistor at RSET on the CFG pin (R_{14}).

(3) Program the function generator to output a continuous square pulse waveform of 593kHz. Program the pulse width to be at least 150ns.

(4) Ensure that the clock signal is stable by monitoring the waveform on an oscilloscope.

(5) After verifying clock stability, connect the output cables from the function generator to test point TP_3 (labeled “SYNC”).

(6) Turn the output of the function generator ON.

(7) Enable the module by setting the Enable switch to “ENABLE”.

(8) Observe the switching frequency at test points TP_{10} “PHASE1” and TP_{11} “PHASE2”.

(9) The module will synchronize to the 593kHz external clock from the function generator.

(10) Ensure that the module is always disabled before changing the frequency of the external clock.

(11) Loss of Sync fault is generated when the external clock is lost.

3.2 Bode Plots Measurement

Assessing the stability of the converter is an important step in the design process. Bode plots are a useful and reliable tool to identify the loop response of the converter. Phase and gain margins give an insight into the stability of the system, while bandwidth can indicate how quickly the converter responds to disturbances in input voltage or load transients. Correctly measuring the loop response is critical for designing stable converter systems.

A network analyzer is required to perform the frequency response measurements on the RTKA2108702H00000BU evaluation board. Complete the following steps to evaluate the converter loop response for the RAA210870 on the RTKA2108702H00000BU evaluation board.

(1) Break the feedback loop by removing the R_{11} resistor in the remote sense path, connected between VSENP and VOUT.

(2) Solder a 20Ω resistor in its place. The value of the resistor could be in the range of 10Ω to 50Ω.

(3) Solder a twisted wire pair to the 20Ω resistor. Ensure that the wires are short in length. A small twisted pair works well by minimizing noise pickup, which is important for a good measurement.

(4) Enable the converter.

(5) Use a “Network Analyzer” to inject a small AC signal (~20mV) across the 20Ω resistor as shown in Figure 2 on page 7.

(6) Measure the amplitudes of the signals at points A and B as shown in Figure 2.

(7) Sweep the frequency using the “Network Analyzer” to observe the bandwidth, phase, and gain margin.

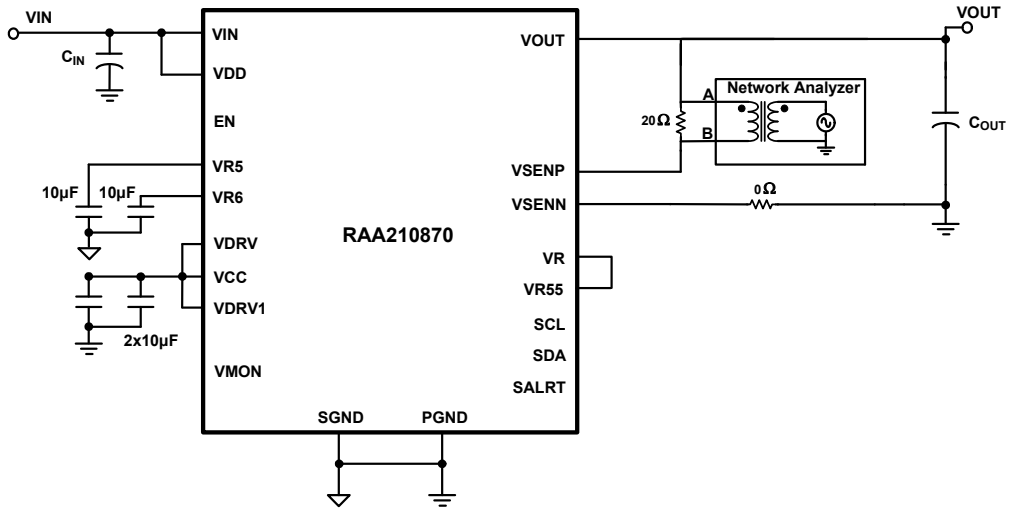

Figure 2. Network Analyzer

Figure 3 shows an example bode plot generated by the network analyzer for the RAA210870 at 12V input, 0.9V output, and 50A load at 615kHz with 10x100µF ceramic + 4x680µF POS output capacitors. ASCR gain and ASCR residual are set as 400 and 90, respectively. The plot shows a crossover frequency of 53kHz with a phase margin of 73°. An 8dB gain margin is observed at 198kHz.

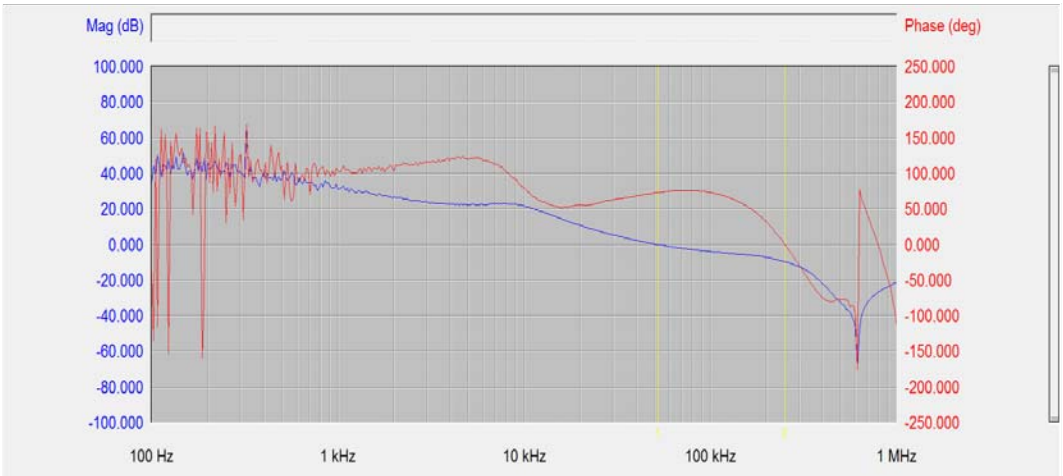

Figure 3. Example Bode Plot

Refer to the "RAA210870 Design Guide Matrix and Output Voltage Response" table in the RAA210870 datasheet for detailed design guidelines including selection of input/output capacitors and different ASCR gain and residual values.

3.3 Interleave Operation

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device, so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, while the power losses proportional to the I^2_{RMS} are reduced dramatically.

To enable phase spreading in a multi-module operation, all converters must be synchronized to the same switching clock. The phase offset of each device may be set to any value between 0° and 360° in 22.5° increments by

choosing the device SMBus address from the "Interleave" table in the RAA210870 datasheet. The lower four bits of the SMBus address set the value of the INTERLEAVE command. Complete the following steps to implement interleave functionality for a two module operation.

(1) Choose SA (SMBus Address) for Module 1 and Module 2 from the "Interleave" table in the RAA210870 datasheet based on the desired phase difference. Populate the corresponding RSET for SA (R_4) according to the "SMBus Address Resistor Selection" table in the RAA210870 datasheet.

(2) For example, when Module 1 has SA = 28h (INTERLEAVE = 8, 180° phase shift from the rising edge of the external clock) and Module 2 has SA = 24h (INTERLEAVE = 4, 90° phase shift from the rising edge of the external clock), the net phase difference between Module 1 and Module 2 will be 180 – 90 = 90°.

(3) Populate RSET on the CFG pin for both boards to sync to an external clock source of a particular switching frequency based on the "External Frequency Sync Settings" table in the RAA210870 datasheet.

(4) Connect the power supply to the VIN connectors (VIN/GND) on both boards.

(5) Connect the ZLUSBEVAL3Z dongle to the 6-pin male connector labeled "PMBus DONGLE In" to one of the boards.

(6) Daisy chain the second board to the first board by connecting "PMBus DONGLE Out" of first board to the "PMBus DONGLE In" of the second board.

(7) Provide an external clock on the SYNC pins of the two boards from a function generator. The external clock frequency from the function generator should be within ±10% of the listed options shown in the "External Frequency Sync Settings" table in the RAA210870 datasheet. The incoming clock signal must be stable before the enable pin is asserted. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns.

(8) Turn the input power supply on. Next, set the ENABLE switch to the "ENABLE" position.

(9) Monitor the switch node at the probe point labeled PHASE1 (TP_{10}) on the two boards using an oscilloscope to verify the phase spread set. This functionality can also be verified using the INTERLEAVE command in PowerNavigator.

Note: Every module gets assigned a unique Rail ID based on the SA setting. This can be observed in the Power Map window of PowerNavigator.

3.4 V_{OUT} Transient Response Check

The RTKA2108702H00000BU board has a built-in transient load test circuit (see the schematic in Figure 4). A 100A N-channel MOSFET (Manufacturer PN: BSC010NE2LSI) is connected across VOUT and PGND next to the remote voltage sensing location (CVSEN). The 10mΩ current-sense resistor R_{54} is used for monitoring the drain-to-source current of the MOSFET. For a transient load test, inject the gate drive pulse signal at J_{16}. The load current can be monitored through J_{15}. When the gate turn-on signal is applied, the MOSFET operates in the saturation region (not the linear region). To avoid MOSFET overheating, both the pulse width and duty cycle of the gate signal must be reduced (recommended duty cycle should be less than 2%). The amplitude of the gate driver pulse voltage can be adjusted to obtain a desired transient load current step size.

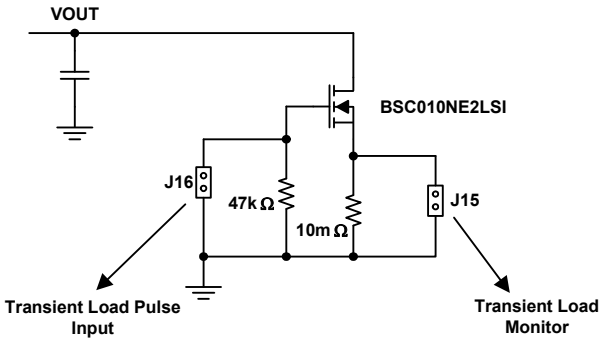

Figure 4. Schematic for Transient Load Measurement

4. PCB Layout Guidelines

The RTKA2108702H00000BU board layout is optimized for electrical performance, low loss, and good thermal performance.

The key features of the RTKA2108702H00000BU layout are:

- Large PGND planes and a separate SGND plane. The SGND plane is connected to PGND on the second layer with a single point connection. Multiple vias are used for small pins such as J16, H16, K16, M5, M14, M17, and N5 to connect to inner SGND or PGND layer.
- Ceramic capacitors between VIN and PGND, VOUT and PGND, and bypass capacitors between VDD, VDRV and the ground plane are placed close to the module to minimize high frequency noise. Some output ceramic capacitors are placed close to the VOUT pads in the direction of the load current path to create a low impedance path for the high frequency inductor ripple current.
- Large copper areas are used for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Multiple vias are used to connect the power planes in different layers.
- Remote sensing traces are connected from the regulation point to VSENP and VSENN pins. The two traces are placed in parallel, to achieve tight output voltage regulation. The regulation point is on the right side of the board in between the VOUT power lugs and the PGND power lugs.
- Multiple vias are used to connect PAD14 and 16 (SW1 and SW2) to inner layers for better thermal performance. The inner layer SW1 and SW2 traces are limited in area and are surrounded by PGND planes to avoid noise coupling. Caution was taken that no sensitive traces, such as the remote sensing traces, were placed close to these noisy planes.
- SWD1 (L3) and SWD2 (P11) pins are connected to SW1 and SW2 pads respectively with short loop wires of 40mil width. The wire width should be at least 20mils.

4.1 Thermal Considerations and Current Derating

Board layout is critical for safe module operation and maximum allowable power delivery. To work in the high temperature environments and carry large currents, the board layout needs to be carefully designed to maximize thermal performance. To achieve this, select enough trace width, copper weight, and the proper connectors.

The RTKA2108702H00000BU evaluation board is designed for running 70A at room temperature without additional cooling systems needed. However, if the output voltage is increased or the board is operated at elevated temperatures, then the available current is derated. Refer to the derated current curves in the RAA210870 datasheet to determine the maximum output current the evaluation board can supply. θ_{JA} is measured by inserting a thermocouple inside the module to measure peak junction temperature.

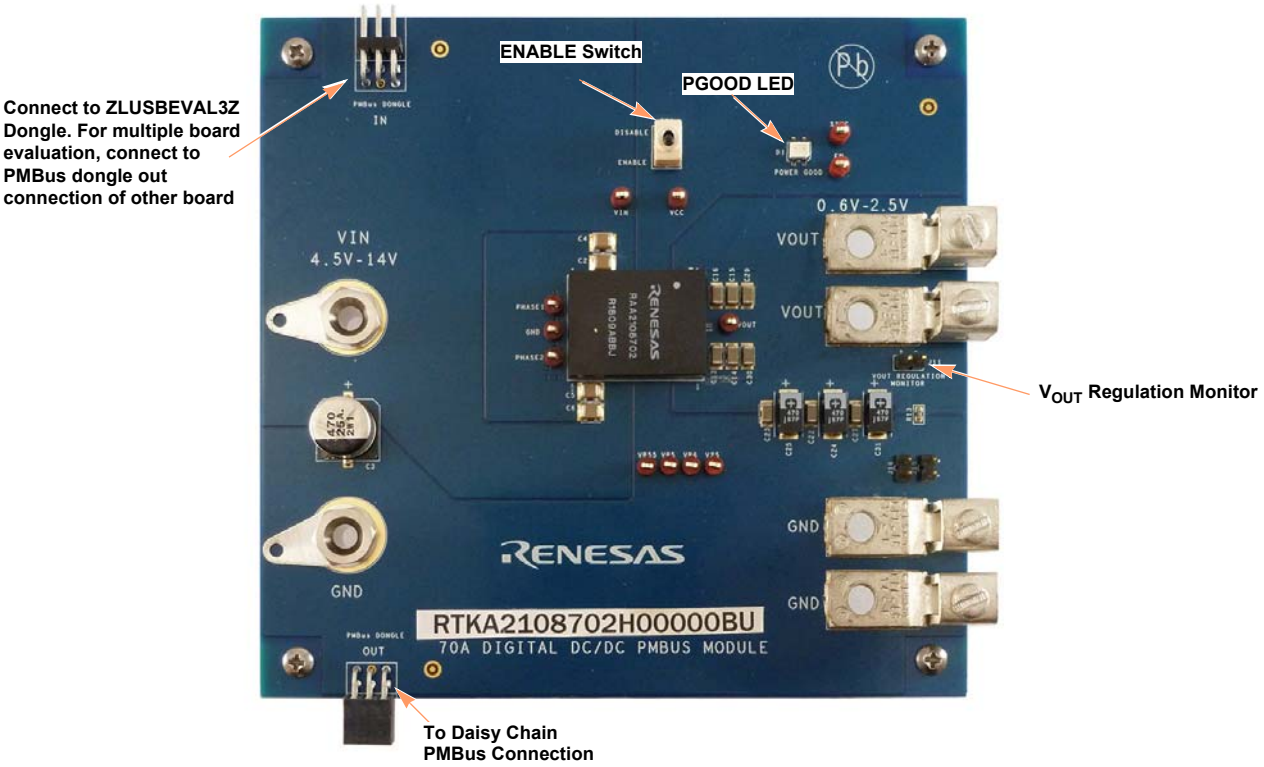

Figure 5. RTKA2108702H00000BU Evaluation Board (Top Side)

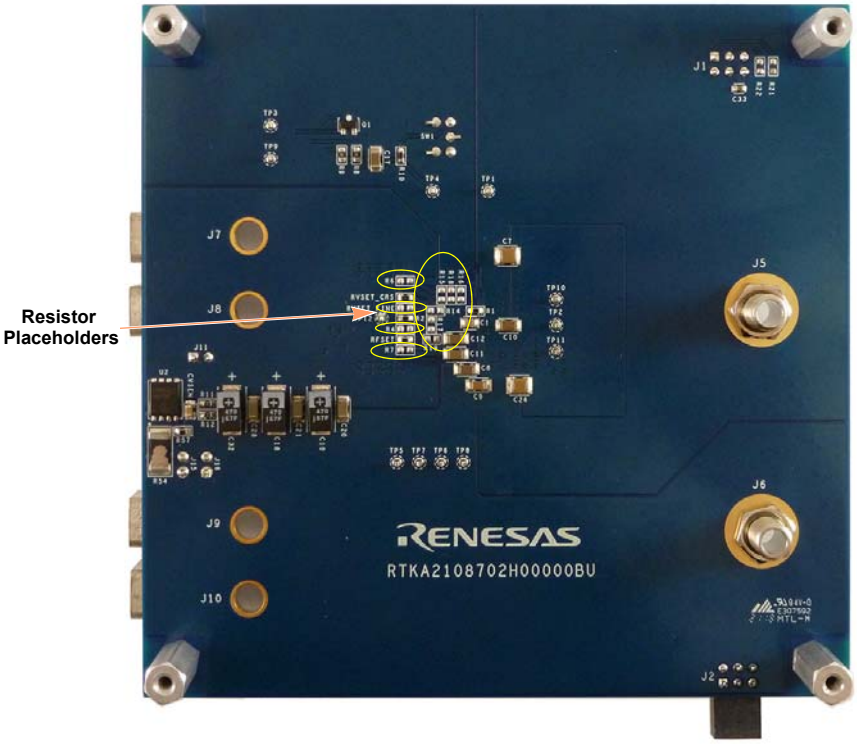

Figure 6. RTKA2108702H00000BU Evaluation Board (Bottom Side)

4.2 RTKA2108702H00000BU Schematic

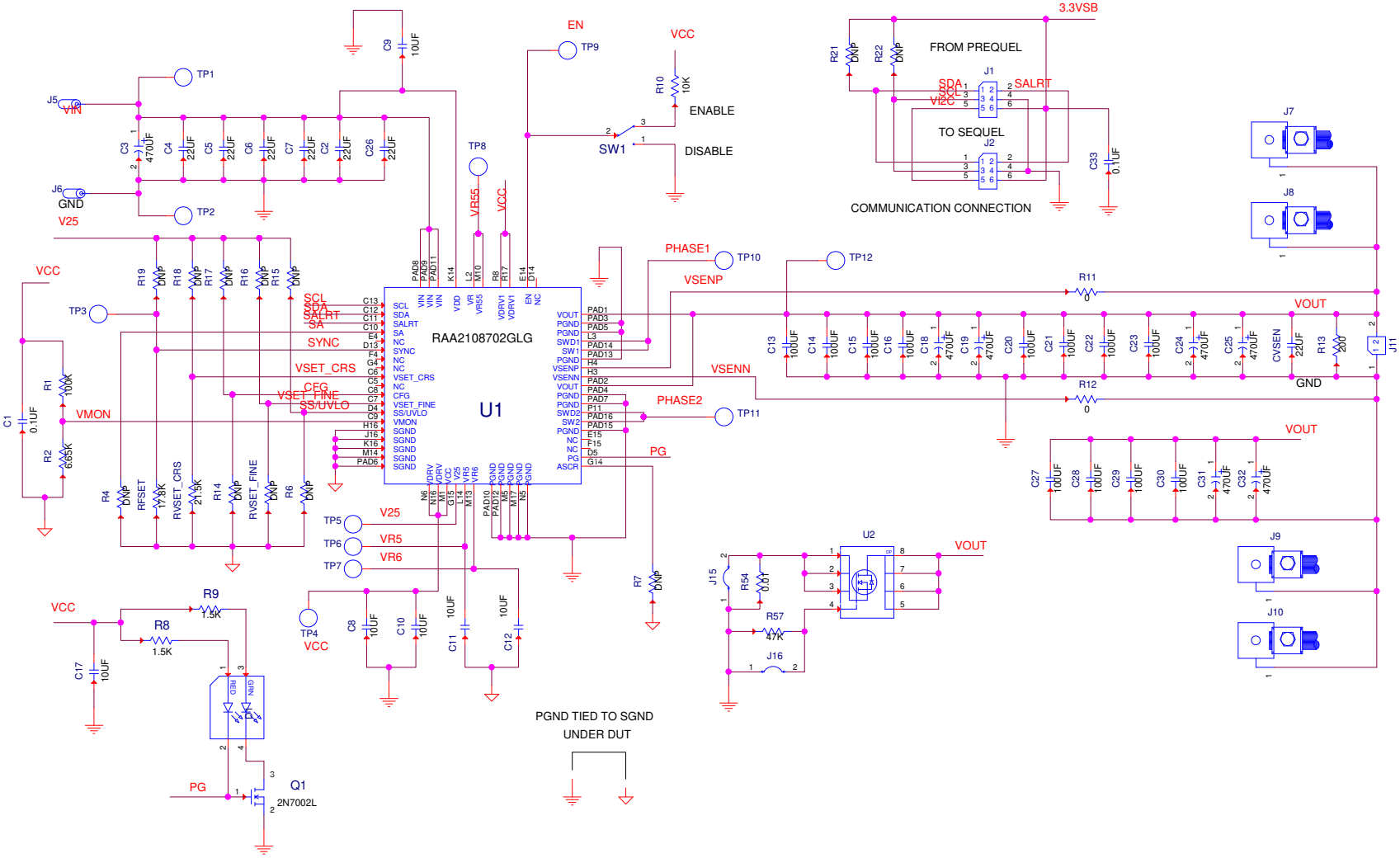

Figure 7. Schematic

4.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PCB, RTKA2108702H00000BU, REVB, RoHS	Multilayer PCB (Hi Tech Circuit)	RTKA2108702H00000BURBPCB
6	C18, C19, C24, C25, C31, C32	CAP TANT POLY 470µF, 6.3V, 20%, 10mΩ, 2917, RoHS	Panasonic	6TPF470MAH
1	CVSEN	CAP CER 22µF, 6.3V, 20%, X5R, 0805, RoHS	TDK	C2012X5R0J226M
1	C3	CAP ALUM 470µF, 25V, 20%, SMD, RoHS	Panasonic	EEE1EA471P
1	C33	CAP CER 0.1µF, 25V, 10%, X7R, 0603, RoHS	Kemet	C0603X104K3RACTU
12	C13-C16, C20-C23, C27-C30	CAP CER 100µF, 6.3V, 20%, X5R, 1206, RoHS	Murata	GRM31CR60J107ME39L
5	C8, C10-C12, C17	CAP CER 10µF, 10V, 10%, X7R, 1206, RoHS	Murata	GRM31CR71A106KA01L
6	C2, C4-C7, C26	CAP CER 22µF, 16V, 10%, X7R, 1210, RoHS	Murata	GRM32ER71C226KE18L
1	C1	CAP CER 0.1µF, 25V, 10%, X7R, 0805, RoHS	Kemet	C0805X104K3RACTU
1	C9	CAP CER 10µF, 25V, 10%, X7R, 1206, RoHS	Kemet	C1206X106K3RAC7800
1	R54	RES 0.01Ω, 1%, 2W, 2512, RoHS	Vishay	WSL2512R0100FEA
12	R4, R6, R7, R14-R19, R21, R22, RVSET_FINE	DO NOT POPULATE_PLACE HOLDER	N/A	N/A
2	R11, R12	RES SMD 0Ω JUMPER, 1/10W, 0603, RoHS	Panasonic	ERJ-3GEY0R00V
1	R10	RES SMD 10kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1002V
1	R1	RES SMD 100kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1003V
2	R8, R9	RES SMD 1.5kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1501V
1	RFSET	RES SMD 17.8kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1782V
1	R13	RES SMD 200Ω, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF2000V
1	RVSET_CRS	RES SMD 21.5kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF2152V
1	R57	RES SMD 47kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF4702V
1	R2	RES SMD 6.65kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF6651V
1	U1	70A Digital DC/DC PMBus Power Module, RoHS	Renesas	RAA2108702GLG
1	U2	MOSFET N-CH 25V, 39A, TDSON-8, RoHS	Infineon	BSC010NE2LS
1	D1	LED GREEN/RED CLEAR AXIAL SMD, RoHS	Lumex Opto	SSL-LXA3025IGC
1	Q1	MOSFET N-CH 60V, 0.115A, SOT-23, RoHS	ON Semiconductor	2N7002L
1	SW1	SWITCH TOGGLE SPDT, 0.4VA, 20V, RoHS	C&K	GT13MCBE
12	TP1-TP12	TEST POINT PC COMPACT 0.063"D RED, RoHS	Keystone Electronics	5005
1	J2	CONN-SOCKET STRIP, TH, 2x3, 2.54mm, TIN, R/A, RoHS	Samtec	SSQ-103-02-T-D-RA
1	J1	CONN-HEADER, 2x3, BRKAWY, 2.54mm, TIN, R/A, RoHS	Samtec	TSW-103-08-T-D-RA
3	J11, J15, J16	CONN HEADER 2POS 0.100" SNGL, RoHS	Samtec	TSW-102-07-F-S
4	J7-J10	HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, RoHS	Burndy	KPA8CTP
2	J5, J6	CONN JACK BANANA UNINS PANEL MOUNT, RoHS	Cinch Connectivity Solutions Johnson	108-0740-001

4.4 Board Layout

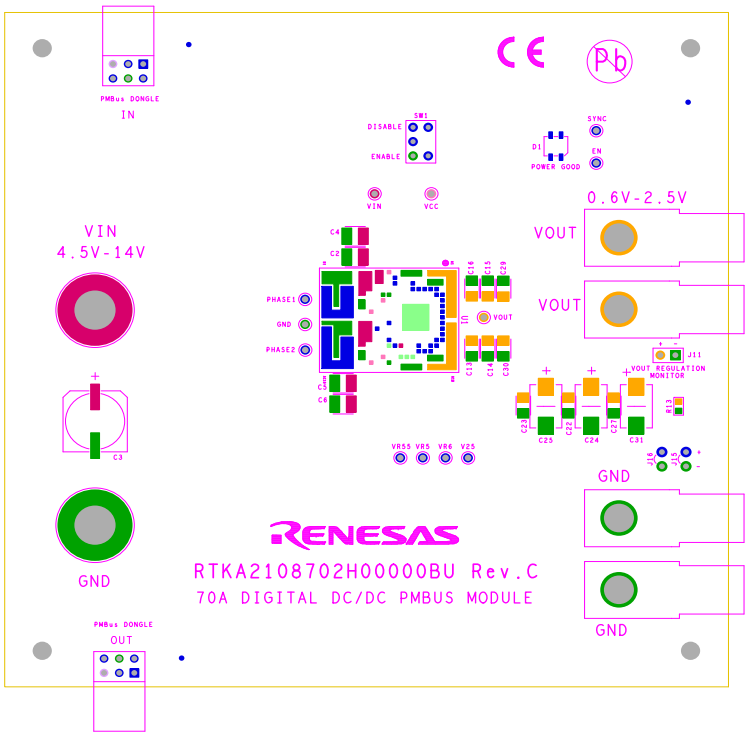

Figure 8. Silkscreen Top

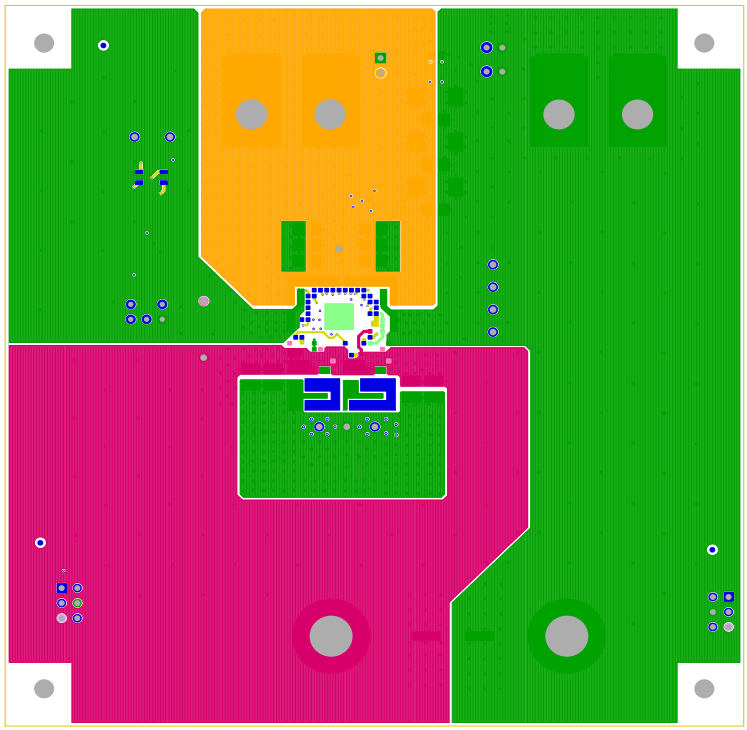

Figure 9. Top Layer Component Side

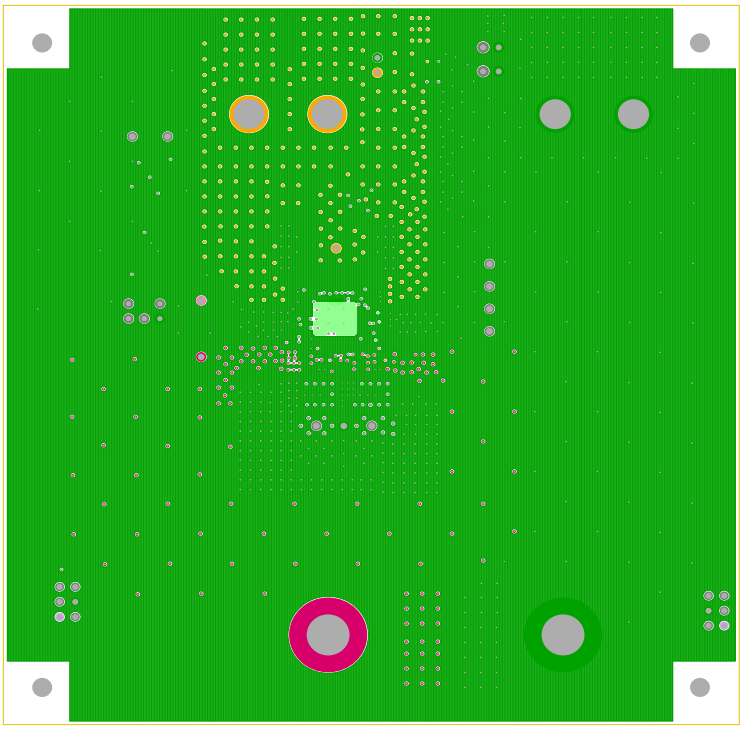

Figure 10. Layer 2

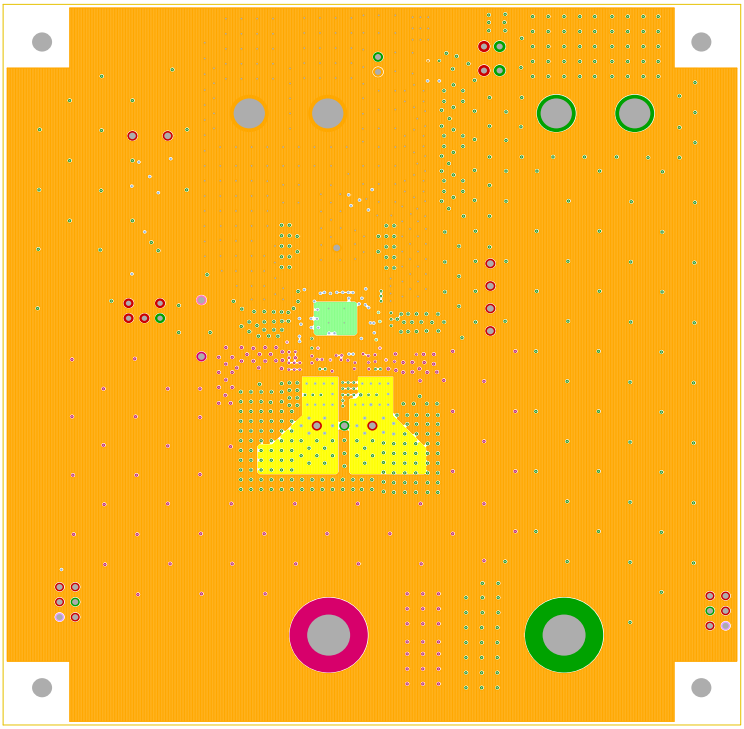

Figure 11. Layer 3

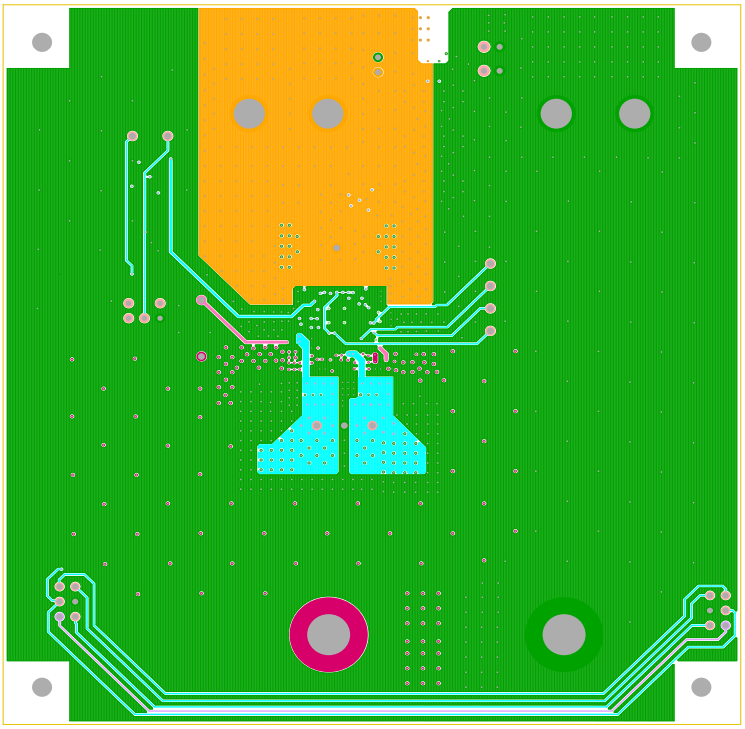

Figure 12. Layer 4

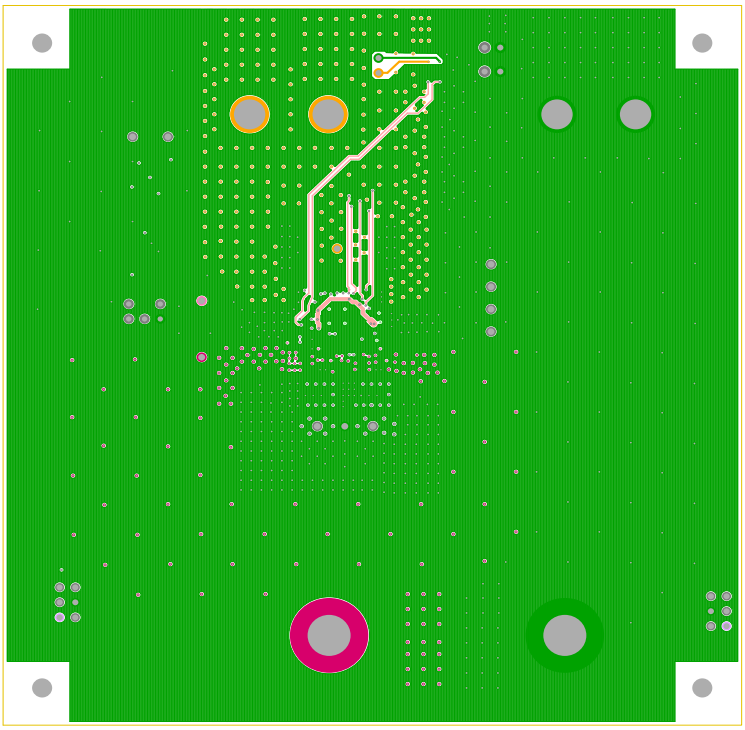

Figure 13. Layer 5

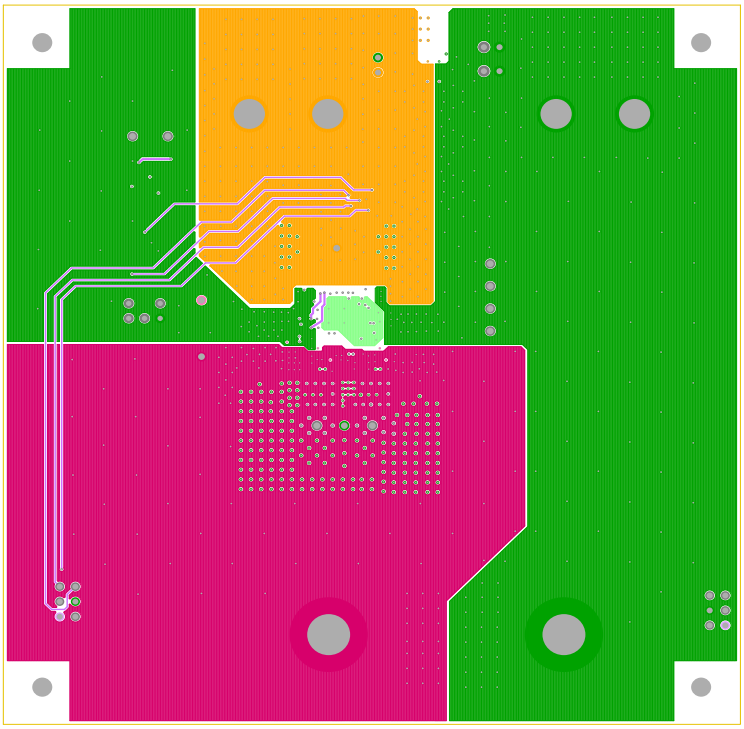

Figure 14. Layer 6

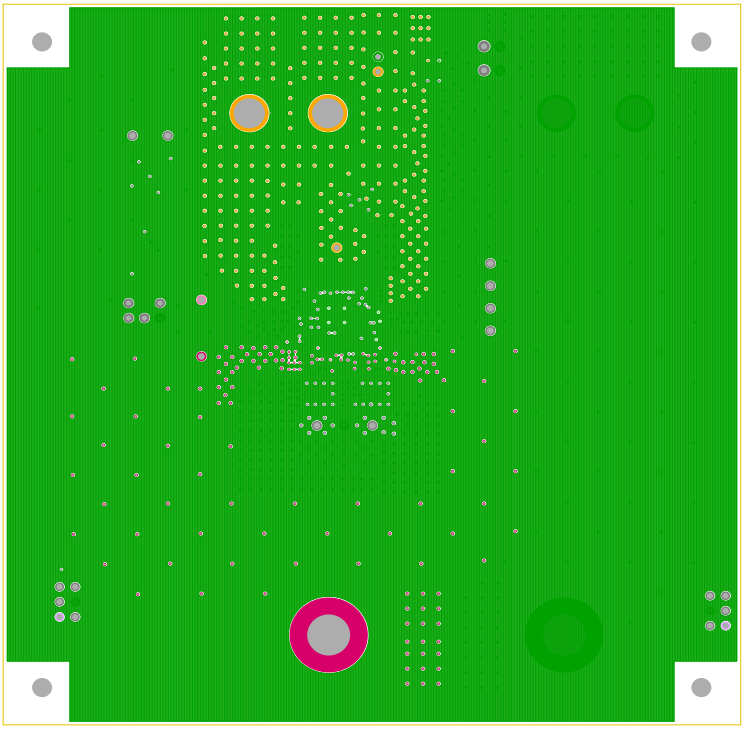

Figure 15. Layer 7

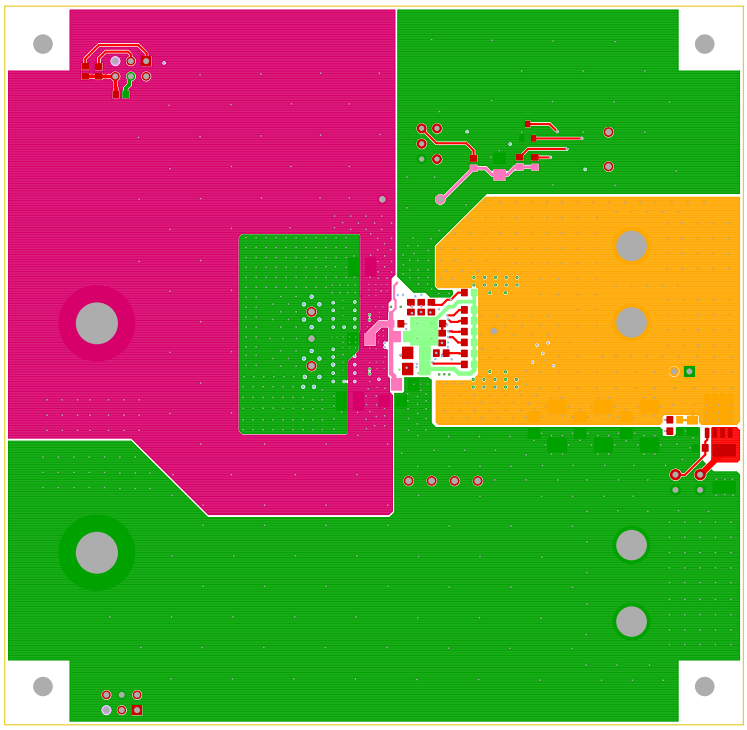

Figure 16. Bottom Layer Solder Side

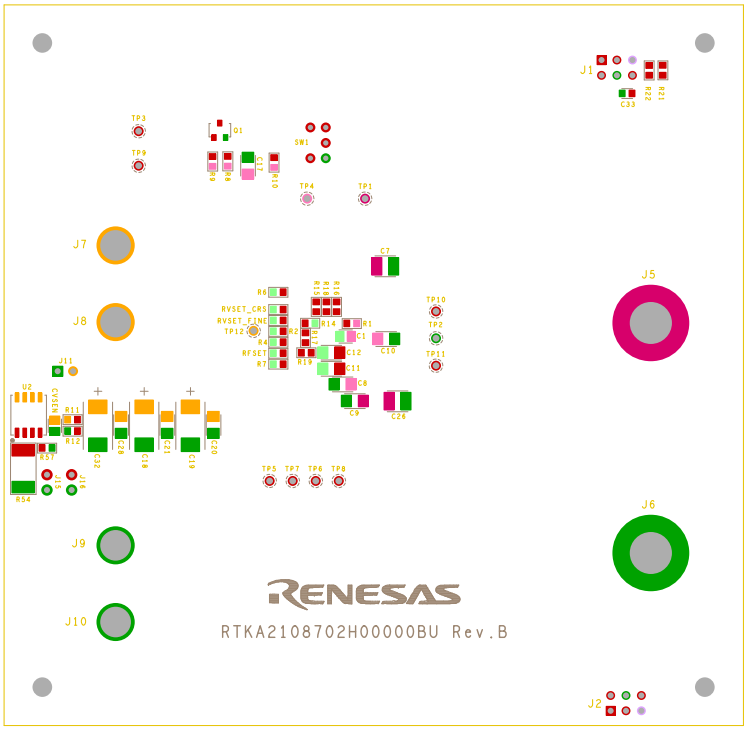

Figure 17. Silkscreen Bottom

5. Typical Performance Data

The following data was acquired using a RTKA2108702H00000BU evaluation board.

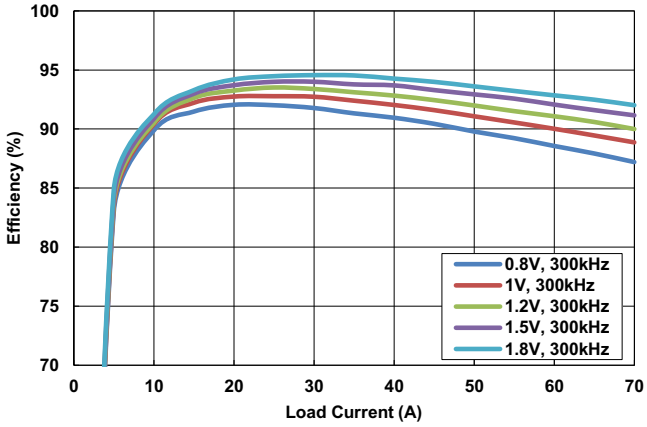

Figure 18. Efficiency vs Output Current at V_{IN} = 5V, f_{SW} = 300kHz for Various Output Voltages

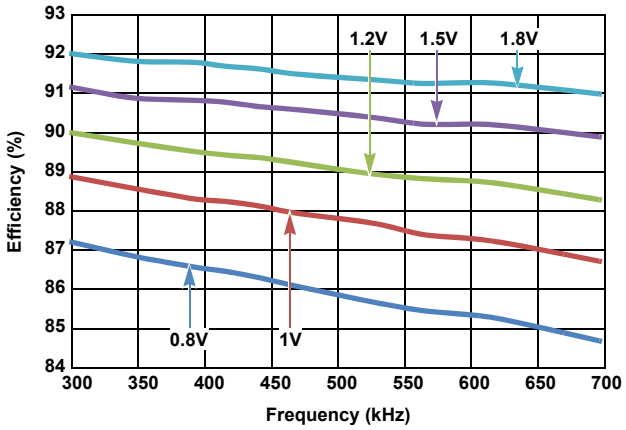

Figure 19. Efficiency vs Switching Frequency at V_{IN} = 5V, I_{OUT} = 70A for Various Output Voltages

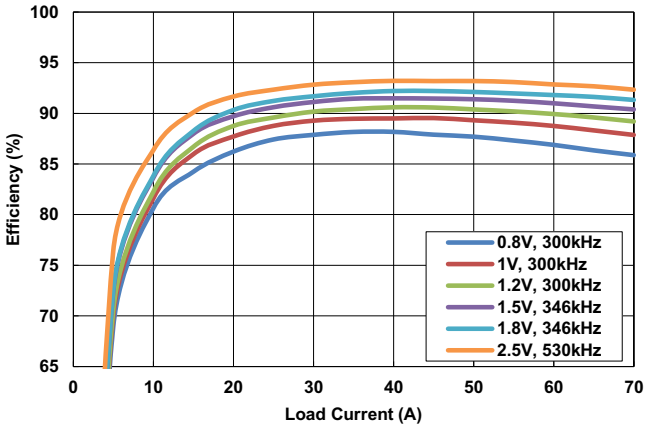

Figure 20. Efficiency vs Output Current at V_{IN} = 12V, for Various Output Voltages

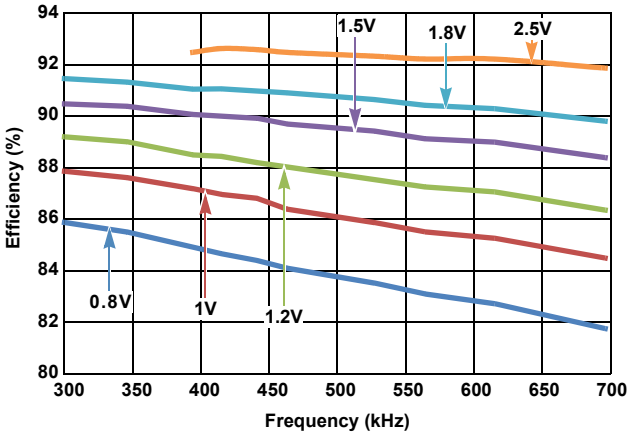

Figure 21. Efficiency vs Switching Frequency at V_{IN} = 12V, I_{OUT} = 70A for Various Output Voltages

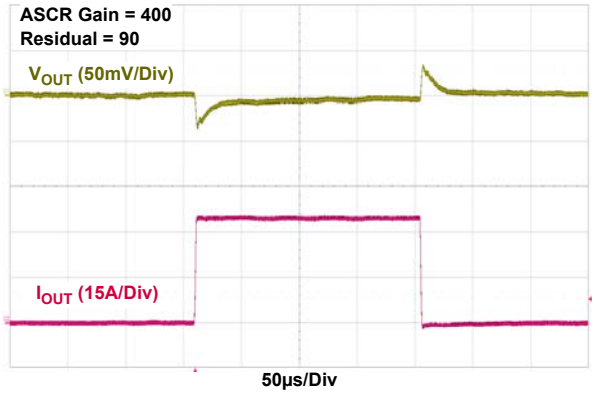

Figure 22. $5V_{IN}$ to $0.9V_{OUT}$ Transient Response, f_{SW} = 615kHz, C_{OUT} = 10x100µF Ceramic + 4x680µF POSCAP

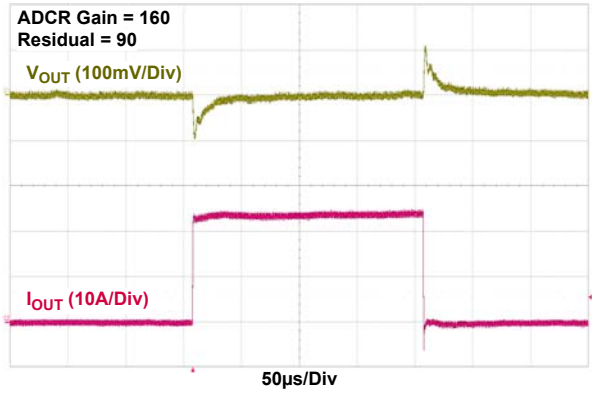

Figure 23. $12V_{IN}$ to $2.5V_{OUT}$ Transient Response, f_{SW} = 533kHz, C_{OUT} = 6x100µF Ceramic + 2x470µF POSCAP

The following data was acquired using a RTKA2108702H00000BU evaluation board. **(Continued)**

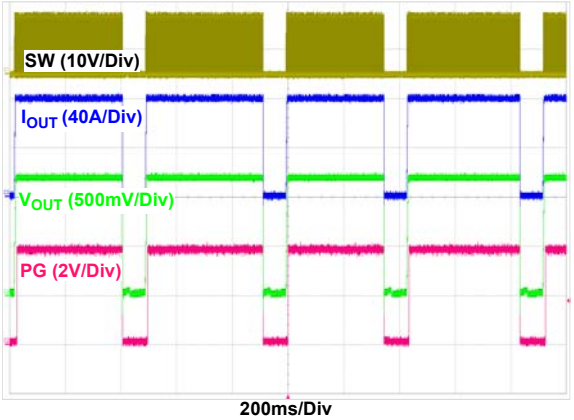

Figure 24. OCP 70ms Retry at V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 80A, f_{SW} = 421kHz, 80A Programmed OCP Fault Limit

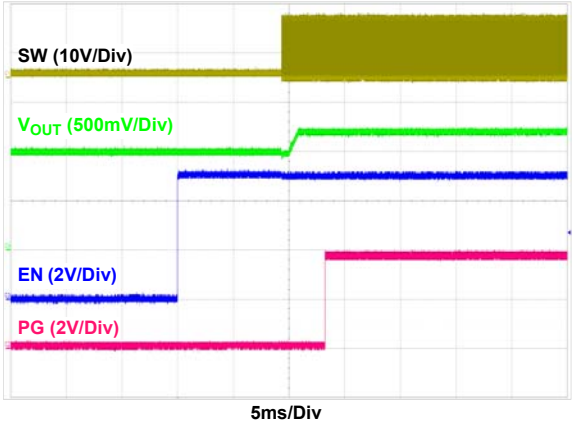

Figure 25. V_{IN} = 12V, V_{OUT} = 1.2V, No load, Prebias Voltage = 1V

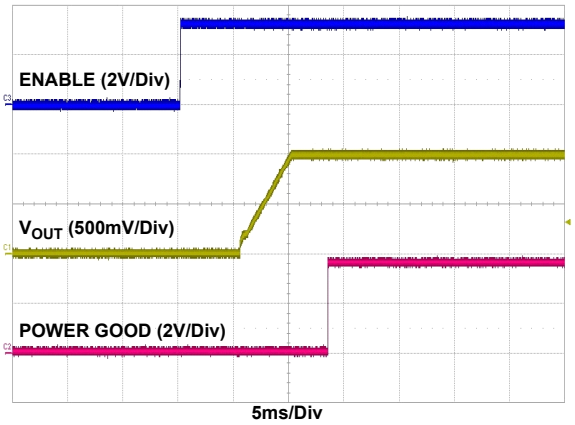

Figure 26. Soft-Start at V_{IN} = 12V, V_{OUT} = 1V, TON_DELAY = 5ms, TON_RISE = 5ms, POWER_GOOD_DELAY = 3ms

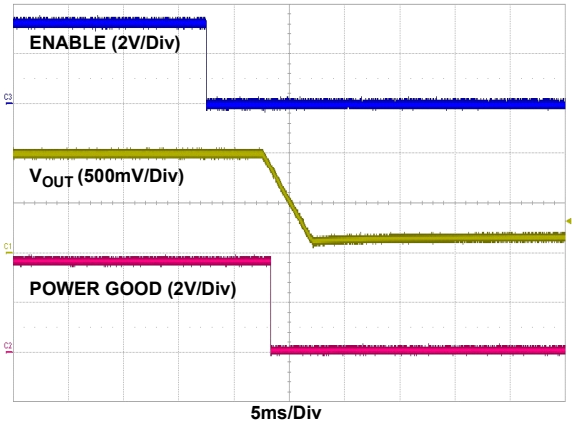

Figure 27. Soft-Stop at V_{IN} = 12V, V_{OUT} = 1V, TOFF_DELAY = 5ms, TOFF_FALL = 5ms

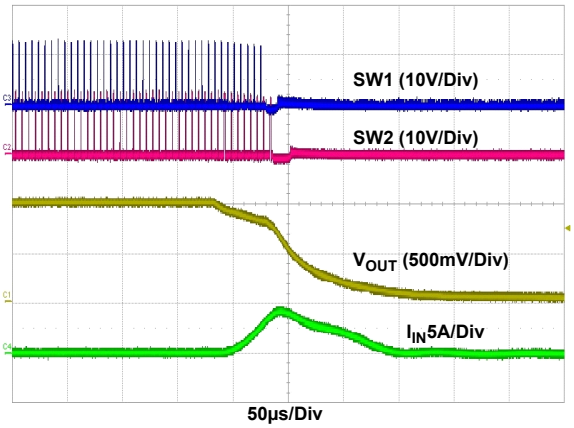

Figure 28. Output Short-Circuit Protection at V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 421kHz

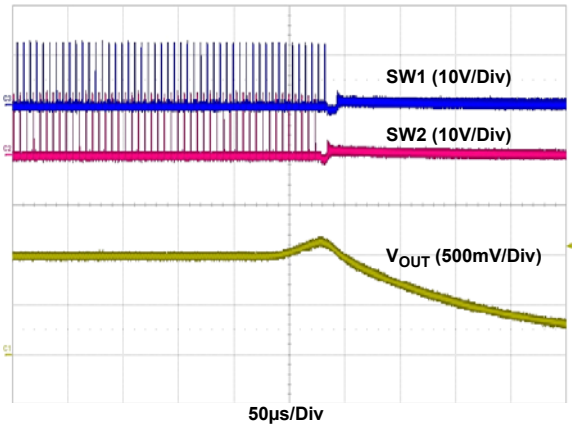

Figure 29. Output Overvoltage Protection at V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 421kHz, VOUT_OV_FAULT_LIMIT = 1.15V

6. Revision History

Rev.	Date	Description
0.00	Sep 13, 2018	Initial release

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