

# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## OptiMOS™

OptiMOS™ Power-Transistor, 60 V  
IPP029N06N

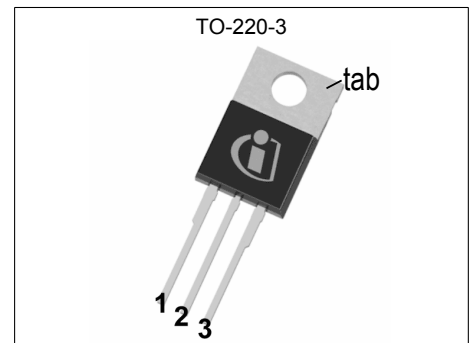
## Data Sheet

Rev. 2.6  
Final

## 1 Description

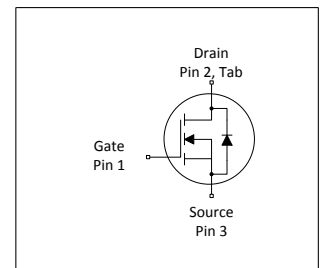
### Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	2.9	mΩ
$I_D$	100	A
$Q_{OSS}$	65	nC
$Q_G(0V..10V)$	56	nC



Type / Ordering Code	Package	Marking	Related Links
IPP029N06N	PG-TO220-3	029N06N	-

<sup>1)</sup> J-STD20 and JESD22

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## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	100	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ , $R_{thJA}=50\text{K/W}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	110	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	136 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	0.7	1.1	K/W	-
Device on PCB, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	40	K/W	-
Soldering temperature, wave and reflow soldering are allowed	$T_{sold}$	-	-	260	°C	Reflow MSL1

<sup>1)</sup> See figure 3 for more detailed information

<sup>2)</sup> See figure 13 for more detailed information

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

## 4 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}, I_D=75\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.5 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ $V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.7 3.3	2.9 4.4	m $\Omega$	$V_{GS}=10\text{ V}, I_D=100\text{ A}$ $V_{GS}=6\text{ V}, I_D=25\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	0.65	1.3	1.95	$\Omega$	-
Transconductance	$g_{fs}$	80	160	-	S	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=100\text{ A}$

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	4100	5125	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	980	1225	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	39	78	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A}, R_{G,ext,ext}=3\text{ }\Omega$
Rise time	$t_r$	-	15	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A}, R_{G,ext,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	30	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A}, R_{G,ext,ext}=3\text{ }\Omega$
Fall time	$t_f$	-	8	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A}, R_{G,ext,ext}=3\text{ }\Omega$

<sup>1)</sup> Defined by design. Not subject to production test

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	20	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0$ to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	11	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0$ to 10 V
Gate to drain charge <sup>2)</sup>	$Q_{gd}$	-	11	15	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0$ to 10 V
Switching charge	$Q_{sw}$	-	19	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0$ to 10 V
Gate charge total <sup>2)</sup>	$Q_g$	-	56	66	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0$ to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0$ to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	49	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0$ to 10 V
Output charge <sup>2)</sup>	$Q_{oss}$	-	65	82	nC	$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	120	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	480	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	1.0	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=100\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery time <sup>2)</sup>	$t_{rr}$	-	54	86	ns	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	77	-	nC	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> See "Gate charge waveforms" for parameter definition

<sup>2)</sup> Defined by design. Not subject to production test

## 5 Electrical characteristics diagrams

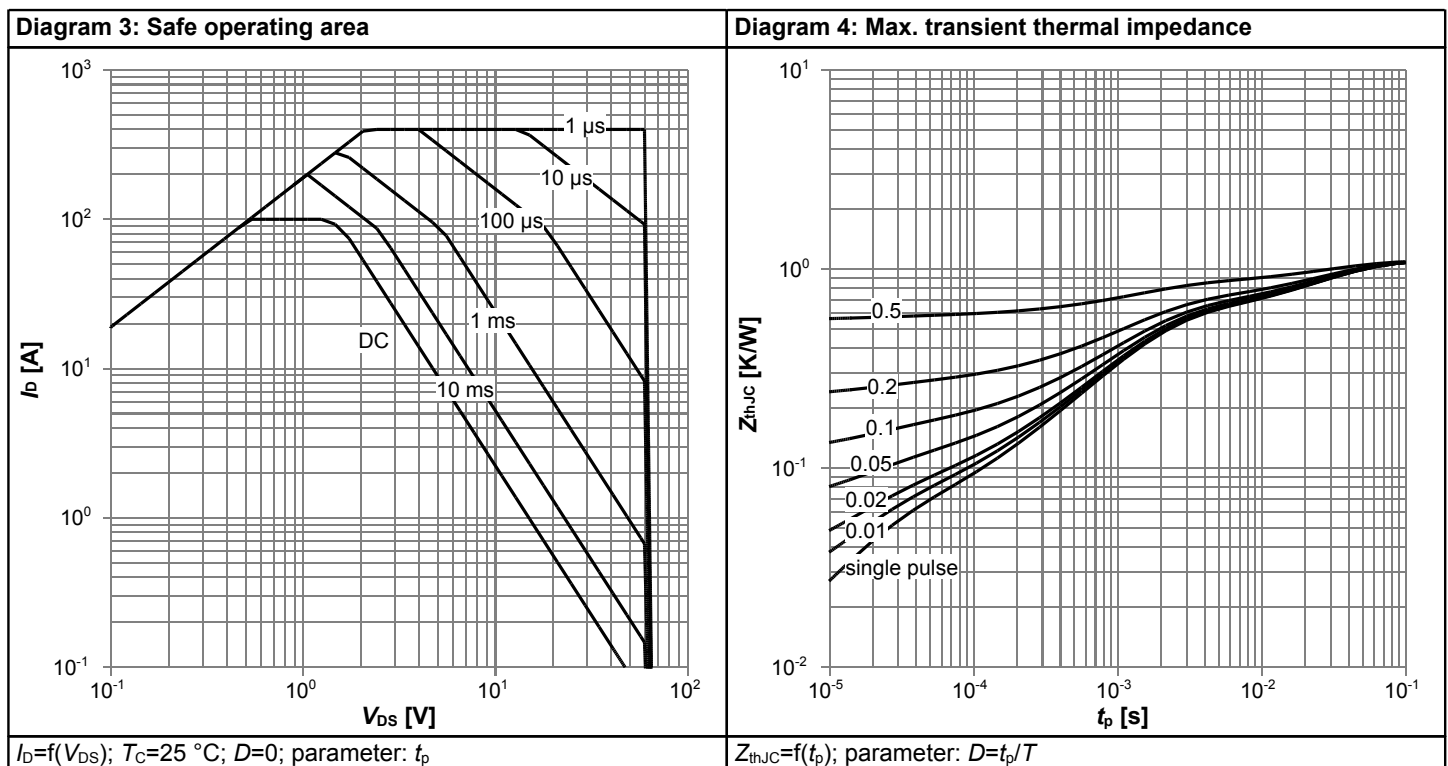
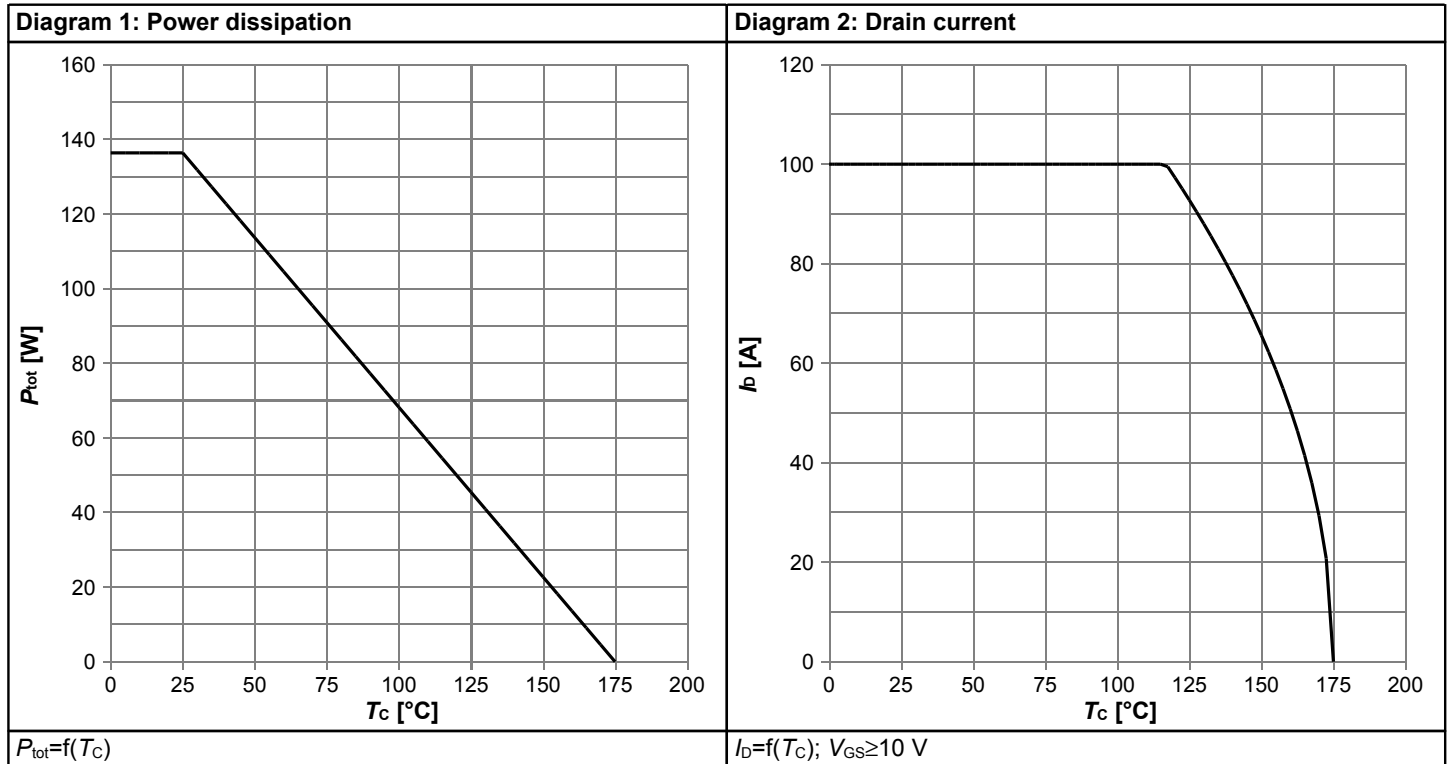
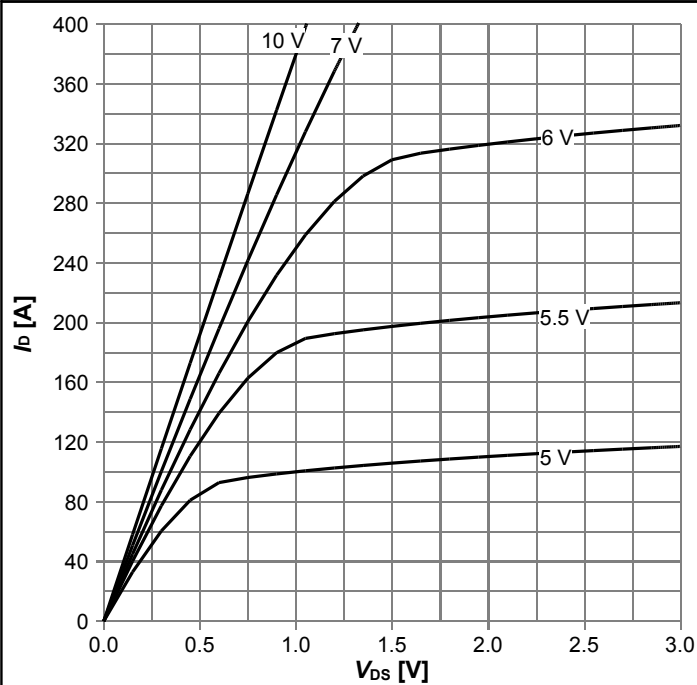
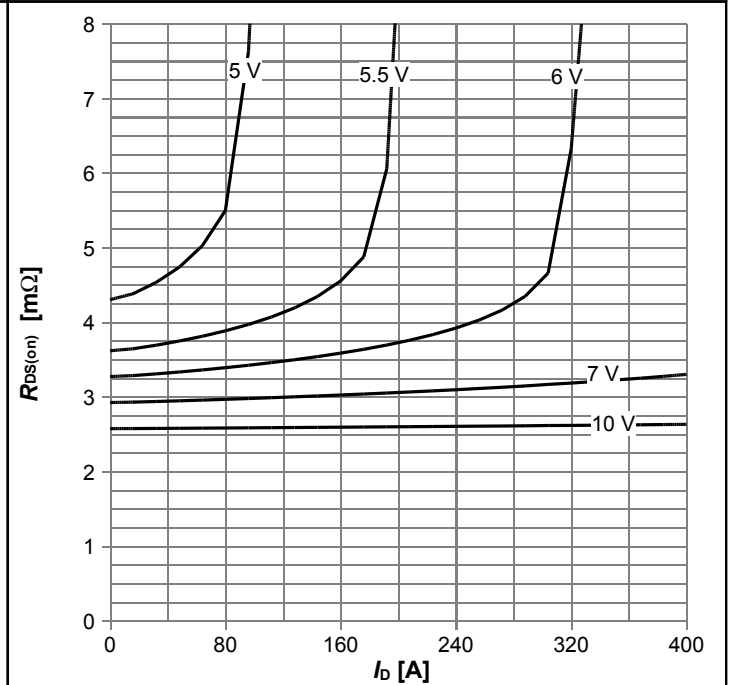


Diagram 5: Typ. output characteristics



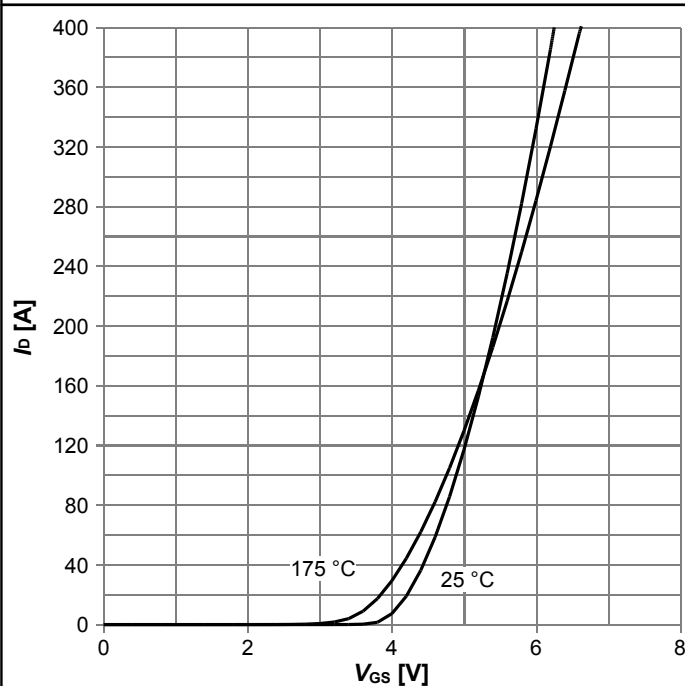
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



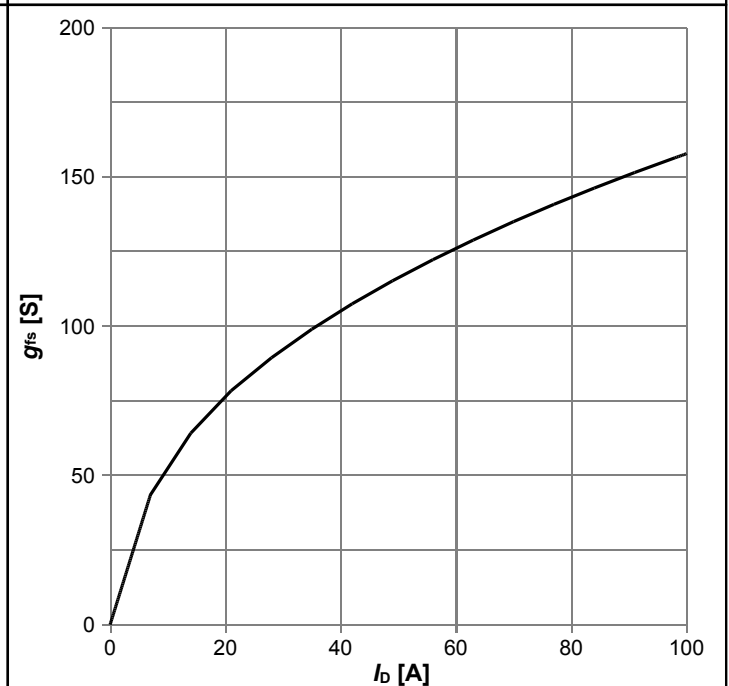
$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max};$  parameter:  $T_j$

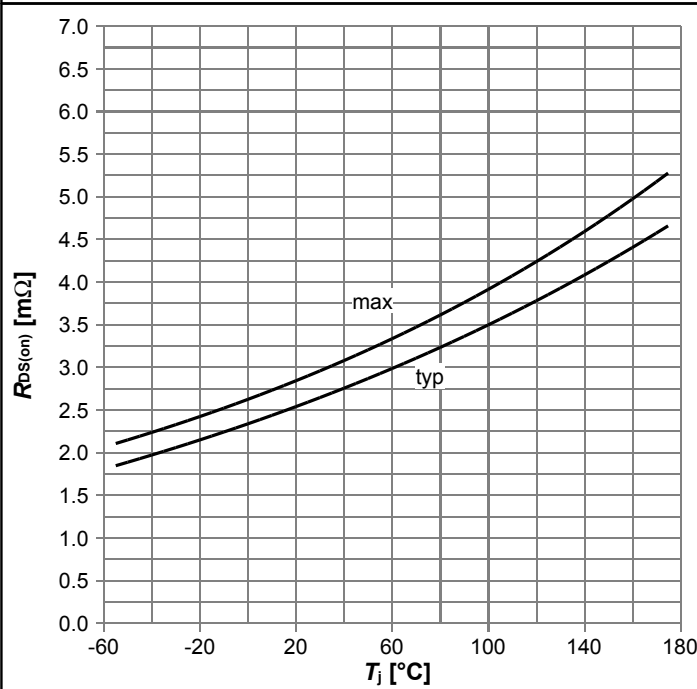
Diagram 8: Typ. forward transconductance



$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$

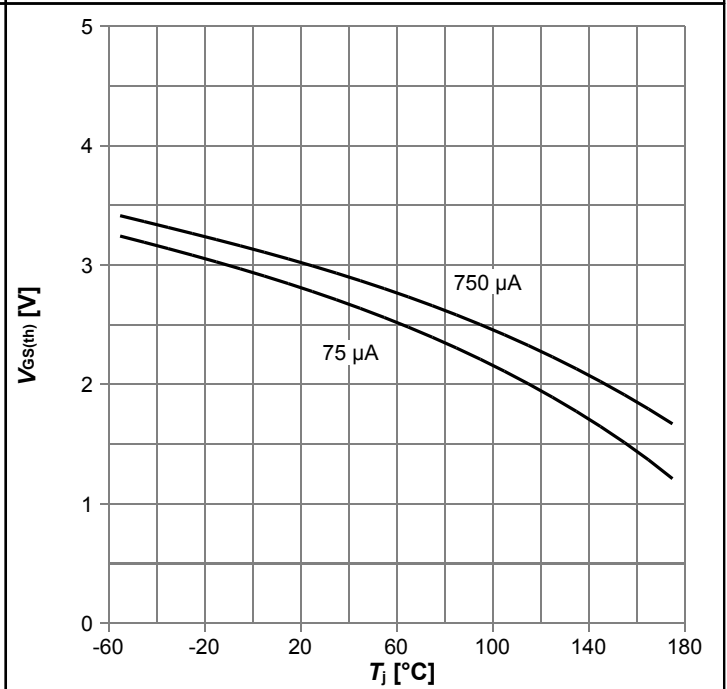


Diagram 9: Drain-source on-state resistance



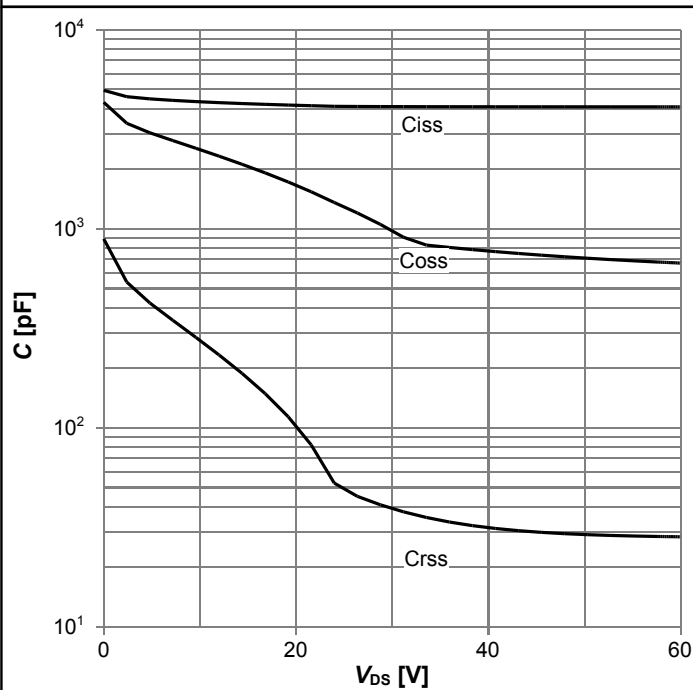
$R_{DS(on)}=f(T_j); I_D=100\text{ A}; V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



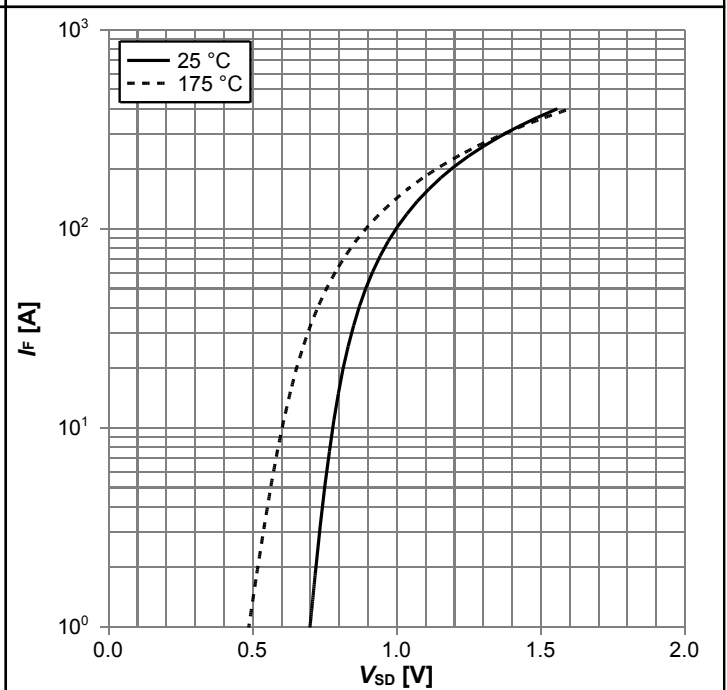
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



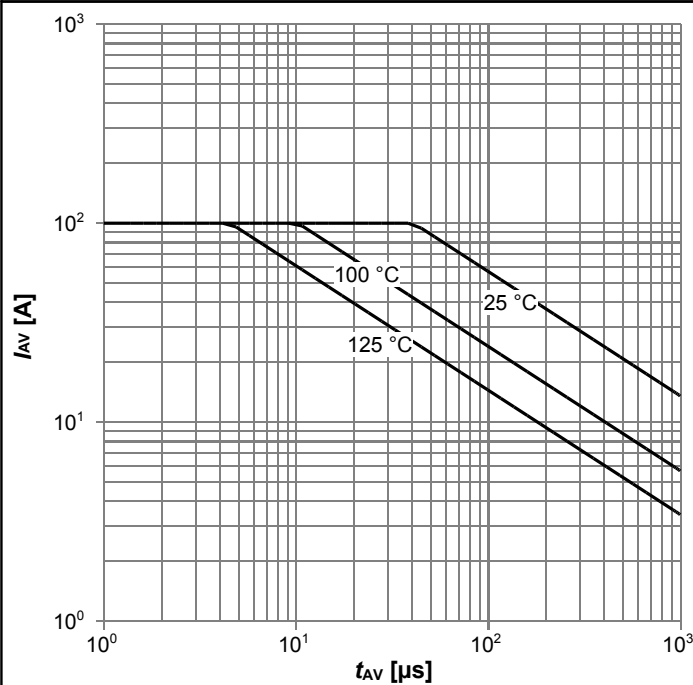
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



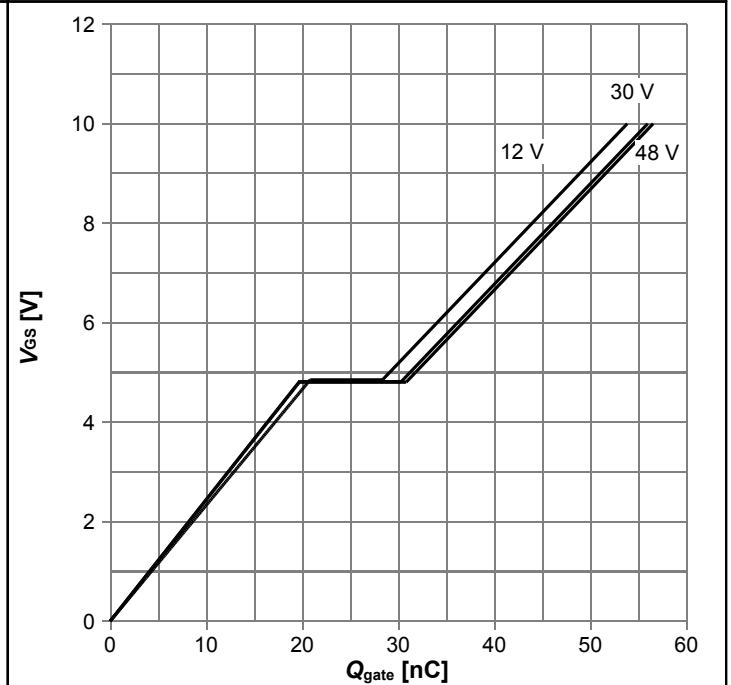
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



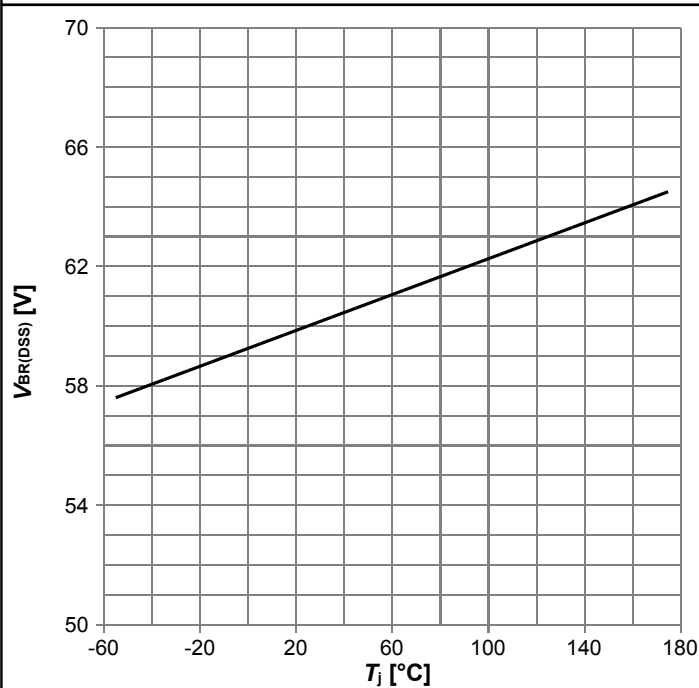
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



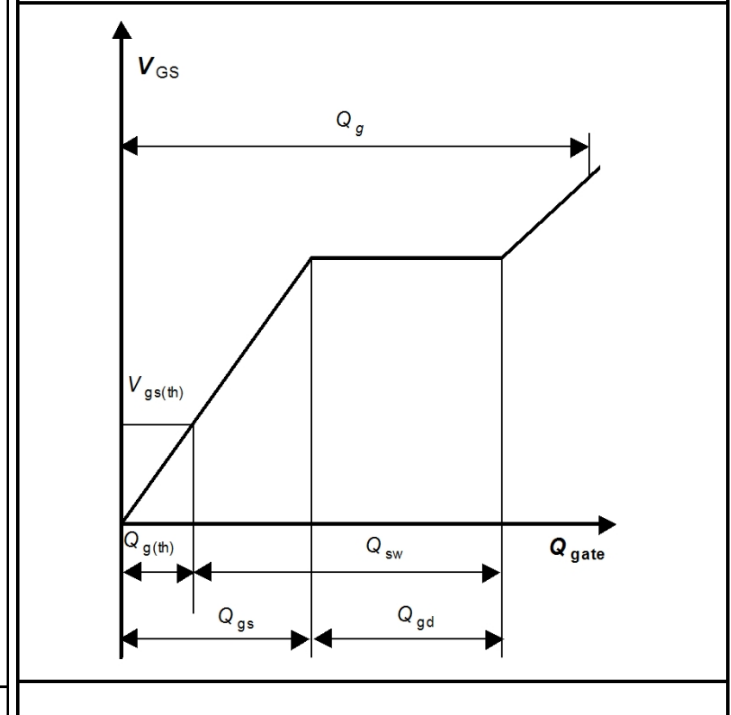
$V_{GS}=f(Q_{gate}); I_D=100 \text{ A pulsed}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

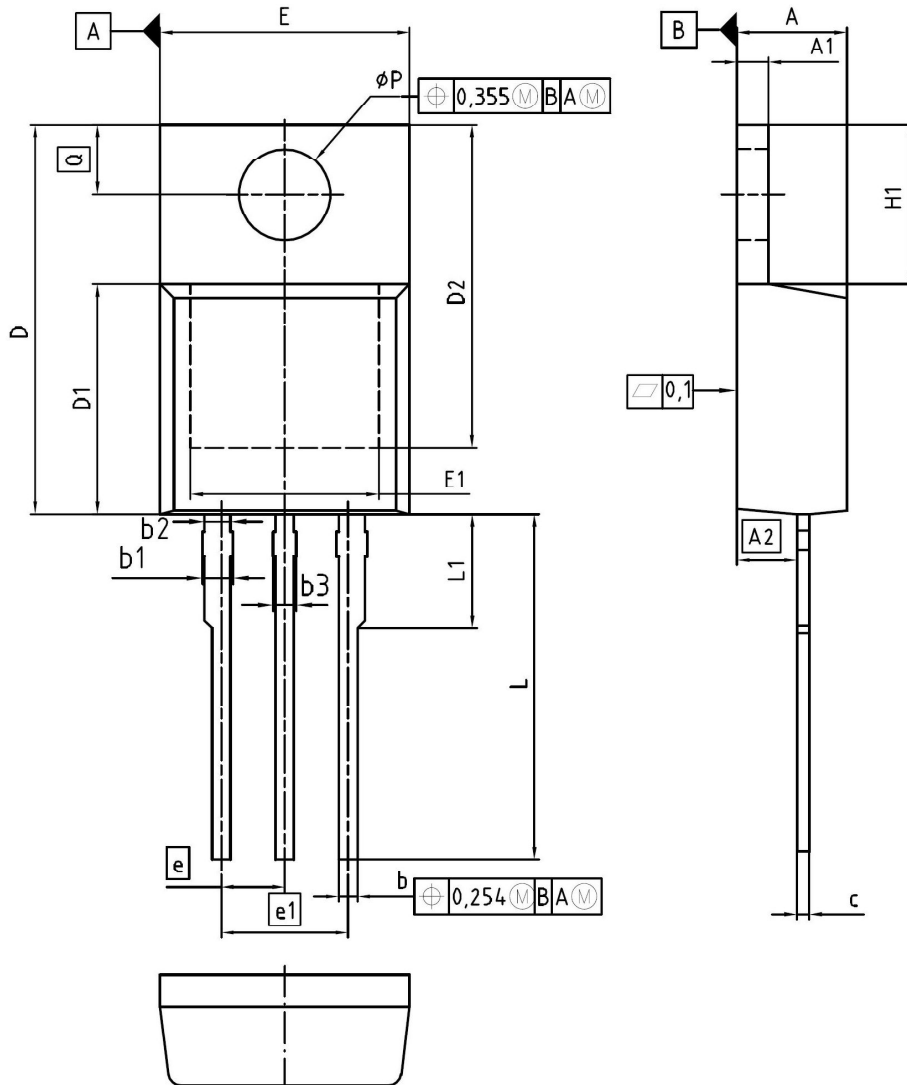


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
φP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.  
Z8B00003318

SCALE

EUROPEAN PROJECTION

ISSUE DATE  
30-07-2009

REVISION  
06

Figure 1 Outline PG-TO220-3, dimensions in mm/inches

## Revision History

IPP029N06N

**Revision: 2015-02-10, Rev. 2.6**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.5	2014-07-25	Rev.2.5
2.6	2015-02-10	Insert Rg min value = 0.65 Ohm

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### Published by

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81726 München, Germany

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