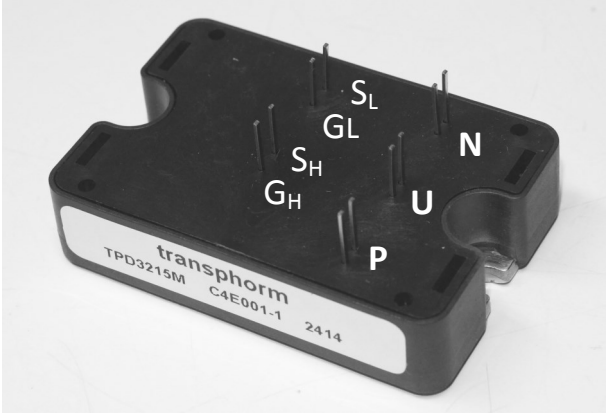
PRODUCT SUMMARY (TYPICAL)	
V_{DS} (V)	600
$R_{DS(on)}$ (mΩ)	30

GaN Power Hybrid HEMT Half-Bridge Module

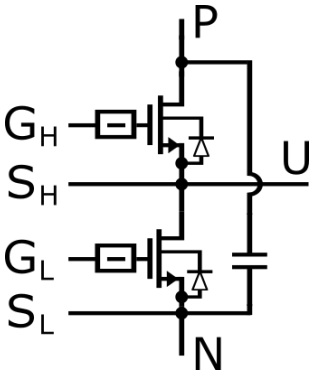


Features

- High frequency operation
- Free-wheeling diode not required

Applications

- Compact DC-DC converters
- AC motor drives
- Battery chargers
- Switch mode power supplies



Absolute Maximum Ratings (T_C=25 °C unless otherwise stated)

Symbol	Parameter	Limit Value	Unit
$I_{D25°C}$	Continuous Drain Current @T_C=25 °C (per switch) [a]	70	A
$I_{D100°C}$	Continuous Drain Current @T_C=100 °C (per switch)	40	A
I_{DM}	Pulsed Drain Current (pulse width: 5μs)	240	A
V_{DSS}	Drain to Source Voltage	600	V
V_{DST}	Transient Drain to Source Voltage [b]	750	V
V_{GSS}	Gate to Source Voltage	±18	V
$P_{D25°C}$	Maximum Power Dissipation (per switch) Maximum Power Dissipation (whole module)	235 470	W
T_J	Junction Operating Temperature	-40 to 150	°C
T_S	Storage Temperature	-40 to 125	°C
T_{Csold}	Soldering peak Temperature [c]	300	°C
V_{iso}	Charged part to base plate, f = 60Hz, AC 1 minute	2500	V
	Torque strength	2.5-3.5	N-m
	Weight	95	g

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{ΘJC1}$	Junction-to-Case (per switch, T_C at base plate center)	0.53	°C/W
$R_{ΘJCT}$	Junction-to-Case (Whole module, T_C at base plate center)	0.27	°C/W
$R_{ΘJA}$	Junction-to-Ambient (module)	18	°C/W

Notes:
a: 80% duty cycle
b: In off state, spike duty cycle D<0.1, duration <1us
c: For 10 sec.

Electrical Characteristics (T_C=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typical	Max	Unit	Test Conditions
Static						
$V_{DSS-MAX}$	Drain-Source Breakdown Voltage	600			V	V_{GS}=0 V
$V_{GS(th)}$	Gate Threshold Voltage		2.2		V	V_{DS}=Vgs, I_D=2mA
$R_{DS(on)}$	Drain-Source On-Resistance (T_J=25°C)		30	34	mΩ	V_{GS}=8 V, I_D=0-30 A, T_J=25 °C
$R_{DS(on)}$	Drain-Source On-Resistance (T_J=125°C)		53	57	mΩ	V_{GS}=8 V, I_D=0-30 A, T_J=125 °C
$R_{DS(on)}$	Drain-Source On-Resistance (T_J=150°C)		62	66	mΩ	V_{GS}=8 V, I_D=0-30 A, T_J=150 °C
I_{DSS}	Drain-to-Source Leakage Current		6	90	µA	V_{DS}=600 V, V_{GS}=0 V, T_J=25 °C
I_{GSS}	Gate-to-Source Forward Leakage Current	-	-	200	nA	V_{GS}= 18 V
	Gate-to-Source Reverse Leakage Current	-	-	-200	nA	V_{GS}= -18 V
Dynamic						
C_{ISS}	Input Capacitance [d]		2260		pF	V_{GS}=0 V, V_{DS}=100V, *f* =1 MHz
C_{OSS}	Output Capacitance [d]		248			
C_{RSS}	Reverse Transfer Capacitance [d]		23			
$C_{O(er)}$	Output Capacitance, energy related [d]		400			V_{GS}=0 V, V_{DS}=0 V to 480 V
$C_{O(tr)}$	Output Capacitance, time related [d]		640			
Q_g	Total Gate Charge [d]		28		nC	V_{DS}=400 V, V_{GS}=0-8 V, I_D=20 A
Q_{gs}	Gate-to-Source Charge [d]		6			
Q_{gd}	Gate-to-Drain Charge [d]		10			
RG	Gate Resistance [d]		0.9	1.5	Ω	
$t_{d(on)}$	Turn-On Delay		36		nS	V_{DS} =400 V , V_{GS}= 0-10 V, I_D = 30 A, R_{Drive}= 2 Ω, T_J=25 °C
t_r	Rise Time		7			
$T_{d(off)}$	Turn-Off Delay		58			
t_f	Fall Time		8			

Notes:
d: Based on data from devices in a discrete package.

Electrical Characteristics (T_C=25 °C unless otherwise stated)						
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Unit**	**Test Conditions**
Reverse Operation						
I_S	Reverse Source current			40(duty=100%) 100(duty=10% pulse < 2ms)	A	V_{GS}=0 V, T_c=100°C
V_{SD}	Reverse Source Voltage (I_S=30 A)		1.53 2.06		V	V_{GS}=0 V, I_F=30 A, T_J=25 °C V_{GS}=0 V, I_F=30 A, T_J=150 °C
t_{rr}	Reverse Recovery Time [e]		32		ns	I_F=30 A, V_{DD}=400 V, di/dt = 800 A /µs, T_J=25 °C
Q_{rr}	Reverse Recovery Charge [e]		292		nC	
t_{rr}	Reverse Recovery Time [e]		34		ns	I_F=30 A, V_{DD}=400 V, di/dt = 800 A /µs, T_J=150 °C
Q_{rr}	Reverse Recovery Charge [e]		304		nC	

Notes:
e: Based on data from die in a discrete package.

Typical Characteristics Curves 25 °C unless otherwise stated.

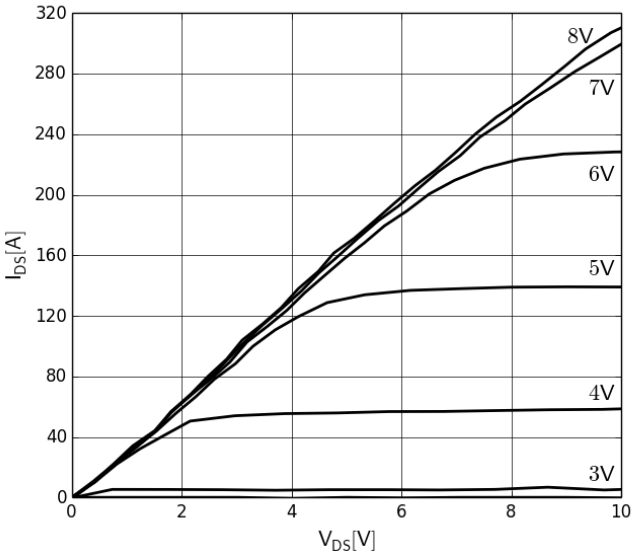


Fig. 1 Typical Output Characteristics T_J= 25°C
Parameter: V_{GS}

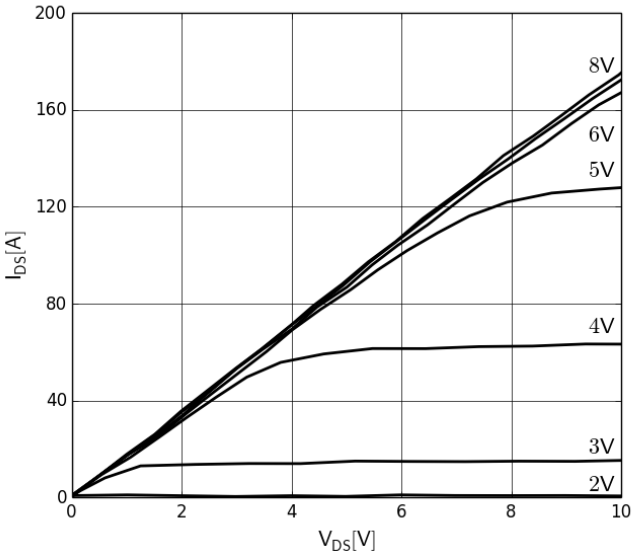


Fig. 2 Typical Output Characteristics T_J=150°C
Parameter: V_{GS}

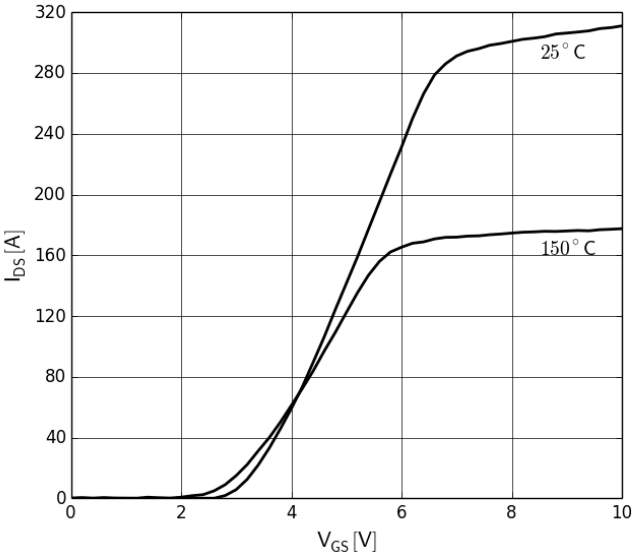


Fig. 3 Typical Transfer Characteristics
V_{DS}=10V, Parameter: T_J

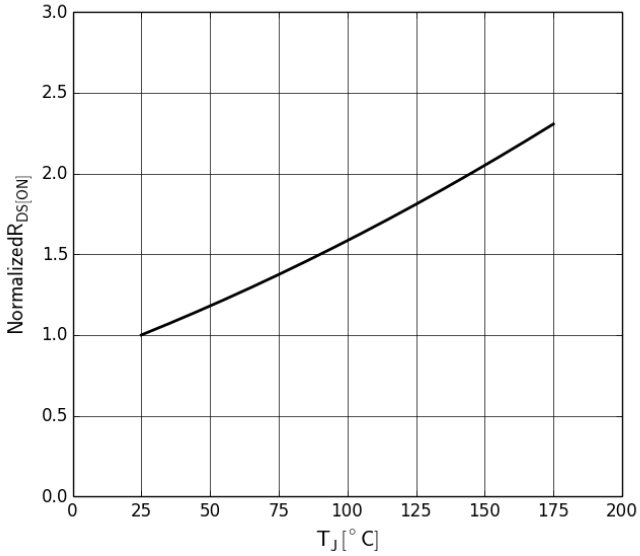


Fig. 4 Normalized On-Resistance
I_D=30 A, V_{GS}=8 V

Typical Characteristics Curves 25 °C unless otherwise stated.

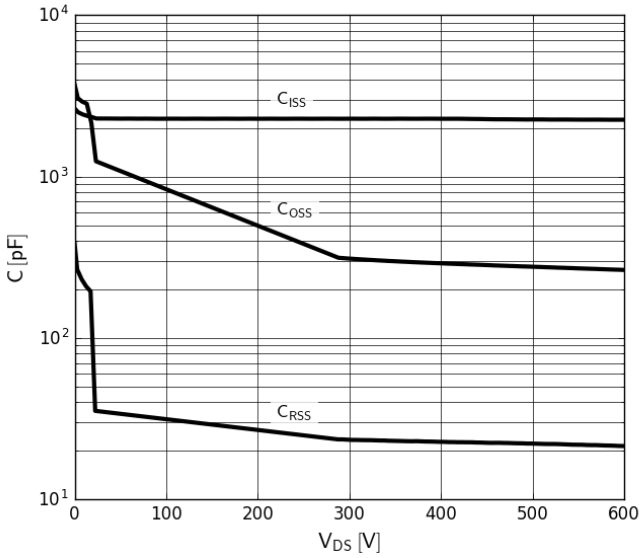


Fig. 5 Typical Capacitance
V_{GS} =0V, f=1 MHz (each switch)

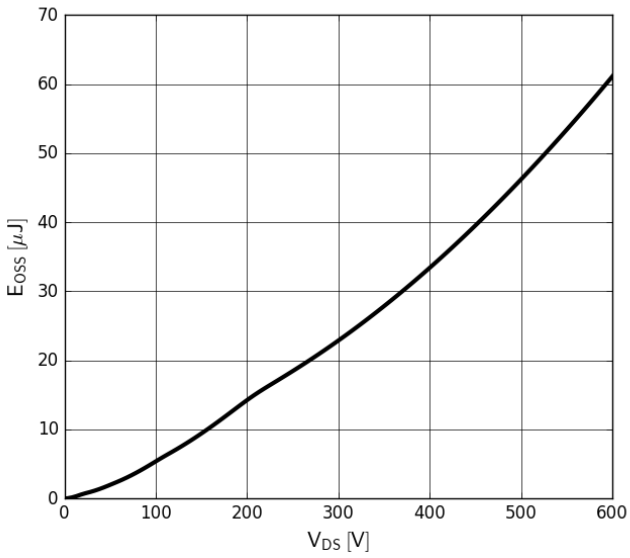


Fig. 6 Typical C_{oss} Stored Energy
(each switch)

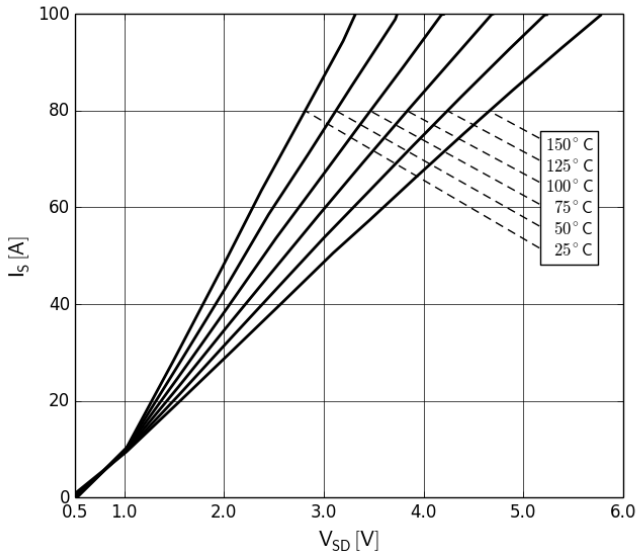


Fig. 7 Reverse I-V Characteristics
I_S= f(V_{SD}); parameter Tj, (each switch)

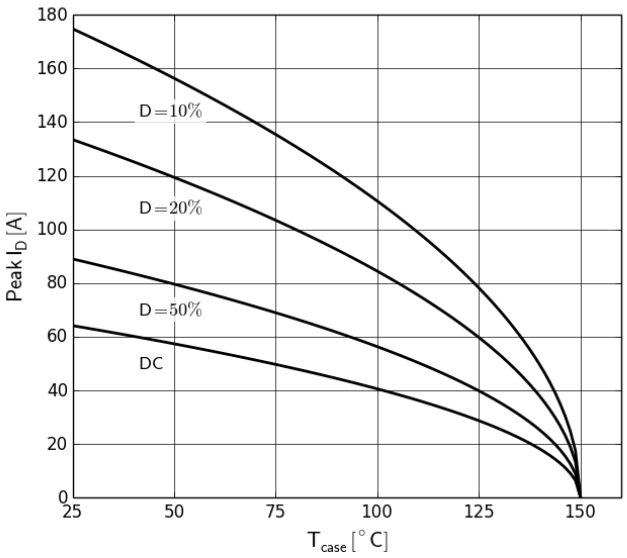


Fig. 8 Maximum Forward Current vs Case Temperature
f=10KHz (each switch)

Typical Characteristics Curves 25 °C unless otherwise stated.

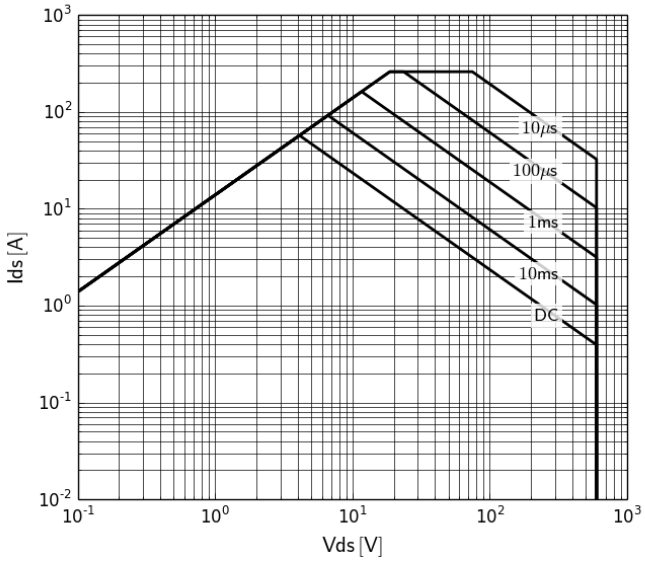


Fig. 9 Safe Operating Area T_c= 25°C
(Each Switch)

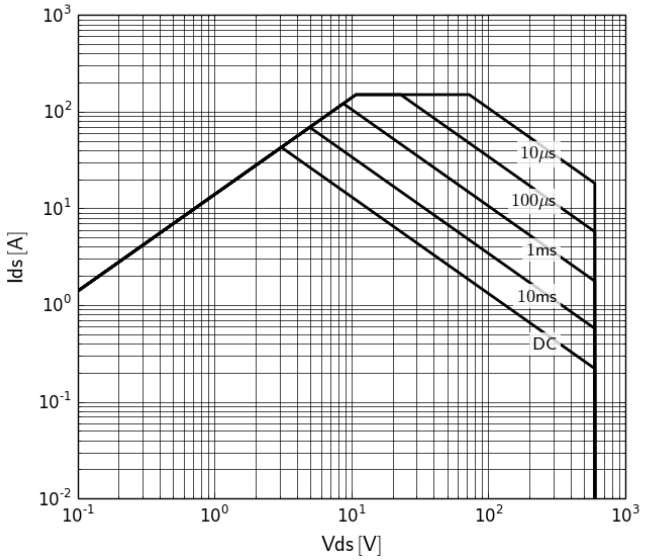


Fig. 10 Safe Operating Area T_c= 80°C
(Each Switch)

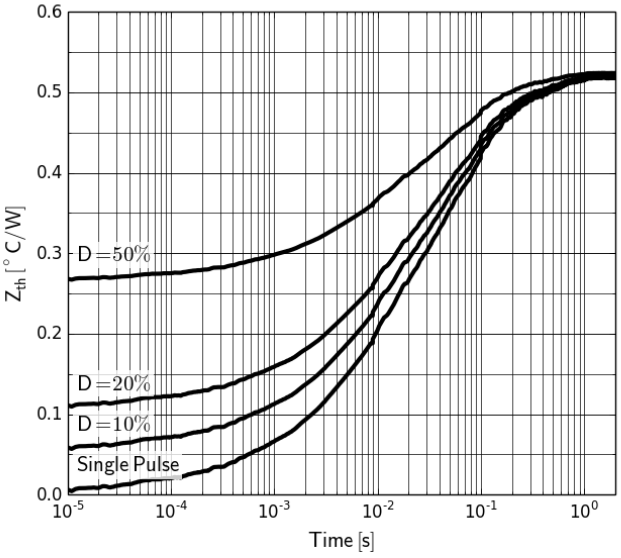


Fig. 11 Transient Thermal Impedance
(Each Switch)

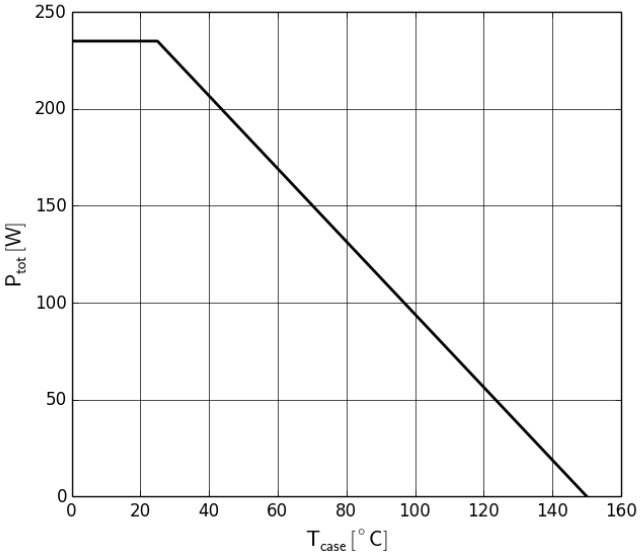


Fig. 12 Power Dissipation (Each Switch)

Test Circuits and Waveforms

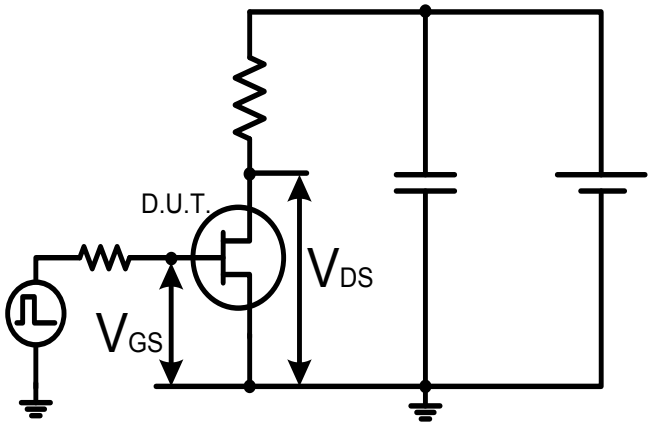


Fig. 13 Switching Time Test Circuit

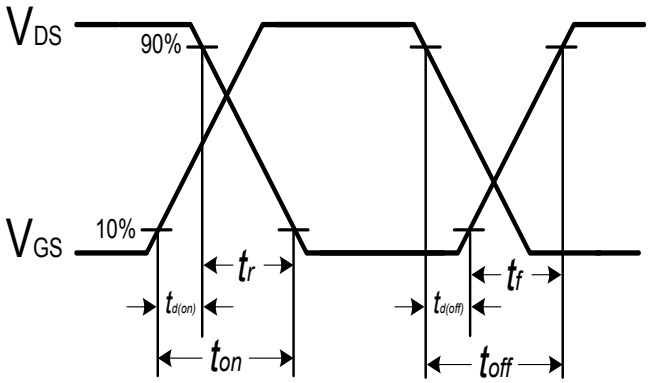


Fig. 14 Switching Time Waveform

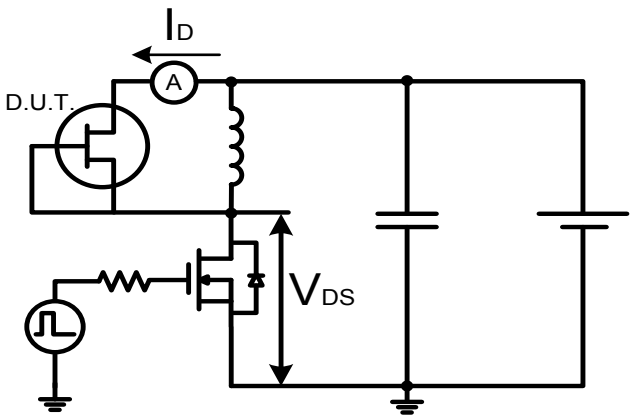


Fig. 15 Test Circuit for Diode Characteristics

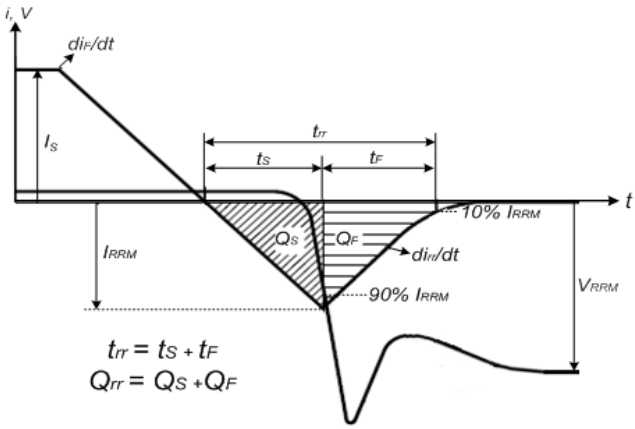
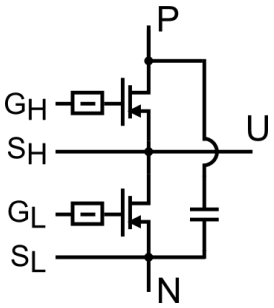


Fig. 16 Diode Recovery Waveform

Circuit diagram:

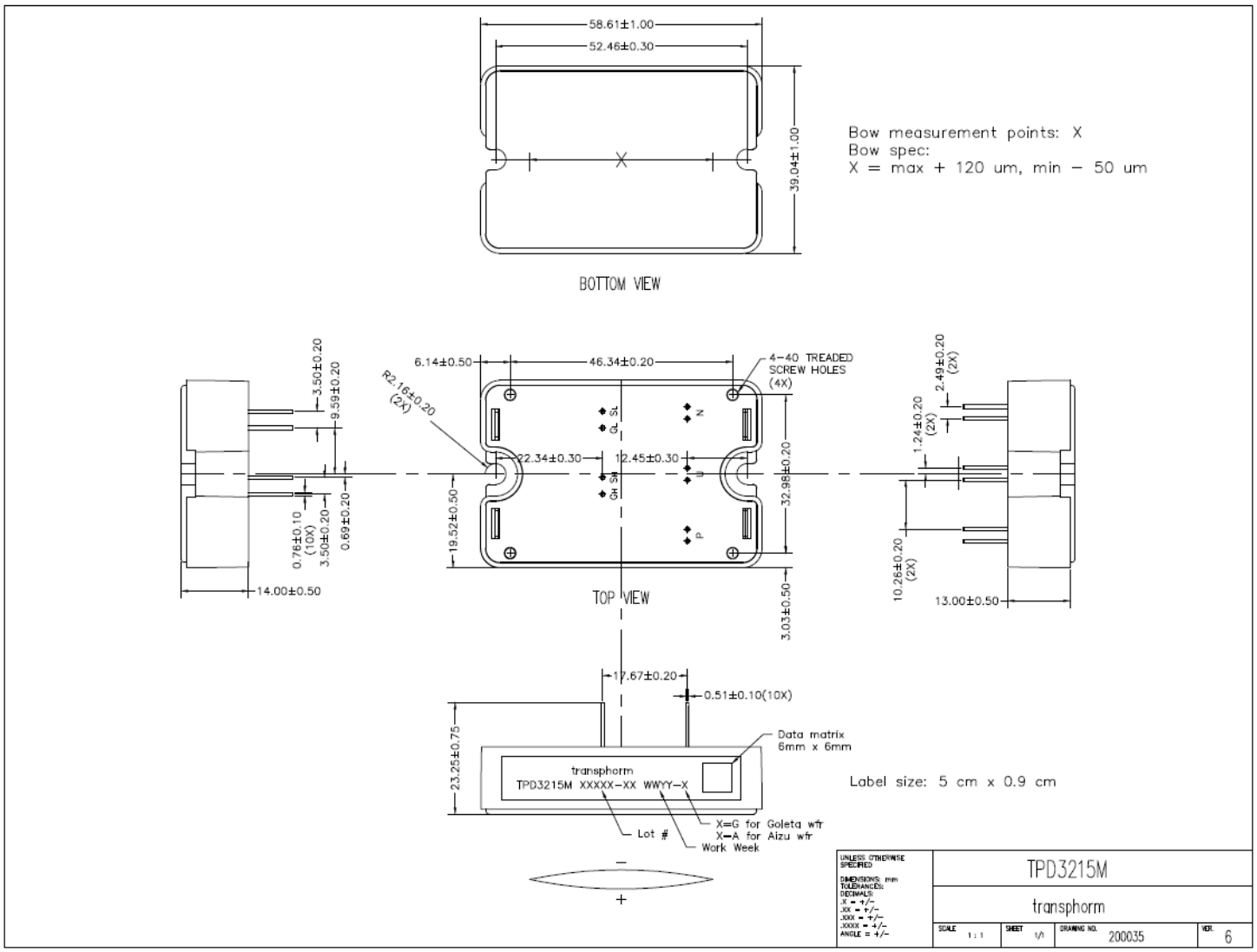


N: Negative terminal, P: Positive terminal, U: Bridge center output

S_L: Low side source, G_L: Low side gate

S_H: High side source, G_H: High side gate

Mechanical drawing:



Important Notice

Transphorm Gallium Nitride (GaN) Switches provide significant advantages over silicon (Si) Superjunction MOSFETs with lower gate charge, faster switching speeds and smaller reverse recovery charge. GaN Switches exhibit in-circuit switching speeds in excess of 150 V/ns and can be even pushed up to 500V/ns, compared to current silicon technology usually switching at rates less than 50V/ns.

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN Switches requires adherence to specific PCB layout guidelines and probing techniques .

Transphorm suggests visiting application note “Printed Circuit Board Layout and Probing for GaN Power Switches” before evaluating Transphorm GaN switches. Below are some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Switches	
DO	**DO NOT**
Minimize circuit inductance by keeping traces short, both in the drive and power loop.	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout.
Minimize lead length from package to PCB. Provide the closest placement of gate driver to drive pins; preferred to have 4 layer PCB with ground planes under gate drives.	Use long traces in gate drive loops, long lead length from PCB to package.
Use shortest sense loop for probing. Attach the probe and its ground connection directly to the test points	Use differential mode probe, or probe ground clip with long wire