

***THS6022 250-mA
Dual Differential Drivers
Evaluation Module***

User's Guide

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Preface

Related Documentation From Texas Instruments

- ***THS6022 250-mA DUAL DIFFERENTIAL DRIVERS*** (literature number SLOS225). This is the data sheet for the THS6022 amplifier integrated circuit used on the EVM
- ***THS4001 HIGH-SPEED LOW-POWER OPERATIONAL AMPLIFIER*** (literature number SLOS206) This is the data sheet for the THS4001 amplifier integrated circuit used on the EVM.
- ***PowerPAD™ Thermally Enhanced Package*** (literature number SLMA002) This is the technical brief for the special PowerPAD package in which the THS6022 amplifier IC is supplied.

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General Information

This chapter details the Texas Instruments (TI™) THS6022 250-mA Dual Differential Line Driver Evaluation Module (EVM), SLOP133. It includes a list of EVM features, a brief description of the module illustrated with a pictorial and schematic diagrams, EVM specifications, details on configuring, connecting, and using the EVM, and a discussion on high-speed amplifier and PowerPAD package design considerations.

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1.1 Features

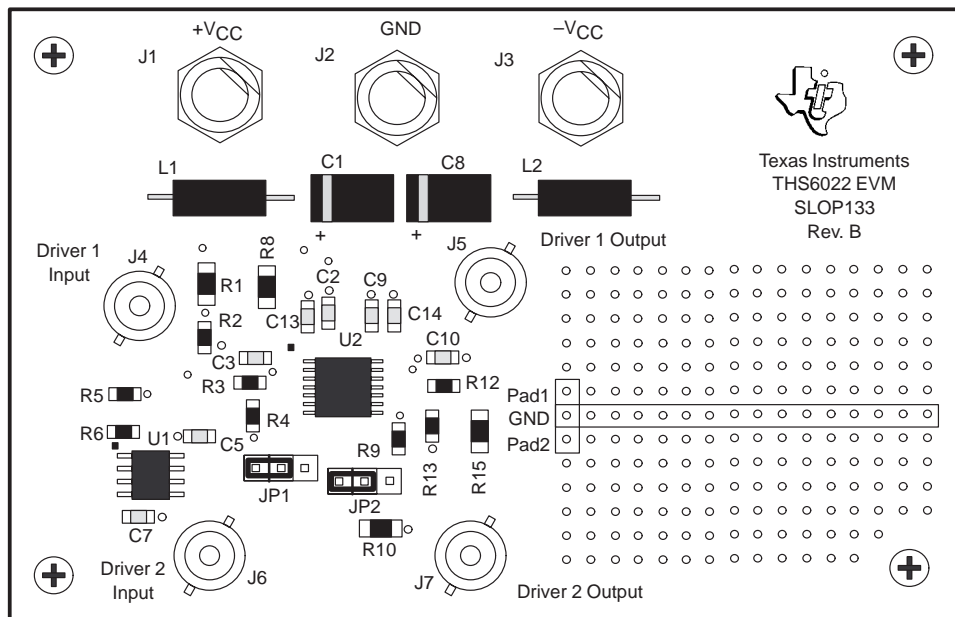
THS6022 250-mA Dual Differential Driver EVM features include:

- A Complete Client Side ADSL Differential Line Driver
- Multiple Input Configurations Set Via On Board Jumpers
- Includes a THS4001 High-Speed Amplifier as an Inverter
- Standard BNC Connectors Inputs and Outputs
- $\pm 5\text{-V}$ to $\pm 15\text{-V}$ Operation
- Nominal $50\text{-}\Omega$ Impedance Inputs
- Pad Area On Board For User Component Placement and Testing
- Good Example of PowerPAD Package and High-Speed Amplifier Design and Layout

1.2 Description

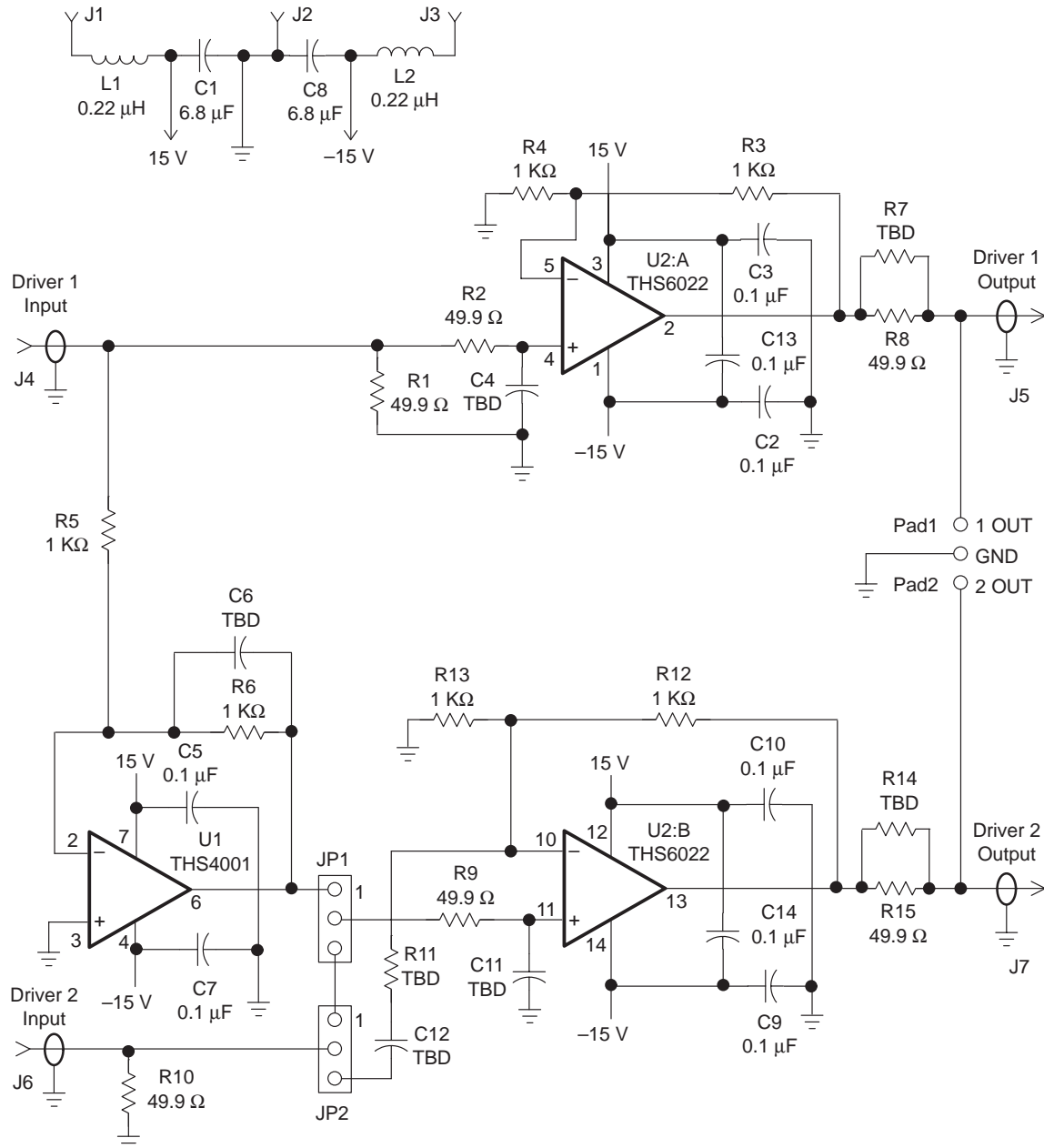
The TI THS6022 250-mA Dual Differential Line Driver Evaluation Module (EVM) is a complete client side ADSL high-speed driver circuit. It consists of the TI THS6022 Dual Differential Line Driver IC, a TI THS4001 High-Speed Low-Power Operational Amplifier IC, and a number of passive parts, all mounted on a multilayer circuit board (Figure 1–1). The EVM uses standard BNC connectors for inputs and outputs and also includes a pad area for user component connection and testing. It is completely assembled, fully tested, and ready to use — just connect it to power, a signal source, and a load (if desired).

Figure 1–1. THS6022 Evaluation Module



Input power is applied to the EVM through banana jacks J1, J2, and J3. An LC filter on each power bus isolates the EVM circuits from the external supply. The schematic for the EVM appears in Figure 1–2.

Figure 1–2. THS6022 Evaluation Module Schematic



The THS6022 EVM is equipped with a separate BNC connector for the Driver 1 input and the Driver 2 input. Each input is terminated with a 50-Ω resistor to provide correct line impedance matching (Figure 1–2). Note that using a source with a 50-Ω output impedance will create a voltage divider at the EVM inputs. Thus, accurate knowledge of the source output characteristics is required to determine proper input signal amplitudes.

Driver outputs are routed through client side ADSL-standard 49.9-Ω resistors to provide correct transmission line impedance matching when run through a 1:1 transformer with a 100-Ω line termination. These resistors also allow separate receivers to view a differential input signal from the transmission line.

All of the amplifiers on the EVM (THS6022 and THS4001) follow the classic operational amplifier gain equations:

$$\text{Inverting Gain} = \frac{-R_F}{R_G} \quad (1)$$

$$\text{Non-Inverting Gain} = 1 + \frac{R_F}{R_G} \quad (2)$$

The gain of the amplifiers can be easily changed to support different applications by changing resistor ratios. Any of the components on the EVM board can be replaced with different values. Also, component pads have been placed in convenient locations on the PCB (shown as components with the value TBD in the schematic) to allow numerous modifications to the basic EVM configuration. However, care must be taken because the surface-mount solder pads on the board are somewhat fragile and will not survive a large number of soldering/desoldering operations.

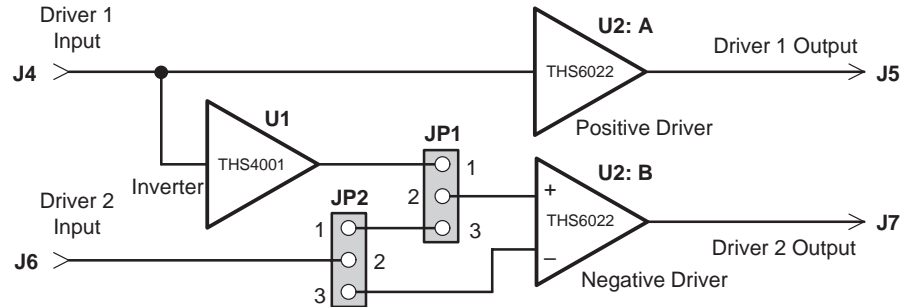
The THS6022 IC is a current-feedback amplifier (CFB) and because of this, extra care must be taken to ensure that a feedback resistor is always included in the design. In addition, there must never be a capacitor directly in the feedback path between the noninverting input and the amplifier output. Disregarding this guideline will likely result in a part that oscillates. The THS4001 IC amplifier used on the EVM, however, is a classic voltage-feedback amplifier (VFB) and has no restrictions on resistors or capacitors in the feedback path. But, to maximize bandwidth, high value resistors and capacitors should be used with discretion.

And finally, the EVM circuit board is a good example of proper board layout for high-speed amplifier and PowerPAD designs. It can be used as a guide for user application layouts.

1.3 Input Configuration

The THS6022 EVM inputs can be configured in several different ways to provide a wide variety of circuits to support different applications (Figure 1–3). Each of the two jumpers on the EVM is a three-pin header that is used as a SPDT switch by placing a shunt across two pins to select either of two possible signal routes.

Figure 1–3. THS6022 Evaluation Module Block Diagram



Jumper JP1:

- 1–2 — connects the noninverting input of driver 2 (U2: B) to the THS4001 inverting amplifier (U1) output
- 2–3 — connects the noninverting input of driver 2 (U2: B) to the input connector (J6) when jumper JP2 is set appropriately

Jumper JP2:

- 1–2 — connects the driver 2 input connector (J6) to the noninverting input of driver 2 (U2:B) when jumper JP1 is set appropriately
- 2–3 — connects the driver 2 input connector (J6) to the inverting input of driver 2 (U2:B) when jumper JP1 is set appropriately

For example, to use a single-ended input, jumper JP1 should be set to 1–2 and the input signal applied to input connector J4. The output of the THS6022 drivers is a differential signal due to the inverter (U1) and JP1 being set to 1–2. For a differential source, JP1 should be set to 2–3, JP2 should be set to 1–2 and the differential input signal applied between input connectors J4 and J6.

If JP2 is in the 2–3 position, components C12 and R11 must be installed, R9 must be removed, and a 0- Ω resistor must be installed in the C11 position for proper operation.

1.4 THS6022 EVM Specifications

Supply voltage range, $\pm V_{CC}$	± 5 V to ± 15 V
Supply current, I_{CC}	23 mA
Input voltage, V_I	$\pm V_{CC}$, max
Output drive, THS6022 Drivers, I_O	250 mA, typ each
Continuous total power dissipation at $T_A = 25^\circ\text{C}$ (THS6022),	3.3 W, max

For complete THS6022 amplifier IC specifications and parameter measurement information, and additional application information, see the THS6022 data sheet, TI Literature Number SLOS225.

1.5 Using The THS6022 EVM

The THS6022 EVM operates from a split power supply with voltages ranging from ± 5 V to ± 15 V. The use of a single supply for this EVM is not recommended. As shipped, the output of driver 1 is equal to a noninverting gain of 2 when using the single-ended input mode. The output of driver 2 is equal to an inverting gain of 2 under the same conditions. An oscilloscope is typically used to view and analyze the EVM output signals.

- 1) Ensure that all power supplies are set to **OFF** before making power supply connections to the THS6022 EVM.
- 2) Select the operating voltage for the EVM and connect appropriate split power supplies to the banana jacks on the module marked **+V_{CC}** (J1) and **-V_{CC}** (J3).
- 3) Connect the power supply ground to the module banana jack marked **GND** (J2).
- 4) Connect an oscilloscope to U2, pin2. This is the driver 1 amplifier output. Connecting directly to the **DRIVER 1 OUTPUT** BNC connector (J5) with a 50- Ω nominal impedance cable and an oscilloscope having a 50- Ω input termination is preferred for examining very high frequency signals.
- 5) Set jumper J1 to the 1–2 position.
- 6) Set jumper J2 to the 1–2 position.
- 7) Set the power supply to **ON**
- 8) Connect a signal input to the **DRIVER 1 INPUT** BNC (J4).

Each input connector on this EVM is terminated with a 50- Ω resistor to ground. With a 50- Ω source impedance, the voltage seen by the THS6022 amplifier IC on the EVM will be 1/2 the source signal voltage applied to the EVM input connector.

- 9) Verify the output signal on the oscilloscope. With a high-impedance scope probe, the output signal should be twice the source amplitude. Using the 50- Ω input impedance of an oscilloscope will show 1/2 the actual THS6022 amplifier IC output voltage. This is due to the voltage division between the source resistance and the oscilloscope 50- Ω input impedance. When connected to J7 (Driver 2 output), the signal should be 180° phase shifted from the Driver 1 output (J5).

1.6 THS6022 EVM Performance

Figure 1–4 shows the typical frequency response of the THS6022 EVM drivers when properly loaded. This data was collected using a single-ended input with a 100-Ω load connected between the driver outputs, as shown in the test circuit of Figure 1–5.

Typical –3-dB bandwidth with a ±15 V power supply is 70 MHz for driver 2 and 60 MHz for driver 1. With a ±5 V power supply, typical –3-dB bandwidth is 75 MHz for driver 2 and 70 MHz for driver 1. The difference between the output signals of driver 1 and driver 2 is primarily due to the high-frequency characteristics of the inverting amplifier (U1). Component values can be changed to cause the two responses to track more closely, but since ADSL signals are limited to 2 MHz and below, the high-frequency imbalance can usually be ignored.

Figure 1–4. THS6022 EVM Driver Frequency Response With a 50-Ω Load

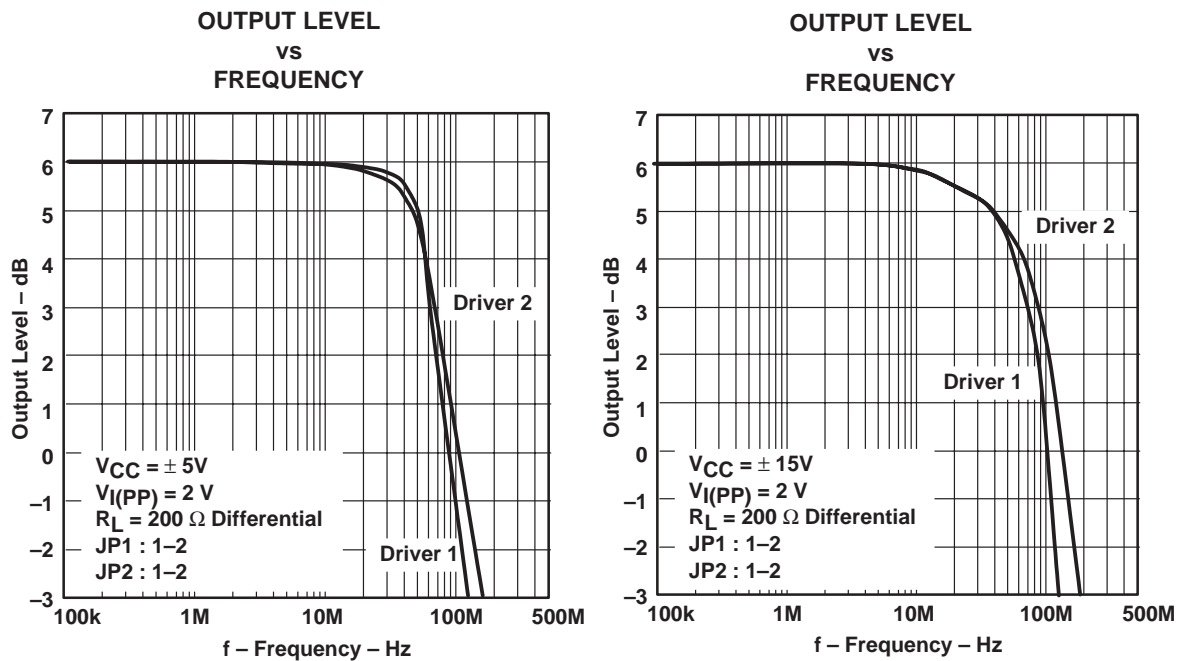
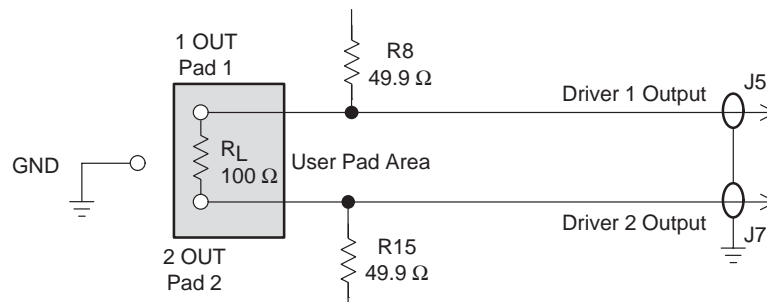


Figure 1–5. THS6022 EVM Driver Frequency Response Test Circuit



1.7 General High-Speed Amplifier Design Considerations

The THS6022 EVM layout has been designed and optimized for use with high-speed signals and can be used as an example when designing THS6022 applications. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregard of these basic design considerations could result in less than optimum performance of the THS6022 250-mA dual differential line driver IC.

Surface-mount components were selected because of the extremely low lead inductance associated with this technology. Also, because surface-mount components are physically small, the layout can be very compact. This helps minimize both stray inductance and capacitance.

Tantalum power supply bypass capacitors (C1 and C8) at the power input pads help supply currents for rapid, large signal changes at the amplifier output. The 0.1 μF power supply bypass capacitors (C2, C3, C5, and C7) were placed as close as possible to the IC power input pins in order to keep the PCB trace inductance to a minimum. This improves high-frequency bypassing and reduces harmonic distortion. Additional 0.1 μF capacitors (C13 and C14) were placed between $+V_{CC}$ and $-V_{CC}$. This helps minimize the harmonic distortion of the amplifiers.

A proper ground plane should always be used with high-speed circuit design. This provides low-inductive ground connections for return current paths. Special attention is needed for the inverting input pins. Stray capacitance at these pins can **seriously degrade** the performance of the amplifiers. In addition, ground plane coupling into these pins can cause noise to appear at the outputs of the amplifiers. This is especially important for the inverting pin while the amplifier is operating in the noninverting mode. Because the voltage at this pin swings directly with the noninverting input voltage, any stray capacitance would allow currents to flow into the ground plane, causing possible gain error and/or oscillation. Capacitance variations at the amplifier IC input pin of less than 1 pF can significantly affect the response of the amplifier.

In general, it is always best to keep signal lines as short and as straight as possible. Sharp 90° corners should generally be avoided — round corners or a series of 45° bends should be used, instead. Stripline techniques should also be incorporated when signal lines are greater than 3 inches in length. These traces should be designed with a characteristic impedance of either 50 Ω or 75 Ω , as required by the application. Such signal lines should also be properly terminated with an appropriate resistor.

Finally, proper termination of all inputs and outputs should be incorporated into the layout. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier IC. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in amplifier phase-margin and improves the amplifier stability for improved performance such as reduced peaking and settling times.

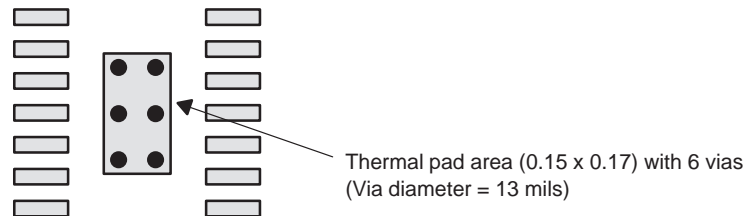
1.8 General PowerPAD Design Considerations

The THS6022 IC is mounted in a special package incorporating a thermal pad that transfers heat from the IC die directly to the PCB. The PowerPAD package is constructed using a downset leadframe. The die is mounted on the leadframe but is electrically isolated from it. The bottom surface of the lead frame is exposed as a metal thermal pad on the underside of the package and makes physical contact with the PCB. Because this thermal pad is in direct physical contact with both the die and the PCB, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad mounting point on the PCB.

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach as used on the THS6022 EVM, which is built on a multilayer PCB with an internal ground plane.

- 1) Prepare the PCB with a top side etch pattern as shown in Figure 1–6. There should be etch for the leads as well as etch for the thermal pad.

Figure 1–6. PowerPAD PCB Etch and Via Pattern – Minimum Requirements



- 2) Place 6 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
- 3) Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This will help dissipate the heat generated from the THS6022. These additional vias may be larger than the 13 mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered, therefore, wicking is generally not a problem.
- 4) Connect all holes to the internal ground plane.
- 5) When connecting these holes to the ground plane, **DO NOT** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6022 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
- 6) The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its 6 holes. The bottom-side solder mask should cover the 6 holes of the thermal pad area. This eliminates the solder from being pulled away from the thermal pad area during the reflow process.

- 7) Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
- 8) With these preparatory steps in place, the THS6022 is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

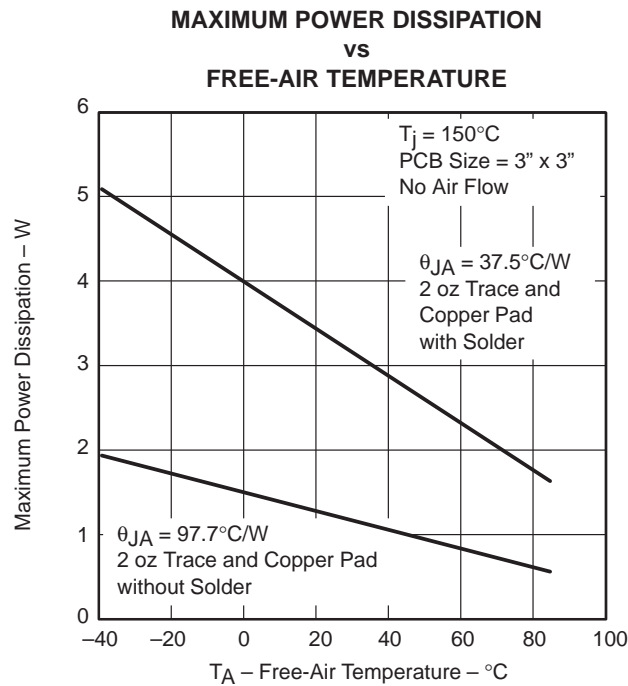
The actual thermal performance achieved with the THS6022 in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA} , is about 37.5°C/W. For a given θ_{JA} , the maximum power dissipation is shown in Figure 1–7 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of THS6022 (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- θ_{JA} = $\theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case (2.07°C/W)
- θ_{CA} = Thermal coefficient from case to ambient air

Figure 1–7. Maximum Power Dissipation vs. Free-Air Temperature



Even though the THS6022 EVM PCB surface area is larger than the one in the example above, the results should correlate very well because the traces and the vias of the EVM PCB interrupt the thermal continuity of the ground plane. The THS6022 EVM is a good example of proper thermal management when using PowerPAD-mounted devices.

Correct PCB layout and manufacturing techniques are critical for achieving adequate transfer of heat away from the PowerPAD IC package. More details on proper board layout can be found in the *THS6022 250-mA DUAL DIFFERENTIAL LINE DRIVER* data sheet (SLOS225). For more general information on the PowerPAD package and its thermal characteristics, see the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package* (SLMA002).



Reference

This chapter includes a parts list and PCB layout illustrations for the THS6022 EVM.

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2.1 THS6022 Dual Differential Line Drivers EVM Parts List

Table 2–1. THS6022 EVM Parts List

Reference	Description	Size	Quantity	Manufacturer/Distributor Part Number
C1, C8	CAPACITOR, 6.8 μ F, CERAMIC, 20%, TANTALUM, SM		2	(SPRAGUE) 293D685X9035D2T
C2, C3, C5, C7, C9, C10, C13, C14	CAPACITOR, 0.1 μ F, CERAMIC, 10%, SM	0805	8	(MuRata) GRM40-X7R104K25
L1,L2	INDUCTOR, 0.22 μ H AXIAL, THRU HOLE		2	(DELEVAN) DN41221/ (DIGI-KEY) DN41221-ND
J4, J5, J6, J7	JACK, BNC, PC-MOUNT (AMPHONEL)		4	(MOUSER) 523-31-5329
J1,J2,J3	JACK, BANANA RECEPTANCE, FOR 0.25" DIA. HOLE		2	
JP1, JP2	HEADER, 3 PIN, 0.1" CTRS., 0.025" SQ. PINS		2	
R2, R9	RESISTOR, 49.9 OHMS, 1/10W, 1% SM	0805	2	
R1, R8, R10, R15	RESISTOR, 49.9 OHMS, 1/8W, 1% SM	1206	6	
R3, R4, R5, R6, R12, R13	RESISTOR, 1 K OHM, 1/10W, 1% SM	0805	6	
U2	IC, THS6022CPWP		1	(TI) THS6022CPWP
U1	IC, OP AMP, THS4001CD	SOIC-8	1	(TI) THS4001CD
R7, R14	RESISTOR, X OHMS, 1/8W, 1%, SM†	1206	2	
R11	RESISTOR, X OHMS, 1/10W, 1%, SM†	0805	1	
C4, C6, C11, C12	CAPACITOR, X μ F, 10% CERAMIC†	0805	4	
	4-40 TREAD HEX STANDOFFS, 0.625" LENGTH, 0.250 O.D.		4	(MOUSER) 534-1804
	4-40 TREAD HEX STANDOFFS SCREWS		4	
PCB1	PCB, THS6022 EVM SLOP133		1	

† The values of these components are to be determined by the user in accordance with the application requirements.

2.2 THS6022 EVM Board Layouts

Board layout examples of the THS6022 EVM PCB are shown in the following illustrations. They are not to scale and appear here only as a reference.

Figure 2–1. THS6022 EVM Component Placement Silkscreen and Layout

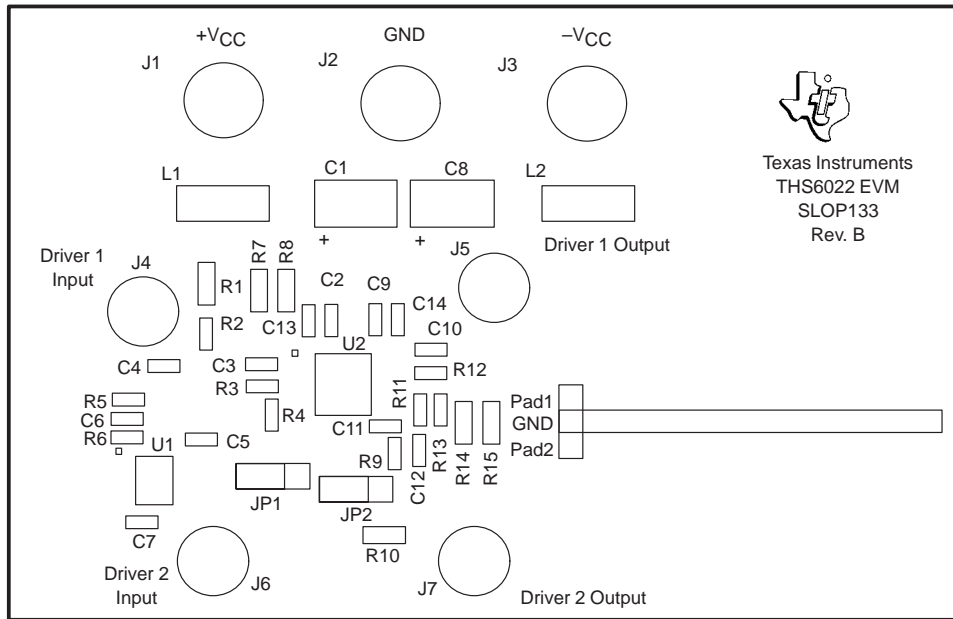


Figure 2–2. THS6022 EVM PC Board: Layer 1 — Top Side Layout

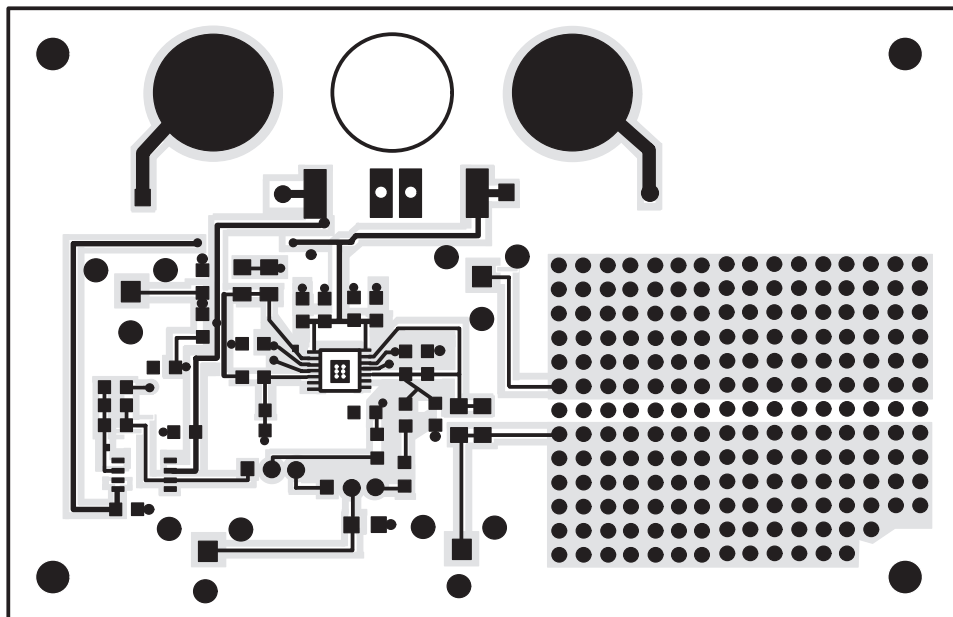


Figure 2–3. THS6022 EVM PC Board: Layer 2 — Back Side Ground Plane Layer

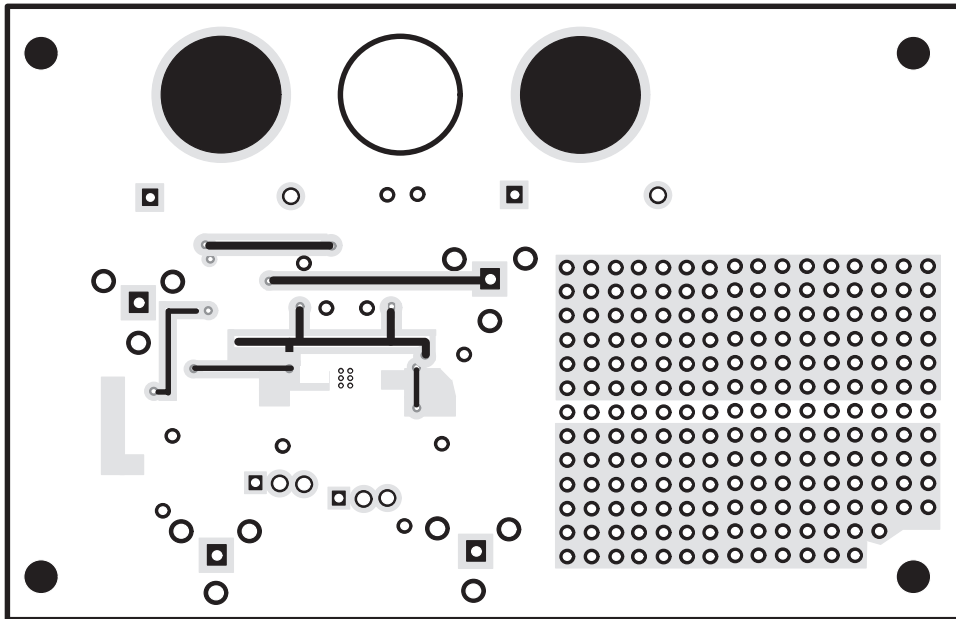


Figure 2–4. THS6022 EVM PC Board: Solder Mask — Back Side

