

TLE4946-1L

High Precision Bipolar Hall-Effect Latch

About this document

Features

- 2.7 V to 24 V supply voltage operation
- Operation from unregulated power supply
- High sensitivity and high stability of the magnetic switching points
- High resistance to mechanical stress by active error compensation
- Reverse battery protection (-18 V)
- Superior temperature stability
- Peak temperatures up to 195°C without damage
- Low jitter (typically 1 μ s)
- High ESD performance ($\pm$ 6 kV HBM)
- Digital output signal
- Leaded package PG-SSO-3-2



Target applications

The TLE4946-1L is an integrated circuit Hall-effect sensor designed specifically for highly accurate applications. Precise magnetic switching points and high temperature stability are achieved by active compensation circuits and chopper techniques on chip.

Type	Package
TLE4946-1L	PG-SSO-3-2

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1 Functional description

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1.1 Pin configuration (top view)

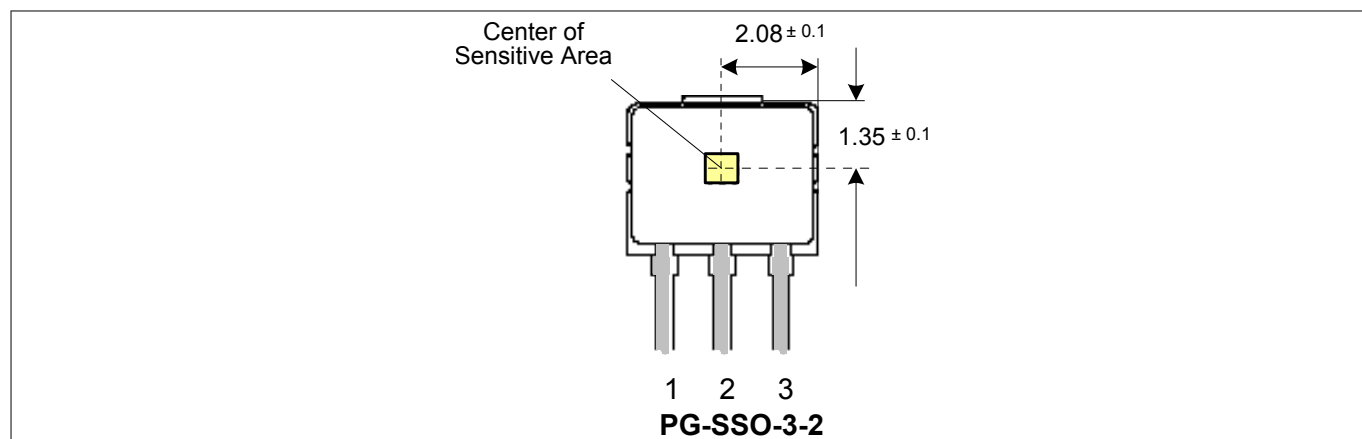


Figure 1 Pin definition and center of sensitive area

Table 1 Pin definitions and functions PG-SSO-3-2

Pin No.	Symbol	Function
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output

2 General

2 General

2.1 Block diagram

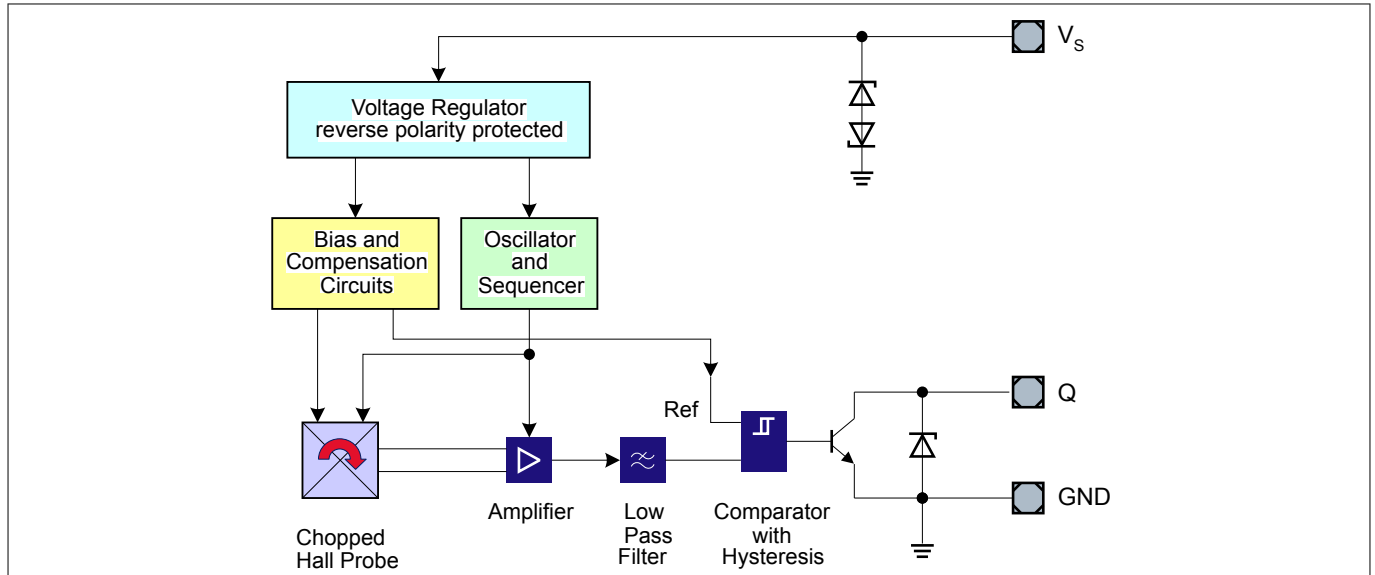


Figure 2 **Block diagram**

2.2 Circuit description

The chopped Hall IC Switch comprises a Hall probe, bias generator, compensation circuits, oscillator, and output transistor

. The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce technology variations.

The Active Error Compensation rejects offsets in signal stages and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stresses in the package.

This chopper technique together with the threshold generator and the comparator ensure high accurate magnetic switching points.

3 Maximum ratings

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

$T_j = -40^{\circ}\text{C}$ to 150°C

Parameter	Symbol	Limit Values		Unit	Conditions
		Min.	Max.		
Supply voltage	V_S	-18	18	V	
		-18	24		for 1 h, $R_S \geq 200\ \Omega$
		-18	26		for 5 min, $R_S \geq 200\ \Omega$
Supply current through protection device	I_S	-50	50	mA	
Output voltage	V_Q	-0.7	18	V	
		-0.7	26		for 5 min @ 1.2 k Ω pull up
Continuous output current	I_Q	-50	50	mA	
Junction temperature	T_j	–	155	$^{\circ}\text{C}$	for 2000 h (not additive)
		–	165		for 1000 h (not additive)
		–	175		for 168 h (not additive)
		–	195		for 3 x 1 h (additive)
Storage temperature	T_S	-40	150	$^{\circ}\text{C}$	
Magnetic flux density	B	–	unlimited	mT	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 ESD Protection⁽¹⁾

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
ESD voltage	V_{ESD}	–	± 6	kV	HBM, $R = 1.5\ \text{k}\Omega$, $C = 100\ \text{pF}$ $T_A = 25^{\circ}\text{C}$

(1) Human Body Model (HBM) tests according to: EOS/ESD Association Standard S5.1-1993 and Mil. Std. 883D method 3015.7

4 Operating range

4 Operating range

Table 4 Operating range

Parameter	Symbol	Limit Values			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_S	2.7	–	18	V	
Output voltage	V_Q	-0.7	–	18	V	
Junction temperature	T_j	-40	–	150	°C	
Output current	I_Q	0	–	20	mA	

5 Electrical and magnetic parameters

Table 5 Electrical characteristics⁽¹⁾

Parameter	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Supply current	I_S	2	4	6	mA	$V_S = 2.7 \text{ V} \dots 18 \text{ V}$
Reverse current	I_{SR}	0	0.2	1	mA	$V_S = -18 \text{ V}$
Output saturation voltage	V_{QSAT}	–	0.3	0.6	V	$I_Q = 20 \text{ mA}$
Output leakage current	I_{QLEAK}	–	0.05	10	μA	for $V_Q = 18 \text{ V}$
Output fall time	t_f	–	0.02	1	μs	$R_L = 1.2 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ see Figure 3
Output rise time	t_r	–	0.4	1	μs	
Chopper frequency	f_{OSC}	–	320	–	kHz	
Switching frequency	f_{SW}	0	–	15 ⁽²⁾	kHz	
Delay time ⁽³⁾	t_d	–	13	–	μs	
Output jitter ⁽⁴⁾	t_{QJ}	–	1	–	μs _{RMS}	Typical value for square wave signal 1 kHz
Power-on time ⁽⁵⁾	t_{PON}	–	13	–	μs	$V_S \geq 2.7 \text{ V}$
Thermal resistance ⁽⁶⁾	R_{thJA}	–	–	190	K/W	PG-SSO-3-2

- (1) over operating range, unless otherwise specified. Typical values correspond to $V_S = 12 \text{ V}$ and $T_A = 25^\circ\text{C}$
(2) To operate the sensor at the max. switching frequency, the value of the magnetic signal amplitude must be 1.4 times higher than for static fields. This is due to the -3 dB corner frequency of the low pass filter in the signal path.
(3) Systematic delay between magnetic threshold reached and output switching
(4) Jitter is the unpredictable deviation of the output switching delay
(5) Time from applying $V_S \geq 2.7 \text{ V}$ to the sensor until the output state is valid
(6) Thermal resistance from junction to ambient

Note: Typical characteristics specify mean values expected over the production spread.

5 Electrical and magnetic parameters

Table 6 **Magnetic characteristics TLE4946-1L⁽¹⁾**

Parameter	Symbol	T _j [°C]	Values			Unit	Notes
			Min.	Typ.	Max.		
Operate point	B _{OP}	-40	11.3	15.4	19.5	mT	
		25	11.0	15.0	19.0		
		150	10.5	14.3	18.1		
Release point	B _{RP}	-40	-19.5	-15.4	-11.3	mT	
		25	-19.0	-15.0	-11.0		
		150	-18.1	-14.3	10.5		
Hysteresis	B _{HYS}	-40	–	–	–	mT	
		25	22.0	30.0	38.0		
		150	–	–	–		
Magnetic Offset	B _{OFF}	-40	–	–	–	mT	⁽²⁾
		25	-2.0	–	2.0		
		150	–	–	–		
Temperature compensation of magn. thresholds	TC	–	–	-350	–	ppm/°C	
Repeatability of magnetic thresholds ⁽³⁾	B _{REP}		–	20	–	μT _{RMS}	Typ. value for ΔB / Δt > 12 mT/ms

(1) over operating range, unless otherwise specified. Typical values correspond to V_S = 12 V

(2) B_{OFF} = (B_{OP} + B_{RP}) ÷ 2

(3) B_{REP} is equivalent to the noise constant

Field Direction Definon

Positive magnetic fields related with south pole of magnet to the branded side of package.

6 Timing diagram

6 Timing diagram

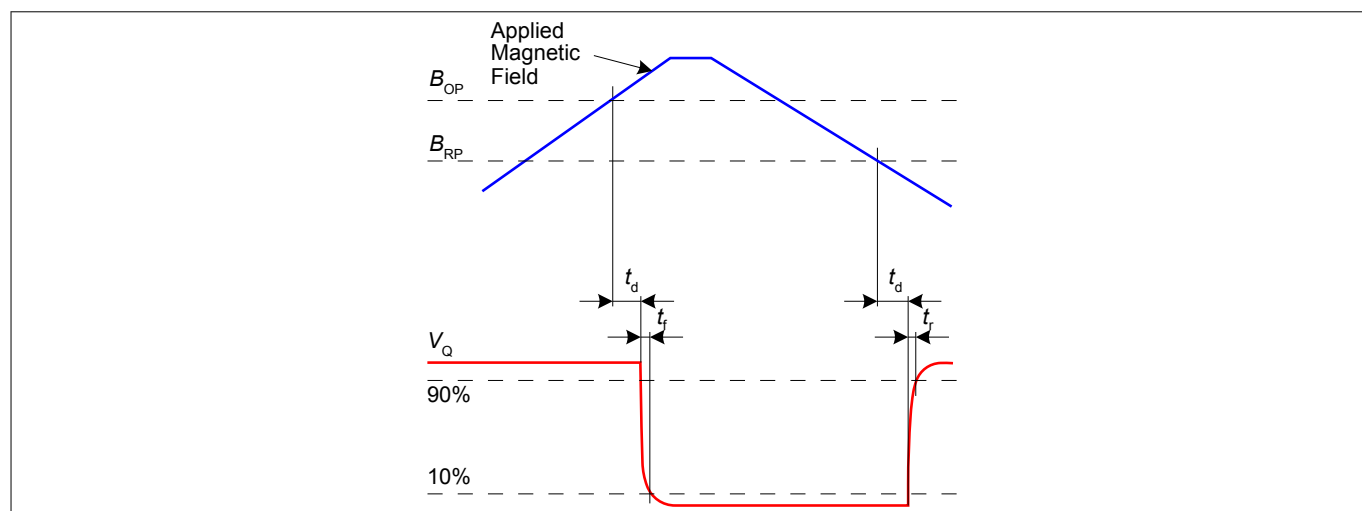


Figure 3 **Timing definition**

7 Package information

7 Package information

7.1 Package marking

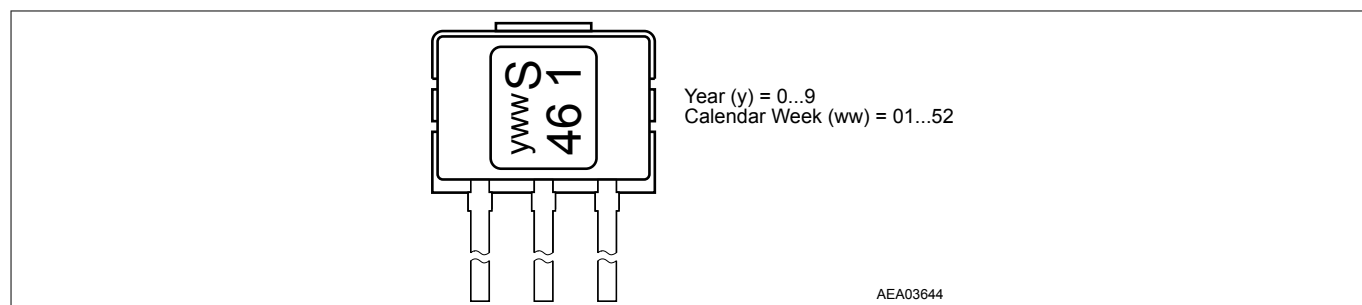


Figure 4 **Marking TLE4946-1L**

7.2 Distance between chip and package surface

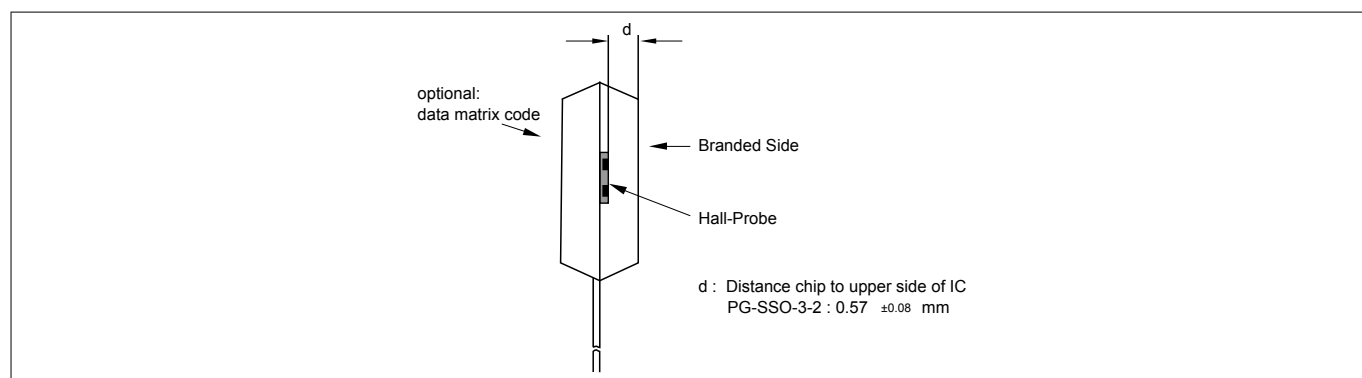


Figure 5 **Distance chip PG-SSO-3-2 to upper side of IC**

7 Package information

7.3 Package outlines

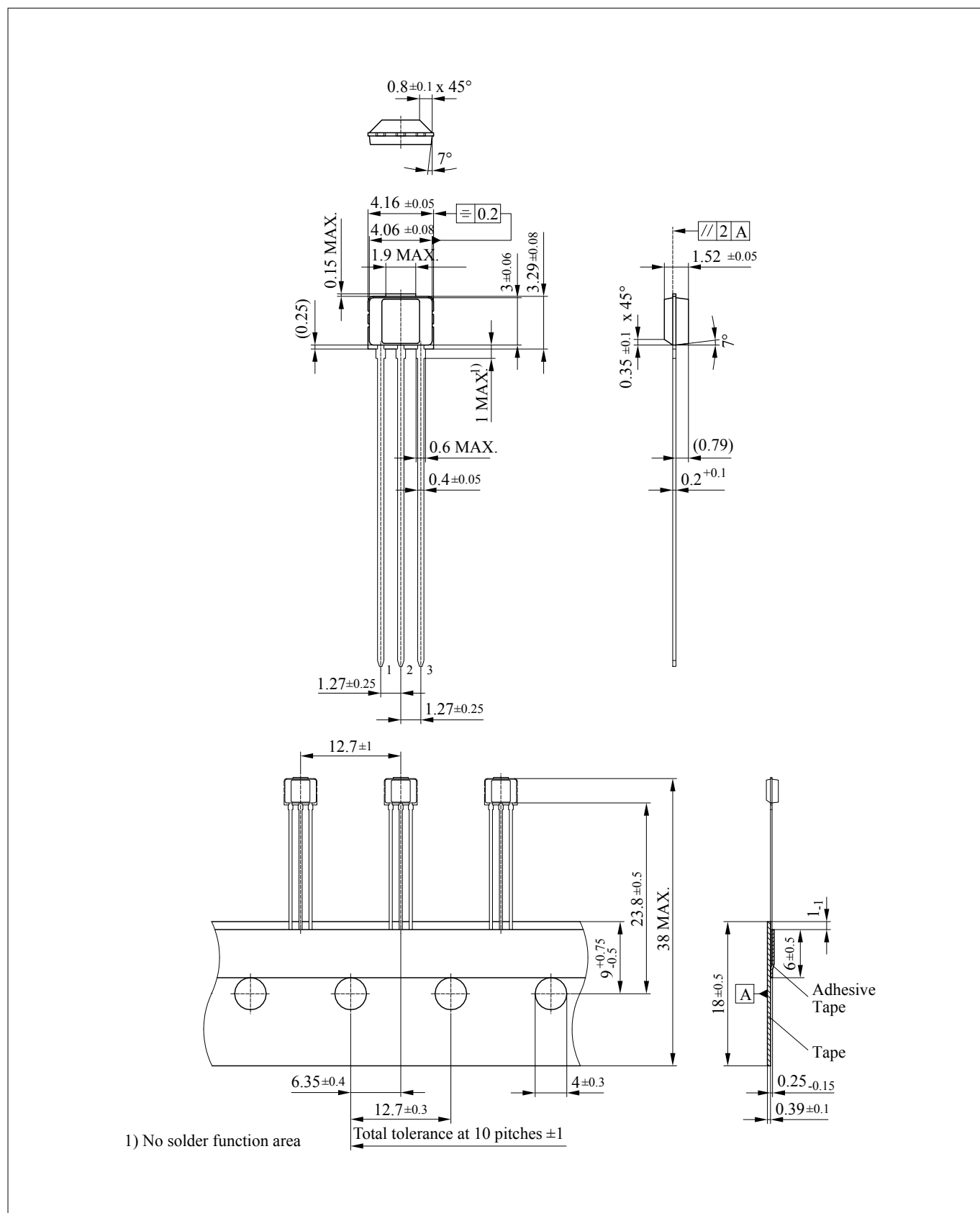


Figure 6 PG-SSO-3-2

7 Package information

Note: You can find all of our packages, sort of packing and others on our Infineon Internet page "Products":
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8 Revision history

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Revision History

Page	Subjects (major changes since last revision)
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Revision History: 2020-08, Rev 1.3

Previous Revisions: Rev 1.2

11	Edited figure 5 (optional: data matrix code)

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Edition 2020-08

Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
IFX-pwe1597744680878

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