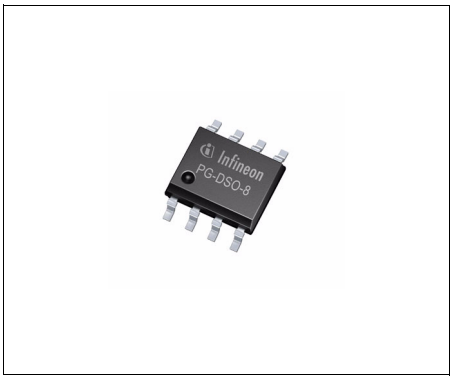
BTS4175SGA

Smart High-Side Power Switch

Automotive Power

Never stop thinking

1 Overview



PG-DSO-8-24

Basic Features

- Fit for 12V and 24V application
- One Channel device
- Very Low Stand-by Current
- CMOS Compatible Inputs
- Electrostatic Discharge Protection (ESD)
- Optimized Electromagnetic Compatibility
- Logic ground independent from load ground
- Very Low Leakage Current from OUT to the load in OFF state
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTS4175SGA is a single channel Smart High-Side Power Switch. It is embedded in a PG-DSO-8-24 package, providing protective functions and diagnostics. The power transistor is built by a N-channel power MOSFET with charge pump. The device is monolithically integrated in Smart technology. It is specially designed to drive Relay, R5W lamp or LED in the harsh automotive environment.

Table 1 Electrical Parameters (short form)

Parameter	Symbol	Value
Operating voltage range	V_{SOP}	6V 52V
Over voltage protection	$V_{S\ (AZ)}$	62V
Maximum ON State resistance at T_j = 150°C	$R_{DS(ON)}$	350mΩ
Nominal load current	$I_{L\ (nom)}$	1.3A
Minimum current limitation	I_{L_SCR}	6A
Standby current for the whole device with load	$I_{S(off)}$	18µA
Maximum reverse battery voltage	$-V_{s(REV)}$	52V

Diagnostic Feature

- Open load in OFF
- Feedback of the thermal shutdown in ON state
- Feedback of the current limitation
- Diagnostic feedback with open drain output

Type	Package	Marking
BTS4175SGA	PG-DSO-8-24	4175SGA

Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Loss of ground and loss of battery protection
- Electrostatic discharge protection (ESD)

Application

- All types of relays, lamps and resistive loads

2 Block Diagram

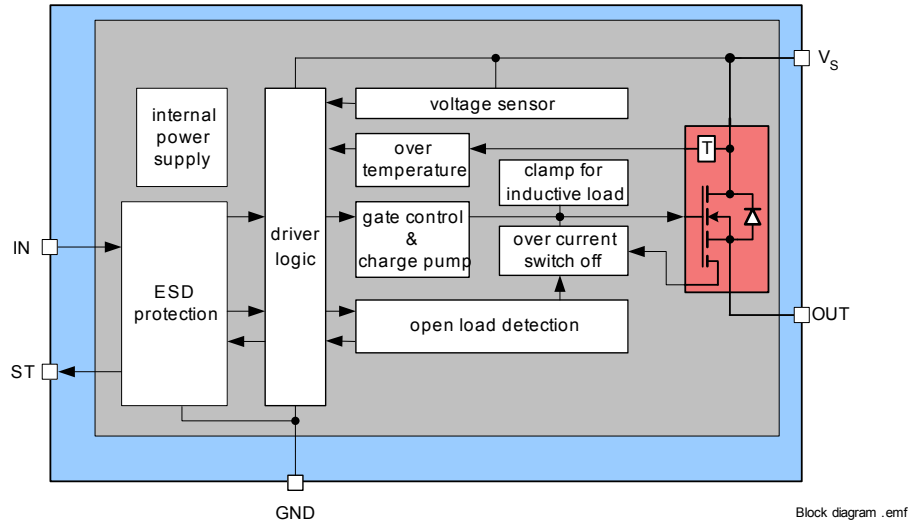


Figure 1 Block diagram for the BTS4175SGA

3 Pin Configuration

3.1 Pin Assignment

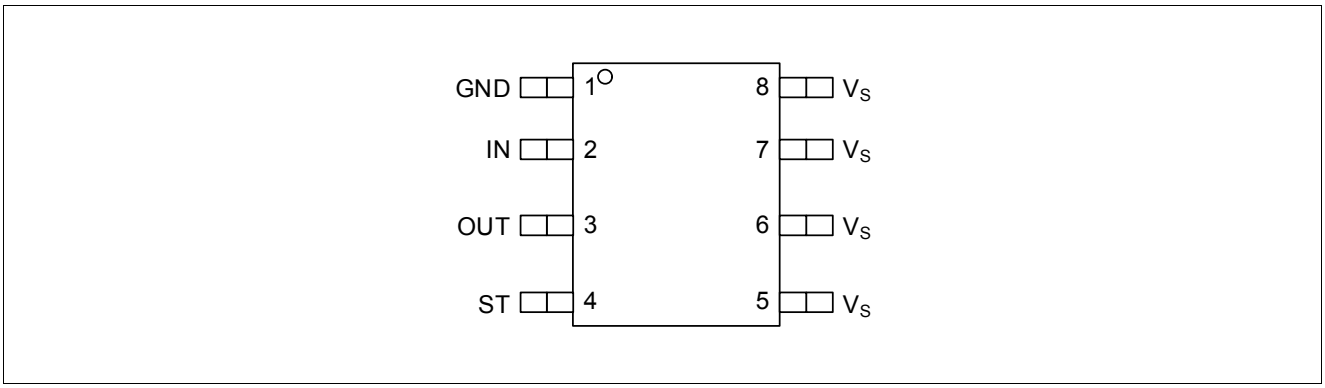


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground**; Ground connection
2	IN	**Input channel;** Input signal. Activate the channel in case of logic high level
3	OUT	**Output;** Protected High side power output channel
4	ST	**Diagnostic feedback;** of channel. Open drain.
5, 6, 7, 8	V_S	**Battery voltage;** Design the wiring for the simultaneous max. short circuit current and also for low thermal resistance

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

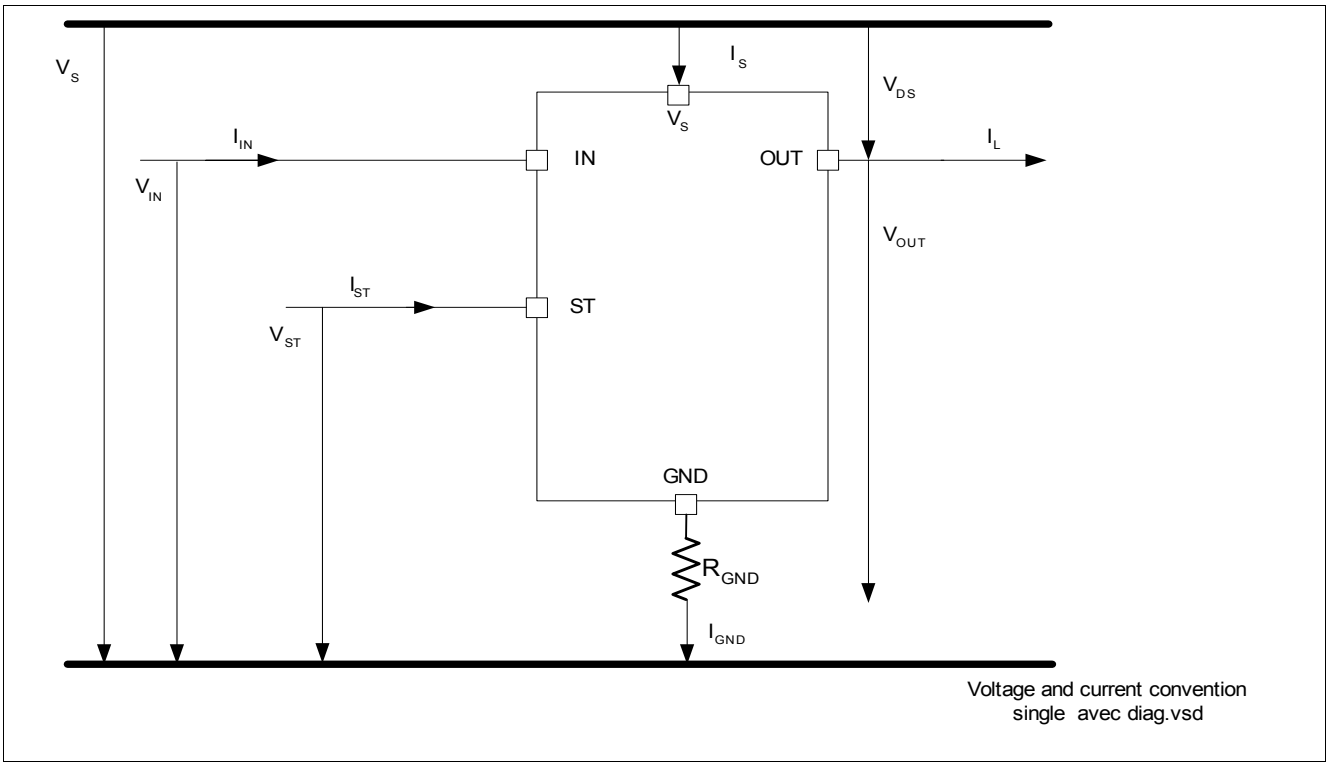


Figure 3 Voltage and current definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_J = 25°C; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	–	52	V	–
4.1.2	Reverse polarity Voltage	- $V_{S(REV)}$	0	52	V	–
4.1.3	Supply voltage for short circuit protection	$V_{bat(SC)}$	0	36	V	R_{ECU} = 20mΩ, R_{Cable}=16mΩ/m, L_{Cable}=1µH/m, ℓ = 0 or 5m [2)] see **Chapter 6**
Input pins						
4.1.4	Voltage at INPUT pins	V_{IN}	-10	16	V	–
4.1.5	Current through INPUT pins	I_{IN}	-5	5	mA	–
Power stage						
4.1.6	Load current	| I_L |	–	$I_{L(LIM)}$	A	–
4.1.7	Power dissipation (DC),	P_{TOT}	–	1.5	W	T_A=85°C, T_j <150°C
4.1.8	Inductive load switch off energy dissipation, Single pulse	E_{AS}	–	125	mJ	T_j=150°C, V_S=13.5V, I_L = 1A
Currents						
Temperatures						
4.1.9	Junction Temperature	T_j	-40	150	°C	–
4.1.10	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.11	ESD Resistivity IN pin	V_{ESD}	-1	1	kV	HBM[3)]
4.1.12	ESD Resistivity all other pins	V_{ESD}	-5	5	kV	HBM[3)]

1) Not subject to production test, specified by design

2) In accordance to AEC Q100–012 and AEC Q101-006

3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Operating Voltage	V_{SOP}	6	52	V	V_{IN} = 4.5V, R_L = 47Ω, V_{DS} < 0.5V
4.2.2	Undervoltage shutdown	V_{SUV}	–	5.5	V	–
4.2.3	Operating current	I_{GND}		2	mA	V_{IN} = 5V
4.2.4	Standby current for whole device with load	$I_{S(OFF)}$	– –	15 18	µA	T_j <85°C T_j = 150°C, R_L = 47Ω, V_{IN} = 0V

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering Point	R_{thJS}	–	–	15	K/W	–[1)]
4.3.2	Junction to Ambient: Channel active	R_{thJA}	–	83	–	K/W	with 6cm² cooling area[1)]

1) Not subject to production test, specified by design

5 Power Stage

The power stage is built by an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_j. **Figure 4** shows the dependencies for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

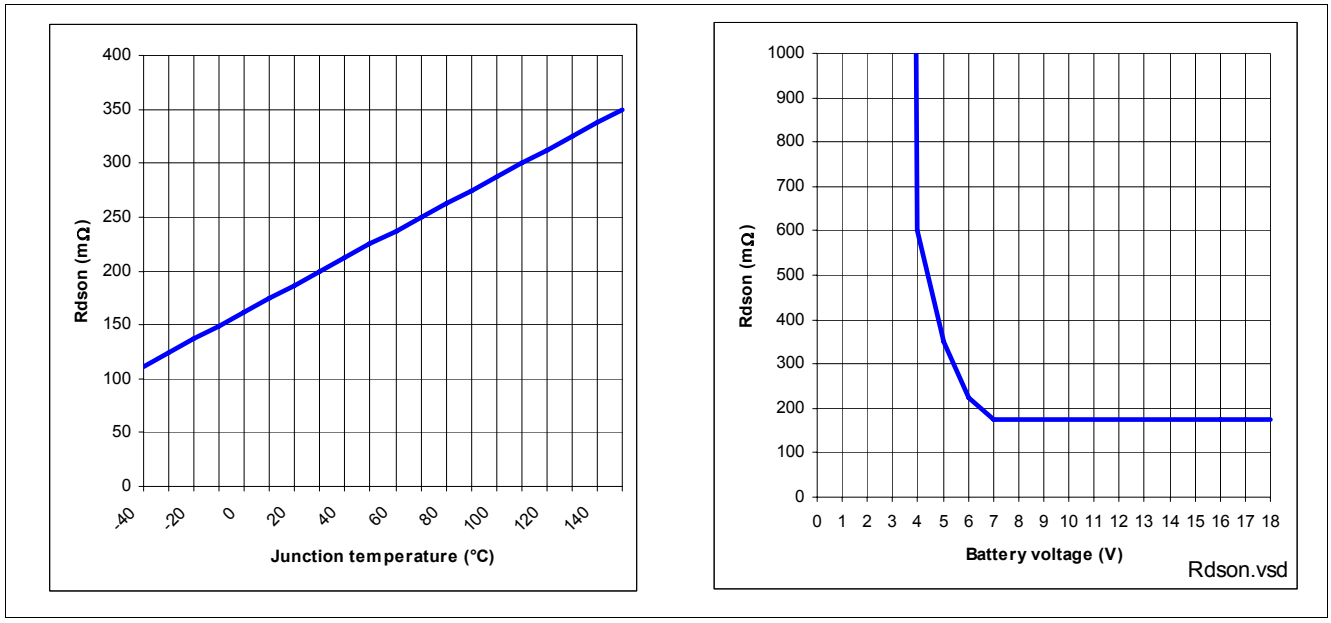


Figure 4 Typical ON-state resistance

A high signal (See **Chapter 8**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.2 Turn ON / OFF Characteristics

Figure 5 shows the typical timing when switching a resistive load.

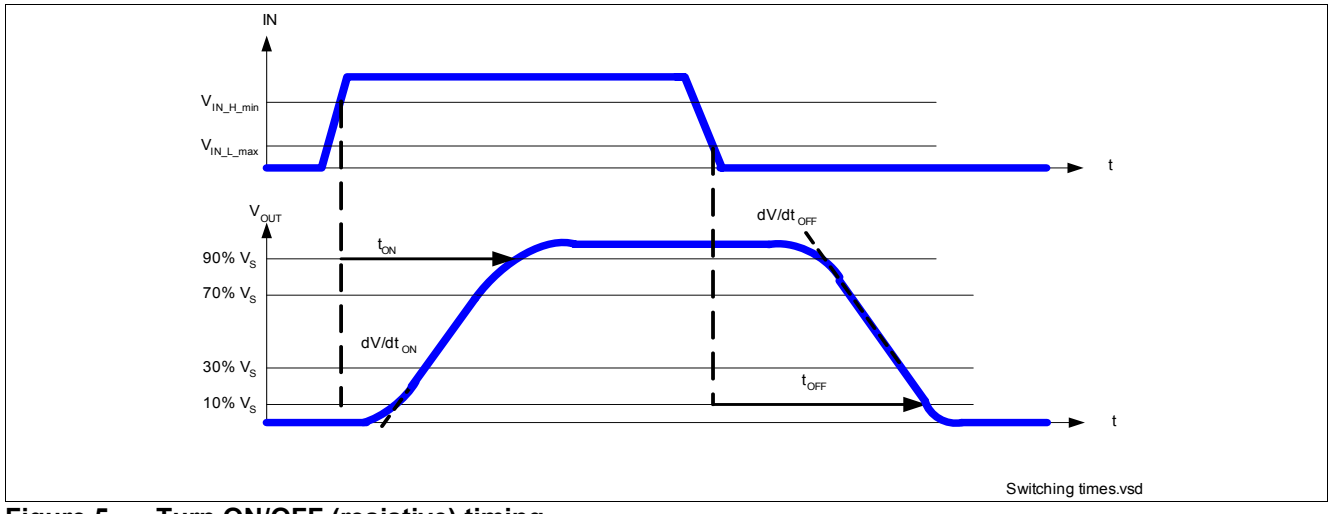


Figure 5 Turn ON/OFF (resistive) timing

5.3 Inductive Output Clamp

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a voltage clamp mechanism implemented that keeps the negative output voltage at a certain level (V_S-$V_{DS(AZ)}$). Please refers to **Figure 6** and **Figure 7** for details. Nevertheless, the maximum allowed load inductance is limited.

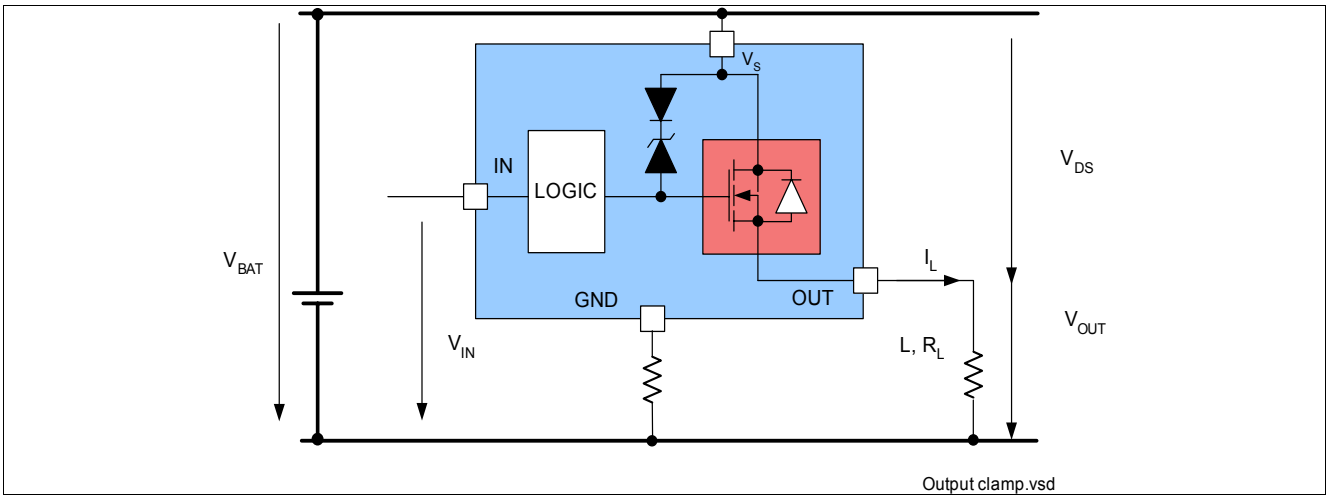


Figure 6 Output clamp

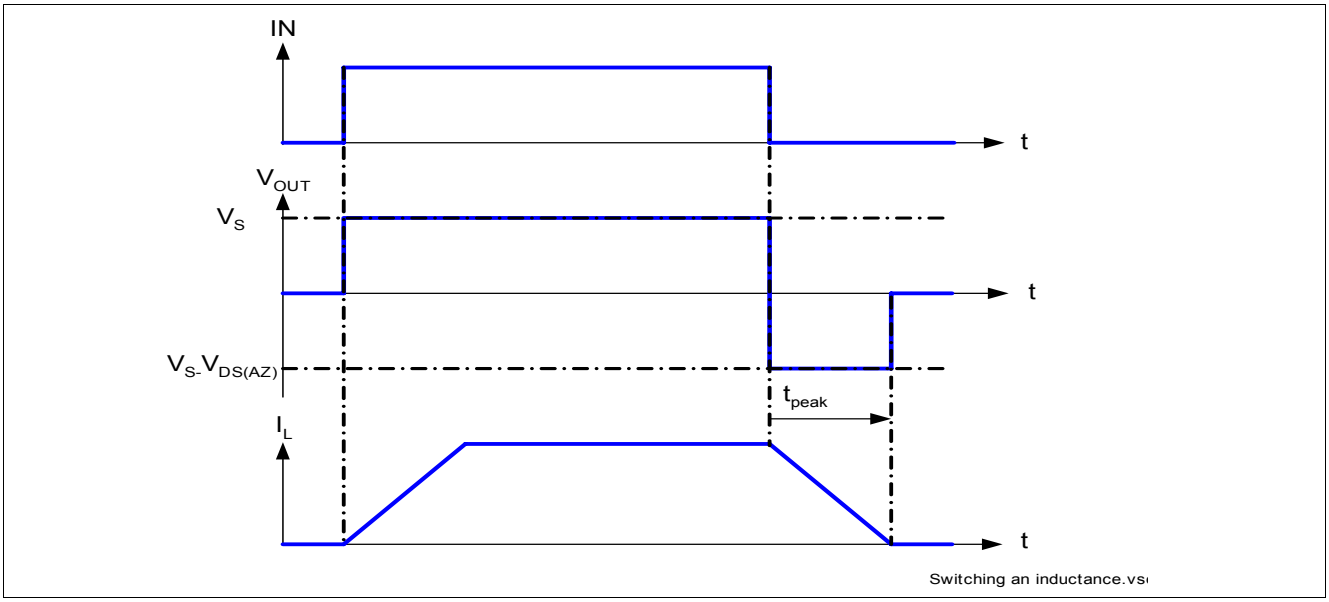


Figure 7 Switching in inductance timing

Maximum Load inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTS4175SGA. This energy can be calculated with following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(AZ)}}{R_L} + \ln\left(\frac{R_L \times I_L}{V_S - V_{DS(AZ)}} \right) + I_L \right]$$

Following equation simplifies under the assumption of R_L = 0Ω.

$$E = \frac{1}{2} \times LI^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 8** for the maximum allowed energy dissipation.

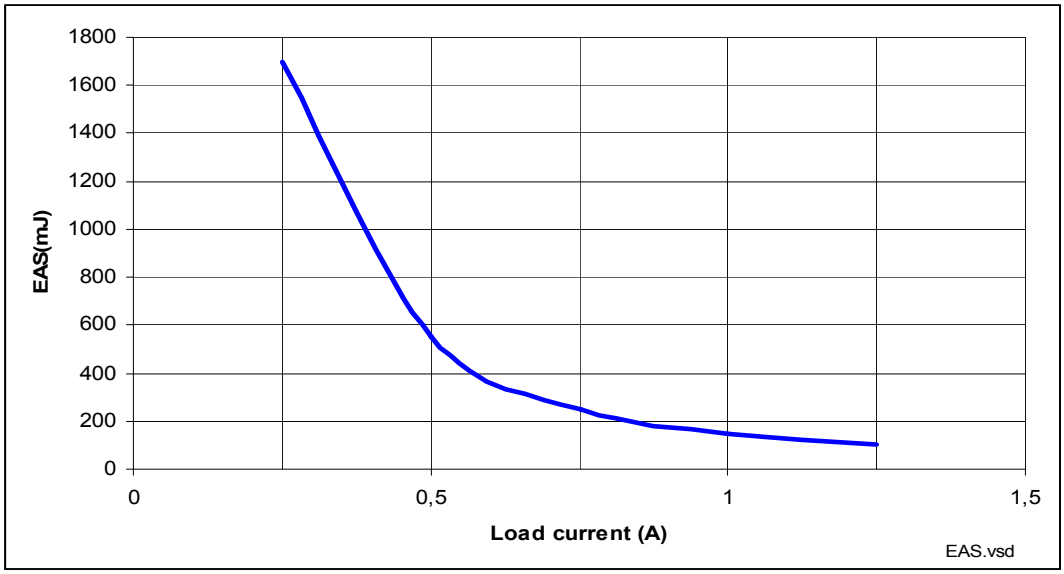


Figure 8 Maximum energy dissipation single pulse, $T_{j,Start}$ = 150 °C; V_S = 13.5V

5.4 Electrical Characteristics Power Stage

Electrical Characteristics: Power stage

V_S = 13.5 V, T_j = -40 °C to +150 °C,(unless otherwise specified). Typical values are given at T_j = 25°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	ON-state resistance per channel	$R_{DS(ON)}$	–	175	–	mΩ	T_j=25°C[1], I_L = 1A, V_{IN}= 5V, See **Figure 4**
			–	280	350		T_j=150°C
5.4.2	Nominal load current	$I_{L(nom)}$	1.3	–	–	A	T_A=85°C[1], T_j <150°C[1]
5.4.3	Drain to Source clamping Voltage $V_{DS(AZ)} = V_S$-V_{OUT}	$V_{DS(AZ)}$	59	63		V	I_{DS} = 4mA[2]
5.4.4	Output leakage current	$I_{L(OFF)}$	–	–	5	µA	V_{IN}=0V
5.4.5	Slew rate ON 10% to 30% V_{OUT}	$dV_{/dtON}$	–	0.7	2	V/µs	R_L=47Ω, V_s=13.5V See **Figure 5**
5.4.6	Slew rate OFF 70% to 40% V_{OUT}	$-dV_{/dtOFF}$	–	0.9	2	V/µs	
5.4.7	Turn-ON time to 90% V_S Includes propagation delay	t_{ON}	–	80	180	µs	
5.4.8	Turn-OFF time to 10% V_S Includes propagation delay	t_{OFF}	–	80	200	µs	
5.4.9	Internal output pull down	R_{PD}		200		kΩ	$V_{OUT(OL)}$ = 4V

1) Not subject to production test, specified by design

2) Voltage is measured by forcing $I_{DS.}$

6 Protection Mechanisms

The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

6.1 Loss of Ground Protection

In case of loss of the module ground, where the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pin. In that case, a maximum $I_{(OUTGND)}$ can flow out of the output.

6.2 Undervoltage Protection

Below V_{SOP_min}, the under voltage mechanism is met. If the supply voltage is below the under voltage mechanism, the device is OFF (turns OFF). As soon as the supply voltage is above the under voltage mechanism, then the device can be switched ON and the protection functions are operational.

6.3 Overvoltage Protection

There is a clamp mechanism for over voltage protection. To guarantee this mechanism operates properly in the application, the current in the zener diode Z_{DAZ} has to be limited by a ground resistor. **Figure 9** shows a typical application to withstand overvoltage issues. In case of supply greater than $V_{S(AZ)}$, the power transistor switches ON and the voltage across logic section is clamped. As a result, the internal ground potential rises to V_S - $V_{S(AZ)}$. Due to the ESD zener diodes, the potential at pin IN rises almost to that potential, depending on the impedance of the connected circuitry. Integrated resistors are provided at the IN pin to protect the input circuitry from excessive current flow during this condition.

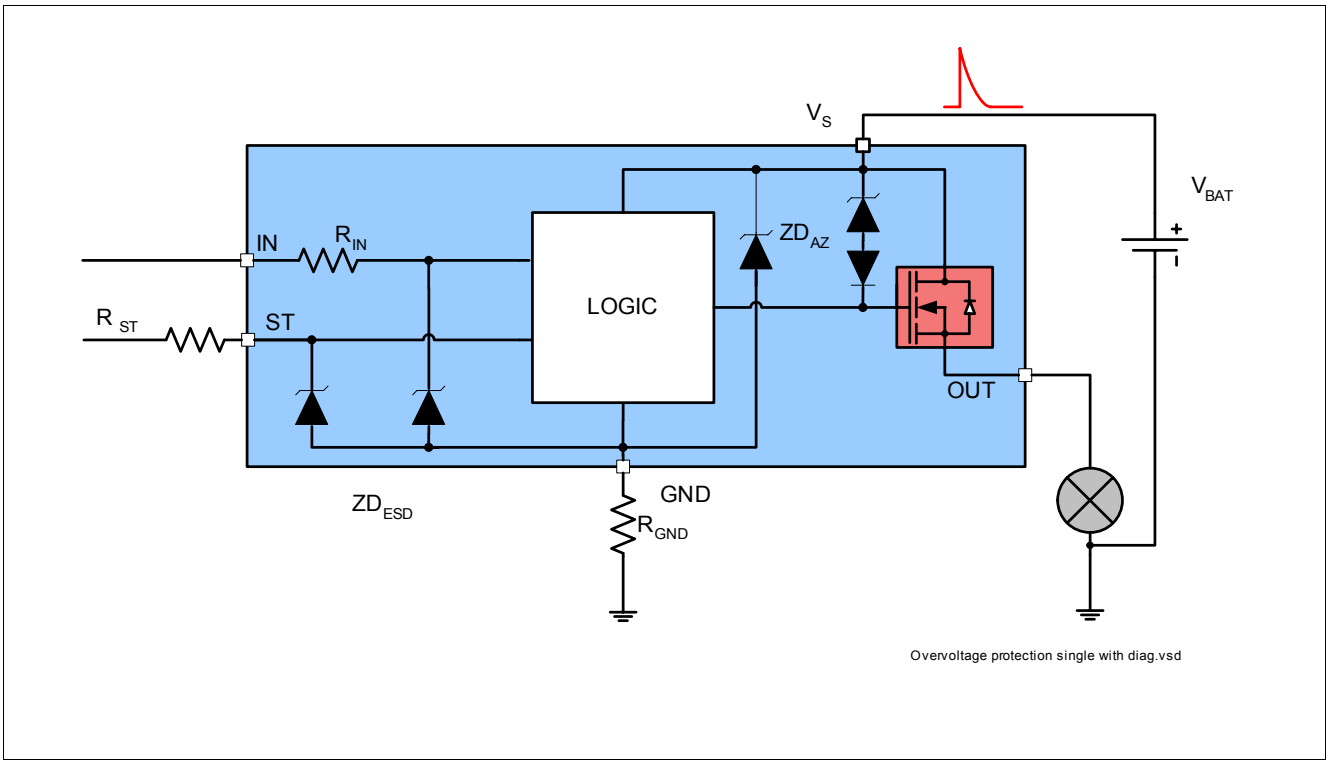


Figure 9 Over voltage protection with external components

In the case the supply voltage is in between of $V_{S(SC)\ max}$ and $V_{DS(AZ)}$, the output transistor is still operational and follow the input. If the channel is in ON state, parameters are no longer warranted and lifetime is reduced compared to normal mode. This specially impacts the short circuit robustness, as well as the maximum energy E_{AS} the device can handle.

6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logical pins has to be limited to the maximum current described in **Chapter 4.1**, sometimes with an external resistor. **Figure 10** shows a typical application. The R_{GND} resistor is used to limit the current in the zener protection of the device. Resistors R_{IN} and R_{ST} is used to limit the current in the logic of the device and in the ESD protection stage. The recommended value for R_{GND} is 150Ω, for $R_{ST\ 0/1}$= 15kΩ. In case the over voltage is not considered in the application, R_{GND} can be replaced by a Shottky diode.

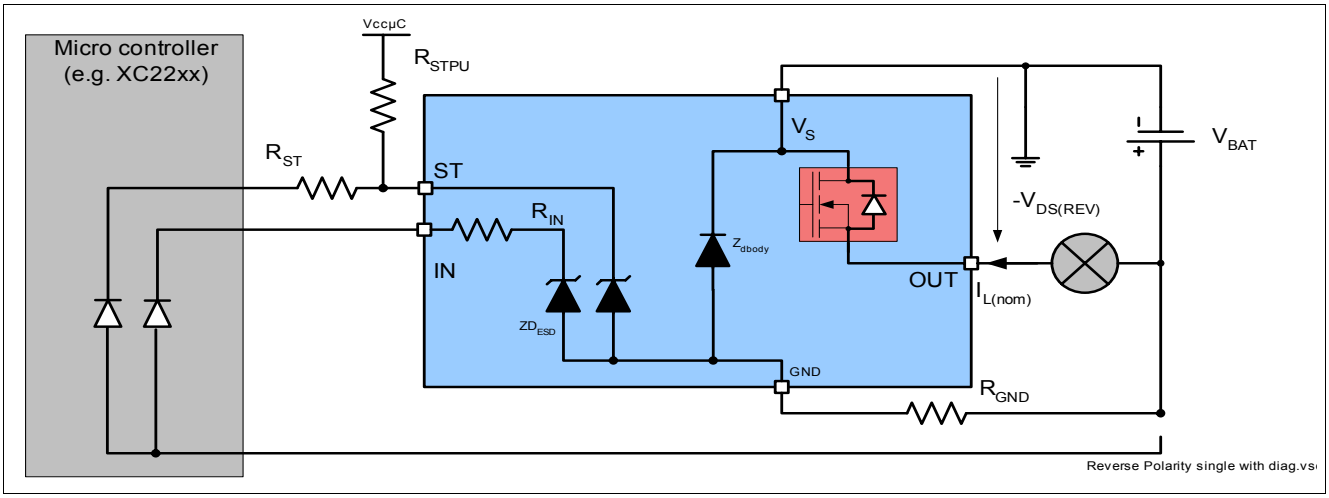


Figure 10 Reverse polarity protection with external components

6.5 Overload Protection

In case of overload, or short circuit to ground, the BTS4175SGA offers two protections mechanisms.

Current limitation

At first step, the instantaneous power in the switch is maintained to a safe level by limiting the current to the maximum current allowed in the switch $I_{L(LIM)}$. During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS.

Thermal protection

At thermal shutdown, the device turns OFF and cools down. A restart mechanism is used, after cooling down, the device restarts and limits the current to $I_{L(SCR)}$. **Figure 11** shows the behavior of the current limitation as a function of time.

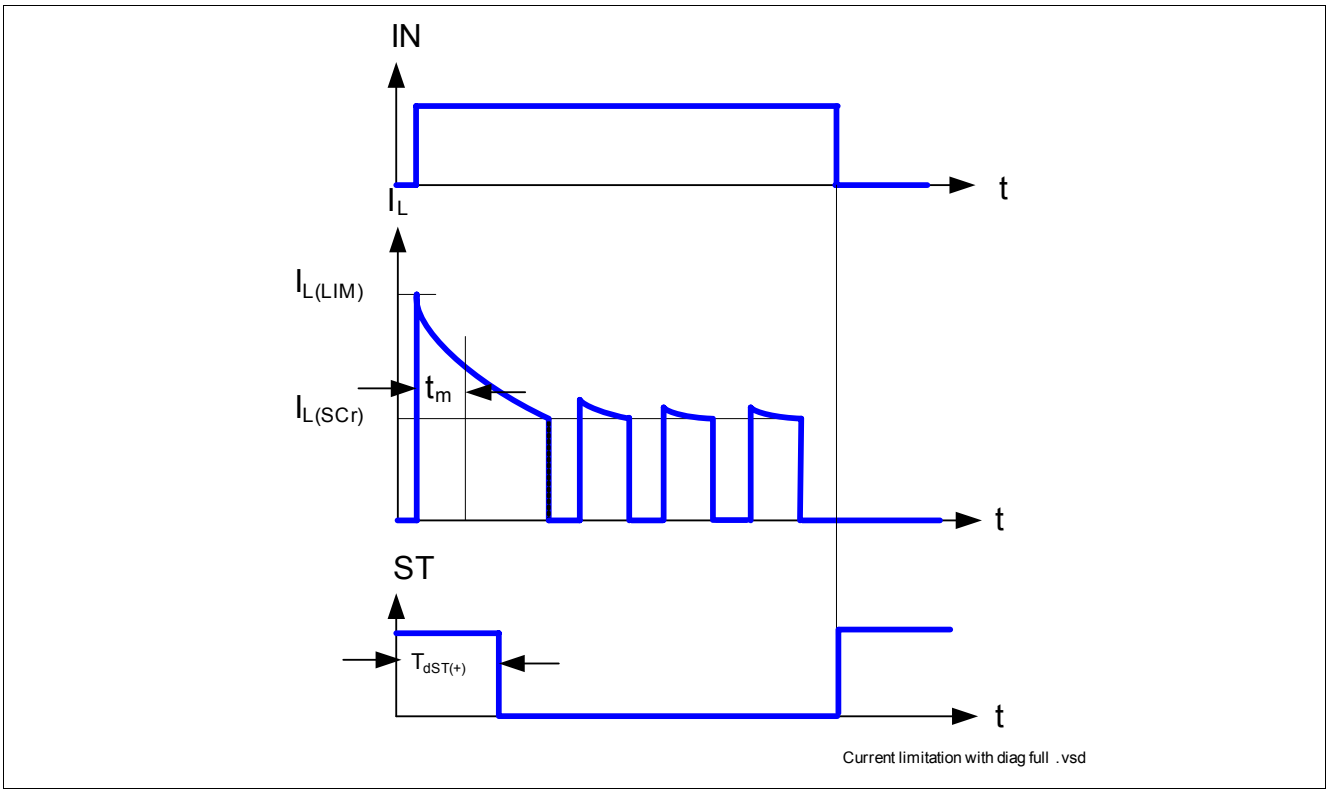


Figure 11 Current limitation function of the time

6.6 Electrical Characteristics Protection Functions

Electrical Characteristics: Protection

V_S = 13.5 V, T_j = -40 °C to +150 °C. Typical values are given at T_j = 25°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reverse polarity							
6.6.1	Drain source diode voltage during reverse polarity	$-V_{DS(REV)}$	–	600	–	mV	T_J = 150°C $V_{OUT} > V_S$
Overvoltage							
6.6.2	Over voltage protection	$V_{S(AZ)}$	62	–	–	V	I_s = 4mA
Overload condition							
6.6.3	Initial peak short circuit current limit (pin 5 to 3) V_S = 20V; t_m = 150µs	$I_{L(LIM)}$	– – 4	– 6.5 –	9 – –	A	T_j = -40°C, T_j = 25°C, T_j = 150°C
6.6.4	Repetitive short circuit current limitation	$I_{L(SCR)}$	–	6.5 4.5	–	A	V_S < 40V[1], V_S > 40V[1]
6.6.5	Thermal shutdown temperature	T_{jSC}	150	–	–	°C	–[1]
6.6.6	Thermal shutdown hysteresis	ΔT_{JT}	–	10	–	K	– [1]

1) Not subject to production test, but specified by design

7 Diagnostic Mechanism

For diagnosis purpose, the BTS4175SGA provides a status pin.

7.1 ST Pin

BTS4175SGA status pin is an open drain, active low circuit. **Figure 12** shows the equivalent circuitry. As long as no “hard” failure mode occurs (Short circuit to GND / Over temperature or open load in OFF), the signal is permanently high, and due to a required external pull-up to the logic voltage will exhibit a logic high in the application. A suggested value for the $R_{PU\ ST}$ is 15kΩ.

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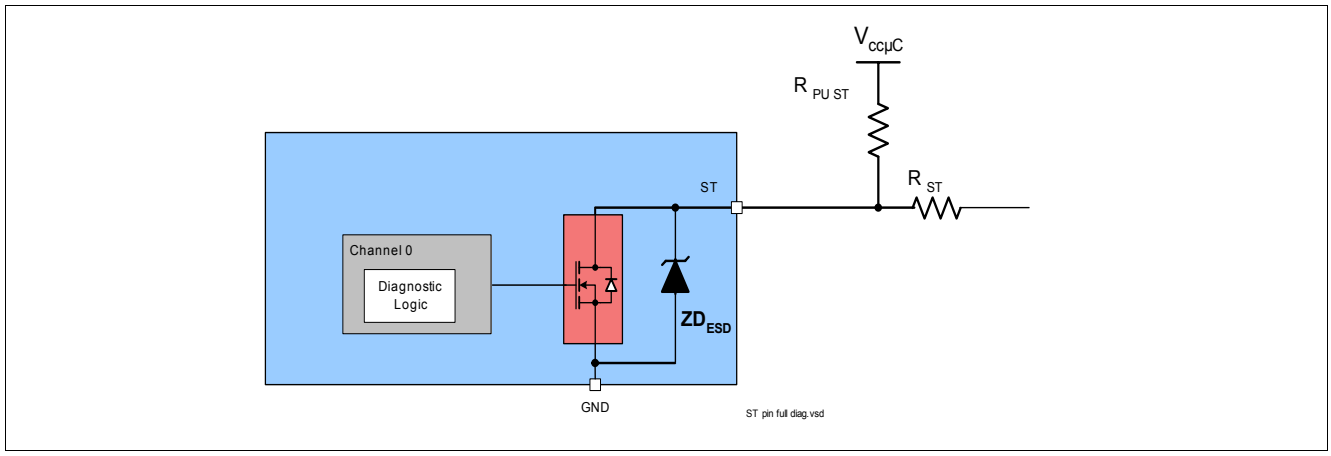

Figure 12 Status output circuitry

7.2 ST Signal in Case of Failures

Table 3 gives a quick reference for the logical state of the ST pin during device operation.

Table 3 ST pin truth table

Device operation	IN	OUT	ST
Normal operation	L	L	H
	H	H	H
Open Load channel	L	> $V_{(OL)}$	L[1)]
	H	H	H
Over temp channel	L	L	H
	H	L	L

1) L if potential at the output exceeds the Openload detection voltage

7.2.1 Diagnostic in Open Load, Channel OFF

For open load diagnosis in OFF-state, an external output pull-up resistor (R_{OL}) is recommended. For calculation of the pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ has to be taken into account. **Figure 13** gives a sketch of the situation and **Figure 14** shows the typical timing diagram.

$I_{leakage}$ defines the leakage current in the complete system, including $I_{L(OFF)}$ (see **Chapter 5.4**) and external leakages e.g due to humidity, corrosion, etc... in the application.

To reduce the stand-by current of the system, an open load resistor switch S_{OL} is recommended.

If the channel is OFF, the output is no longer pulled down by the load and V_{OUT} voltage rises to nearly V_S. This is recognized by the device as open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the ST signal is switched to a logical low V_{STL}.

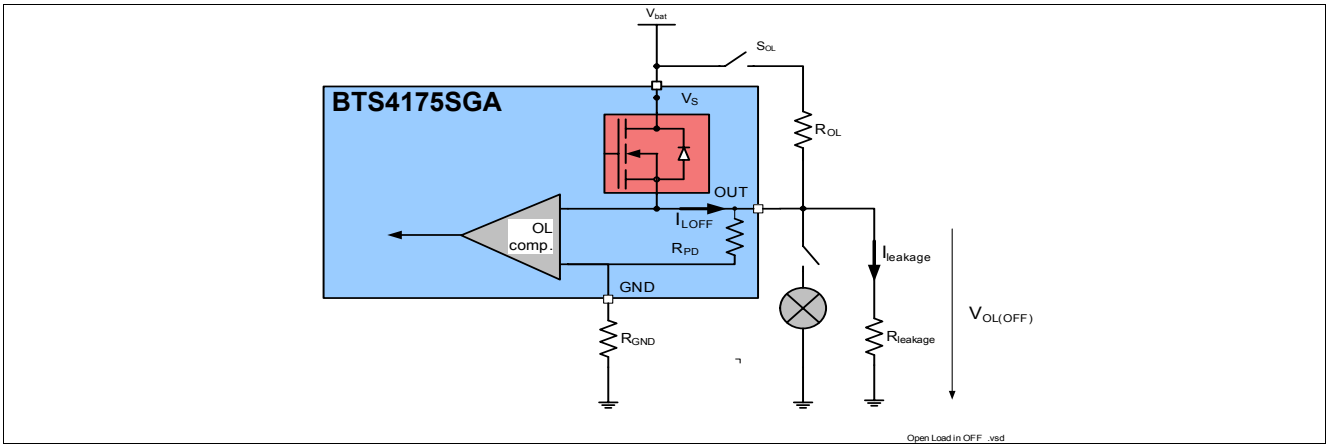

Figure 13 Open load detection in OFF electrical equivalent circuit

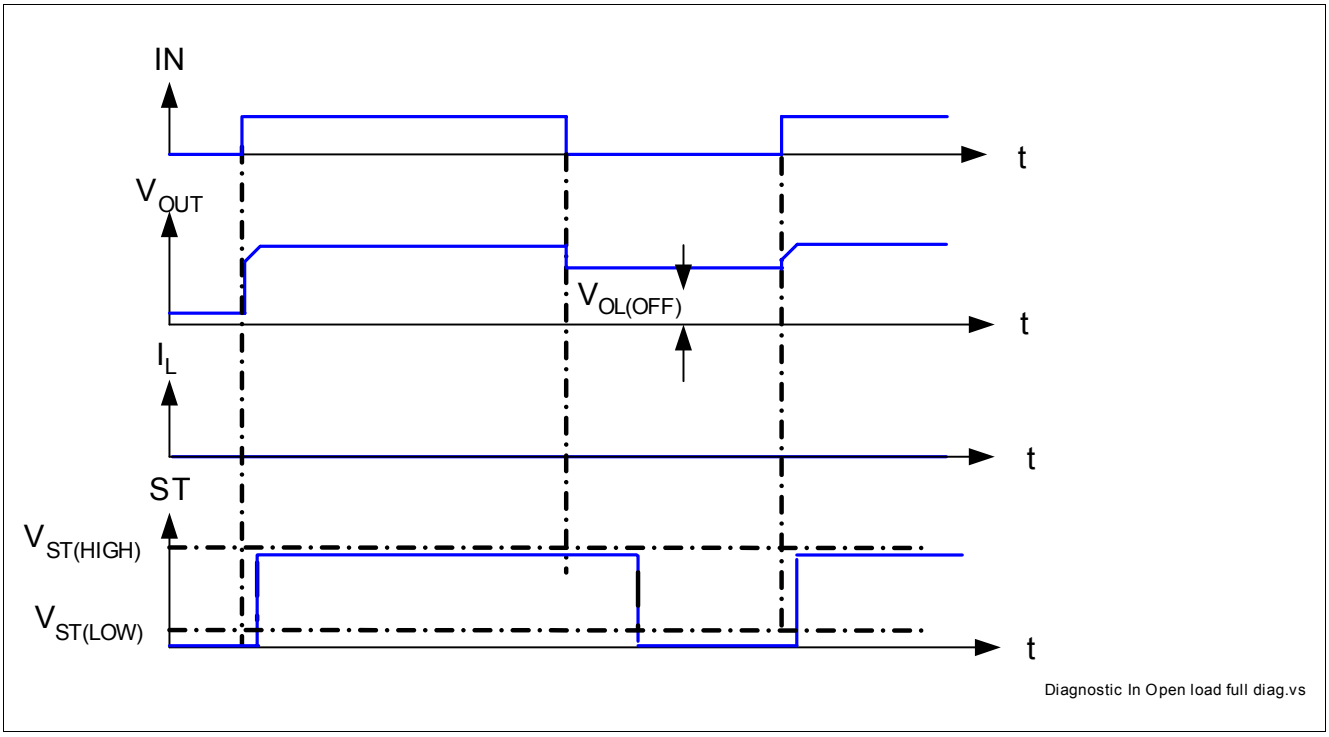

Figure 14 ST in open load condition

7.2.2 ST Signal in case of Over Temperature

In case of over temperature, the junction temperature reaches the thermal shutdown temperature T_{jSC}.

In that case, the ST signal is stable and remains to toggling between $V_{ST(L)}$ and $V_{ST(H)}$. **Figure 15** gives a sketch of the situation.

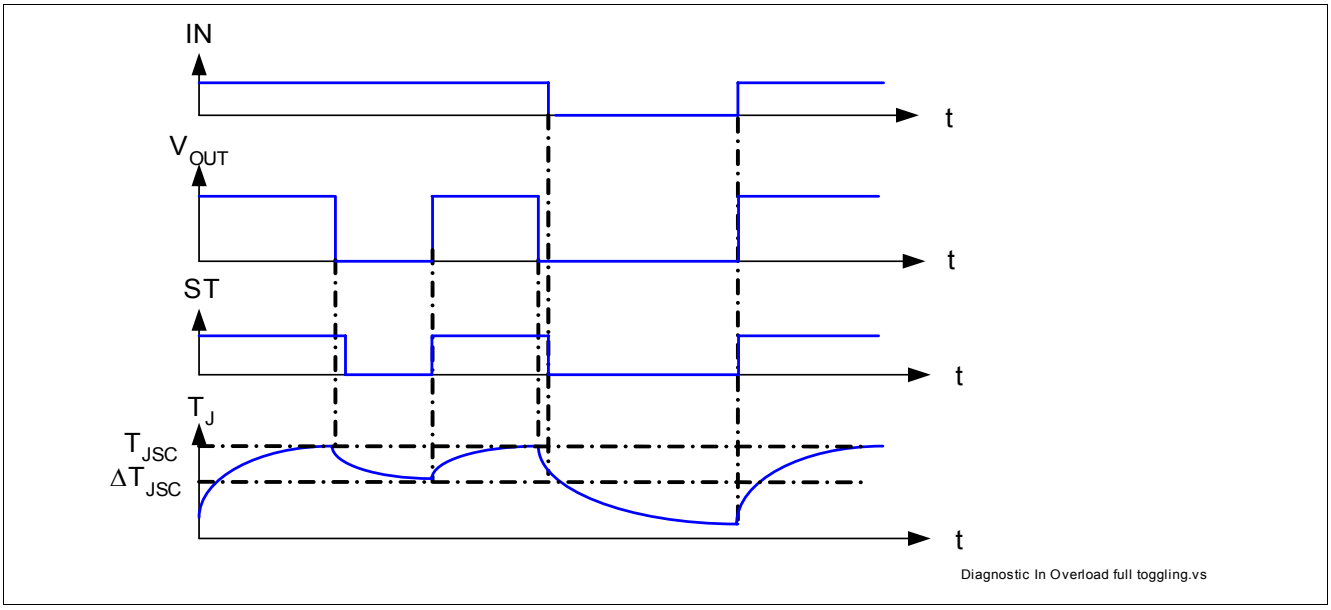

Figure 15 Sense signal in overtemperature condition

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7.3 Electrical Characteristics Diagnostic Functions

Electrical Characteristics: Diagnostics

V_S = 13.5 V, T_j = -40 °C to +150 °C, (unless otherwise specified) Typical values are given at V_s = 13.5V, T_j = 25°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Load condition threshold for diagnostic							
7.3.1	Open Load detection threshold in OFF state[1]	$V_{OL(OFF)}$	–	3.0	4.0	V	V_{IN} = 0V
7.3.1	Short circuit detection voltage	$V_{OUT(SC)}$	–	2.8	–	V	–[3]
ST pin							
7.3.2	Status output (open drain) High level; Zener limit voltage	$V_{ST\ (HIGH)}$	5.4	6.1	–	V	I_{ST} = +1,6mA[2], Zener Limit voltage
7.3.3	Status output (open drain) Low level	$V_{ST\ (LOW)}$	–	–	0.6	V	I_{ST} =+1,6mA[2]
Diagnostic timing							
7.3.4	Status invalid after positive input slope	$t_{dST(+)}$	–	120	160	µs	–[3]
7.3.5	Status invalid after negative input slope	$t_{dST(-)}$	–	250	400	µs	–

1) External pull up resistor required for open load detection in OFF state

2) If ground resistor R_{GND} is used, the voltage drop across this resistor has to be added

3) Not subject to production test, specified by design

8 Input Pin

8.1 Input Circuitry

The input circuitry is CMOS compatible. The concept of the Input pin is to react to voltage transition and not to voltage threshold. With the Schmidt trigger, it is impossible to have the device in an un-defined state, if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in an linear or undefined state. The input circuitry is compatible with PWM applications. **Figure 16** shows the electrical equivalent input circuitry. The pull down current source ensures the channel is OFF with a floating input.

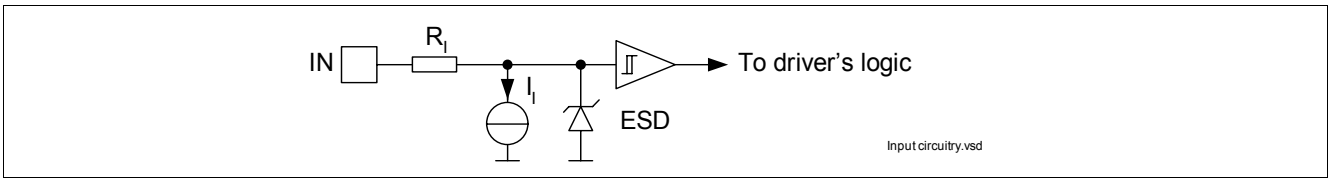

Figure 16 Input pin circuitry

8.2 Electrical Characteristics

Electrical Characteristics: Diagnostics

V_S = 13.5 V, T_j = -40 °C to +150 °C, Typical values are given at V_s = 13.5V, T_j = 25°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
INput pins characteristics							
8.2.1	Low level input voltage	$V_{IN(L)}$	–	–	0.8	V	–[1]
8.2.2	High level input voltage	$V_{IN(H)}$	2.2	–	–	V	–[1]
8.2.3	Input voltage hysteresis	$V_{IN(HYS)}$	–	0.4	–	V	–[2]
8.2.4	Low level input current	$I_{IN(L)}$	1	–	25	µA	V_{IN}= 0,7V
8.2.5	High level input current	$I_{IN(H)}$	3	–	25	µA	V_{IN}= 5V
8.2.6	Input resistance	R_I	2	3.5	5	kΩ	See **Figure 16**

1) If ground resistor R_{GND} is used, the voltage drop across this resistor has to be added

2) Not subject to production test, specified by design

9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

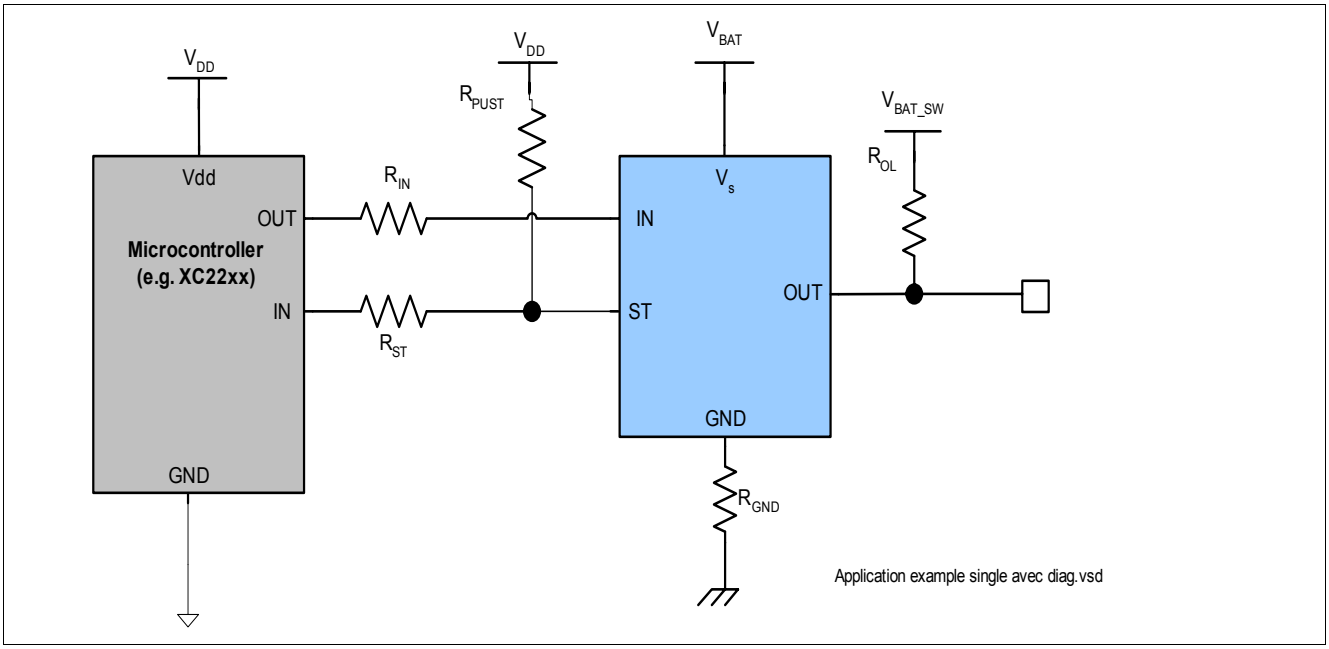

Figure 17 Application diagram with BTS4175SGA

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

9.1 Further Application Information

- For further information you may visit **http://www.infineon.com/**

10 Package Outlines

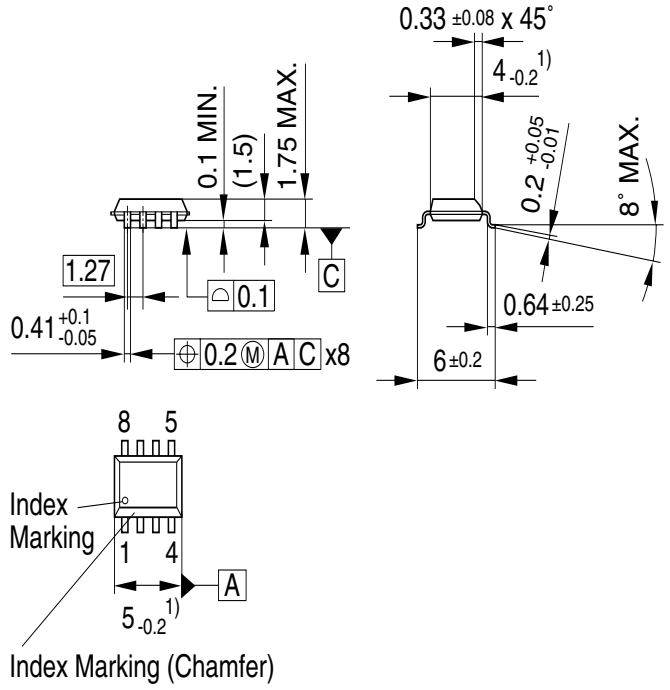

Figure 18 PG-DSO-8-24 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

11 Revision History

Version	Date	Changes
1.0	2008-03-12	Creation of the data sheet

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