Programmable Timing Control Hub™ for Mobile P4™ Systems

Recommended Application:

CK410M Compliant Main Clock with Integrated LCD Spread Spectrum Clock.

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 5 - 0.7V current-mode differential SRC pair for SATA and PCI-E
- 1 - 0.7V current-mode differential CPU/SRC selectable pair
- 4 - PCI (33MHz)
- 2 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 1 - REF, 14.318MHz
- 1 - 0.7V current-mode differential LCD/SRC selectable pair.

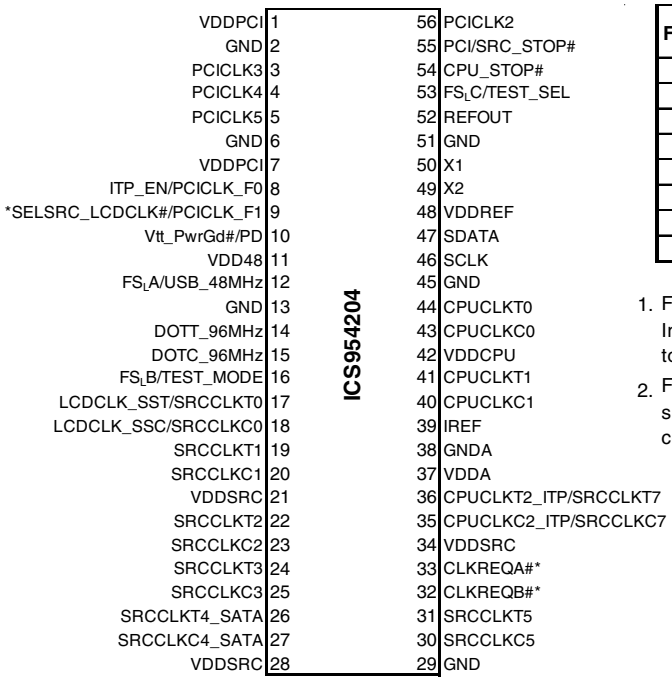
Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks
- +/- 100ppm frequency accuracy on USB clocks

Features/Benefits:

- Supports tight ppm accuracy clocks for Serial-ATA and SRC
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD# for power management.
- CLKREQ pins to support SRC power management.

Pin Configuration



56-pin TSSOP

*100Kohm Pull-Up Resistor

Functionality

FS_C	FS_B	FS_A	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266.67	100.00	33.33	14.318	48.00	96.00
0	0	1	133.33	100.00	33.33	14.318	48.00	96.00
0	1	0	200.00	100.00	33.33	14.318	48.00	96.00
0	1	1	166.67	100.00	33.33	14.318	48.00	96.00
1	0	0	333.33	100.00	33.33	14.318	48.00	96.00
1	0	1	100.00	100.00	33.33	14.318	48.00	96.00
1	1	0	400.00	100.00	33.33	14.318	48.00	96.00
1	1	1	200.00	100.00	33.33	14.318	48.00	96.00

1. FS_C is a three-level input. Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS_B and FS_A are low-threshold inputs. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
2	GND	PWR	Ground pin.
3	PCICLK3	OUT	PCI clock output.
4	PCICLK4	OUT	PCI clock output.
5	PCICLK5	OUT	PCI clock output.
6	GND	PWR	Ground pin.
7	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
8	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality 1 = CPU_ITP pair 0 = SRC pair
9	*SELSRC_LCDCLK#/PCICLK_F1	I/O	Latched input select for LCD_ss/ SRCCLK output frequency: 0 = LCD, 1 = SRCCLK/ 3.3V free-running PCI clock output.
10	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
11	VDD48	PWR	Power pin for the 48MHz output.3.3V
12	FSLA/USB_48MHz	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
13	GND	PWR	Ground pin.
14	DOTT_96MHz	OUT	True clock of differential pair for 96.00MHz DOT clock.
15	DOTC_96MHz	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
16	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
17	LCDCLK_SST/SRCCLKT0	OUT	True clock of LCDCLK_SS output / True clock of SRCCLK differential pair. Selected by SEL_LCDCLK#
18	LCDCLK_SSC/SRCCLKC0	OUT	Complementary clock of LCDCLK_SS output / Complementary clock of SRCCLK differential pair. Selected by SEL_LCDCLK#
19	SRCCLKT1	OUT	True clock of differential SRC clock pair.
20	SRCCLKC1	OUT	Complement clock of differential SRC clock pair.
21	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
22	SRCCLKT2	OUT	True clock of differential SRC clock pair.
23	SRCCLKC2	OUT	Complement clock of differential SRC clock pair.
24	SRCCLKT3	OUT	True clock of differential SRC clock pair.
25	SRCCLKC3	OUT	Complement clock of differential SRC clock pair.
26	SRCCLKT4_SATA	OUT	True clock of differential SRC/SATA pair.
27	SRCCLKC4_SATA	OUT	Complement clock of differential SRC/SATA pair.
28	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal

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Pin Description (Continued)

PIN #	PIN NAME	Type	Pin Description
29	GND	PWR	Ground pin.
30	SRCCLKC5	OUT	Complement clock of differential SRC clock pair.
31	SRCCLKT5	OUT	True clock of differential SRC clock pair.
32	CLKREQB#*	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = enabled, 1 = tri-stated
33	CLKREQA#*	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = enabled, 1 = tri-stated
34	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
35	CPUCLKC2_ITP/SRCCLKC7	OUT	Complementary clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
36	CPUCLKT2_ITP/SRCCLKT7	OUT	True clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
37	VDDA	PWR	3.3V power for the PLL core.
38	GNDA	PWR	Ground pin for the PLL core.
39	IREF	IN	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
40	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
43	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	GND	PWR	Ground pin.
46	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
47	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
48	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
49	X2	OUT	Crystal output, Nominally 14.318MHz
50	X1	IN	Crystal input, Nominally 14.318MHz.
51	GND	PWR	Ground pin.
52	REFOUT	OUT	Reference Clock output
53	FSLC/TEST_SEL	IN	3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
54	CPU_STOP#	IN	Stops all CPUCLK, except those set to be free running clocks
55	PCI/SRC_STOP#	IN	Stops all PCICLKs and SRCCLKs besides the free-running clocks at logic 0 level, when input low
56	PCICLK2	OUT	PCI clock output.

*Pins 32 and 33 have pull-ups.

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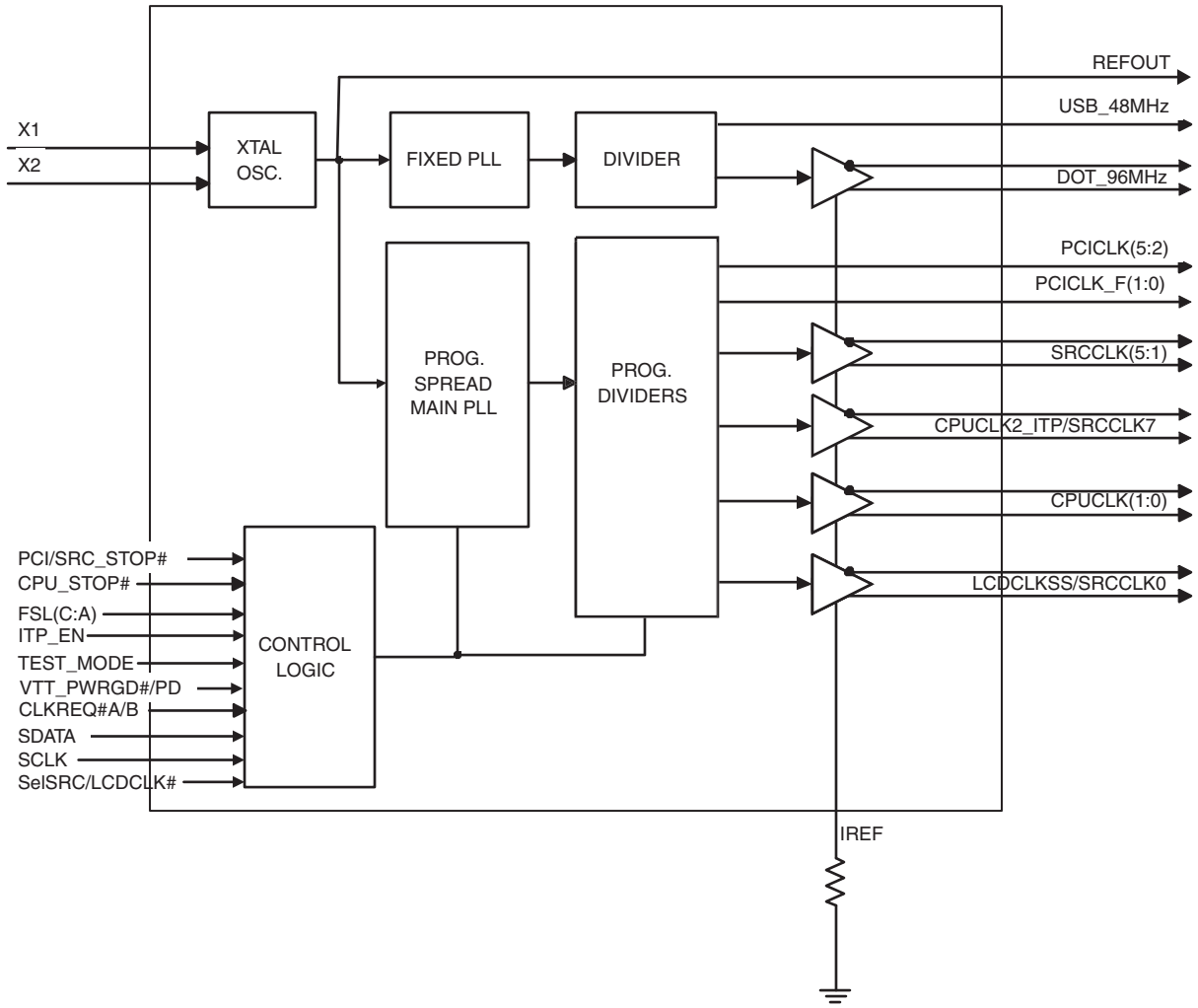
General Description

954204 is a CK410M Compliant clock synthesizer. **954204** provides a single-chip solution for mobile systems built with Intel P4-M processors and Intel mobile chipsets. **954204** is driven with a 14.318MHz crystal and generates CPU outputs up to 400MHz. It provides the tight ppm accuracy required by Serial ATA and PCI-Express.

Block Diagram



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General SMBus serial interface information for the 954204

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X***
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
○		
○		○
○		○
		○
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
	X Byte		Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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Absolute Max

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		V_{DD} + 0.5V	V
VDD_In	3.3V Logic Input Supply Voltage	GND - 0.5	V_{DD} + 0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input Low Voltage		3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;		275	400	mA	
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven		64	70	mA	
		all differential pairs tri-stated		5	12	mA	
Input Frequency[3]	F_i	V_{DD} = 3.3 V		14.31818		MHz	3
Pin Inductance[1]	L_{pin}				7	nH	1
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization[1,2]	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock		1.3	1.8	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_SRC		SRC output enable after PCI_STOP de-assertion			10	ns	1
Tdrive_PD		Differential output enable after PD# de-assertion			300	us	1
Tfall_PD		PD# fall time of			5	ns	1
Trise_PD		PD# rise time of			5	ns	2
Tdrive_CPU_STOP		CPU output enable after CPU_STOP de-assertion			10	ns	1
Tfall_CPU_STOP		CPU_STOP fall time of			5	ns	1
Trise_CPU_STOP#		CPU_STOP rise time of			5	ns	2
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	SDATA, SCLK @ I_{PULLUP}			0.4	V	1
Current sinking	I_{PULLUP}	V_{OL} = 0.4 V	4			mA	1
SCLK/SDATA	T_{RI2C}	(Max VIL - 0.15) to			1000	ns	1,3
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1,3

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet

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Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	750	850	mV	1,3
Voltage Low	VLow		-150	0	150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		790	1150	mV	1
Min Voltage	Vuds		-300	0			1
Crossing Voltage (abs)	Vcross(abs)		250	390	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		50	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	T_{period}	400MHz non-spread	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz non-spread	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz non-spread	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz non-spread	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz non-spread	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz non-spread	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		5.4000	ns	2
		100.00MHz non-spread	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min/max period	T_{abs}	400MHz non-spread	2.4143		2.5750	ns	1,2
		400MHz spread			2.5983	ns	1,2
		333.33MHz non-spread	2.9141		3.0859	ns	1,2
		333.33MHz spread			3.1010	ns	1,2
		266.66MHz non-spread	3.6639		3.8361	ns	1,2
		266.66MHz spread			3.8550	ns	1,2
		200MHz non-spread	4.9135		5.0865	ns	1,2
		200MHz spread			5.1116	ns	1,2
		166.66MHz non-spread	5.9132		6.0868	ns	1,2
		166.66MHz spread			6.1170	ns	1,2
		133.33MHz non-spread	7.4128		7.5873	ns	1,2
		133.33MHz spread			7.6250	ns	1,2
		100.00MHz non-spread	9.9120		10.0880	ns	1,2
		100.00MHz spread			10.1383	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	310	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	305	700	ps	1
Rise Time Variation	d-t_r			20	125	ps	1
Fall Time Variation	d-t_f			15	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50	55	%	1
Skew	t_{sk3}	CPU(1:0), V_T = 50%		20	100	ps	1
		CPU2_ITP, V_T = 50%		90	150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Differential waveform measurement, CPU(1:0)		35	85	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Differential waveform measurement, CPU2_ITP		45	125	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope	660	750	850	mV	1,3
Voltage Low	VLow		-150	0	150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		790	1150	mV	1
Min Voltage	Vuds		-300	0			1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see T_{period} min-max values	-300		300	ppm	1,2
Average period	T_{period}	100.00MHz non-spread	9.9970		10.0030	ns	2
		100.00MHz spread			10.0533	ns	2
Absolute min/max period	T_{abs}	100.00MHz non-spread	9.8720		10.1280	ns	1,2
		100.00MHz spread			10.1783	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	308	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V, V_{OL} = 0.175V	175	310	700	ps	1
Rise Time Variation	d-t_r			30	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50	55	%	1
Skew	t_{sk3}	V_T = 50%		100	250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom		40	125	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - LCD_SS 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope	660	750	850	mV	1,2
Voltage Low	VLow		-150	0	150		1,2
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		790	1150	mV	1
Min Voltage	Vuds		-300	0			1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	308	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V, V_{OL} = 0.175V	175	310	700	ps	1
Rise Time Variation	d-t_r			30	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50	55	%	1
Skew	t_{sk3}	V_T = 50%		100	250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom		40	125	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - PCICLK/PCICLK_F

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	33.33MHz output non-spread	29.9910		30.0090	ns	2
		33.33MHz output spread			30.1598	ns	2
Absolute min/max period	T_{abs}	33.33MHz output non-spread	29.4910		30.5090	ns	1,2
		33.33MHz output spread			30.6598	ns	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-33			mA	1
		V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30			mA	1
		V_{OL} = 0.4 V			38	mA	1
Edge Rate		Rising edge rate	1	1.37	4	V/ns	1
Edge Rate		Falling edge rate	1	1.6	4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50	55	%	1
Skew	t_{sk1}	V_T = 1.5 V		50	500	ps	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V		95	500	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - 48MHz, USB

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00000 MHz output	20.83125		20.83542	ns	2
Absolute min/max period	T_{abs}	48.00000 MHz output	20.4813		21.1854	ns	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-29			mA	1
		V_{OH} = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	29			mA	1
		V_{OL} = 0.4 V			27	mA	1
Edge Rate		Rising edge rate	1	1.8	2	V/ns	1
Edge Rate		Falling edge rate	1	1.6	2	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.43	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.33	2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	48	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		150	350	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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Electrical Characteristics - DOT, 96MHz 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope	660	790	850	mV	1,3
Voltage Low	VLow		-150	0	150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		810	1150	mV	1
Min Voltage	Vuds		-300	0			1
Crossing Voltage (abs)	Vcross(abs)		250	400	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		10	140	mV	1
Long Accuracy	ppm	see T_{period} min-max values	-100		100	ppm	1,2
Average period	T_{period}	96.00MHz	10.4135		10.4198	ns	2
Absolute min/max period	T_{abs}	96.00MHz	10.1635		10.6698	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	250	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V, V_{OL} = 0.175V	175	240	700	ps	1
Rise Time Variation	d-t_r			15	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom		90	250	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - REF-14.318MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-33				
		V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30			mA	1
		V_{OL} = 0.4 V			38	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1	2	ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	53	55	%	1,2
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V		750	1000	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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SMBus Table: Output Enable Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	35, 36	CPUCLK2_ITP/SRCCLK7 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 6	-	Reserved					1
Bit 5	30, 31	SRCCLK5 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 4	26, 27	SRCCLK4/SATA Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 3	24, 25	SRCCLK3 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 2	22, 23	SRCCLK2 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 1	19, 20	SRCCLK1 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 0	17, 18	SRCCLK0 Enable	Output Enable	RW	Disable (HiZ)	Enable	1

SMBus Table: PLL1 Spread and Output Enable Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	8	PCI_F0 Enable	Output Enable	RW	Disable	Enable	1
Bit 6	14,15	DOT_96MHz Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 5	12	USB_48MHz Enable	Output Enable	RW	Disable	Enable	1
Bit 4	52	REFOUT Enable	Output Enable	RW	Disable	Enable	1
Bit 3	-	Reserved					-
Bit 2	41, 40	CPU_1 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 1	44, 43	CPU_0 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 0	-	Spread Spectrum Mode (CPU, SRC, PCIF, PCI)	Spread Control for PLL1	RW	SPREAD OFF	SPREAD ON	0

SMBus Table: Output Enable Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	5	PCICLK5	Output Enable	RW	Disable	Enable	1
Bit 6	4	PCICLK4	Output Enable	RW	Disable	Enable	1
Bit 5	3	PCICLK3	Output Enable	RW	Disable	Enable	1
Bit 4	56	PCICLK2	Output Enable	RW	Disable	Enable	1
Bit 3		Reserved					1
Bit 2		Reserved					1
Bit 1		Reserved					1
Bit 0	9	PCI_F1 Enable	Output Enable	RW	Disable	Enable	1

SMBus Table: SRC Free-Running Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	35, 36	SRCCLK7	Free-Running Control	RW	Free-Running	Stoppable	0
Bit 6	-	Reserved					0
Bit 5	30, 31	SRCCLK5	Free-Running Control, not affected by PCI/SRC_STOP#	RW	Free-Running	Stoppable	0
Bit 4	26, 27	SRCCLK4/SATA		RW	Free-Running	Stoppable	0
Bit 3	24, 25	SRCCLK3		RW	Free-Running	Stoppable	0
Bit 2	22, 23	SRCCLK2		RW	Free-Running	Stoppable	0
Bit 1	19, 20	SRCCLK1		RW	Free-Running	Stoppable	0
Bit 0	17, 18	SRCCLK0		RW	Free-Running	Stoppable	0

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SMBus Table: DOT PD Mode and Output Free-Running Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					0
Bit 6	14, 15	DOT_96MHz Power Down Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 5		Reserved					0
Bit 4	9	PCICLK_F1	Free-Running Control, not affected by PCI/SRC_STOP#	RW	Free-Running	Stoppable	0
Bit 3	8	PCICLK_F0		RW	Free-Running	Stoppable	0
Bit 2	35, 36	CPUCLK_2	Free-Running Control, not affected by CPU_STOP#	RW	Free-Running	Stoppable	1
Bit 1	40, 41	CPUCLK_1		RW	Free-Running	Stoppable	1
Bit 0	43, 44	CPUCLK_0		RW	Free-Running	Stoppable	1

SMBus Table: Output Mode Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	17-20, 22-27, 30, 31, 35, 36	SRC(7:0) PCI/SRC_STOP# Drive Mode	Driven in PCI/SRC_STOP#	RW	Driven	Hi-Z	0
Bit 6	35, 36	CPUCLK2_ITP CPU_STOP# Drive Mode	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 5	40, 41	CPUCLK_1 CPU_STOP# Drive Mode	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 4	43, 44	CPUCLK_0 CPU_STOP# Drive Mode	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 3	17-20, 22-27, 30, 31, 35, 36	SRC(7:0), 96MHz_SS PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 2	35, 36	CPUCLK2_ITP PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 1	40, 41	CPUCLK_1 PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 0	43, 44	CPUCLK_0 PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0

SMBus Table: Test Mode, FS Readback, and PCI Stop# Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Test Mode Selection (Active only when B6b6 = 1)	Test Mode Selection	RW	Hi-Z	REF/N	0
Bit 6	-	Test Clock Mode Entry	Test Mode	RW	Normal Operation	Test Mode per B6b7	0
Bit 5		Reserved					-
Bit 4	52	REFOUT STRENGTH	Strength Prog	RW	1X	2X	1
Bit 3	-	PCI/SRC_STOP#	Stop all PCI and SRC clocks	RW	Outputs Stopped	Outputs Active	1
Bit 2	53	FS_C	Readback	RW	-	-	LATCHED
Bit 1	16	FS_B	Readback	RW	-	-	LATCHED
Bit 0	12	FS_A	Readback	RW	-	-	LATCHED

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SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	x
Bit 6	-	RID2		R	-	-	x
Bit 5	-	RID1		R	-	-	x
Bit 4	-	RID0		R	-	-	x
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Clock Request Control Register

Byte 8	Pin #	Name	Control	Type	0	1	PWD
Bit 7	-	Reserved					-
Bit 6	32	CLKREQB# Control	SRCCLK5 is controlled	RW	Not Controlled	Controlled	1
Bit 5	32	CLKREQB# Control	SRCCLK3 is controlled	RW	Not Controlled	Controlled	0
Bit 4	32	CLKREQB# Control	SRCCLK1 is controlled	RW	Not Controlled	Controlled	0
Bit 3	-	Reserved					-
Bit 2	33	CLKREQA# Control	SRCCLK4 is controlled	RW	Not Controlled	Controlled	1
Bit 1	33	CLKREQA# Control	SRCCLK2 is controlled	RW	Not Controlled	Controlled	0
Bit 0	33	CLKREQA# Control	SRCCLK0 is controlled	RW	Not Controlled	Controlled	0

SMBus Table: LCDCLK_SS Control Register

Byte 9	Pin #	Name	Control	Type	0	1	PWD
Bit 7	17,18	LCDCLK_SS3	Bit S3	RW	See LCDCLK_SS Frequency Select Table 2		0
Bit 6		LCDCLK_SS2	Bit S2	RW			1
Bit 5		LCDCLK_SS1	Bit S1	RW			1
Bit 4		LCDCLK_SS0	Bit S0	RW			1
Bit 3	9	*SEL SRC_LCDCLK#	Select LCDCLK_SS/SRCCLK0	R	LCDCLK	SRCCLK0	-
Bit 2	17, 18	LCDCLK_SS/SRCCLK0 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 1	17, 18	LCDCLK_SS Spread Enable	Enable SS	RW	OFF	ON	1
Bit 0	-	Reserved					0

Table 2: LCDCLK_SS Frequency Select

Byte9/ bit1	S3	S2	S1	S0	Pin 17/18 MHz	Spread %	Spread Type
0	X	X	X	X	100.00	-	-
1	0	0	0	0	100.00	0.8	Down
1	0	0	0	1	100.00	1	Down
1	0	0	1	0	100.00	1.25	Down
1	0	0	1	1	100.00	1.5	Down
1	0	1	0	0	100.00	1.75	Down
1	0	1	0	1	100.00	2	Down
1	0	1	1	0	100.00	2.5	Down
1	0	1	1	1	100.00	3	Down
1	1	0	0	0	100.00	+/-0.3	Center
1	1	0	0	1	100.00	+/-0.4	Center
1	1	0	1	0	100.00	+/-0.5	Center
1	1	0	1	1	100.00	+/-0.6	Center
1	1	1	0	0	100.00	+/-0.8	Center
1	1	1	0	1	100.00	+/-1.0	Center
1	1	1	1	0	100.00	+/-1.25	Center
1	1	1	1	1	100.00	+/-1.5	Center

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Table 3. Power-Up CLKREQ# Timing[1]

Symbol	Parameter	Min	Max	Units
T_{PVCRL}	Power Valid to CLKREQ# Output Active (Fig. 1)		100	µs
$T_{SRCSTBL}$	SRC Clock Stablilzation Time from assertion of CLKREQ# (Fig. 1)		800	µs

[1]This timing is valid only after system clocks are stable.

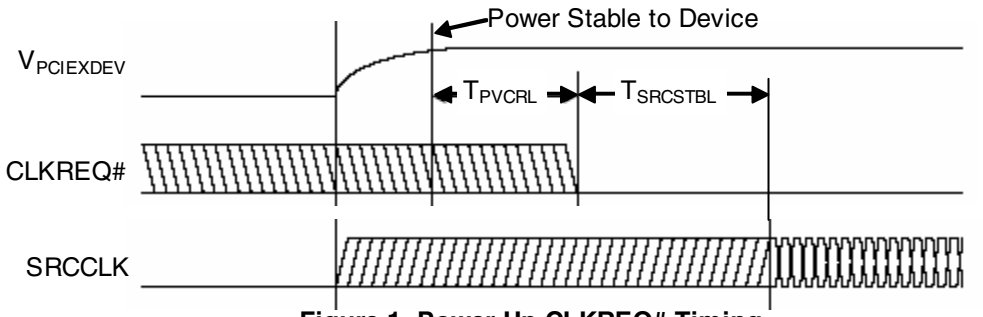

Figure 1. Power-Up CLKREQ# Timing

Table 4. CLKREQ# Control Timing

Symbol	Parameter	Min	Max	Units
T_{CRHoff}	CLKREQ# De-asserted High to SRCCLK Parked (Fig. 2)	0		µs
T_{CRHon}	CLKREQ# Asserted LOW to SRCCLK Active (Fig. 2)		0.4	µs

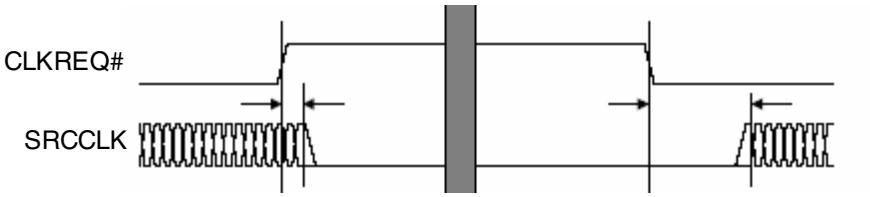

Figure 2. CLKREQ# Control Timing

CLKREQ# - Assertion (transition from logic "1" to logic "0")
The impact of asserting the CLKREQ# pin is that the SRCCLK output will become active per the timing found in Table 4. The clock will become active in a glitch free manner, providing a full cycle at the time it becomes active.

CLKREQ# - De-Assertion (transition from logic "0" to logic "1")

The impact of asserting the CLKREQ# pin is that the SRCCLK output will become inactive setliing in the Tristate condition per the timing found in Table 4. The clock will become inactive in a glitch free manner.

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Table 5: PCI_STOP# Functionality

PCI_STOP#	CPU	CPU#	SRC	SRC#	PCIF/PCI	DOT	DOT#	USB	REF
0	Normal	Normal	Normal	Normal	33MHz	Normal	Normal	48MHz	14.318MHz
1	Normal	Normal	Iref*6 or Float	Low	Low	Normal	Normal	48MHz	14.318MHz

Table 6: PD Functionality

PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	DOT	DOT#	USB	REF
0	Normal	Normal	Normal	Normal	33MHz	Normal	Low	48MHz	14.318MHz
1	Iref*2 or Float	Float	Iref*2 or Float	Float	Low	Iref*2 or Float	Float	Low	Low

Table 7: Tristate CPU Clock Control Truth Table

Signal	PD	CPU_STOP#	CPU_STOP Tristate BIT	PD Tristate BIT	NON-STOP OUTPUTS	STOPPABLE OUTPUTS
	10	54	B5b[6, 5, 4]	B5b[2,1,0]		
CPU[2:0]	0	1	X	X	Running	Running
CPU[2:0]	0	0	0	X	Running	Driven @ I_{REF} X6
CPU[2:0]	0	0	1	X	Running	Tristate
CPU[2:0]	1	X	X	1	Driven @ I_{REF} X2	Driven @ I_{REF} X2
CPU[2:0]	1	X	X	0	Tristate	Tristate

Table 8: Tristate SRC Clock Control Truth Table

Signal	PD	PCI/SRC_STOP#	PCI/SRC_STOP Tristate BIT	PD Tristate BIT	NON-STOP OUTPUTS	STOPPABLE OUTPUTS
	10	55	B5b7	B5b3		
SRC	0	1	X	X	Running	Running
SRC	0	0	0	X	Running	Driven @ IREF X6
SRC	0	0	1	X	Running	Tristate
SRC	1	X	X	1	Driven @ I_{REF} X2	Driven @ I_{REF} X2
SRC	1	X	X	0	Tristate	Tristate

Table 9: Tristate DOT Clock Control Truth Table

Signal	PD	PD Tristate BIT	STOPPABLE OUTPUTS
	10	B4b6	
DOT_96	0	X	Running
DOT_96	1	1	Driven @ I_{REF} X2
DOT_96	1	0	Tristate

Table10: CLKREQ# Clock Control Truth Table

Signal	PD	PCI/SRC_STOP#	CLKREQA# CLKREQB#	SELECTED OUTPUTS
	10	55	33, 32	
SRC	0	1	0	Running
SRC	0	1	1	Tristate
SRC	0	0	0	Tristate
SRC	0	0	1	Stopped per B5b7
SRC	1	X	X	Stopped per B5b3

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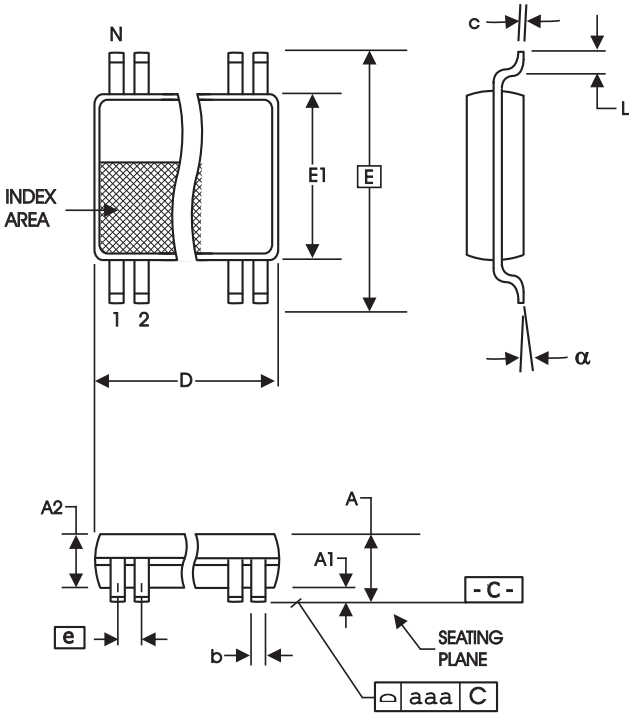

56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

954204CGLFT

Example:

XXXX C G Lx T

Designation for tape and reel packaging
Lead Option (optional)

LF = Lead Free
LN = Lead Free Annealed

Package Type
G = TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

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Revision History

11/21/2017	Rebranded datasheet with "IDT" logo, added company information and legal disclaimer.

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