CS4271

24-Bit, 192 kHz Stereo Audio CODEC

D/A Features

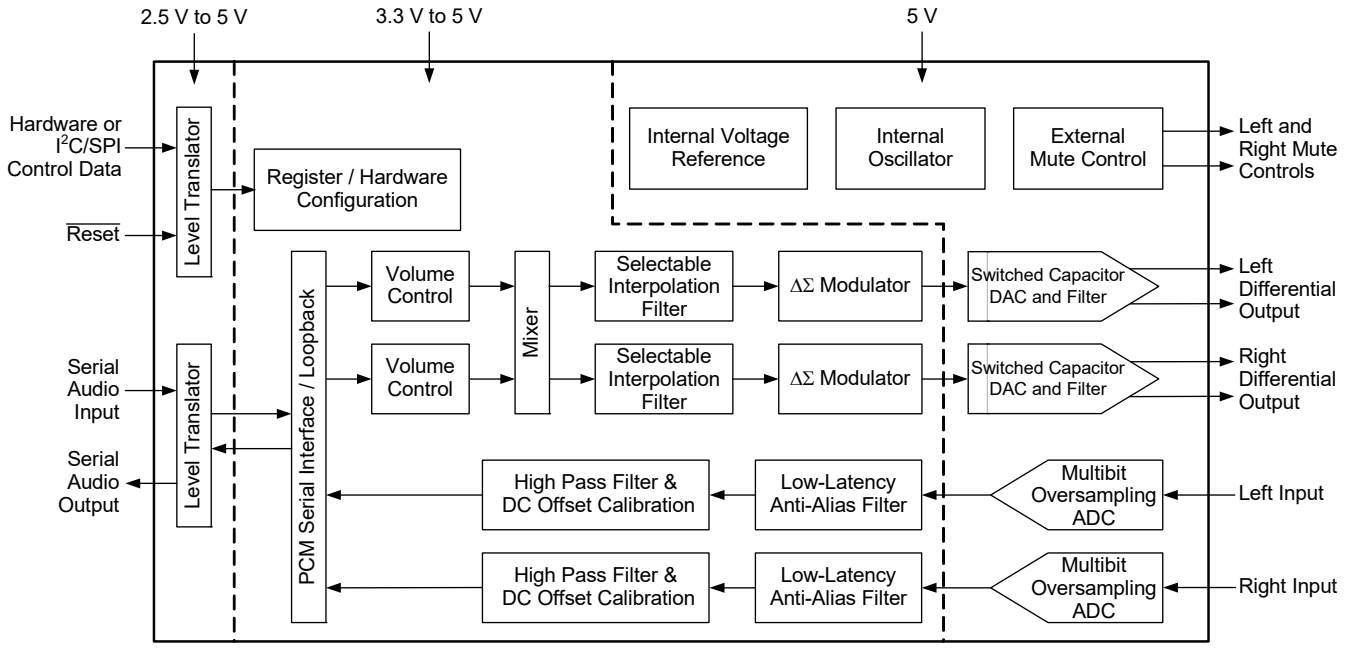
- High Performance
  - 114 dB Dynamic Range
  - -100 dB THD+N
- Up to 192 kHz Sampling Rates
- Differential Analog Architecture
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-free Transitions
- Selectable Digital Filters
  - Fast and Slow Roll Off
- ATAPI Mixing Functions
- Selectable Serial Audio Interface Formats
  - Left Justified up to 24-bit
  - I^2S up to 24-bit
  - Right Justified 16-, 18-, 20-, and 24-Bit
- Control Output for External Muting
- Selectable 50/15 μs De-emphasis

A/D Features

- High Performance
  - 108 dB Dynamic Range
  - -98 dB THD+N
- Up to 192 kHz Sampling Rates
- Single-Ended Analog Architecture
- Multi-bit Delta Sigma Conversion
- High-pass Filter or DC Offset Calibration
- Low-Latency Digital Anti-alias Filtering
- Automatic Dithering of 16-bit Data
- Selectable Serial Audio Interface Formats
  - Left Justified up to 24-bit
  - I^2S up to 24-bit

System Features

- Direct Interface with 5V to 2.5V Logic Levels
- Internal Digital Loopback
- On-chip Oscillator
- Stand-Alone or Control Port Functionality



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Stand-Alone Mode Feature Set

- System Features
  - Serial Audio Port Master or Slave Operation
  - Internal Oscillator for Master Clock
- D/A Features
  - Auto-mute on Static Samples
  - 44.1 kHz 50/15 μs De-emphasis Available
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit
- A/D Features
  - Automatic Dithering for 16-bit Data
  - High-pass Filter
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit

Software Mode Feature Set

- System Features
  - Serial Audio Port Master or Slave Operation
  - Internal Oscillator for Master Clock
  - Internal Digital Loopback Available
- D/A Features
  - Selectable Auto-mute
  - Selectable Interpolation Filters
  - Selectable 32-, 44.1-, and 48-kHz De-emphasis Filters
  - Configurable ATAPI Mixing Functions
  - Configurable Volume and Muting Controls
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit
    - Right Justified 16, 18, 20, and 24-bit
- A/D Features
  - Selectable Dithering for 16-bit Data
  - Selectable High-pass Filter or DC Offset Calibration
  - Selectable Serial Audio Interface Formats
    - Left Justified up to 24-bit
    - I^2S up to 24-bit

General Description

The CS4271 is a high-performance, integrated audio CODEC. The CS4271 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

The D/A offers a volume control that operates with a 1 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

The D/A's integrated digital mixing functions allow a variety of output configurations ranging from a channel swap to a stereo-to-mono downmix.

Standard 50/15 μs de-emphasis is available for sampling rates of 32, 44.1, and 48 kHz for compatibility with digital audio programs mastered using the 50/15 μs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4271 and other devices operating over a wide range of logic levels.

An on-chip oscillator eliminates the need for an external crystal oscillator circuit. This can reduce overall design cost and conserve circuit board space. The CS4271 automatically uses the on-chip oscillator in the absence of an applied master clock, making this feature easy to use.

Independently addressable high-pass filters are available for the right and left channel of the A/D. This allows the A/D to be used in a wide variety of applications where one audio channel and one DC measurement channel is desired.

The CS4271's wide dynamic range, negligible distortion, and low noise make it ideal for applications such as A/V receivers, DVD-R, CD-R, digital mixing consoles, effects processors, set-top box systems, and automotive audio systems.

Ordering Information

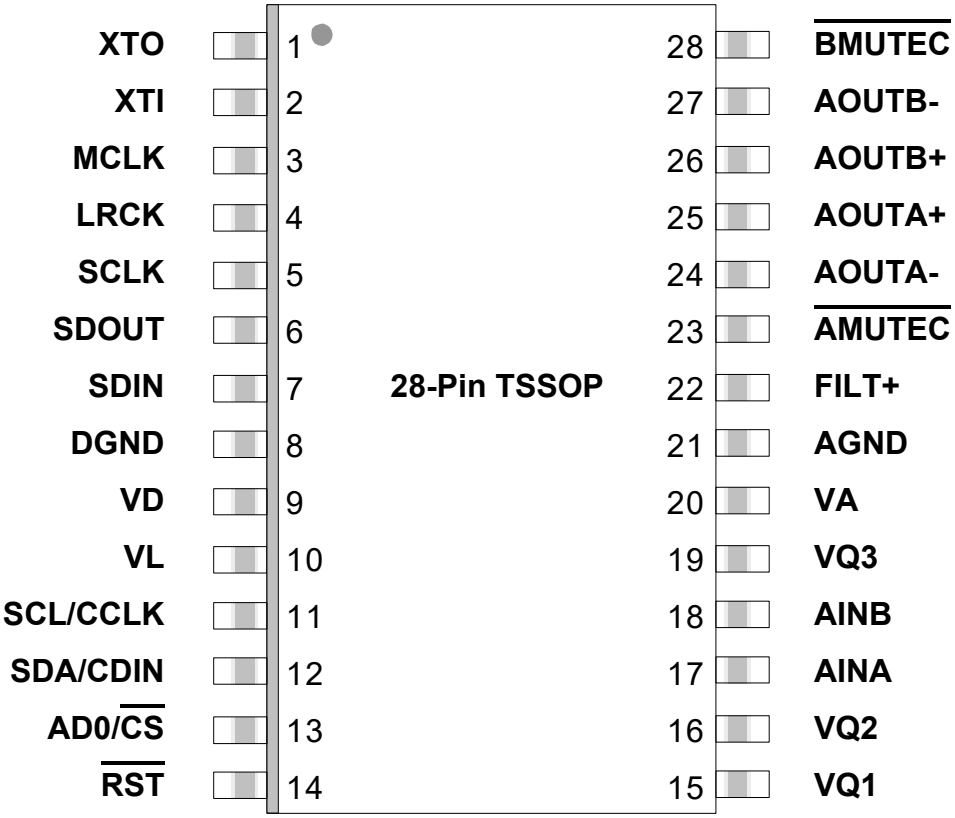
Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4271	24-Bit, 192 kHz Stereo Audio CODEC	28-pin TSSOP	YES	Commercial	-10° to +70° C	Tube	CS4271K-CZZ
						Tape & Reel	CS4271K-CZZR
				Automotive	-40° to +85° C	Tube	CS4271K-DZZ
						Tape & Reel	CS4271K-DZZR
CDB4271	CS4271 Evaluation Board		No	-	-	-	CDB4271

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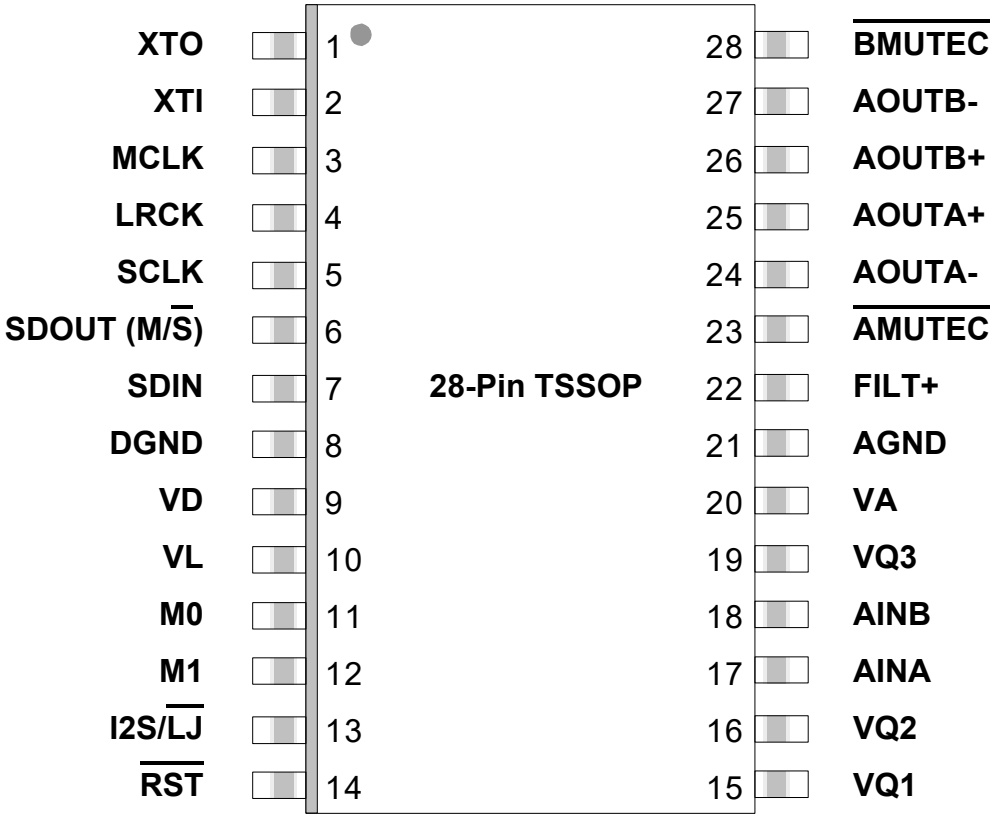
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1. PIN DESCRIPTIONS - SOFTWARE MODE



Pin Name	#	Pin Description
XTO **XTI**	1,2	**Crystal Connections** (*Input/Output*) - I/O pins for an external crystal which may be used to generate MCLK. See “Crystal Applications (XTI/XTO)” on page 24 or “Crystal Applications (XTI/XTO)” on page 27.
MCLK	3	**Master Clock** (*Input/Output*) -Clock source for the delta-sigma modulators. See “Crystal Applications (XTI/XTO)” on page 24 or “Crystal Applications (XTI/XTO)” on page 27.
LRCK	4	**Left Right Clock** *(Input/Output***) -** Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	**Serial Clock** *(Input/Output***) -** Serial clock for the serial audio interface.
SDOUT	6	**Serial Audio Data Output** (*Output*) **-** Output for two’s complement serial audio data.
SDIN	7	**Serial Audio Data Input** (*Input*) - Input for two’s complement serial audio data.
DGND	8	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	9	**Digital Power** (*Input*) **-** Positive power for the internal digital section.
VL	10	**Logic Power** (*Input*) - Positive power for the digital input/output interface.
SCL/CCLK	11	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
SDA/CDIN	12	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C mode. CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{\text{CS}}$	13	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C mode; $\overline{\text{CS}}$ is the chip select signal for SPI format.
$\overline{\text{RST}}$	14	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VQ1	15	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VQ2	16	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
AINA **AINB**	17, 18	**Analog Input** (*Input*) **-** The full scale input level is specified in the ADC Analog Characteristics specification table.
VQ3	19	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
VA	20	**Analog Power** *(Input)* **-** Positive power for the internal analog section.
AGND	21	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	22	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
$\overline{\text{AMUTEC}}$	23	**Channel A Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA- **AOUTA+** **AOUTB+** **AOUTB-**	24, 25, 26, 27	**Differential Analog Audio Output** (*Output*) - The full scale differential output level is specified in the DAC Analog Characteristics specification table.
$\overline{\text{BMUTEC}}$	28	**Channel B Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.

2. PIN DESCRIPTIONS - STAND-ALONE MODE



Pin Name	#	Pin Description
XTO **XTI**	1,2	**Crystal Connections** (*Input/Output*) - I/O pins for an external crystal which may be used to generate the master clock. See “Crystal Applications (XTI/XTO)” on page 24 or “Crystal Applications (XTI/XTO)” on page 27.
MCLK	3	**Master Clock** (*Input/Output*) -Clock source for the delta-sigma modulators. See “Crystal Applications (XTI/XTO)” on page 24 or “Crystal Applications (XTI/XTO)” on page 27.
LRCK	4	**Left Right Clock** *(Input/Output)* **-** Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	5	**Serial Clock** *(Input/Output)* **-** Serial clock for the serial audio interface.
SDOUT **(M/S)**	6	**Serial Audio Data Output** (*Output*) **-** Output for two’s complement serial audio data. This pin must be pulled-up or pulled-down to select Master or Slave Mode. See “Master/Slave Mode” on page 24.
SDIN	7	**Serial Audio Data Input** (*Input*) - Input for two’s complement serial audio data.
DGND	8	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	9	**Digital Power** (*Input*) **-** Positive power for the internal digital section.
VL	10	**Logic Power** (*Input*) - Positive power for the digital input/output interface.
M0	11	**Mode Select 0** (*Input*) - In conjunction with M1, selects operating mode. Functionality is described in the Hardware Mode Speed Configuration table.
M1	12	**Mode Select 1** (*Input*) - In conjunction with M0, selects operating mode. Functionality is described in the Hardware Mode Speed Configuration table.
I2S/$\overline{\text{LJ}}$	13	**Serial Audio Interface Select** *(Input)* - Selects either the left-justified or I^2S format for the Serial Audio Interface.
$\overline{\text{RST}}$	14	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VQ1	15	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
VQ2	16	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
AINA **AINB**	17, 18	**Analog Input** (*Input*) **-** The full scale input level is specified in the ADC Analog Characteristics specification table.
VQ3	19	**Quiescent Voltage** (*Input*) **-** Connection for internal quiescent reference voltage.
VA	20	**Analog Power** *(Input)* **-** Positive power for the internal analog section.
AGND	21	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
FILT+	22	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
$\overline{\text{AMUTEC}}$	23	**Channel A Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
AOUTA- **AOUTA+** **AOUTB+** **AOUTB-**	24, 25, 26, 27	**Differential Analog Audio Output** (*Output*) - The full scale differential output level is specified in the Analog Characteristics specification table.
$\overline{\text{BMUTEC}}$	28	**Channel B Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.

3. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (AGND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Positive Analog	VA	4.75	5.0	5.25	V
	Positive Digital	VD	3.1	3.3	5.25	V
	Positive Logic	VL	2.37	3.3	5.25	V
Ambient Operating Temperature (Power Applied)						
	Commercial Grade	T_A	-10	-	+70	°C
	Automotive Grade		-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS (GND = 0 V, All voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Logic	VL	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
Input Current	(Note 2)	I_{in}	-	-	±10	mA
Analog Input Voltage		V_{IN}	GND-0.3	-	VA+0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	VL+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-50	-	+95	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

DAC ANALOG CHARACTERISTICS - COMMERCIAL GRADE (Notes 3 to 7)

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance							
Dynamic Range	24-Bits	A-Weighted		108	114	-	dB
		unweighted		105	111	-	dB
	16-Bits	unweighted		-	94	-	dB
Total Harmonic Distortion + Noise		0 dB	THD+N	-	-100	-94	dB
		-20 dB		-	-91	-	dB
		-60 dB		-	-51	-45	dB
Idle Channel Noise / Signal-to-Noise Ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	dB
DC Accuracy							
Interchannel Gain Mismatch			ICGM	-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output Characteristics and Specifications							
Full Scale Differential Output Voltage			V_{FS}	0.91xVA	0.96xVA	1.01xVA	Vpp
Output Resistance		(note 7)	Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance			R_L	-	3	-	kΩ
Maximum Load Capacitance			C_L	-	100	-	pF

Notes: 3. One-half LSB of Triangular PDF dither is added to data.

4. Performance measurements taken with a full-scale 997 Hz sine wave under Test load R_L = 3 kΩ, C_L = 10 pF

5. Measurement bandwidth is 10 Hz to 20 kHz.

6. Logic “0” = GND = 0V; Logic “1” = VL; VL = VA unless otherwise noted.

7. V_{FS} is tested under load R_L but does not include attenuation due to Z_{OUT}

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE (Notes 3 to 7)

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance							
Dynamic Range	24-Bits	A-Weighted		106	114	-	dB
		unweighted		103	111	-	dB
	16-Bits	unweighted		-	94	-	dB
Total Harmonic Distortion + Noise		0 dB	THD+N	-	-100	-92	dB
		-20 dB		-	-91	-	dB
		-60 dB		-	-51	-43	dB
Idle Channel Noise / Signal-to-Noise Ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	dB
DC Accuracy							
Interchannel Gain Mismatch			ICGM	-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output Characteristics and Specifications							
Full Scale Differential Output Voltage			V_{FS}	0.91xVA	0.96xVA	1.01xVA	Vpp
Output Resistance		(note 7)	Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance			R_L	-	3	-	kΩ
Maximum Load Capacitance			C_L	-	100	-	pF

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(Note 12)

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Unit
Single Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.454	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		.547	-	-	Fs
StopBand Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	12/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Double Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.430	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	80	-	-	dB
Group Delay		-	4.6/Fs	-	s
Quad Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.105	Fs
	to -3 dB corner	0	-	.490	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.635	-	-	Fs
StopBand Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	4.7/Fs	-	s

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(cont) (Note 12)

Parameter		Slow Roll-Off (Note 8) Min	Typ	Max	Unit
Single Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	64	-	-	dB
Group Delay		-	6.5/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Double Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.792	-	-	Fs
StopBand Attenuation	(Note 10)	70	-	-	dB
Group Delay		-	3.9/Fs	-	s
Quad Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.868	-	-	Fs
StopBand Attenuation	(Note 10)	75	-	-	dB
Group Delay		-	4.2/Fs	-	s

Notes:
8. Slow Roll-Off interpolation filter is only available in control port mode.
9. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 21 to 44) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
10. Single and Double Speed Mode Measurement Bandwidth is from stopband to 3 Fs.
Quad Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.
11. De-emphasis is available only in Single Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone Mode.
12. Plots of this data are contained in the “Appendix” on page 47. See Figure 21 through Figure 44.

ADC ANALOG CHARACTERISTICS - COMMERCIAL GRADE

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode	**Fs = 48 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
Total Harmonic Distortion + Noise	(Note 13)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
Double Speed Mode	**Fs = 96 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 13)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Quad Speed Mode	**Fs = 192 kHz**					
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 13)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.51xVA	0.565xVA	0.62xVA	Vpp
Input Impedance			18	-	-	kΩ

Notes: 13. Referred to the typical full-scale input voltage.

ADC ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.)

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
Total Harmonic Distortion + Noise	(Note 14)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
Double Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 14)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Quad Speed Mode Fs = 192 kHz						
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
40kHz bandwidth	unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 14)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
40kHz bandwidth	-1 dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.51xVA	0.565xVA	0.62xVA	Vpp
Input Impedance			18	-	-	kΩ

Notes: 14. Referred to the typical full-scale input voltage.

ADC DIGITAL FILTER CHARACTERISTICS (Note 17)

Parameter			Symbol	Min	Typ	Max	Unit
Single Speed Mode							
Passband	(-0.1 dB).	(Note 15)		0	-	0.47	Fs
Passband Ripple.				-	-	±0.035	dB
Stopband.		(Note 15)		0.58	-	-	Fs
Stopband Attenuation.				-95	-	-	dB
Group Delay.			t_{gd}	-	12/Fs	-	s
Double Speed Mode							
Passband	(-0.1 dB).	(Note 15)		0	-	0.45	Fs
Passband Ripple.				-	-	±0.035	dB
Stopband.		(Note 15)		0.68	-	-	Fs
Stopband Attenuation.				-92	-	-	dB
Group Delay.			t_{gd}	-	9/Fs	-	s
Quad Speed Mode							
Passband	(-0.1 dB).	(Note 15)		0	-	0.24	Fs
Passband Ripple.				-	-	±0.035	dB
Stopband.		(Note 15)		0.78	-	-	Fs
Stopband Attenuation.				-97	-	-	dB
Group Delay.			t_{gd}	-	5/Fs	-	s
High Pass Filter Characteristics							
Frequency Response	-3.0 dB. -0.13 dB.	 (Note 16)		-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz.	(Note 16)		-	10	-	Deg
Passband Ripple.				-	-	0	dB
Filter Settling Time.					10^5/Fs		s

Notes: 15. The filter frequency response scales precisely with Fs.

16. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

17. Plots of this data are contained in the “Appendix” on page 47. See Figure 45 through Figure 56.

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply						
Power Supply Current	VA	I_A	-	45	53	mA
(Normal Operation)	VL,VD = 5 V	I_D	-	41.5	49	mA
	VL,VD = 3.3 V	I_D	-	24	28	mA
Power Supply Current	VA	I_A	-	0.025	-	mA
(Power-Down Mode)(Note 18)	VL,VD=5 V	I_D	-	1.76	-	mA
Power Consumption	VL, VD=5 V	-	-	433	510	mW
(Normal Operation)	VL, VD = 3.3 V	-	-	305	358	mW
	(Power-Down Mode)	-	-	9	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 19)	PSRR	-	60	-	dB
Quiescent Voltage						
Nominal Quiescent Voltage		VQ	-	0.48xVA	-	VDC
Maximum DC Current Source/Sink from VQ			-	1	-	μA
VQ Output Impedance			-	25	-	kΩ
FILT+						
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
MUTEC						
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 18. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

19. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 2 mA		V_{OH}	VL - 1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	μA

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (Logic "0" = GND = 0 V; Logic "1" = VL, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single Speed Mode	Fs	4	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
	Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications						
MCLK Frequency (note 20)	Stand-Alone Mode	f_{mclk}	1.024	-	25.600	MHz
	Control Port Mode	f_{mclk}	1.024	-	51.200	MHz
MCLK Input Pulse Width High/Low (note 20)	Stand-Alone Mode	t_{clkhl}	16	-	-	ns
	Control Port Mode	t_{clkhl}	8	-	-	ns
MCLK Output Duty Cycle			45	50	55	%
Master Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Duty Cycle			-	50	-	%
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	32	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Period (note 20)	Single Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	s
	Double Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	s
	Quad Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	s
SCLK Pulse Width High		t_{sclkh}	30	-	-	ns
SCLK Pulse Width Low		t_{sclkl}	48	-	-	ns
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	32	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns
Crystal Oscillator Specifications (XTI/XTO)						
Crystal Frequency Range		f_{osc}	16.384	-	25.600	MHz

Notes: 20. In Control Port Mode, the Ratio[1:0] bits must be configured according to tables 8 and 9 on pages 28 and 29.

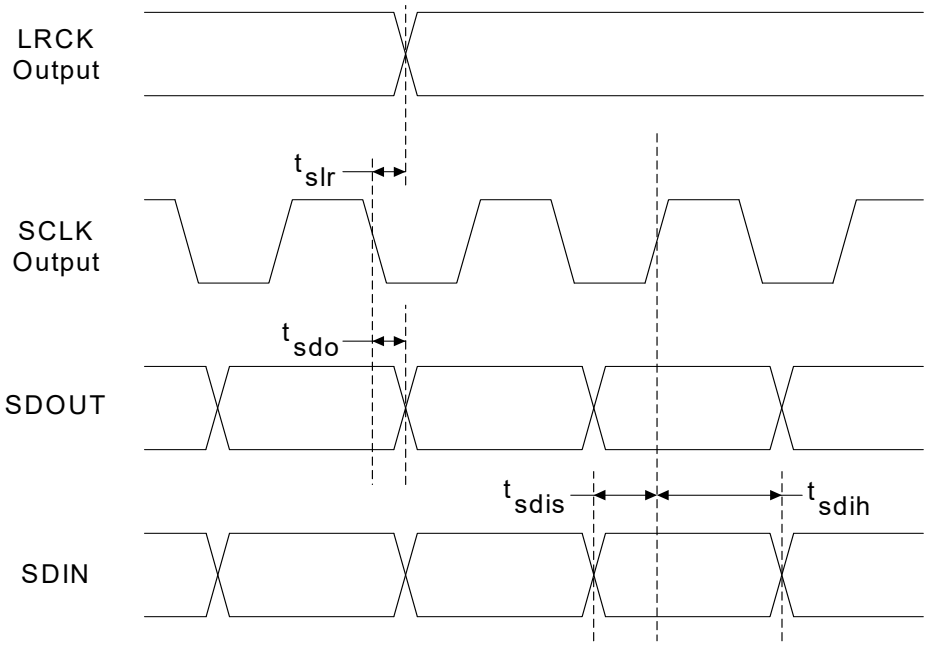


Figure 1. Master Mode Serial Audio Port Timing

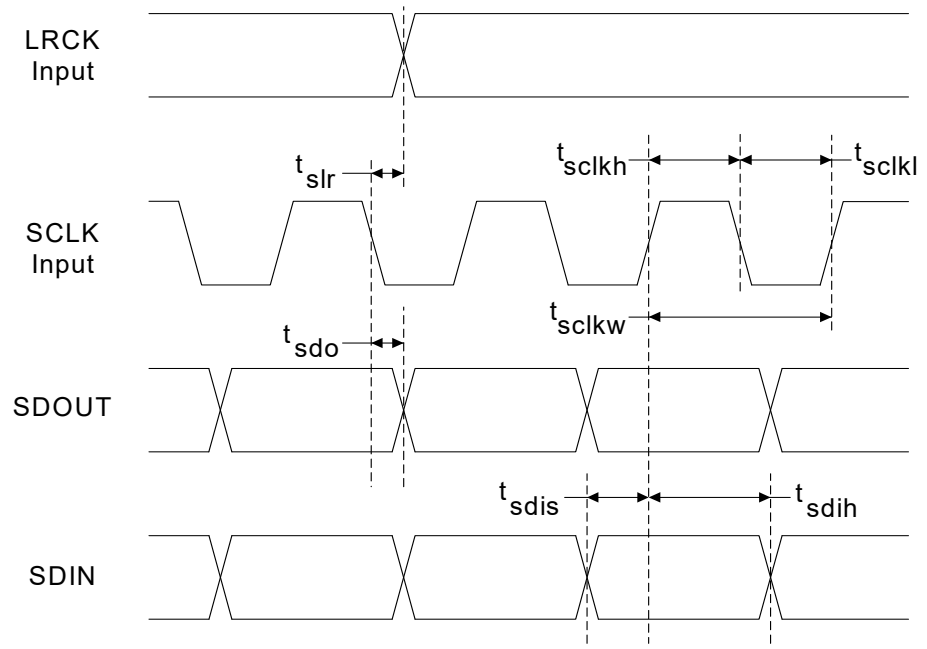


Figure 2. Slave Mode Serial Audio Port Timing

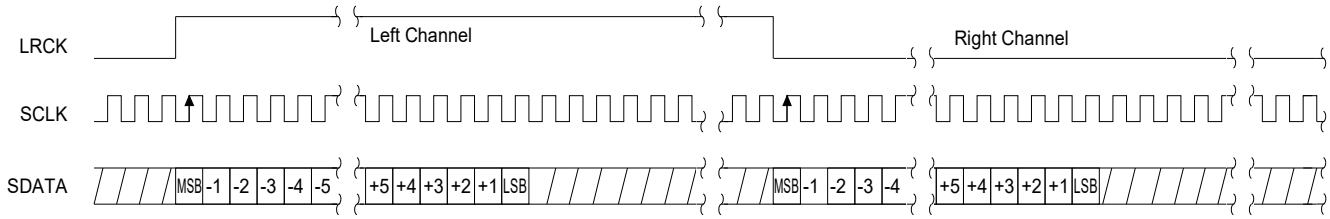


Figure 3. Format 0, Left Justified up to 24-Bit Data

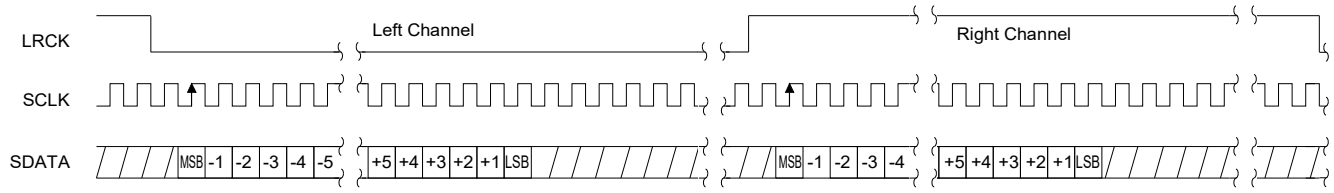


Figure 4. Format 1, I²S up to 24-Bit Data

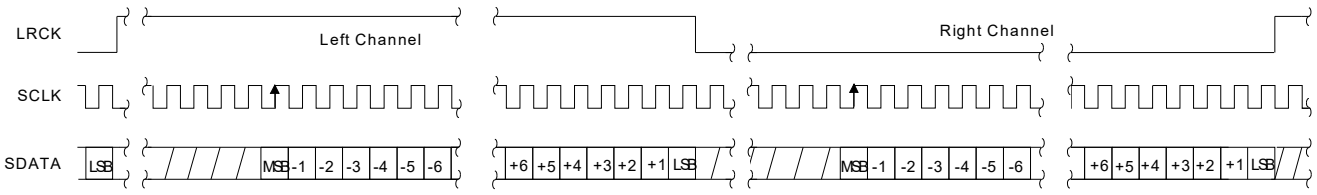


Figure 5. Format 2, Right Justified 16-Bit Data. (Available in Control Port Mode only)
Format 3, Right Justified 24-Bit Data. (Available in Control Port Mode only)
Format 4, Right Justified 20-Bit Data. (Available in Control Port Mode only)

SWITCHING CHARACTERISTICS - I²C MODE CONTROL PORT

(Inputs: logic 0 = AGND, logic 1 = VL)

Parameter	Symbol	Min	Max	Unit
I²C Mode				
SCL Clock Frequency.	f_{scl}	-	100	KHz
$\overline{RST}$ Rising Edge to Start.	t_{irs}	500	-	ns
Bus Free Time Between Transmissions.	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse).	t_{hdst}	4.0	-	µs
Clock Low time.	t_{low}	4.7	-	µs
Clock High Time.	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition.	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling. (Note 21)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising.	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines.	t_r	-	1	µs
Fall Time of Both SDA and SCL Lines.	t_f	-	300	ns
Setup Time for Stop Condition.	t_{susp}	4.7	-	µs

Notes: 21. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

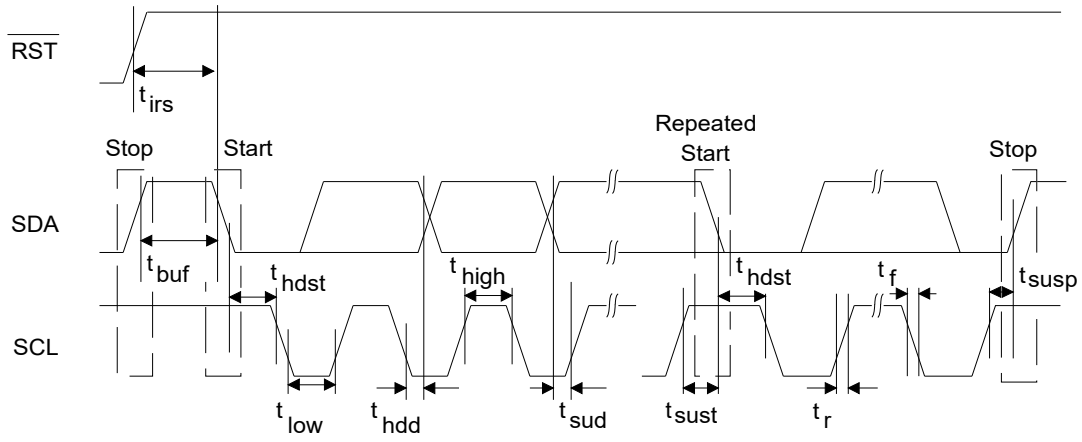


Figure 6. I²C Mode Control Port Timing

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: logic 0 = AGND, logic 1 = VL)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency.		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling.		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling.	(Note 22)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions.		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge.		t_{css}	20	-	ns
CCLK Low Time.		t_{scl}	82	-	ns
CCLK High Time.		t_{sch}	82	-	ns
CDIN to CCLK Rising Setup Time.		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time.	(Note 23)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN.	(Note 24)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN.	(Note 24)	t_{f2}	-	100	ns

Notes: 22. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

23. Data must be held for sufficient time to bridge the transition time of CCLK.

24. For F_{SCK} < 1 MHz

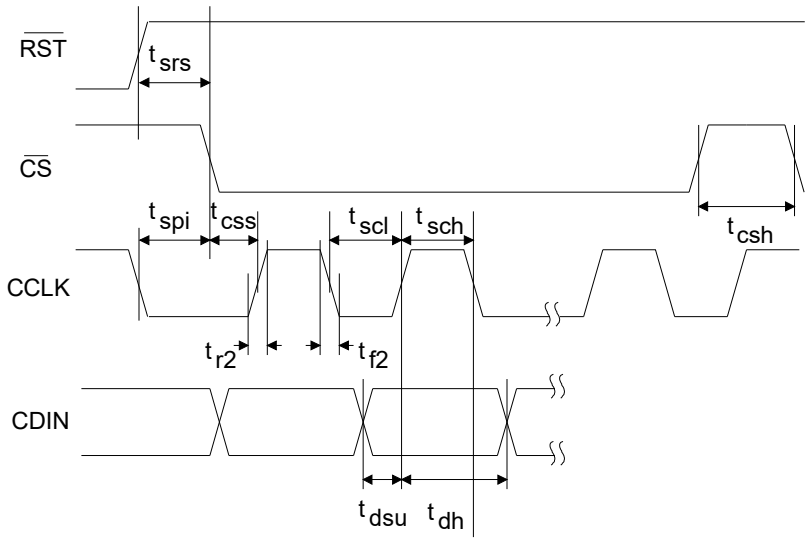


Figure 7. SPI Control Port Timing

4. TYPICAL CONNECTION DIAGRAM

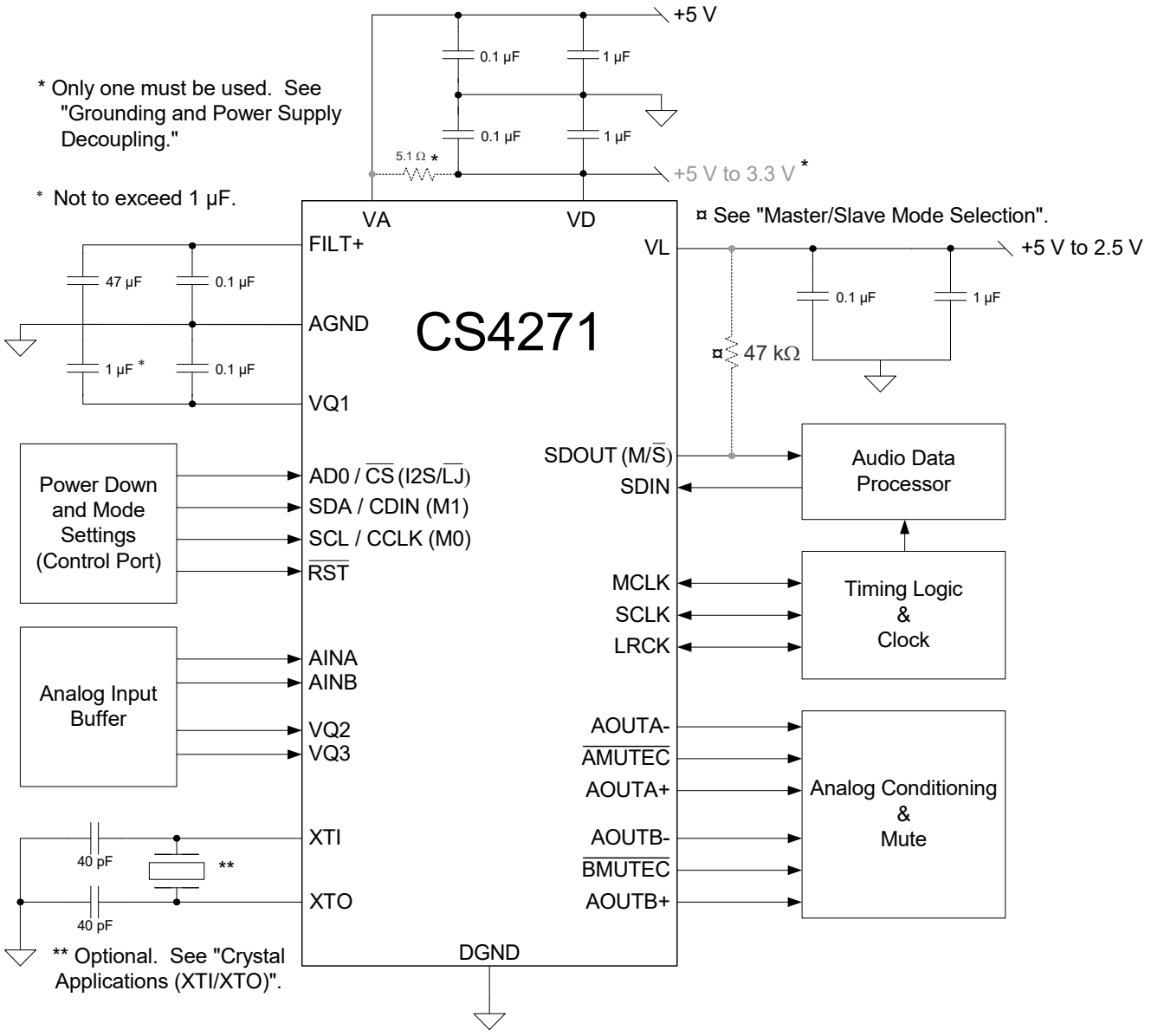


Figure 8. CS4271 Typical Connection Diagram

5. APPLICATIONS

5.1 Stand-Alone Mode

5.1.1 Recommended Power-Up Sequence

1) When using the CS4271 with an external MCLK, hold $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable. When using the CS4271 with internally generated MCLK, hold $\overline{\text{RST}}$ low until the power supply is stable.
2) Bring $\overline{\text{RST}}$ high. If the internally generated MCLK is being used, it will appear on the MCLK pin prior to 1 ms from the release of $\overline{\text{RST}}$.

5.1.2 Master/Slave Mode

The CS4271 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to Fs and SCLK is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 64x Fs to maximize system performance.

In Stand-Alone Mode, the CS4271 will default to Slave Mode. Master Mode may be accessed by placing a 47 kΩ pull-up to VL on the SDOUT (M/$\overline{\text{S}}$) pin.

Configuration of clock ratios in each of these modes will be outlined in the Tables 3 and 4.

5.1.3 System Clocking

The CS4271 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 1 below.

Table 1. Speed Modes

Mode	Sampling Frequency
Single Speed	4-50 kHz
Double Speed	50-100 kHz
Quad Speed	100-200 kHz

5.1.3.1 Crystal Applications (XTI/XTO)

An external crystal may be used in conjunction with the CS4271 to generate the master clock signal. To accomplish this, a 20 pF fundamental mode parallel resonant crystal must be connected between the XTI and XTO pins as shown in the Typical Connection Diagram on page 23. This crystal must oscillate at the frequency shown in Table 2. In this configuration, MCLK is a buffered output and, as shown in the Typical Connection Diagram, nothing other than the crystal and its load capacitors should be connected to XTI and XTO. The MCLK signal will appear on the MCLK pin prior to 1 ms from the release of $\overline{\text{RST}}$.

Table 2. Crystal Frequencies

Mode	Crystal Frequency
Single Speed	512 x Fs
Double Speed	256 x Fs
Quad Speed	128 x Fs

To operate the CS4271 with an externally generated MCLK signal, no crystal should be used, XTI should be connected to ground and XTO should be left unconnected. In this configuration, MCLK is an input and must be driven externally with an appropriate speed clock.

5.1.3.2 Clock Ratio Selection

Depending on the use of an external crystal, or whether the CS4271 is in Master or Slave Mode, different MCKL/LRCK and SCLK/LRCK ratios may be used. These ratios are shown in the Tables 3 and 4 below.

Table 3. Clock Ratios - Stand Alone Mode With External Crystal

External Crystal Used, MCLK=Output			
Master Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	64	Fs
Double Speed	128	64	Fs
Quad Speed	128	64	Fs
Slave Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	32, 64, 128	Fs
Double Speed	128	32, 64	Fs
Quad Speed	128	32, 64	Fs

Table 4. Clock Ratios - Stand Alone Mode Without External Crystal

External Crystal Not Used, MCLK=Input			
Master Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	64	Fs
Double Speed	128	64	Fs
Quad Speed	64	32	Fs
Slave Mode			
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**
Single Speed	256	32, 64, 128	Fs
	384	32, 48, 64, 96, 128	Fs
	512	32, 64, 128	Fs
Double Speed	128	32, 64	Fs
	192	32, 48, 64	Fs
	256	32, 64	Fs
Quad Speed	64	32	Fs
	96	48	Fs
	128	32, 64	Fs

5.1.4 16-Bit Auto-Dither

The CS4271 will auto-configure to output properly dithered 16-bit data when placed in Slave Mode and a 32x SCLK to LRCK ratio is used. In this configuration, one half of a bit of dither is added to the LSB of the 16-bit word. This applies only to the serial audio output of the ADC and will not affect DAC performance. See Figure 9.

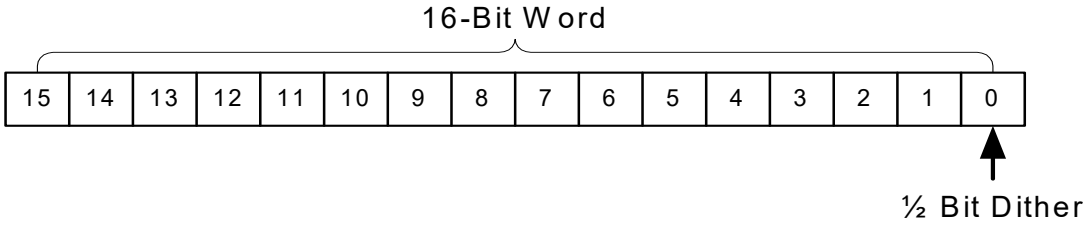


Figure 9. ADC 16-Bit Auto-Dither

5.1.5 Auto-Mute

The DAC output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting are done independently for each channel. The common mode on the output will be retained and the Mute Control pin for that channel will go active during the mute period.

5.1.6 High Pass Filter

The operational amplifiers in the input circuitry driving the CS4271 may generate a small DC offset into the ADC. The CS4271 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

In Stand-Alone Mode, the high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. This function cannot be disabled in Stand-Alone Mode.

5.1.7 Interpolation Filter

In Stand-Alone Mode, the fast roll-off interpolation filter is used.

Filter specifications can be found in Section 3. Plots of the data are contained in the “Appendix” on page 47.

5.1.8 Mode Selection & De-Emphasis

The sample rate, Fs, can be adjusted from 4 kHz to 200 kHz. In Stand-Alone Mode, the CS4271 must be set to the proper mode via the mode pins, M1 and M0. De-emphasis, optimized for a 44.1 kHz sampling frequency, is available.

Table 5. CS4271 Stand-Alone Mode Control

Mode 1	Mode 0	Mode	Sample Rate (Fs)	De-Emphasis
0	0	Single Speed Mode	4 kHz - 50 kHz	44.1 kHz
0	1	Single Speed Mode	4 kHz - 50 kHz	Off
1	0	Double Speed Mode	50 kHz - 100 kHz	Off
1	1	Quad Speed Mode	100 kHz - 200 kHz	Off

5.1.9 Serial Audio Interface Format Selection

Either I^2S or left justified serial audio data format may be selected in Stand-Alone Mode. The selection will affect both the input and output format. Placing a 10 kΩ pull-up to VL on the I2S/$\overline{LJ}$ pin will select the I^2S format, while placing a 10 kΩ pull-down to DGND on the I2S/$\overline{LJ}$ pin will select the left justified format.

5.2 Control Port Mode

5.2.1 Recommended Power-Up Sequence - Access to Control Port Mode

1) When using the CS4271 with an external MCLK, hold $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable. When using the CS4271 with internally generated MCLK, hold $\overline{\text{RST}}$ low until the power supply is stable. In this state, the Control Port is reset to its default settings.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state and the control port will be accessible. If internally generated MCLK is being used, it will appear on the MCLK pin prior to 1 ms from the release of $\overline{\text{RST}}$.
3) Write 03h to register 07h within 10 ms following the release of $\overline{\text{RST}}$. This sets the Control Port Enable (CPEN) and Power Down (PDN) bits, activating the Control Port and placing the part in power-down. When using the CS4271 with internally generated MCLK, it is necessary to wait 1 ms following the release of $\overline{\text{RST}}$ before initiating this Control Port write.
4) The desired register settings can be loaded while keeping the PDN bit set.
5) Clear the PDN bit to initiate the power-up sequence. This power-up sequence requires approximately 85 µS.

5.2.2 Master / Slave Mode Selection

The CS4271 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to Fs and SCLK is equal to 64x Fs.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be 64x Fs to maximize system performance.

Configuration of clock ratios in each of these modes will be outlined in the Tables 8 and 9.

In Control Port Mode the CS4271 will default to Slave Mode. The user may change this default setting by changing the status of the M/$\overline{\text{S}}$ bit in the Mode Control 1 register (01h).

5.2.3 System Clocking

The CS4271 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 6 below.

Table 6. Speed Modes

Mode	Sampling Frequency
Single Speed	4-50 kHz
Double Speed	50-100 kHz
Quad Speed	100-200 kHz

5.2.3.1 Crystal Applications (XTI/XTO)

An external crystal may be used in conjunction with the CS4271 to generate the MCLK signal. To accomplish this, a 20 pF fundamental mode parallel resonant crystal must be connected between the XTI and XTO pins as shown in the Typical Connection Diagram on page 23. This crystal must oscillate at the frequency shown in Table 7. In this configuration, MCLK is a buffered output and, as shown in the Typical Connection Diagram, nothing other than the crystal and its load capacitors should be connected to XTI and XTO. The MCLK signal will appear on the MCLK pin prior to 1 ms from the release of $\overline{\text{RST}}$.

Table 7. Crystal Frequencies

Mode	Crystal Frequency
Single Speed	512 x Fs
Double Speed	256 x Fs
Quad Speed	128 x Fs

To operate the CS4271 with an externally generated MCLK signal, no crystal should be used, XTI should be connected to ground and XTO should be left unconnected. In this configuration, MCLK is an input and must be driven externally with an appropriate speed clock.

5.2.3.2 Clock Ratio Selection

Depending on the use of an external crystal, or whether the CS4271 is in Master or Slave Mode, different MCKL/LRCK and SCLK/LRCK ratios may be used. These ratios as well as the Control Port Register Bits that must be set in order to obtain them are shown in Tables 8 and 9 below.

Table 8. Clock Ratios - Control Port Mode With External Crystal

External Crystal Used, MCLK=Output					
Master Mode					
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**	**Ratio1 Bit**	**Ratio0 Bit**
Single Speed	256	64	Fs	0	d^{25}
	512	64	Fs	1	d^{25}
Double Speed	128	64	Fs	0	d^{25}
	256	64	Fs	1	d^{25}
Quad Speed	128	64	Fs	d^{25}	d^{25}
Slave Mode					
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**	**Ratio1 Bit**	**Ratio0 Bit**
Single Speed	256	32, 64, 128	Fs	0	d^{25}
	512	32, 64, 128	Fs	1	d^{25}
Double Speed	128	32, 64	Fs	0	d^{25}
	256	32, 64	Fs	1	d^{25}
Quad Speed	128	32, 64	Fs	d^{25}	d^{25}

Notes: 25. For the Ratio1 and Ratio0 bits listed above, “d” indicates that any value may written.

Table 9. Clock Ratios - Control Port Mode Without External Crystal

External Crystal Not Used, MCLK=Input					
Master Mode					
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**	**Ratio1 Bit**	**Ratio0 Bit**
Single Speed	256	64	Fs	0	0
	384	64	Fs	0	1
	512	64	Fs	1	0
	768	64	Fs	1	1
Double Speed	128	64	Fs	0	0
	192	64	Fs	0	1
	256	64	Fs	1	0
	384	64	Fs	1	1
Quad Speed	64	32	Fs	0	0
	96	32	Fs	0	1
	128	64	Fs	1	0
	192	64	Fs	1	1
Slave Mode					
	MCLK/LRCK	**SCLK/LRCK**	**LRCK**	**Ratio1 Bit**	**Ratio0 Bit**
Single Speed	256	32, 64, 128	Fs	0	d[26]
	384	32, 48, 64, 96, 128	Fs	0	d[26]
	512	32, 64, 128	Fs	0	d[26]
	768	32, 48, 64, 96, 128	Fs	1	d[26]
	1024	32, 64, 128	Fs	1	d[26]
Double Speed	128	32, 64	Fs	0	d[26]
	192	32, 48, 64	Fs	0	d[26]
	256	32, 64	Fs	0	d[26]
	384	32, 48, 64	Fs	1	d[26]
	512	32, 64	Fs	1	d[26]
Quad Speed	64	32	Fs	0	d[26]
	96	48	Fs	0	d[26]
	128	32, 64	Fs	0	d[26]
	192	48	Fs	1	d[26]
	256	32, 64	Fs	1	d[26]

Notes: 26. For the Ratio0 bit listed above, “d” indicates that any value may written.

5.2.4 Internal Digital Loopback

In Control Port Mode, the CS4271 supports an internal digital loopback mode in which the output of the ADC is routed to the input of the DAC. This mode may be activated by setting the LOOP bit in the Mode Control 2 register (07h).

When this bit is set, the status of the DAC_DIF(2:0) bits in register 01h will be disregarded by the CS4271. Any changes made to the DAC_DIF(2:0) bits while the LOOP bit is set will have no impact on operation until the LOOP bit is released, at which time the Digital Interface Format of the DAC will operate according to the format selected in the DAC_DIF(2:0) bits. While the LOOP bit is set, data will be present on the SDOUT pin in the format selected in the ADC_DIF bit in register 06h.

5.2.5 Dither for 16-Bit Data

The CS4271 may be configured to properly dither for 16-bit data. To do this, the Dither16 bit in the ADC Control Register (06h) must be set. When set, a half bit of dither is added to the least significant bit of the 16 most significant bits of the data word. The remaining bits should be disregarded. See Figure 10. This function is useful when 16-bit devices are downstream of the ADC. This bit should not be set when using word lengths greater than 16 bits.

It should be noted that this function is supported for all serial audio output formats, and may be activated in either Master or Slave Mode.

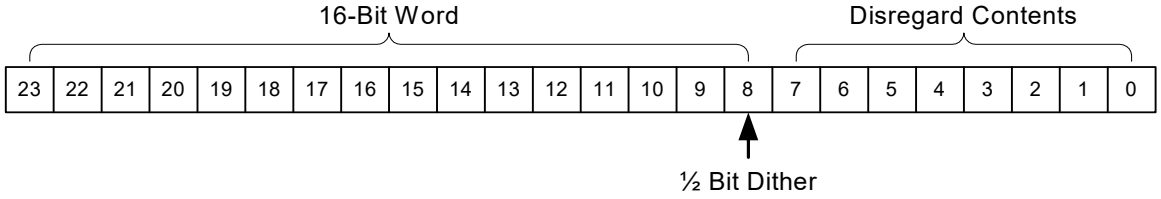


Figure 10. Example of Dither for 16-Bit Data with 24-Bit Left Justified Format

5.2.6 Auto-Mute

The Auto-Mute function is controlled by the status of the AMUTE bit in the DAC Control register. When set, the DAC output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting are done independently for each channel. Auto-Mute detection and muting can become dependent on either channel if the MUTECA=B function is enabled. The common mode on the output will be retained and the Mute Control pin for that channel will become active during the mute period. The muting function is effected, similar to volume control changes, by the Soft and ZeroCross bits in the DAC Volume and Mixing Control register. The AMUTE bit is set by default.

5.2.7 High Pass Filter and DC Offset Calibration

The operational amplifiers in the input circuitry driving the CS4271 may generate a small DC offset into the A/D converter. The CS4271 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. The high pass filter can be independently enabled and disabled for channels A and B. If the HPFDisableA or HPFDisableB bit is set during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1) Running the CS4271 with the high pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2) Disabling the high pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS4271.

5.2.8 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4271 incorporates selectable interpolation filters for each mode of operation. Fast and slow roll-off filters are available in each of Single, Double, and Quad Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit in the DAC Control register (02h) is used to select which filter is used. By default, the fast roll-off filter is selected.

Filter specifications can be found in Section 3. Plots of the data are contained in the “Appendix” on page 47.

5.2.9 De-Emphasis

Three de-emphasis modes are available via the Control Port. The available filters are optimized for 32 kHz, 44.1 kHz, and 48 kHz sampling rates. See Table 13 for de-emphasis selection in Control Port Mode.

5.2.10 Oversampling Modes

The CS4271 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the M1 and M0 bits in the Mode Control 1 register. Single-Speed mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x. See Table 11 for Control Port Mode settings.

5.3 De-Emphasis Filter

The CS4271 includes on-chip digital de-emphasis. Figure 11 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. Please see section 5.1.8 for the desired de-emphasis control for Stand-Alone mode and section 5.2.9 for control port mode.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 μS pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single Speed Mode.

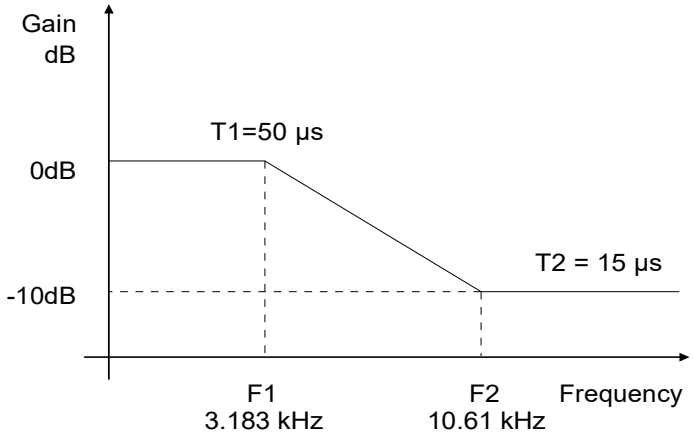


Figure 11. De-Emphasis Curve

5.4 Analog Connections

5.4.1 Input Connections

The analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are (n × 6.144 MHz) the digital passband frequency, where n=0,1,2,... Refer to Figure 12 for a recommended analog input buffer that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. Figure 13 shows the full-scale analog input levels.

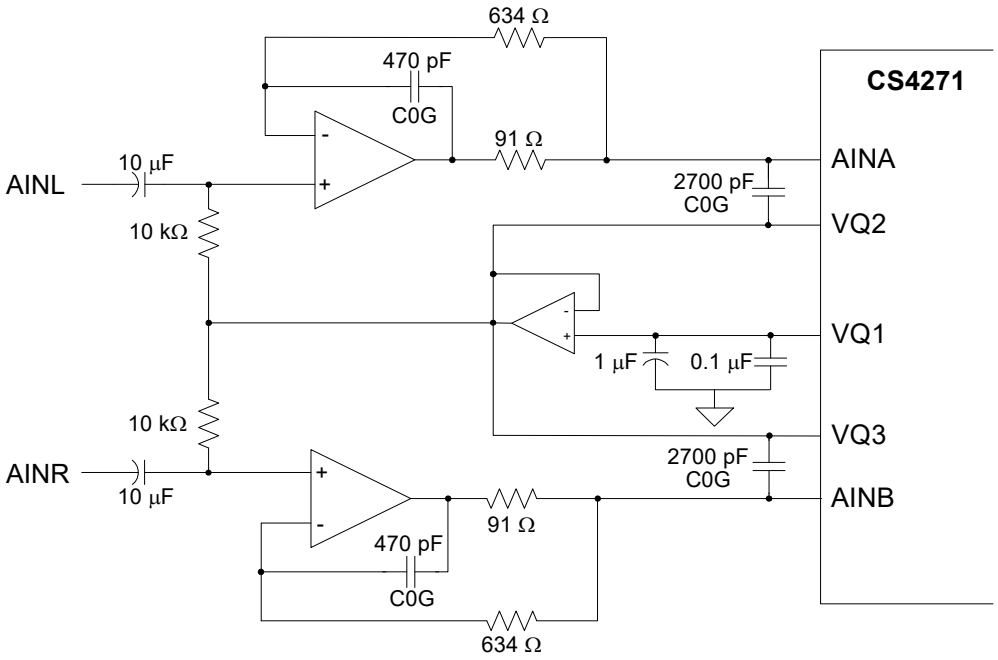
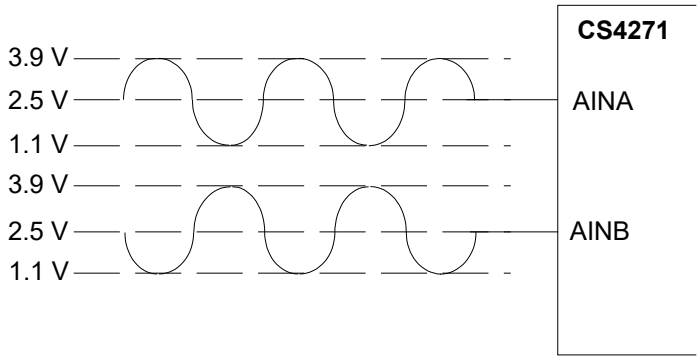


Figure 12. CS4271 Recommended Analog Input Buffer



Full-Scale Input Level = 2.8 Vpp

Figure 13. Full-Scale Analog Input

5.4.2 Output Connections

The recommended output filter configuration is shown in Figure 14. This filter configuration accounts for the normally differing AC loads on the AOUT+ and AOUT- differential output pins. It also shows an AC coupling configuration which minimizes the number of required AC coupling capacitors.

The CS4271 does not include phase or amplitude compensation for an external filter, and therefore the DAC system phase and amplitude response will be dependent on the external analog circuitry. Figure 15 shows the full-scale analog output levels.

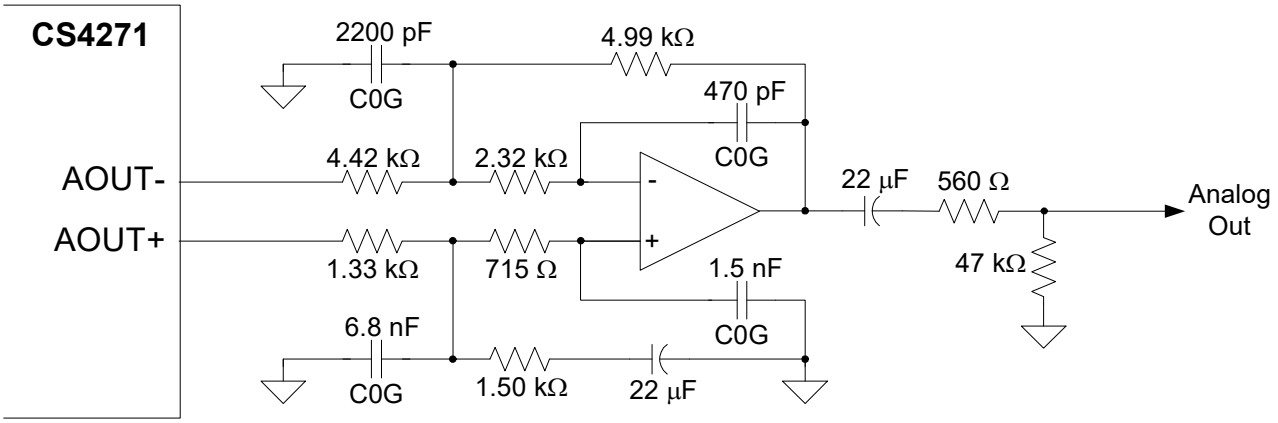
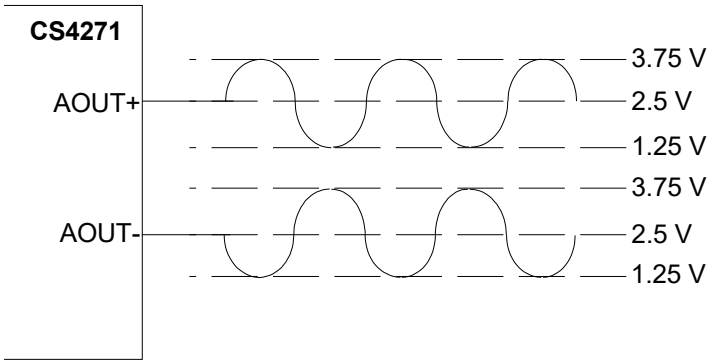


Figure 14. CS4271 Recommended Analog Output Filter



Full-Scale Output Level= (AIN+) - (AIN-)= 5 Vpp

Figure 15. Full-Scale Analog Output

5.5 Mute Control

The Mute Control pins become active during power-up initialization, reset, muting, if the MCLK to LRCK ratio is incorrect, and during power-down. The Auto-Mute function causes the MUTEC pin corresponding to an individual channel to activate following the reception of 8192 consecutive audio samples of static 0 or -1 on the respective channel. A single sample of non-zero data on this channel will cause the MUTEC pin to deactivate. In Control Port Mode, however, auto-mute detection and muting can become dependent on either channel if the MuteB=A function is enabled. The MUTEC pins are intended to be used as control for an external mute circuit in order to add off-chip mute capability.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. The MUTEC pins are active-low. See Figure 16 below for a suggested active-low mute circuit.

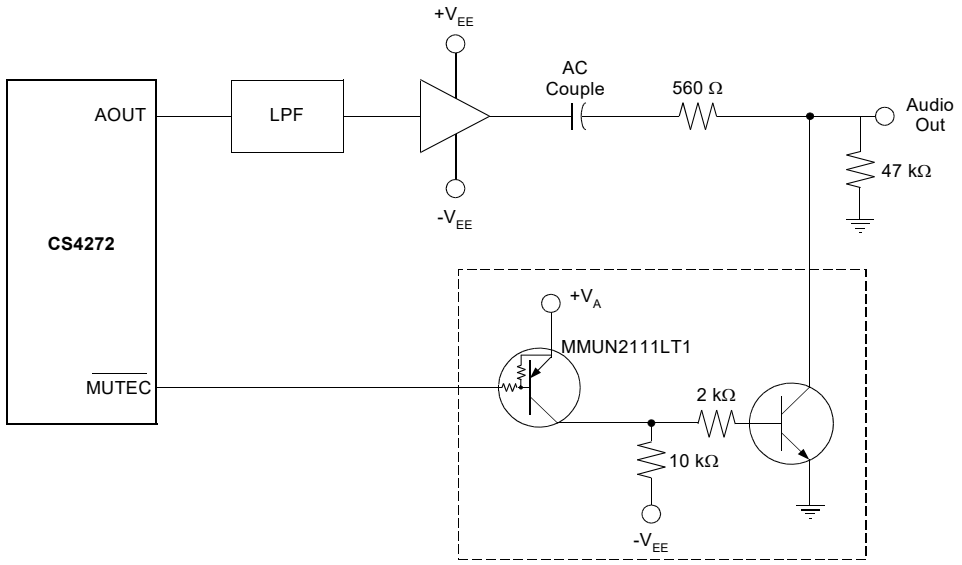


Figure 16. Sug

5.6 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS4271's in the system. If only one MCLK source is needed, one solution is to place one CS4271 in Master Mode, and slave all of the other CS4271's to the one master. If multiple MCLK sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS4271 reset with the inactive edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

5.7 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4271 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 8 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply (VL) or may be powered from the analog supply (VA) via a resistor. In this case, no additional devices should be powered from VD. Power supply decoupling capacitors should be as near to the CS4271 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the modulators. The VREF and VCOM decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF and AGND. The CDB4271 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS4271 digital outputs only to CMOS inputs.

6. CONTROL PORT INTERFACE

The Control Port is used to load all the internal settings of the CS4271. The operation of the Control Port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the Control Port pins should remain static if no operation is required.

The Control Port has 2 modes: SPI and I²C, with the CS4271 operating as a slave to control messages in both modes. If I²C operation is desired, AD0/$\overline{CS}$ should be tied to VA or AGND. If the CS4271 ever detects a high to low transition on AD0/$\overline{CS}$ after power-up, SPI mode will be selected. The Control Port registers are write-only in SPI mode.

Upon release of the $\overline{RST}$ pin, the CS4271 will wait approximately 10 ms before it begins its start-up sequence. The part defaults to Stand-Alone Mode, in which all operational modes are controlled as described under “Stand-Alone Mode” on page 24. The Control Port is active at all times, and if bit 1 of register 07h (CPEN) is set, the part enters Control-Port Mode and all operational modes are controlled by the Control Port registers. This bit can be set at any time, but to avoid unpredictable output noises, bit 1 (CPEN) and bit 0 (PDN) of register 07h should be set by writing 03h before the end of the 10 ms start-up wait period. All registers can then be set as desired before releasing the PDN bit to begin the start-up sequence. If system requirements do not allow writing to the control port immediately following the release of $\overline{RST}$, the SDIN line should be held at logic “0” until the proper serial mode can be selected.

6.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4271 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All control signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 17 shows the operation of the Control Port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP. See Table 10 on page 36.

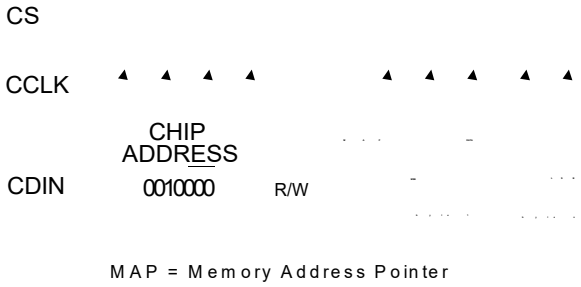


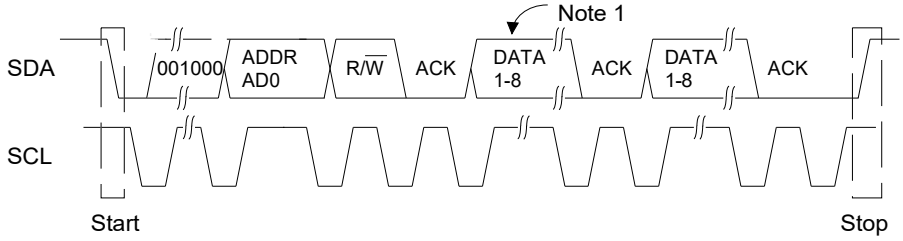
Figure 17. Control Port Timing, SPI mode

The CS4271 has MAP auto increment capability, enabled by the INCR bit in the MAP. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set, then MAP will auto increment after each byte is written, allowing block writes to successive registers.

6.2 I²C Mode

In I²C mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 18. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VA or AGND as required. The upper 6 bits of the 7-bit address field must be 001000. To communicate with the CS4271, the LSB of the chip address field, which is the first byte sent to the CS4271, should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.

The CS4271 has MAP auto increment capability, enabled by the INCR bit in the MAP. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 18. Control Port Timing, I²C Mode

Table 10. Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

INCR - Auto MAP Increment Enable
Default = '0'.
0 - Disabled
1 - Enabled

MAP(3:0) - Memory Address Pointer
Default = '0000'.

7. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Mode Control 1	M1	M0	Ratio1	Ratio0	M/$\overline{S}$	DAC_DIF2	DAC_DIF1	DAC_DIF0
		0	0	0	0	0	0	0	0
02h	DAC Control	AMUTE	FILT_SEL	DEM1	DEM0	RMP_UP	RMP_DN	INV_B	INV_A
		1	0	0	0	0	0	0	0
03h	DAC Volume & Mixing Control	Reserved	B=A	Soft	ZeroCross	ATAPI3	ATAPI2	ATAPI1	ATAPI0
		0	0	1	0	1	0	0	1
04h	DAC Ch A Volume Control	MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
		0	0	0	0	0	0	0	0
05h	DAC Ch B Volume Control	MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
		0	0	0	0	0	0	0	0
06h	ADC Control	Reserved	Reserved	Dither16	ADC_DIF0	MUTEA	MUTEB	HPFDisableA	HPFDisableB
		0	0	0	0	0	0	0	0
07h	Mode Control 2	Reserved	Reserved	Reserved	LOOP	MUTECA=B	FREEZE	CPEN	PDN
		0	0	0	0	0	0	0	0
08h	Chip ID	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		0	0	0	0	0	0	0	0

8. REGISTER DESCRIPTION

** All registers are read/write in I²C mode and write only in SPI mode, unless otherwise noted**

8.1 Mode Control 1 - Address 01h

7	6	5	4	3	2	1	0
M1	M0	Ratio1	Ratio0	M/$\overline{S}$	DAC_DIF2	DAC_DIF1	DAC_DIF0

8.1.1 Functional Mode (Bits 7:6)

Function:

Selects the required range of input sample rates.

Table 11. Functional Mode Selection

M1	M0	Mode
0	0	Single-Speed Mode: 4 to 50 kHz sample rates (default)
0	1	Single-Speed Mode: 4 to 50 kHz sample rates
1	0	Double-Speed Mode: 50 to 100 kHz sample rates
1	1	Quad-Speed Mode: 100 to 200 kHz sample rates

8.1.2 Ratio Select (Bits 5:4)

Function:

These bits are used to select the clocking ratios in Control Port Mode. Please refer to Table 8, “Clock Ratios - Control Port Mode With External Crystal,” on page 28 or Table 9, “Clock Ratios - Control Port Mode Without External Crystal,” on page 29 for information on which of these bits to set to obtain specific clock ratios.

8.1.3 Master / Slave Mode (Bit 3)

Function:

This bit selects either master or slave operation. Setting this bit will select master mode, while clearing this bit will select slave mode.

8.1.4 DAC Digital Interface Format (Bits 2:0)

Function:

The required relationship between LRCK, SCLK and SDIN for the DAC is defined by the DAC Digital Interface Format and the options are detailed in Table 12 and Figures 3-5.

Table 12. DAC Digital Interface Formats

DAC_DIF2	DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	0	0	Left Justified, up to 24-bit data (default)	0	3
0	0	1	I^2S, up to 24-bit data	1	4
0	1	0	Right Justified, 16-bit Data	2	5
0	1	1	Right Justified, 24-bit Data	3	5
1	0	0	Right Justified, 20-bit Data	4	5
1	0	1	Right Justified, 18-bit Data	5	5
1	1	0	Reserved		
1	1	1	Reserved		

8.2 DAC Control - Address 02h

7	6	5	4	3	2	1	0
AMUTE	FILT_SEL	DEM1	DEM0	RMP_UP	RMP_DN	INV_A	INV_B

8.2.1 Auto-Mute (Bit 7)

Function:

When set, enables the Auto-Mute function. See “Auto-Mute” on page 30.

8.2.2 Interpolation Filter Select (Bit 6)

Function:

This Function allows the user to select whether the Interpolation Filter has a fast or slow roll off. When set, this bit selects the slow roll off filter, when cleared it selects the fast roll off filter. The - 3 dB corner is approximately the same for both filters, but the slope of the roll off is greater for the fast roll off filter.

8.2.3 De-Emphasis Control (Bits 5:4)

Function:

Implementation of the standard 50/15 μs digital de-emphasis filter response, Figure 19, requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates. NOTE: De-emphasis is available only in Single-Speed Mode. See Table 13 below.

Table 13. De-Emphasis Mode Selection

DEM1	DEM0	Description
0	0	Disabled (default)
0	1	44.1 kHz de-emphasis
1	0	48 kHz de-emphasis
1	1	32 kHz de-emphasis

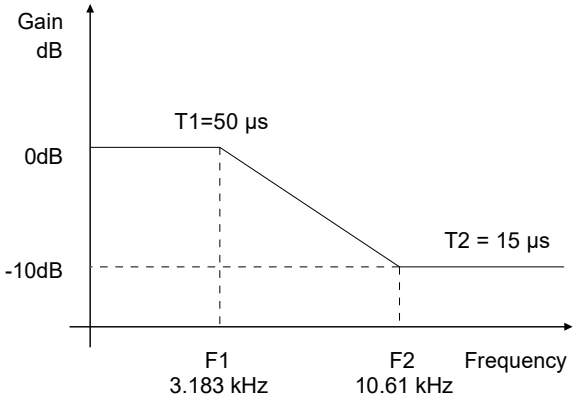


Figure 19. De-Emphasis Curve

8.2.4 Soft Volume Ramp-Up After Error (Bit 3)

Function:

An un-mute will be performed after executing a filter mode change, after a MCLK/LRCK ratio change or error, and after changing the Functional Mode. When this bit is set, this un-mute is effected, similar to attenuation changes, by the Soft and ZeroCross bits in the DAC Volume & Mixing Control register. When cleared, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this feature be used with the RMP_DN bit.

8.2.5 Soft Ramp-Down Before Filter Mode Change (Bit 2)

Function:

A mute will be performed prior to executing a filter mode change. When this bit is set, this mute is effected, similar to attenuation changes, by the Soft and ZeroCross bits in the DAC Volume & Mixing Control register. When cleared, an immediate mute is performed prior to executing a filter mode change.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

8.2.6 Invert Signal Polarity (Bits 1:0)

Function:

When set, this bit activates an inversion of the signal polarity for the appropriate channel. This is useful if a board layout error has occurred, or other situations where a 180 degree phase shift is desirable.

8.3 DAC Volume & Mixing Control - Address 03h

7	6	5	4	3	2	1	0
Reserved	B=A	Soft	ZeroCross	ATAPI3	ATAPI2	ATAPI1	ATAPI0

8.3.1 Channel B Volume = Channel A Volume (Bit 6)

Function:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled. Volume and muting functions are effected by the Soft Ramp and ZeroCross functions below.

8.3.2 Soft Ramp or Zero Cross Enable (Bits 5:4)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 14 on page 41.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently mon-

itored and implemented for each channel. See Table 14 on page 41.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 14 on page 41.

Table 14. Soft Cross or Zero Cross Mode Selection

Soft	ZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled (default)
1	1	Soft Ramp and Zero Cross enabled

8.3.3 ATAPI Channel Mixing and Muting (Bits 3:0)

Function:

The CS4271 implements the channel mixing functions of the ATAPI CD-ROM specification. See Table 15 on page 42

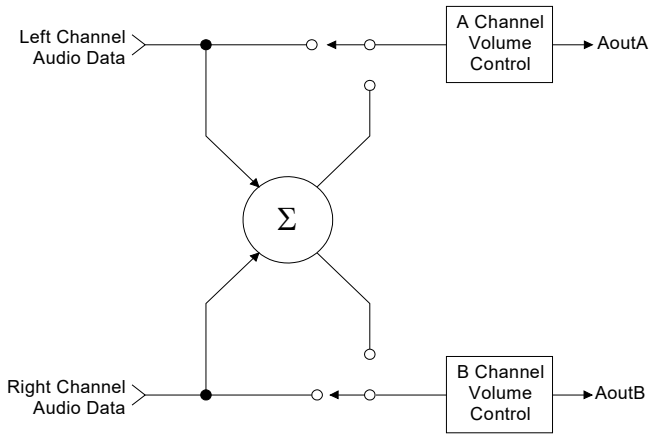


Figure 20. ATAPI Block Diagram

Table 15. ATAPI Decode

ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	bR
0	0	1	0	MUTE	bL
0	0	1	1	MUTE	b[(L+R)/2]
0	1	0	0	aR	MUTE
0	1	0	1	aR	bR
0	1	1	0	aR	bL
0	1	1	1	aR	b[(L+R)/2]
1	0	0	0	aL	MUTE
1	0	0	1	aL	bR
1	0	1	0	aL	bL
1	0	1	1	aL	b[(L+R)/2]
1	1	0	0	a[(L+R)/2]	MUTE
1	1	0	1	a[(L+R)/2]	bR
1	1	1	0	a[(L+R)/2]	bL
1	1	1	1	a[(L+R)/2]	b[(L+R)/2]

8.4 DAC Channel A Volume Control - Address 04h

See 8.5 DAC Channel B Volume Control - Address 05h

8.5 DAC Channel B Volume Control - Address 05h

7	6	5	4	3	2	1	0
MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

8.5.1 Mute (Bit 7)

Function:

The DAC output will mute when this bit is set. Though this bit is active high, it should be noted that the MUTEC pins are active low. The common mode voltage on the output will be retained when this bit is set. The muting function is effected, similar to attenuation changes, by the Soft and ZeroCross bits in the Volume and Mixing Control register. The MUTEC pin for the respective channel will become active during the mute period if the MUTE bit is set. Both the AMUTEC and BMUTEC will become active if either MUTE register is enabled and the MUTECB=A bit (register 7) is enabled.

8.5.2 Volume Control (Bits 6:0)

Function:

The digital volume control allows the user to attenuate the signal in 1 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 16. The volume changes are implemented as dictated by the Soft and ZeroCross bits in the DAC Volume & Mixing Control register (see section 8.3.2).

Table 16. Digital Volume Control Example Settings

Binary Code	Decimal Value	Volume Setting
0000000	0	0 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

8.6 ADC Control - Address 06h

7	6	5	4	3	2	1	0
Reserved	Reserved	Dither16	ADC_DIF	MUTEA	MUTEB	HPFDisableA	HPFDisableB

8.6.1 Dither for 16-Bit Data (Bit 5)

Function:

When set, this bit activates the Dither for 16-Bit Data feature as described in “Dither for 16-Bit Data” on page 30.

8.6.2 ADC Digital Interface Format (Bit 4)

Function:

The required relationship between LRCK, SCLK and SDOUT for the ADC is defined by the ADC Digital Interface Format. The options are detailed in Table 17 and may be seen in Figure 3 and 4.

Table 17. ADC Digital Interface Formats

ADC_DIF	Description	Format	Figure
0	Left Justified, up to 24-bit data (default)	0	3
1	I^2S, up to 24-bit data	1	4

8.6.3 ADC Channel A & B Mute (Bits 3:2)

Function:

When this bit is set, the output of the ADC for the selected channel will be muted.

8.6.4 Channel A & B High Pass Filter Disable (Bits 1:0)

Function:

When this bit is set, the internal high-pass filter for the selected channel will be disabled.The current DC offset value will be frozen and continue to be subtracted from the conversion result. See “High Pass Filter and DC Offset Calibration” on page 30.

8.7 Mode Control 2 - Address 07h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LOOP	MUTECA=B	FREEZE	CPEN	PDN

8.7.1 Digital Loopback (Bit 4)

Function:

When this bit is set, an internal digital loopback from the ADC to the DAC will be enabled. Please refer to “Internal Digital Loopback” on page 30.

8.7.2 AMUTEC = BMUTEC (Bit 3)

Function:

When this function is enabled, the individual controls for AMUTEC and BMUTEC are internally connected through an AND gate prior to the output pins. Therefore, the external AMUTEC and BMUTEC pins will go active only when the requirements for both AMUTEC and BMUTEC are valid.

8.7.3 Freeze (Bit 2)

Function:

This function allows modifications to the control port registers without the changes taking effect until FREEZE is disabled. To make multiple changes in the Control Port registers take effect simultaneously, set the FREEZE bit, make all register changes, then clear the FREEZE bit.

8.7.4 Control Port Enable (Bit 1)

Function:

This bit is cleared by default, allowing the device to power-up in Stand-Alone Mode. Control Port Mode can be accessed by setting this bit. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. See “Recommended Power-Up Sequence - Access to Control Port Mode” on page 27.

8.7.5 Power Down (Bit 0)

Function:

The device will enter a low-power state whenever this bit is set. The power-down bit is set by default and must be cleared before normal operation in Control Port Mode can occur. The contents of the control registers are retained when the device is in power-down.

8.8 Chip ID - Register 08h

B7	B6	B5	B4	B3	B2	B1	B0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

This is a Read-Only register.

8.8.1 Chip ID (Bits 7:4)

Function:

Chip ID code for the CS4271. Permanently set to 0000b (0h).

8.8.2 Chip Revision (Bits 3:0)

Function:

Chip Revision code for the CS4271.

Revision A is coded as 0000b (0h).
Revision B is coded as 0000b (0h).

9. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

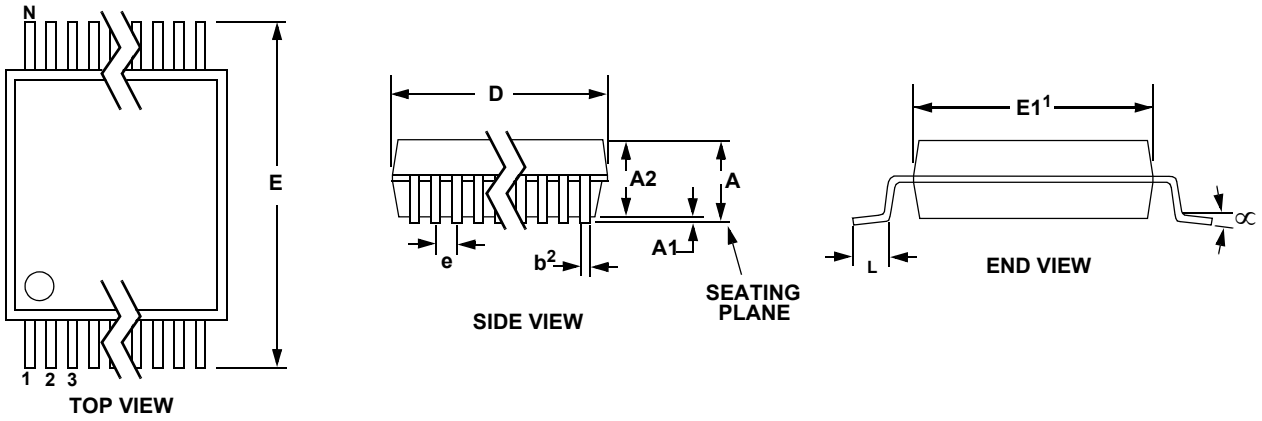
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

10.PACKAGE DIMENSIONS

28L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.47	--	--	1.20	
A1	0.002	0.004	0.006	0.05	0.10	0.15	
A2	0.03150	0.035	0.04	0.80	0.90	1.00	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.378 BSC	0.382 BSC	0.386 BSC	9.60 BSC	9.70 BSC	9.80 BSC	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.029	0.50	0.60	0.75	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes: 1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance (Note 4)	28-TSSOP	θ_{JA}	-	37	-	°C/Watt
		θ_{JC}	-	13	-	°C/Watt
Allowable Junction Temperature			-	-	135	°C

Notes: 4. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

11.APPENDIX

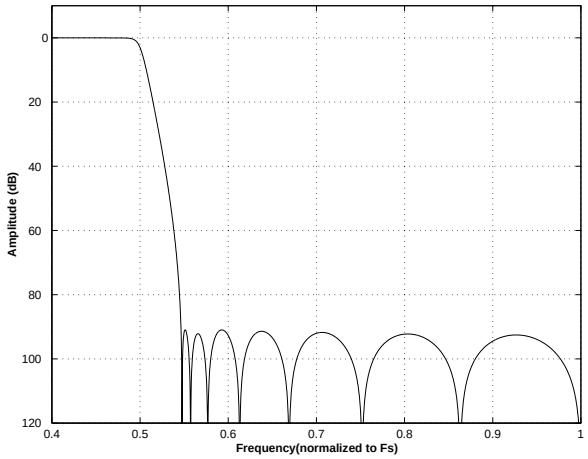


Figure 21. DAC Single Speed (fast) Stopband Rejection

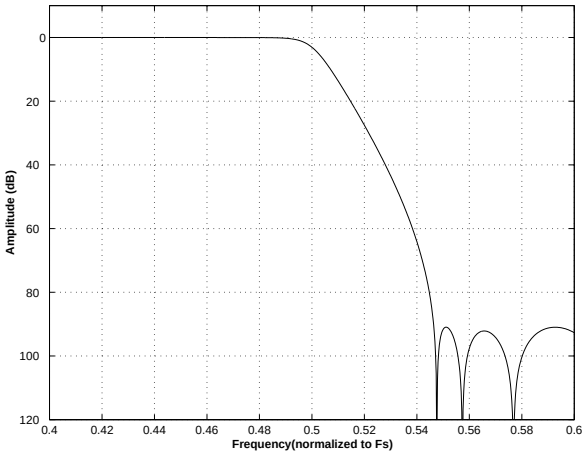


Figure 22. DAC Single Speed (fast) Transition Band

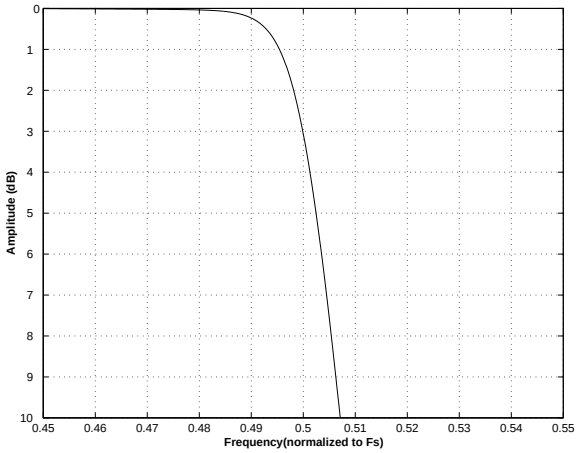


Figure 23. DAC Single Speed (fast) Transition Band (detail)

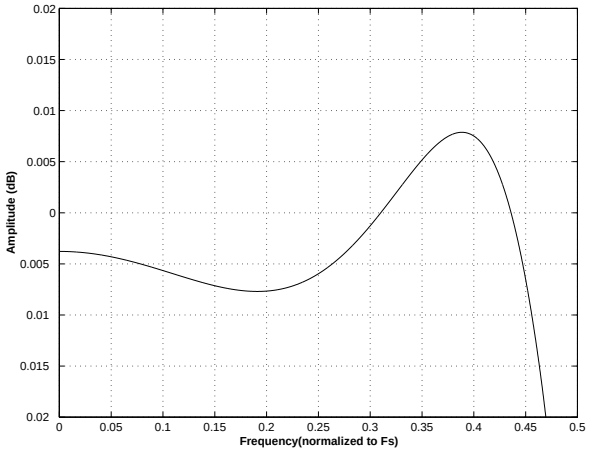


Figure 24. DAC Single Speed (fast) Passband Ripple

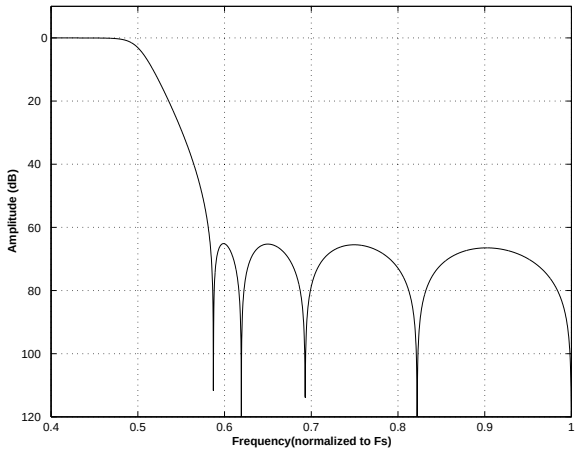


Figure 25. DAC Single Speed (slow) Stopband Rejection

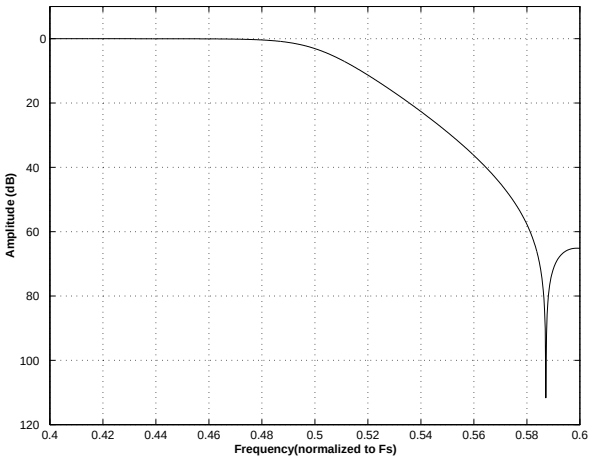


Figure 26. DAC Single Speed (slow) Transition Band

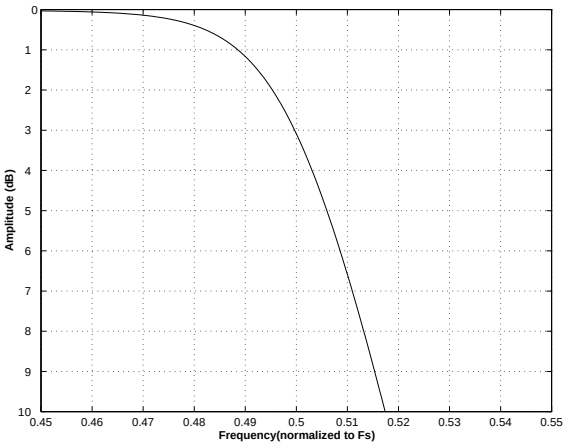


Figure 27. DAC Single Speed (slow) Transition Band (detail)

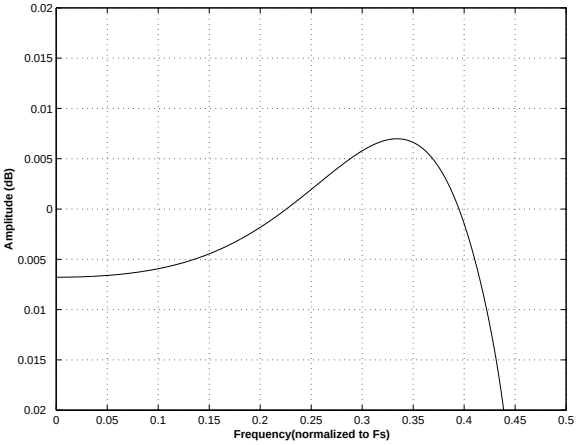


Figure 28. DAC Single Speed (slow) Passband Ripple

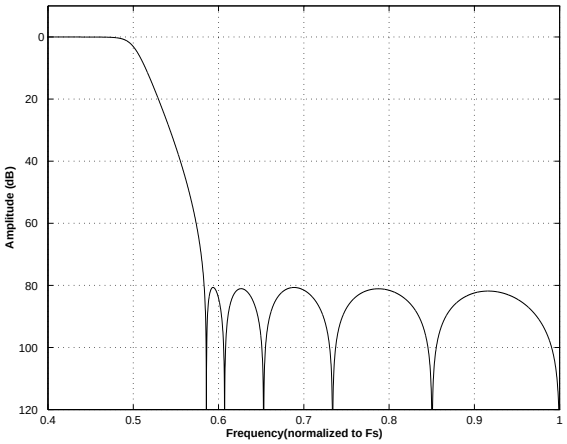


Figure 29. DAC Double Speed (fast) Stopband Rejection

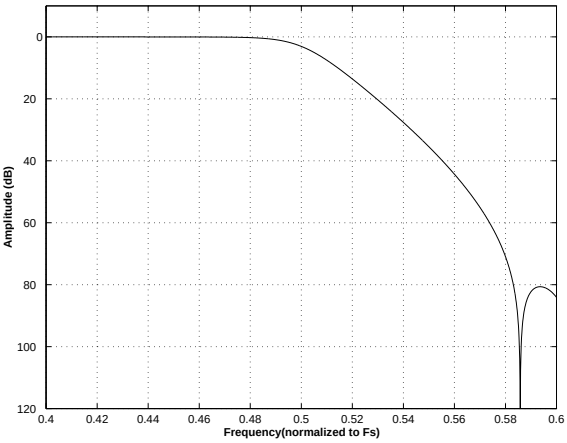


Figure 30. DAC Double Speed (fast) Transition Band

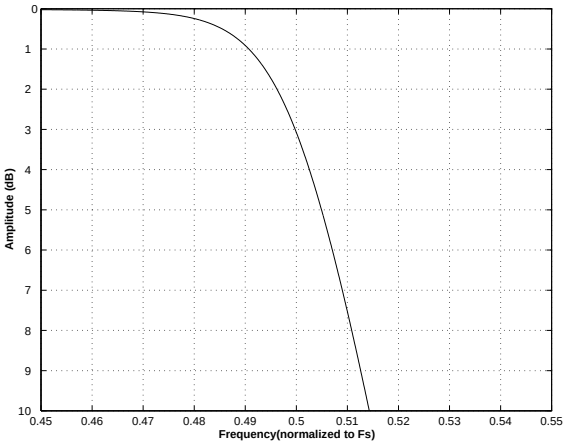


Figure 31. DAC Double Speed (fast) Transition Band (detail)

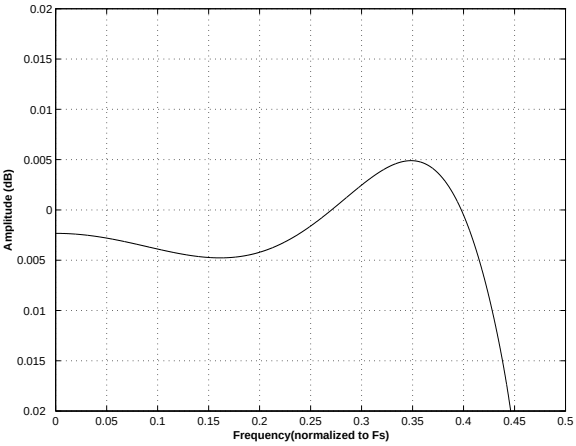


Figure 32. DAC Double Speed (fast) Passband Ripple

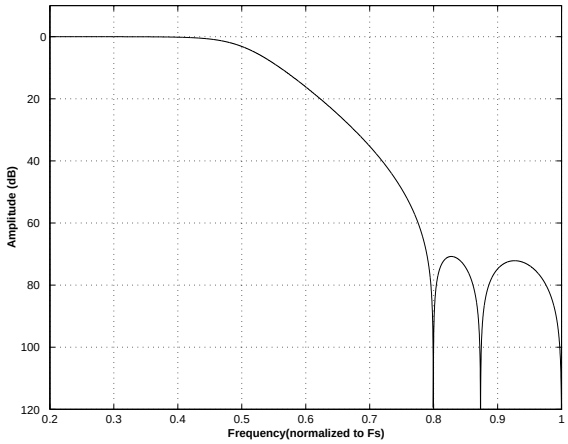


Figure 33. DAC Double Speed (slow) Stopband Rejection

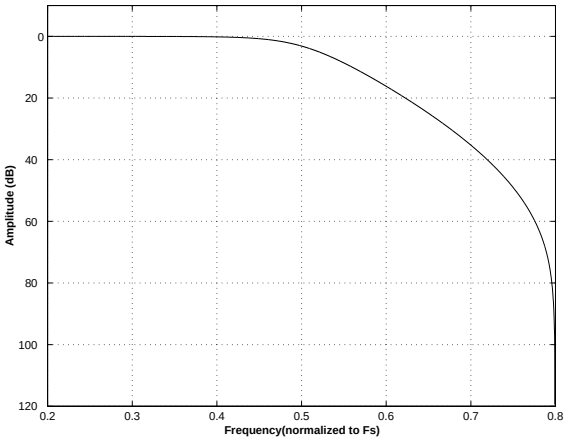


Figure 34. DAC Double Speed (slow) Transition Band

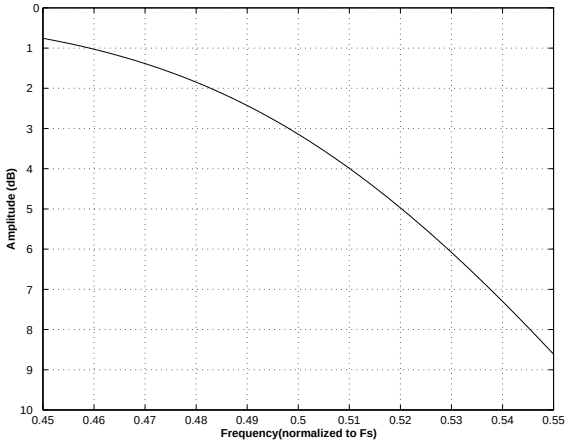


Figure 35. DAC Double Speed (slow) Transition Band (detail)

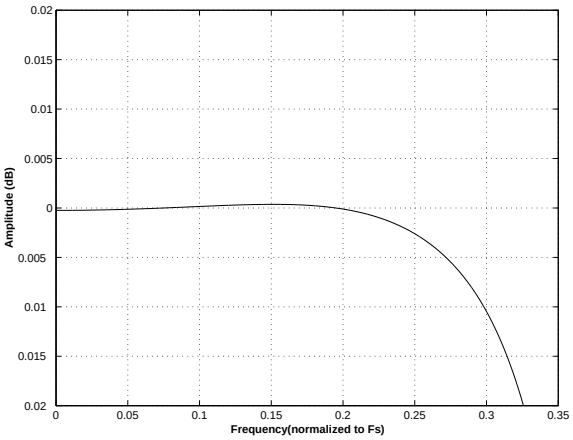


Figure 36. DAC Double Speed (slow) Passband Ripple

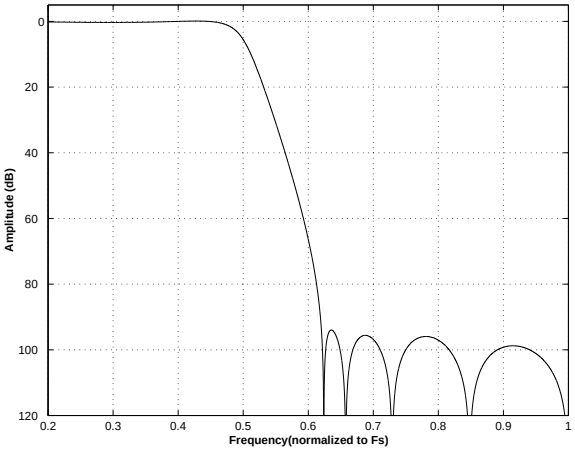


Figure 37. DAC Quad Speed (fast) Stopband Rejection

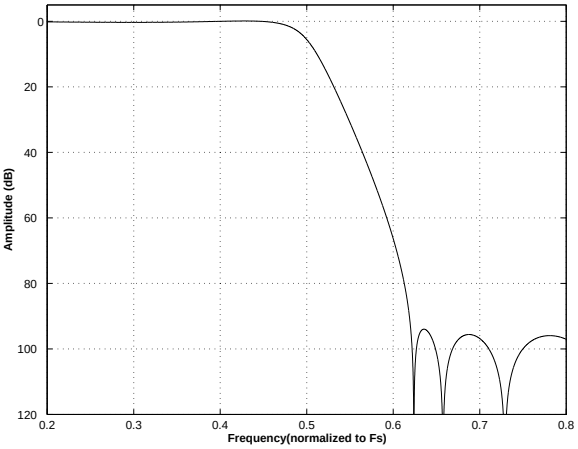


Figure 38. DAC Quad Speed (fast) Transition Band

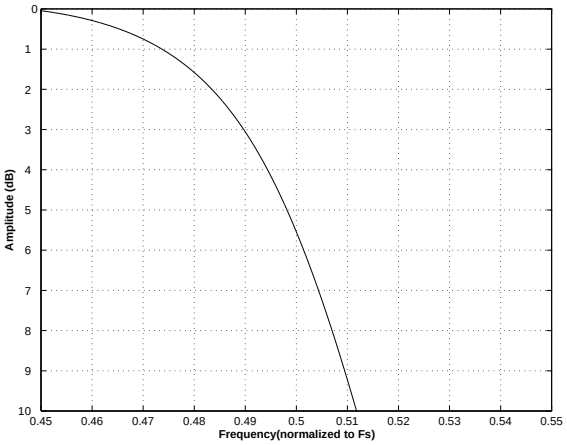


Figure 39. DAC Quad Speed (fast) Transition Band (detail)

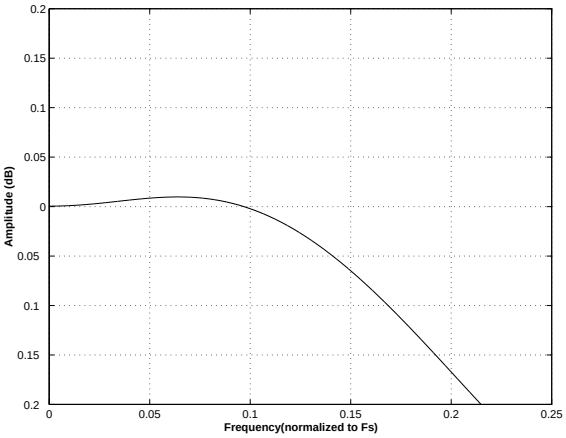


Figure 40. DAC Quad Speed (fast) Passband Ripple

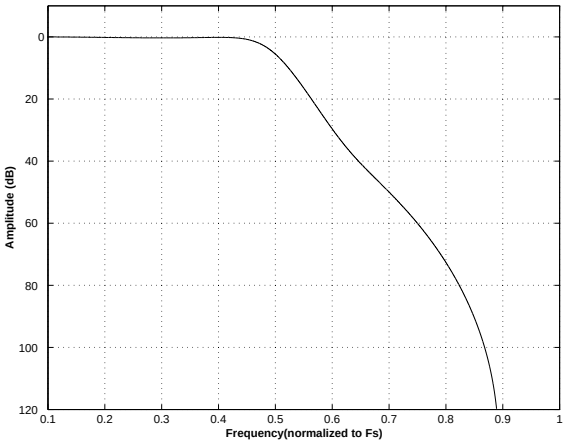


Figure 41. DAC Quad Speed (slow) Stopband Rejection

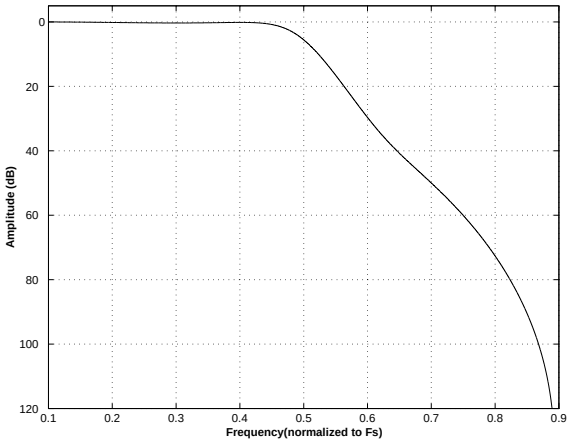


Figure 42. DAC Quad Speed (slow) Transition Band

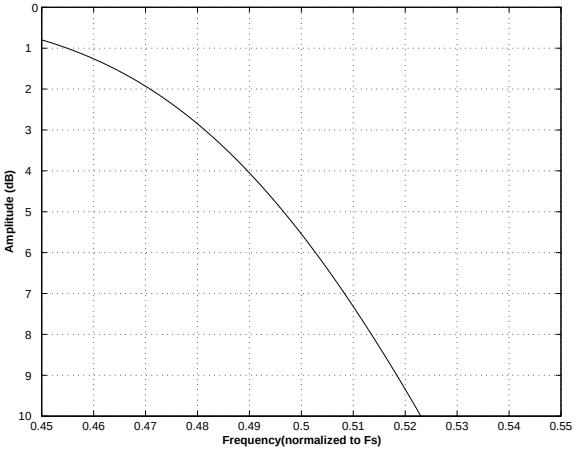


Figure 43. DAC Quad Speed (slow) Transition Band (detail)

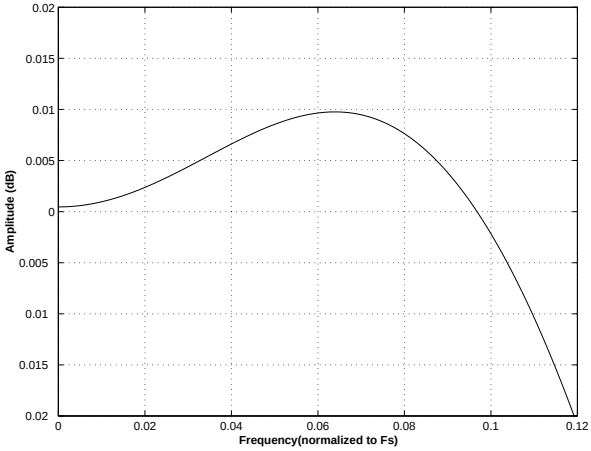


Figure 44. DAC Quad Speed (slow) Passband Ripple

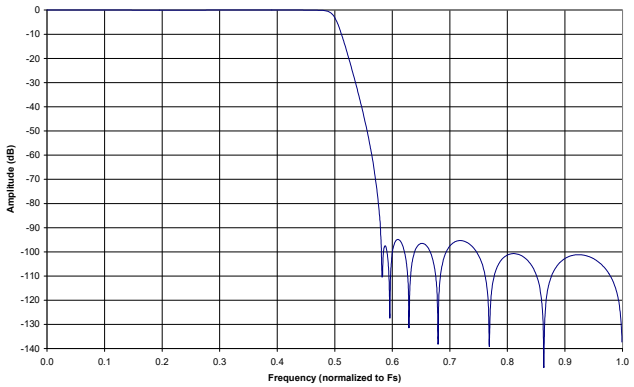


Figure 45. ADC Single Speed Mode Stopband Rejection

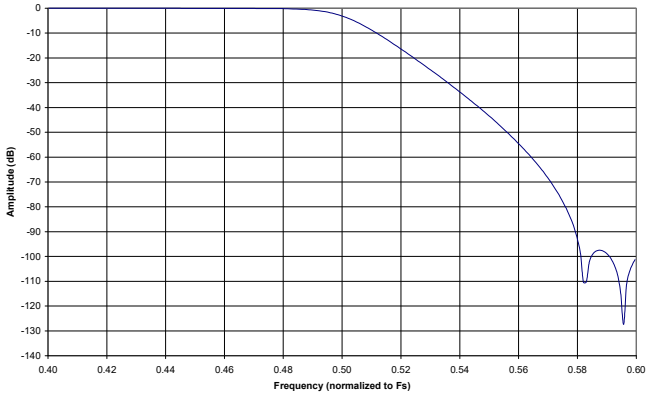


Figure 46. ADC Single Speed Mode Transition Band

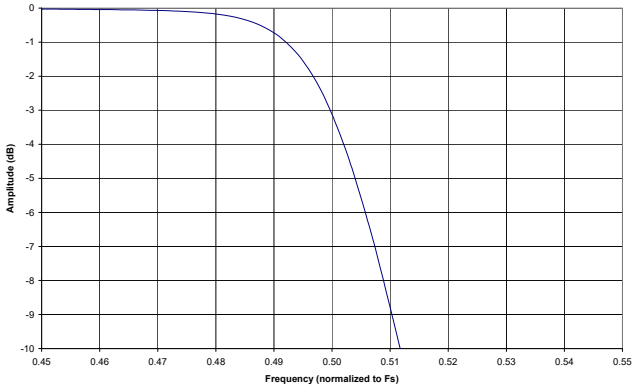


Figure 47. ADC Single Speed Mode Transition Band (Detail)

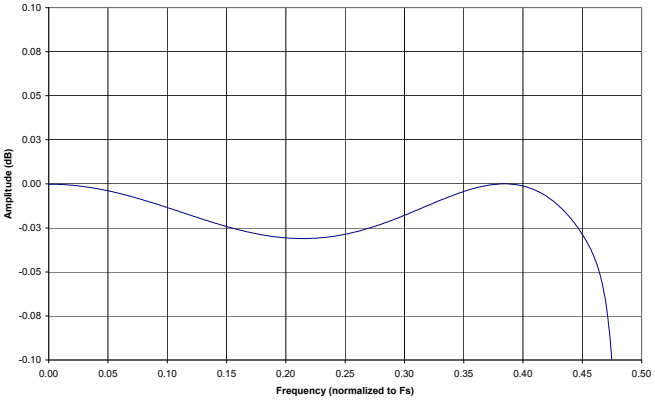


Figure 48. ADC Single Speed Mode Passband Ripple

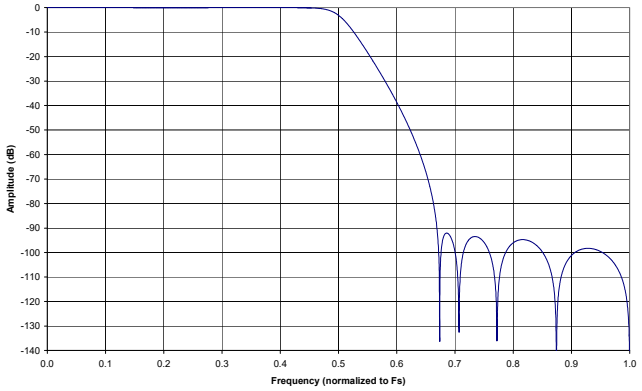


Figure 49. ADC Double Speed Mode Stopband Rejection

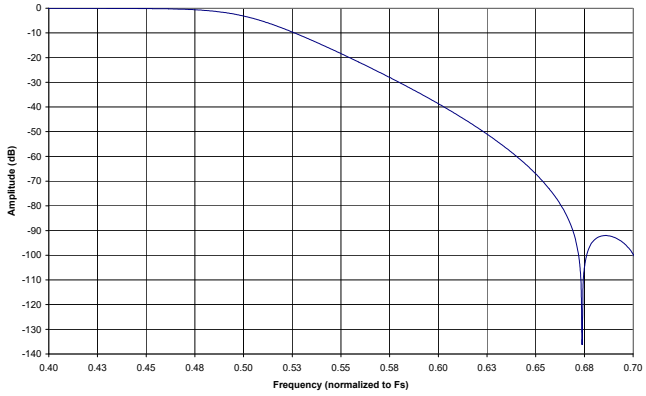


Figure 50. ADC Double Speed Mode Transition Band

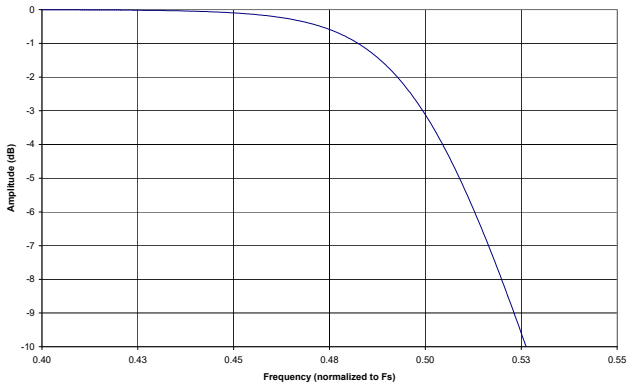


Figure 51. ADC Double Speed Mode Transition Band (Detail)

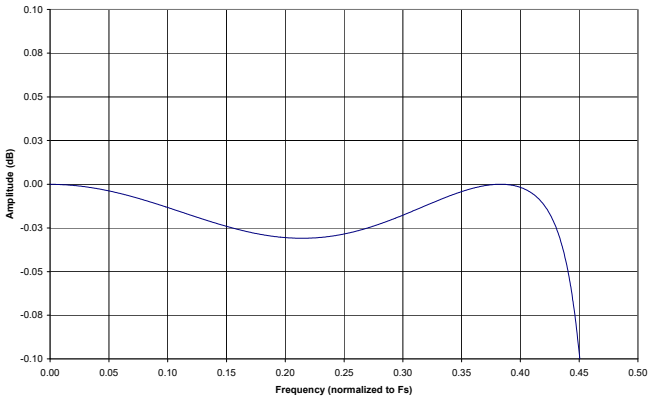


Figure 52. ADC Double Speed Mode Passband Ripple

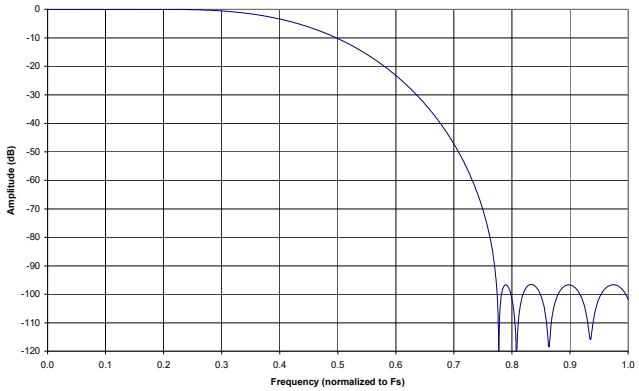


Figure 53. ADC Quad Speed Mode Stopband Rejection

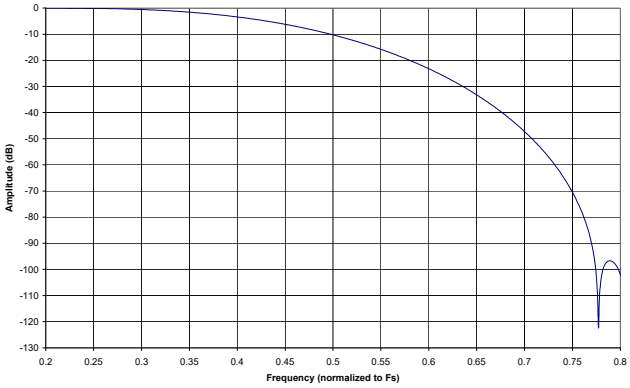


Figure 54. ADC Quad Speed Mode Transition Band

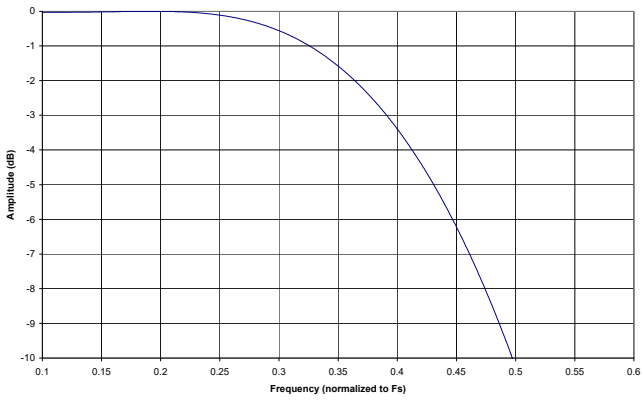


Figure 55. ADC Quad Speed Mode Transition Band (Detail)

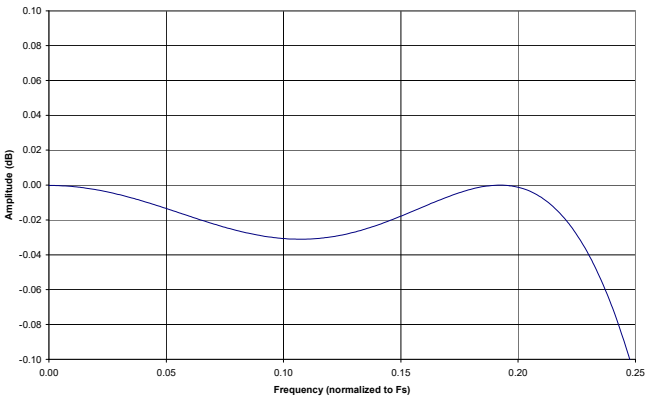


Figure 56. ADC Quad Speed Mode Passband Ripple

Table 18. Revision History

Release	Date	Changes
A1	January 2003	Advance Release
PP1	March 2003	Preliminary Release
PP2	October 2003	- Corrected the description of pins 17 and 18 on page 6. - Corrected the description of pins 17 and 18 on page 8. - Updated Figure 8 on page 23. - Updated Table 9 on page 29. - Updated the DC Electrical Characteristics table on page 17. - Updated the DAC Analog Filter Response tables on pages 10 and 11. - Updated the ADC Digital Filter Characteristics table on page 16. - Updated the DAC Full Scale Differential Output Voltage specification on pages 10 and 11.
PP3	September 2004	Add lead-free device ordering info.
F1	August 2005	Final Release - Updated Ordering Information on page 2. - Updated Specified Operating Conditions table on page 9 to reflect ordering-suffix independent temperature grade information. - Updated DAC Analog Characteristics tables on pages 10 and 11 to reflect ordering-suffix independent temperature grade information. - Updated ADC Analog Characteristics tables on pages 14 and 15 to reflect ordering-suffix independent temperature grade information. - Updated the DC Electrical Characteristics table on page 17. - Corrected error in the SCLK Period units shown in the Switching Characteristics - Serial Audio Port table on page 18. - Corrected error in the Memory Address Pointer table on page 36. - Updated Chip ID register description on page 44.
F2	October 2021	- Updated Ordering Information as per PCN-2020-141.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

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