User's Guide

LMQ61460EVM-400K User's Guide

Sam Jaffe

The LMQ61460-Q1 evaluation module (EVM) is designed to help customers evaluate the performance of the LMQ61460-Q1 synchronous step-down voltage converter. This EVM implements the LMQ61460-Q1 in a 14-pin wettable flanks Hotrod™ package, as shown in Table 1-1. It is capable of delivering 5-V output voltage and up to 6-A load current switching at 400 kHz with exceptional efficiency and output accuracy in a very small solution size. The EVM provides multiple power connectors and test points. In addition to an optimized EMI board layout, the LMQ61460-Q1 utilizes integrated bypass capacitors which results in great EMI performance.

Table 1-1. Device and Package Configurations

CONVERTER	IC	PACKAGE
U1	LMQ61460-Q1	14-pin wettable flanks Hotrod package 4.0 mm × 3.5 mm × 1.0 mm

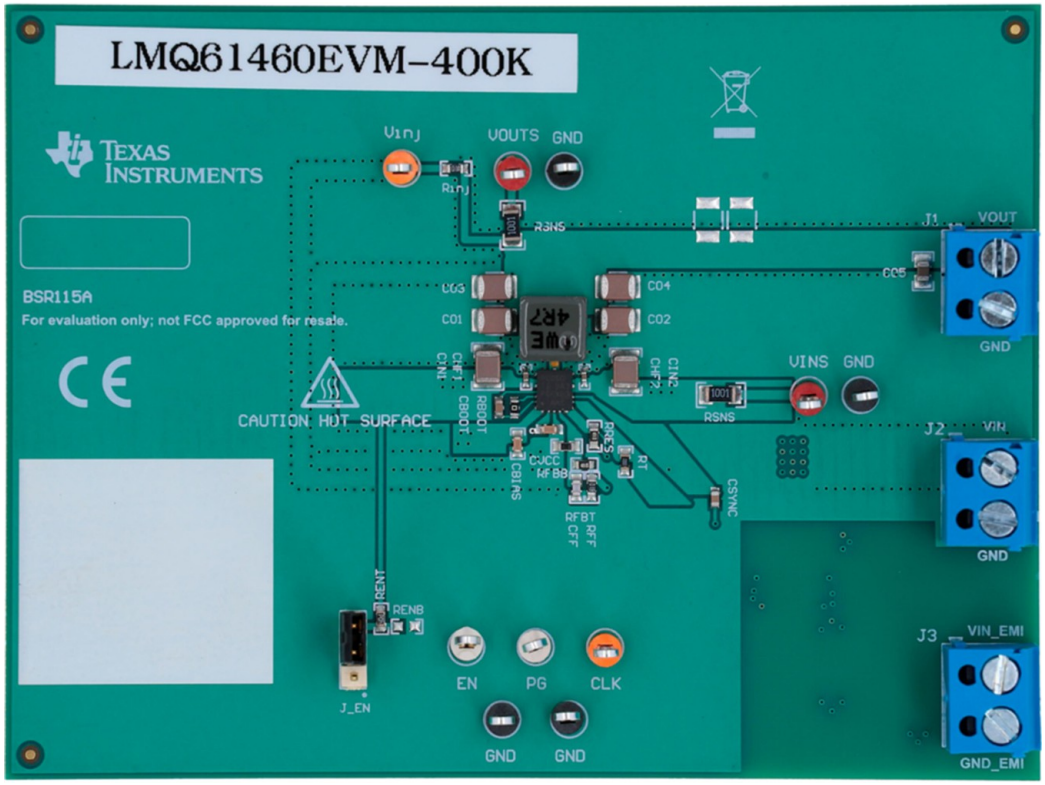


Figure 1-1. LMQ61460EVM-400K Top View

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1 Introduction

1.1 LMQ61460-Q1 Synchronous Step-Down Voltage Converter

The LMQ61460-Q1 is an easy-to-use synchronous step-down DC/DC converter capable of delivering up to 6 A of load current from a supply voltage ranging from 3 V to 36 V. The LMQ61460-Q1 provides exceptional efficiency and output accuracy in a very small solution size. The LMQ61460-Q1 is capable of delivering 6 A of load current and implements peak current mode control. The following are additional features that provide both flexible and easy-to-use solutions for a wide range of applications:

- Adjustable switching frequency (RT)
- Synchronization to an external clock (CLK jumper)
- FPWM variant (LMQ61460AFS) (IC swap)
- Power-good flag (PG jumper)
- Precision enable (EN jumper with RENT and RENB resistors)

Automatic frequency foldback at light load and optional external bias improve efficiency over the entire load range. The device requires few external components and has a pinout designed for optimal EMI and thermal performance. Protection features include the following:

- Thermal shutdown
- Input undervoltage lockout
- Cycle-by-cycle current limiting
- Hiccup short-circuit protection

For a quick reference, Figure 1-1 shows the pin configuration of the LMQ61460-Q1.

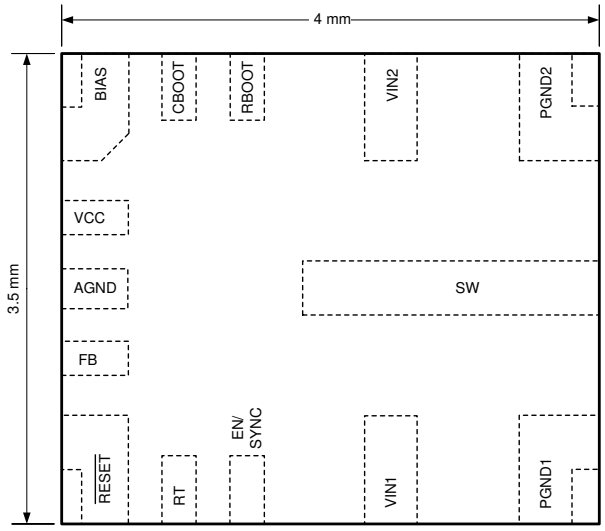


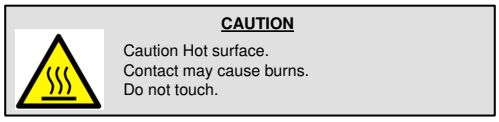
Figure 1-1. LMQ61460-Q1 Pin Configuration (Top View)

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2 Quick Start Guide

1. Connect the voltage supply between the VIN and GND connectors or between VIN_EMI and GND_EMI to include the on-board input filter in the input path. Use short and thick gauge wires to minimize inductance and IR drop. Note that sense points for V_{IN} and V_{OUT} are provided.
2. Connect the load of the converter between VOUT and GND connectors using short and thick wires.
3. Set the supply voltage at an appropriate level between 6 V to 36 V. The 6 V minimum input voltage ensures enough head room for V_{OUT} to equal 5 V at a 6 A load current. Set the current limit of the supply to an appropriate level to supply needed current and protection.
4. Turn on the power supply. With the default configuration, the EVM powers up and provides V_{OUT} equal to 5 V.
5. Monitor the output voltage with sense points. The maximum load current is 6 A with the LMQ61460-Q1. Note that the maximum output current may need to derate if ambient temperature is high, especially if device is operated at higher frequency, that is 2.1 MHz.

See Figure 5-1 for connector locations.



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3 Detailed Descriptions

This section describes the connectors on the EVM and how to properly connect, set up, and use the EVM. See Figure 1-1 for a top view of the EVM.

VOUT Output voltage of the converter

VOUT connectors connect to the power inductor and output capacitors. Connect the load between the VOUT connector and the GND connector to provide load current. Connect the loading device to the board with short and thick wires to handle the large DC output current.

GND Ground of the converter

The GND is connected to the PGND and AGND pins of the device as well as the ground of the input and output capacitors. The GND connections next to VIN, VIN_EMI, and VOUT connectors are meant for current return path for the supply voltage and load, respectively. Connectors are provided in pairs to allow easy and accurate sensing of voltages. Connect to supply and load grounds with short and thick wires. Other GND connectors are for signal measurement and probing.

V_{IN} Input voltage to the converter

The V_{IN} connector connects to the input capacitors and the VIN pins of the LMQ61460-Q1. Connect the supply voltage from a power supply or a battery between VIN and GND connectors as power input to the device. The input voltage (V_{IN}) range must be higher than 3.9 V for the device to start up and above 3 V to maintain operation. A V_{IN} higher than 6 V provides a regulated 5-V output voltage. Maximum V_{IN} is limited to 36 V to avoid damaging the device. The current limit on the supply must be high enough to provide the needed supply current. The supply voltage must be connected to the board with short and thick wires to handle the required input current at maximum load current. If long cables are used to power up the board, damping must be provided by adding CFLT3 and RFLT3 to avoid oscillation between the cable parasitic inductance and the existing low-ESR ceramic capacitors.

VIN_EMI Low EMI option

If the input filter is required, connect the supply voltage between VIN_EMI and GND_EMI. The supply voltage must be connected to the board with short and thick wires.

The input filter consists of the following: CF1, CF2, CF3, CF4, CF5, CF6, and L2. CD1, CD2, RD1, and RD2 are provided to allow more options for filter optimization. To include the input filter in the power path, connect the supply voltage between the VIN_EMI and GND_EMI connectors. The output of the filter is connected to V_{IN}, which is connected to the V_{IN} pins of the LMQ61460-Q1.

Conducted EMI arises from the operation of switching circuits.

GND_EMI Ground return for the input filter

This is the current return path for the supply connected to VIN_EMI. It provides a short-loop connection to the input filter capacitors to best filter the conducted noise generated from the PCB. Use VIN_EMI and GND_EMI connection if input filter is used and conducted EMI test is desired.

CLK For synchronization clock input

The CLK input connector is designed for external clock input to the EN/SYNC pin. Switching action of the buck is synchronized to the external clock when it is present. The operation mode automatically changes to forced PWM mode, maintaining a constant switching frequency over the entire load range while the clock signal is present.

EN To monitor the EN pin or control EN signal

This test point is used to monitor the voltage on the device EN pin. By default, the EN pin is connected to the mid-point of an enable divider. Note that the lower resistor in this divider, RENB, is not populated so the IC turns on by default. Populate RENB to adjust UVLO. Apply a voltage to EN to externally enable or disable the device.

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PG To monitor the PGOOD/RESET pin

The PGOOD flag indicates whether the output voltage is within the regulation band. The RESET pin (synonymous with PGOOD pin) of the device is an open-drain output and is pulled up to V_{OUT} through a 100 k resistor. This pin pulls to GND when the output voltage is out of regulation.

Vinj For measuring AC response

A low value resistor, Rinj, is placed between VOUT and this node. The feedback divider of the board is connected to this node. An AC signal is applied across Rinj when taking measurements for bode plots.

VOUTS VOUT sense

This connector is provided for measuring the output voltage accurately.

VINS VIN sense

This connector is provided for measuring the input voltage accurately.

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4 Schematic

The bill of materials is tabulated in *Section 7*. In addition, Figure 4-1 shows the corresponding schematic.

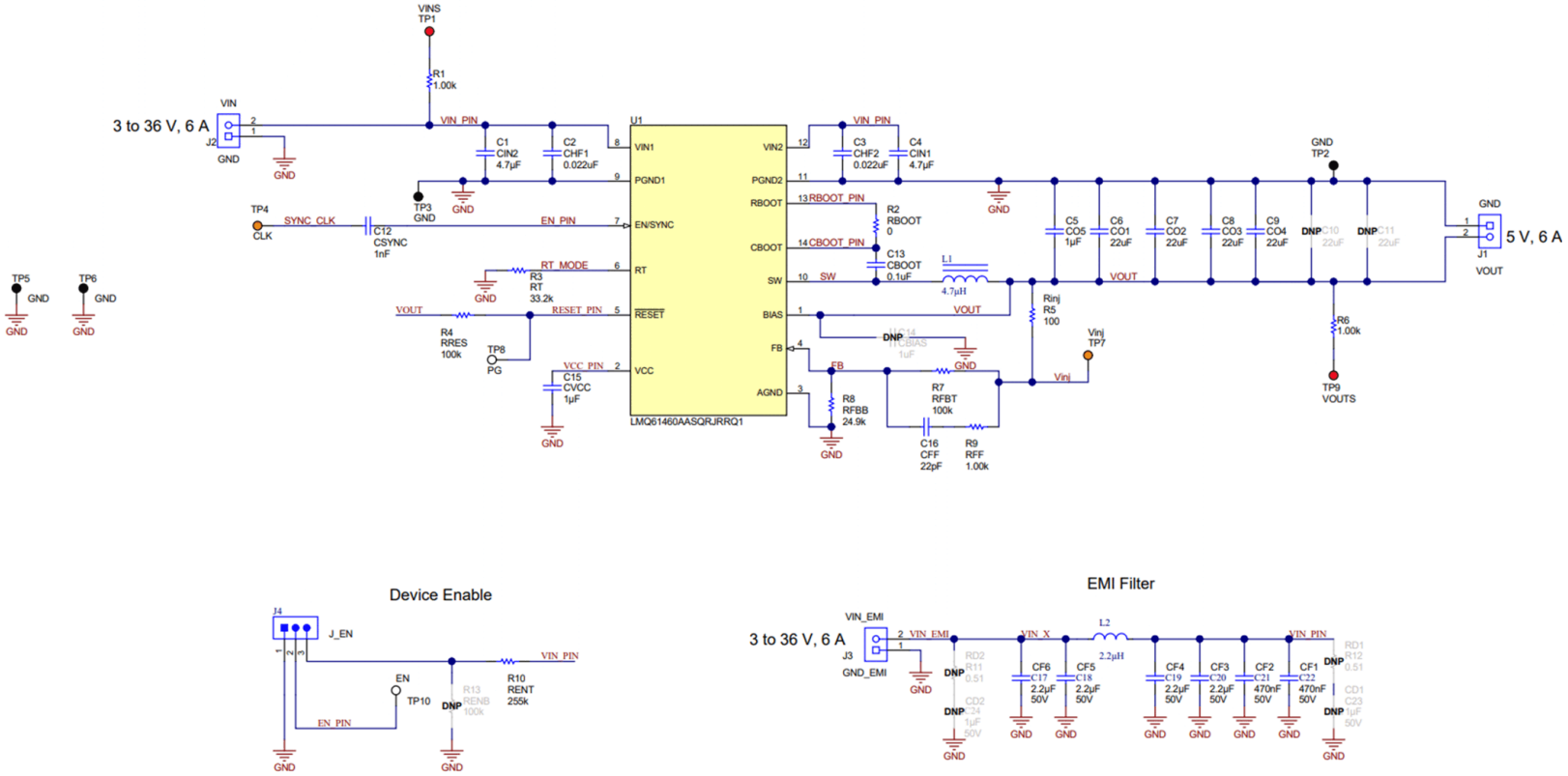


Figure 4-1. LMQ61460EVM-400K Schematic

Note

Long leads and additional inductance in used to power the DC/DC may cause issues for ideal device operation. RD2, CD2, RD1, and CD1 are placeholders for damping networks to be populated. For more information regarding this topic, reference the *EMI Filter Components and Their Nonidealities for Automotive DC/DC Regulators Technical Brief*.

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4.1 Alternative BOM Configurations

Table 4-1. Different BOM Configurations

VOUT	FREQUENCY	RFBB	RT	COUT	CIN + CHF	L1
3.3 V	400 kHz	43.2 kΩ	33.2 kΩ	6 x 22 µF	2 x 4.7 µF + 2 x 100 nF	4.7 µH (XHMI6060)
3.3 V	2100 kHz	43.2 kΩ	6.04 kΩ	3 x 22 µF	2 x 4.7 µF + 2 x 100 nF	1 µH (XEL5030)
5 V	400 kHz	24.9 kΩ	33.2 kΩ	4 x 22 µF	2 x 4.7 µF + 2 x 100 nF	4.7 µH (XHMI6060)
5 V	2100 kHz	24.9 kΩ	6.04 kΩ	3 x 22 µF	2 x 4.7 µF + 2 x 100 nF	1 µH (XEL5030)

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5 Board Layout

Figure 5-1 through Figure 5-5 show the board layout for the LMQ61460-Q1 EVM. The EVM offers resistors, capacitors, and test points to configure the following:

- Output voltage (RFBT and RFBB)
- Precision enable pin (RENT and RENB)
- Set frequency (RT)
- External clock synchronization (CLK jumper)

The 14-pin Hotrod package with integrated capacitors offers a very small size and low-noise solution. The PCB consists of a 4-layer design. There are 2-oz copper planes on the top and bottom and 1-oz copper mid-layer planes to route signals and dissipate heat with an array of thermal vias to connect to all four layers.

Test points have been provided for ease of use to connect the power supply and required load, and to monitor critical signals.

The board measures 3.00" x 4.00" (76mm x 101mm).

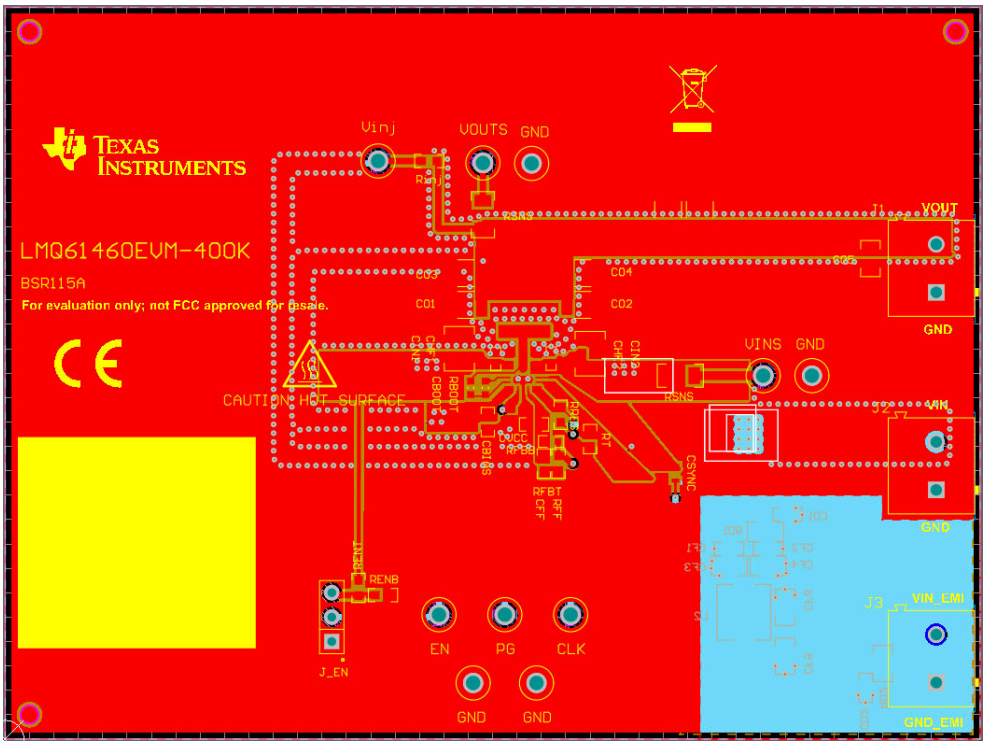


Figure 5-1. Top View with Silkscreen

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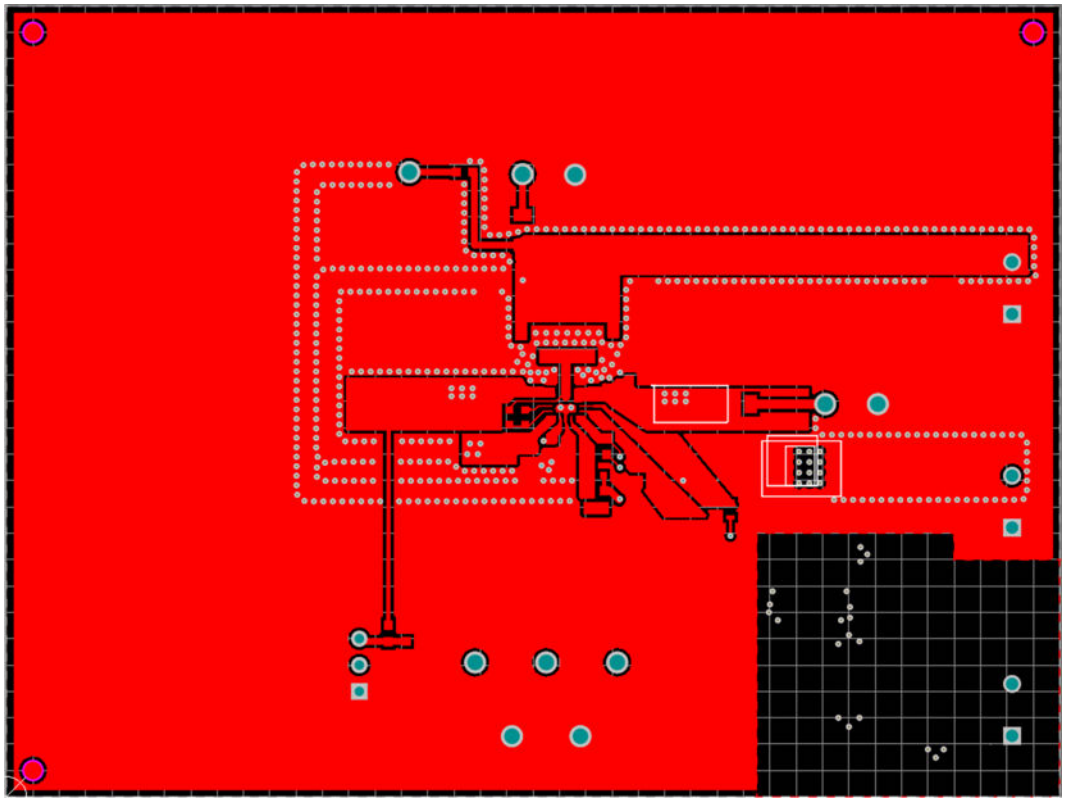


Figure 5-2. Top Layer

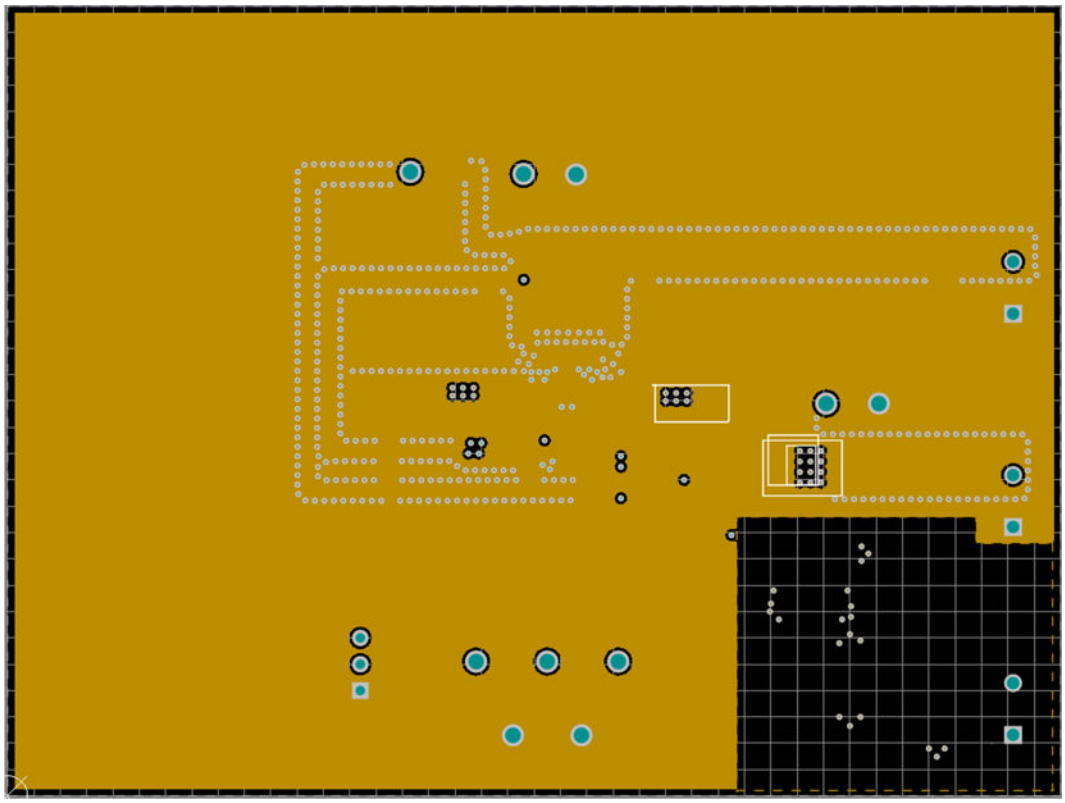


Figure 5-3. Signal Layer 1 - Ground Plane

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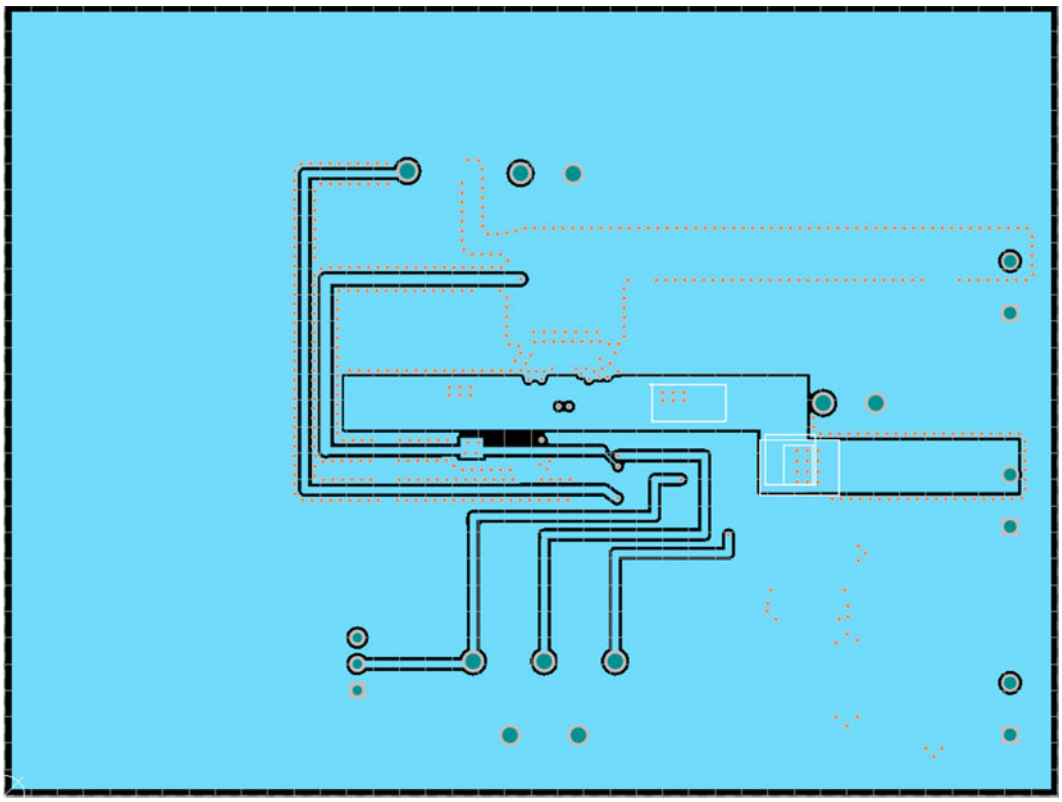


Figure 5-4. Signal Layer 2 - Routing

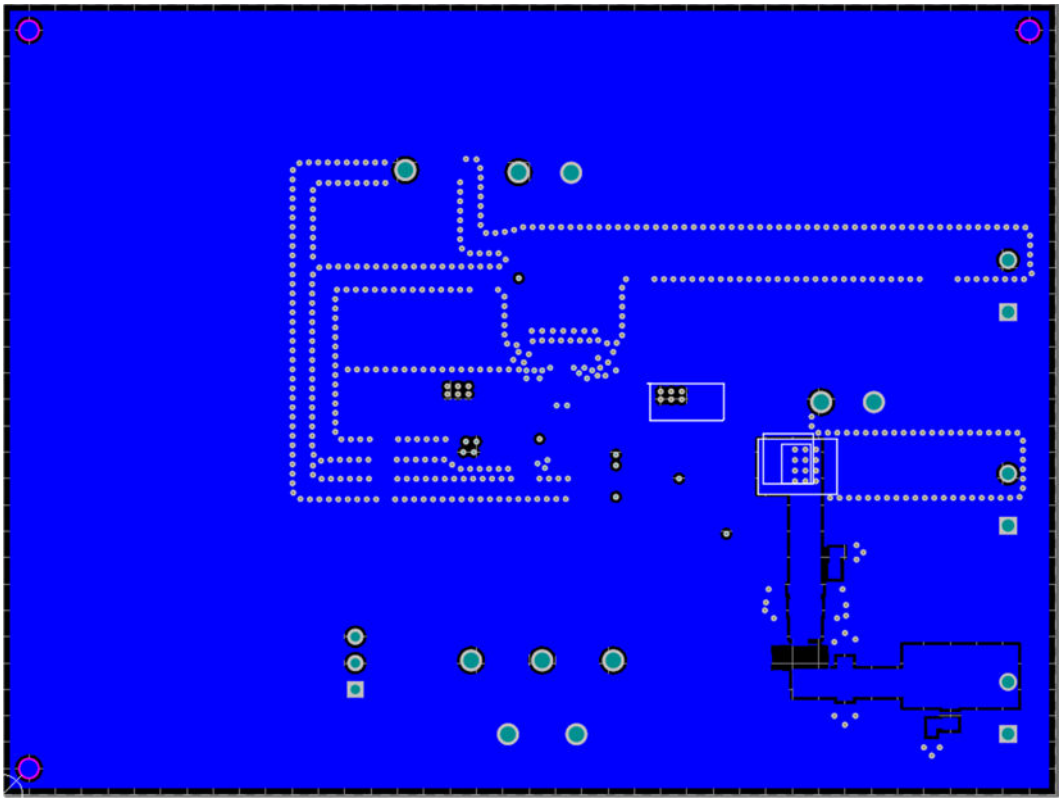


Figure 5-5. Bottom Layer

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6 LMQ61460EVM-400K Board Test Results

6.1 EMI

The EMI measurements were taken following CISPR 25, Class 5 standards. The measurements were taken at 13.5 VIN, 5 VOUT with a 6 A load switching at 400kHz.

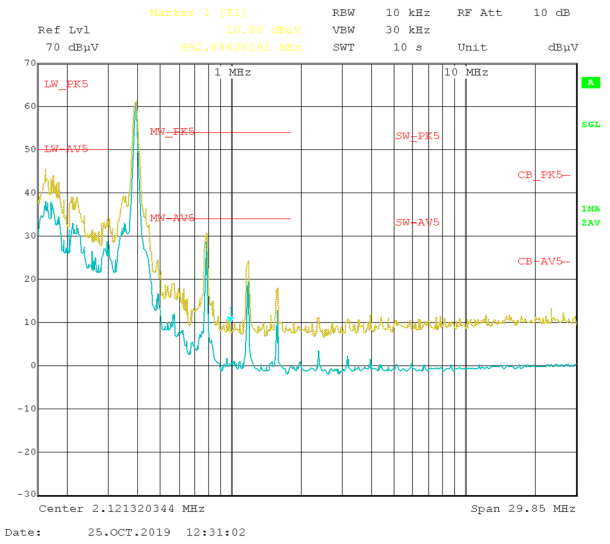


Figure 6-1. Conducted EMI Measurement with CISPR 25 Class 5 Limit Lines (150 kHz to 30 MHz)

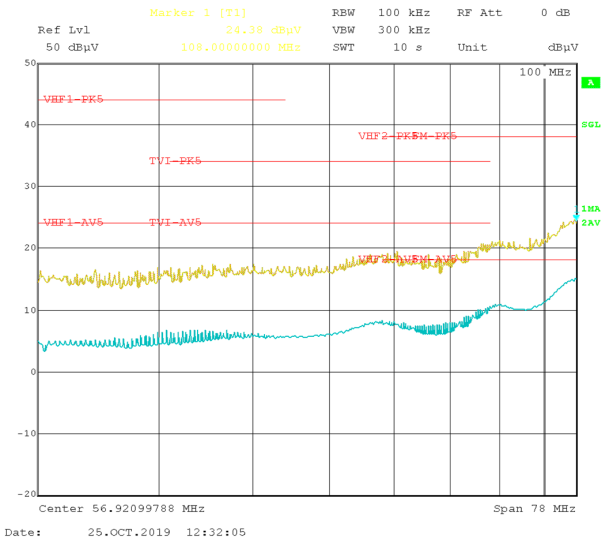


Figure 6-2. Conducted EMI Measurement with CISPR 25 Class 5 Limit Lines (30 MHz to 108 MHz)

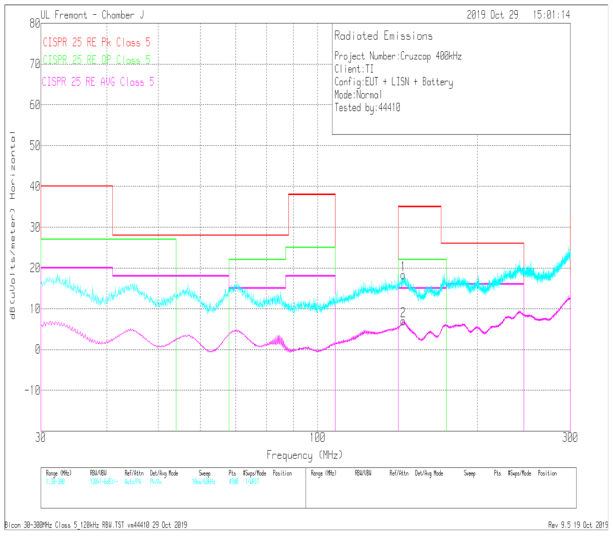


Figure 6-3. Radiated EMI Measurement with Horizontal Bicon Antenna Under CISPR 25 Class 5 Limits

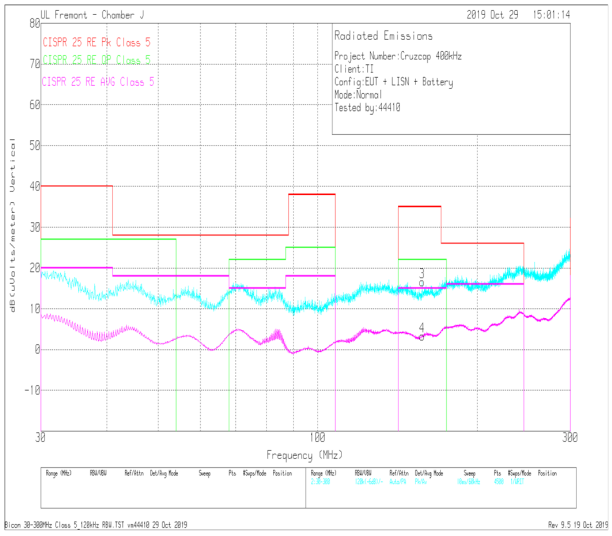


Figure 6-4. Radiated EMI Measurement with Vertical Bicon Antenna Under CISPR 25 Class 5 Limits

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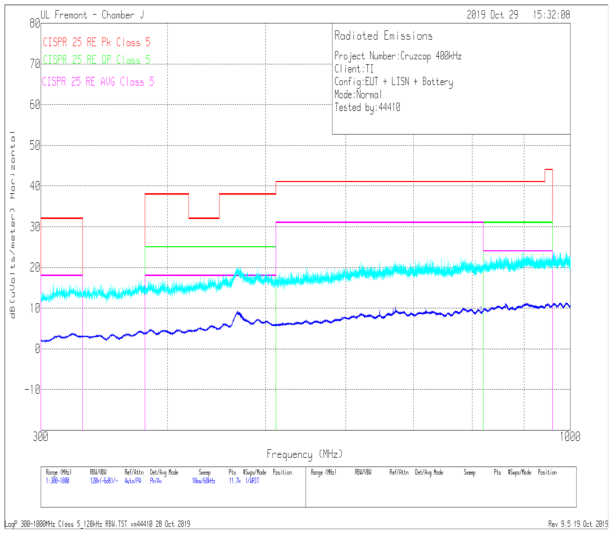


Figure 6-5. Radiated EMI Measurement with Horizontal Log Antenna Under CISPR 25 Class 5 Limits

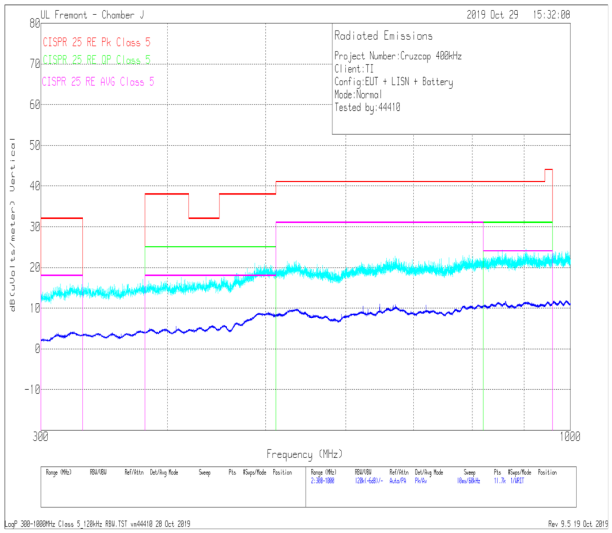


Figure 6-6. Radiated EMI Measurement with Vertical Log Antenna Under CISPR 25 Class 5 Limits

6.2 Board Efficiency

This section provides efficiency plots for the board with LMQ61460AAS populated for Auto mode efficiency and LMQ61460AFS populated for FPWM mode efficiency. For 2.1-MHz data, the output stage has to be changed from the default BOM. The inductor (L1) selected was XEL5030-102MEB.

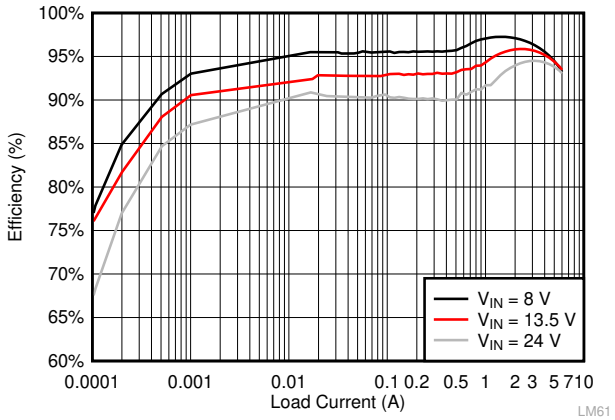


Figure 6-7. F_{SW} = 400 kHz, 5 VOUT, Auto Mode

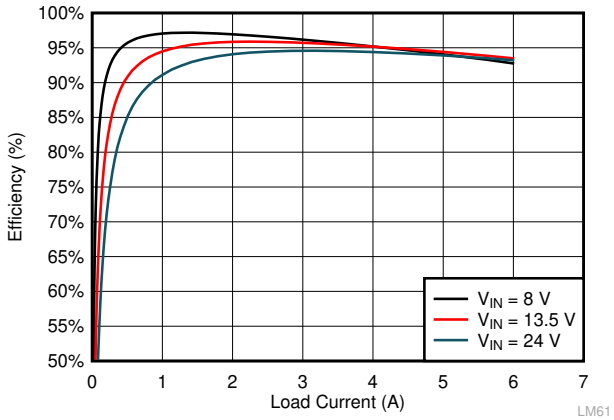


Figure 6-8. F_{SW} = 400 kHz, 5 VOUT, FPWM Mode

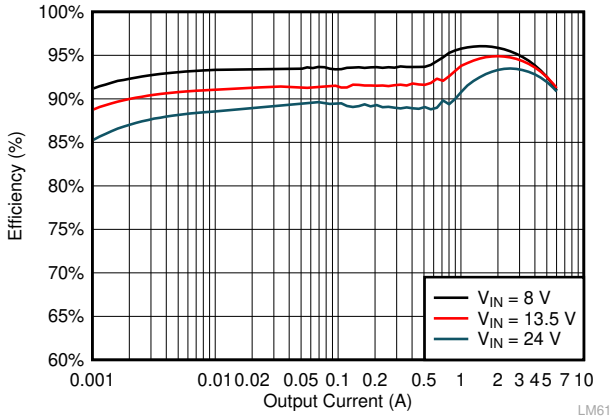


Figure 6-9. F_{SW} = 400 kHz, 3.3 VOUT, Auto Mode

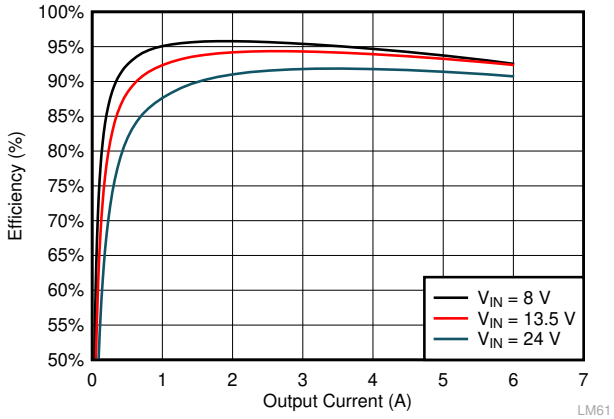


Figure 6-10. F_{SW} = 400 kHz, 3.3 VOUT, FPWM Mode

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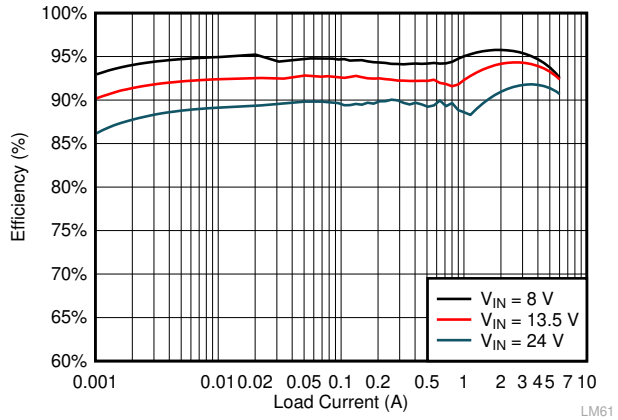


Figure 6-11. F_{SW} = 2.1 MHz, 5 VOUT, Auto Mode

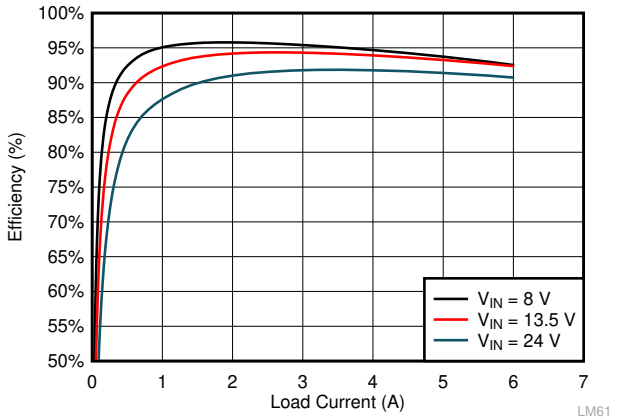


Figure 6-12. F_{SW} = 2.1 MHz, 5 VOUT, FPWM Mode

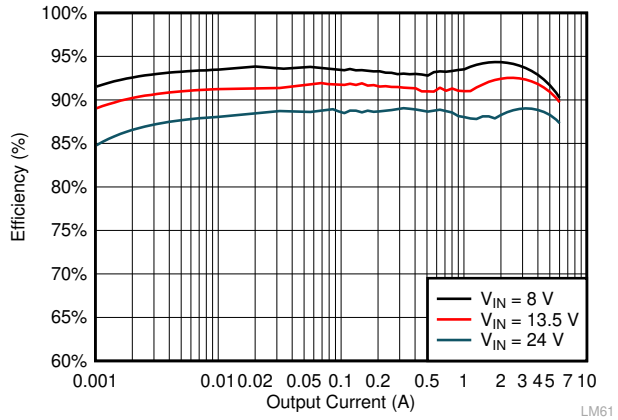


Figure 6-13. F_{SW} = 2.1 MHz, 3.3 VOUT, Auto Mode

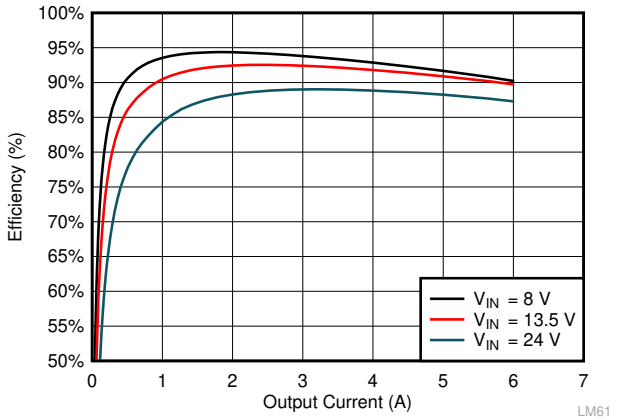


Figure 6-14. F_{SW} = 2.1 MHz, 3.3 VOUT, FPWM Mode

6.3 Load Regulation

This section provides efficiency plots for the board with LMQ61460AAS populated for Auto mode efficiency and LMQ61460AFS populated for FPWM mode efficiency. For 2.1-MHz data, the output stage has to be changed from the default BOM. The inductor (L1) selected was XEL5030-102MEB.

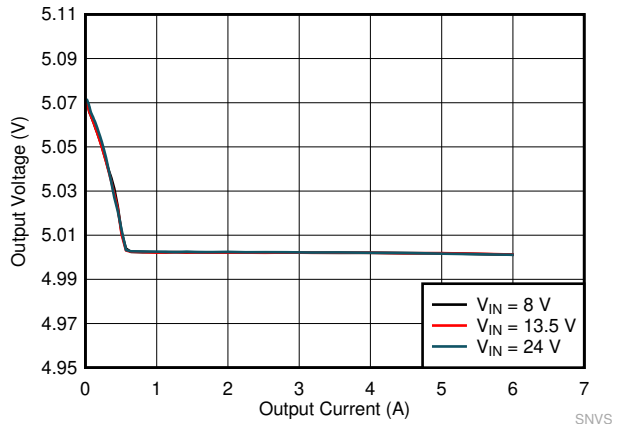


Figure 6-15. F_{SW} = 400 kHz, 5 VOUT, Auto Mode

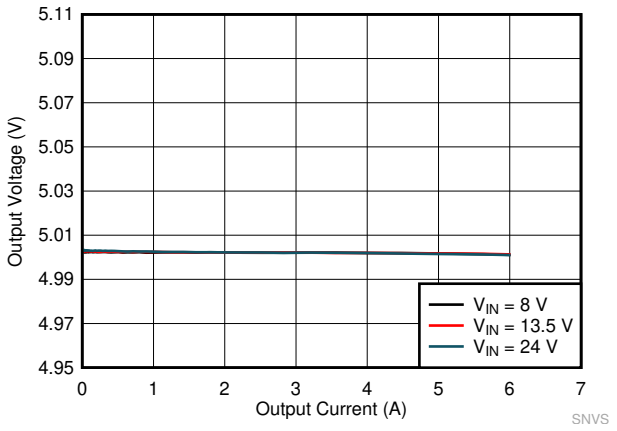


Figure 6-16. F_{SW} = 400 kHz, 5 VOUT, FPWM Mode

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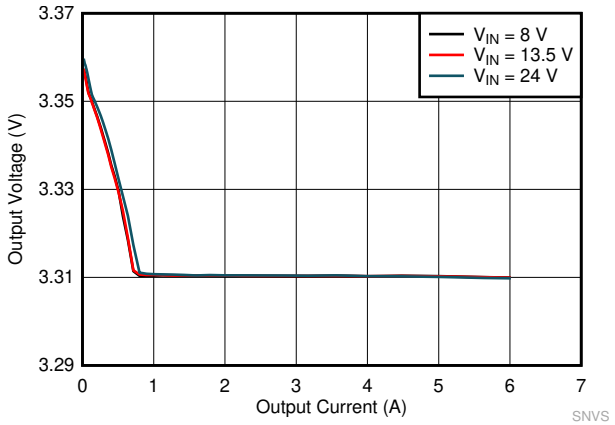


Figure 6-17. F_{SW} = 400 kHz, 3.3 VOUT, Auto Mode

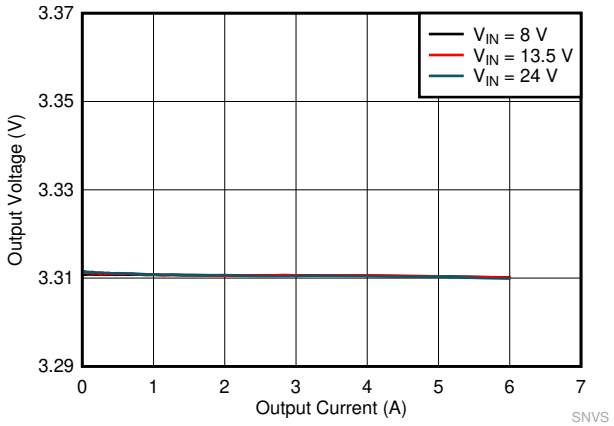


Figure 6-18. F_{SW} = 400 kHz, 3.3 VOUT, FPWM Mode

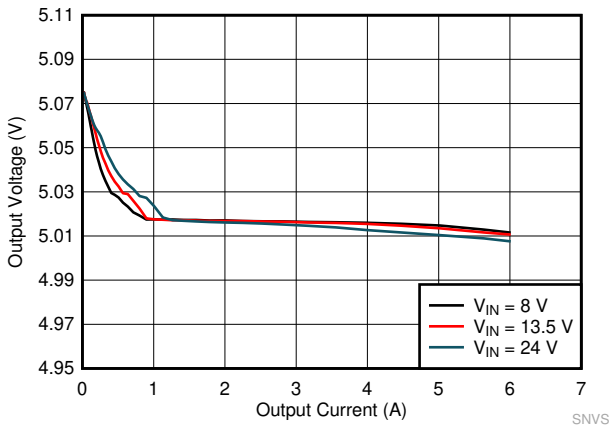


Figure 6-19. F_{SW} = 2.1 MHz, 5 VOUT, Auto Mode

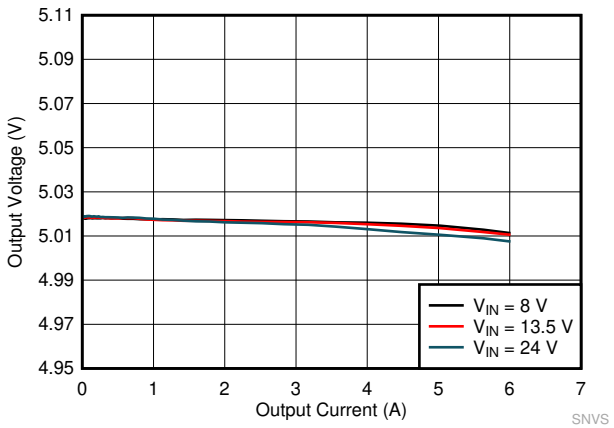


Figure 6-20. F_{SW} = 2.1 MHz, 5 VOUT, FPWM Mode

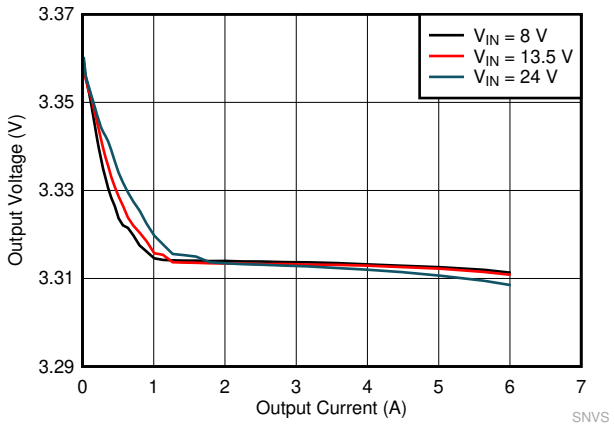


Figure 6-21. F_{SW} = 2.1 MHz, 3.3 VOUT, Auto Mode

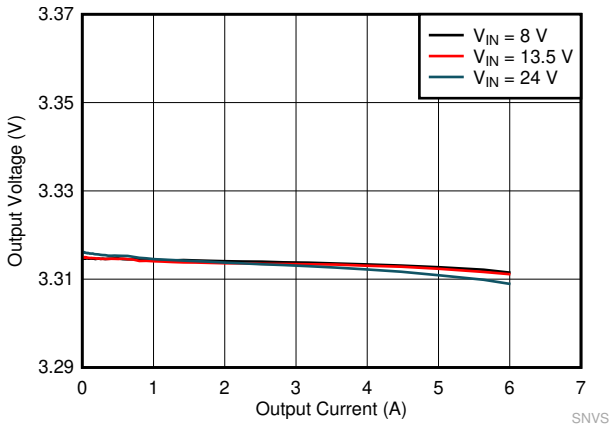


Figure 6-22. F_{SW} = 2.1 MHz, 3.3 VOUT, FPWM Mode

6.4 Thermals

A thermal image of the IC was captured to determine rise in temp with a 5-V, 6-A load. The device was soaked for 30 minutes to obtain accurate measurement.

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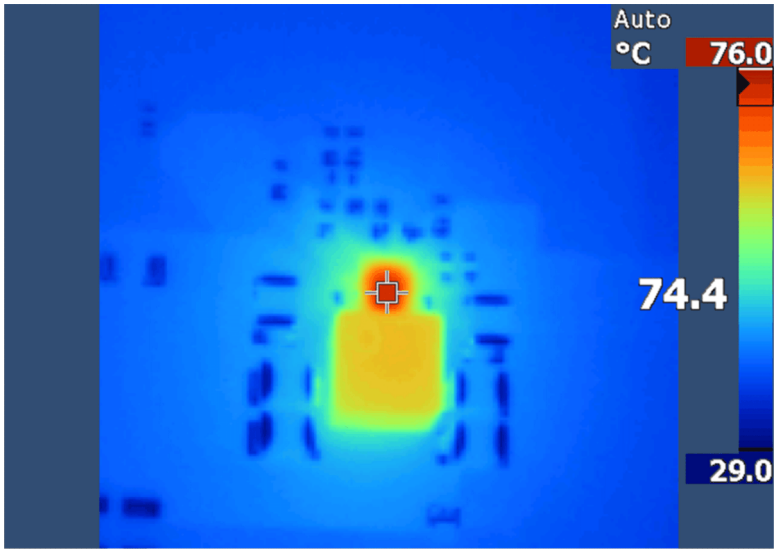


Figure 6-23. Thermal Image Capture of IC at VIN = 13.5 V, VOUT = 5 V, Load = 6 A

Note

Thermal image captures top of case temperature. This is essentially junction temperature as the case package is very thin, resulting in low psi-jt. This demonstrates device capability of operating greater than 85°C ambient with headroom.

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7 Bill of Materials

The bill of materials is shown Table 7-1 for the LMQ61460EVM-400K.

Table 7-1. LMQ61460EVM-400K EVM Bill of Materials

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1, C4	2	4.7 µF	CAP, CERM, 4.7 µF, 50 V, ±20%, X7R, AEC-Q200 Grade 1, 1210	1210	UMK325B7475MMHT	Taiyo Yuden
C2, C3	2	0.022 µF	CAP, CERM, 0.022 µF, 50 V, ±10%, X7R, 0402	0402	GRM155R71H223KA12D	MuRata
C5	1	1 µF	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0805	0805	C0805C105K3RACTU	Kemet
C6, C7, C8, C9	4	22 µF	CAP, CERM, 22 µF, 16 V, ±20%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P1X7R1C226M250AC	TDK
C12	1	1000 pF	CAP, CERM, 1000 pF, 50 V, ±0%, X7R, 0603	0603	C0603C102K5RACTU	Kemet
C13	1	0.1 µF	CAP, CERM, 0.1 µF, 10 V, ±10%, X7R, 0603	0603	C0603X104K8RACTU	Kemet
C15	1	1 µF	CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603	0603	885012206052	Wurth Elektronik
C16	1	22 pF	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603	CGA3E2C0G1H220J080AA	TDK
C17, C18, C19, C20	4	2.2 µF	CAP, CERM, 2.2 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0805	0805	CGA4J3X7R1H225K125AB	TDK
C21, C22	2	0.47 µF	CAP, CERM, 0.47 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7R1H474K080AE	TDK
J1, J2, J3	3		Terminal Block, 5 mm, 2x1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik
J4	1		Header, 100 mil, 3x1, Gold, TH	Header, 100 mil, 3x1, TH	HTSW-103-07-G-S	Samtec
L1	1	4.7 µH	Inductor, Shielded, Hyperflux, 4.7 µH, 7.4 A, 0.0143 Ω, SMD	6.65x6.45 mm	74439346047	Wurth Elektronik
L2	1		1.2 µH Shielded Molded Inductor 7.5 A, 11.3 mΩ Max 2-SMD	SMD2	744316220	Wurth Electronics
LBL1	1			PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R6	2	1.00 k Ω	RES, 1.00 k, 1%, 0.25 W, 1206	1206	RC1206FR-071KL	Yageo America
R2	1	0 Ω	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R3	1	33.2 kΩ	RES, 33.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060333K2FKEA	Vishay-Dale
R4, R7	2	100 kΩ	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo
R5	1	100 Ω	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo
R8	1	24.9 kΩ	RES, 24.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0724K9L	Yageo
R9	1	1.00 kΩ	RES, 1.00 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1001V	Panasonic
R10	1	255 kΩ	RES, 255 k, 1%, 0.1 W, 0603	0603	RC0603FR-07255KL	Yageo
SH-J1	1		Shunt, 100 mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity

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Table 7-1. LMQ61460EVM-400K EVM Bill of Materials (continued)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
TP1, TP9	2		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP2, TP3, TP5, TP6	4		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP4, TP7	2		Test Point, Multipurpose, Orange, TH	Orange Multipurpose Testpoint	5013	Keystone
TP8, TP10	2		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
U1	1		Automotive 6-A Low Noise Synchronous Buck Regulators, RJR0014A (VQFN-HR-14)	RJR0014A	LMQ61460AASQRJRRQ1	Texas Instruments
C10, C11	0	22 µF	CAP, CERM, 22 µF, 16 V, ±20%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P1X7R1C226M250AC	TDK
C14	0	1 µF	CAP, CERM, 1 µF, 10 V, ±10%, X7R, 0603	0603	GRM188R71A105KA61D	MuRata
C23, C24	0	1 µF	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R12	0	0.51 Ω	RES, 0.51, 1%, 0.25 W, 0805	0805	CRM0805-FX-R510ELF	Bourns
R13	0	100 kΩ	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2020) to Revision B (January 2021)	Page
• Revised Board Efficiency Curve - 5V, 2.1MHz, FPWM	13

Changes from Revision * (March 2020) to Revision A (September 2020)	Page
• Changed image from 3D imaging to a physical board image	1
• Added Board Efficiency	13
• Added Load Regulation	14
• Added Thermals	15

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