PFC demoboard based on CoolMOS™ P7 600 V

800 W 65 kHz platinum server design

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About this document

Scope and purpose

This document presents design considerations and results from testing an 800 W 65 kHz platinum server Power Factor Correction (PFC) Continuous Conduction Mode (CCM) boost converter, based on:

- 600 V CoolMOS™ P7 superjunction MOSFET and 650 V CoolSiC™ schottky diode generation 5
- 2EDN7524F non-isolated gate driver (EiceDRIVER™)
- ICE3PCS01G PFC controller
- ICE2QR2280Z flyback controller

Intended audience

This document is intended for design engineers who want to verify the performance of the latest 600 V CoolMOS™ P7 MOSFET technology working at 65 kHz in a CCM PFC boost converter along with EiceDRIVER™ ICs and 650 V CoolSiC™ schottky diode generation 5 using analog control.

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1 Introduction

PFC shapes the input current of the power supply so that it is synchronized with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as if it is a pure resistor, without any input current harmonics or phase shift.

This document is intended to demonstrate the design and practical results of an 800 W 65 kHz platinum server PFC demo board based on Infineon Technologies devices including power semiconductors, non-isolated gate drivers and an analog controller for the PFC converter as well as a flyback controller for the auxiliary supply.

1.1 Topology

Although active PFC can be achieved by several topologies, the boost converter (Figure 1) is the most popular topology used in server PFC applications, for the following reasons:

- The line voltage varies from zero to some peak value - typically 375 V_{PK}; hence a step up converter is needed to deliver a DC bus voltage of 380 V DC or more. For that reason the buck converter is eliminated, and the buck-boost converter has high switch voltage stress (V_{in}+V_o), therefore it is not popular.
- The boost converter has the filter inductor on the input side, which provides a smooth continuous input current waveform as opposed to the discontinuous input current of the buck or buck-boost topology. The continuous input current is much easier to filter, which is a major advantage of this design as any additional filtering needed on the converter input will increase the cost and reduce the power factor due to capacitive loading of the line.

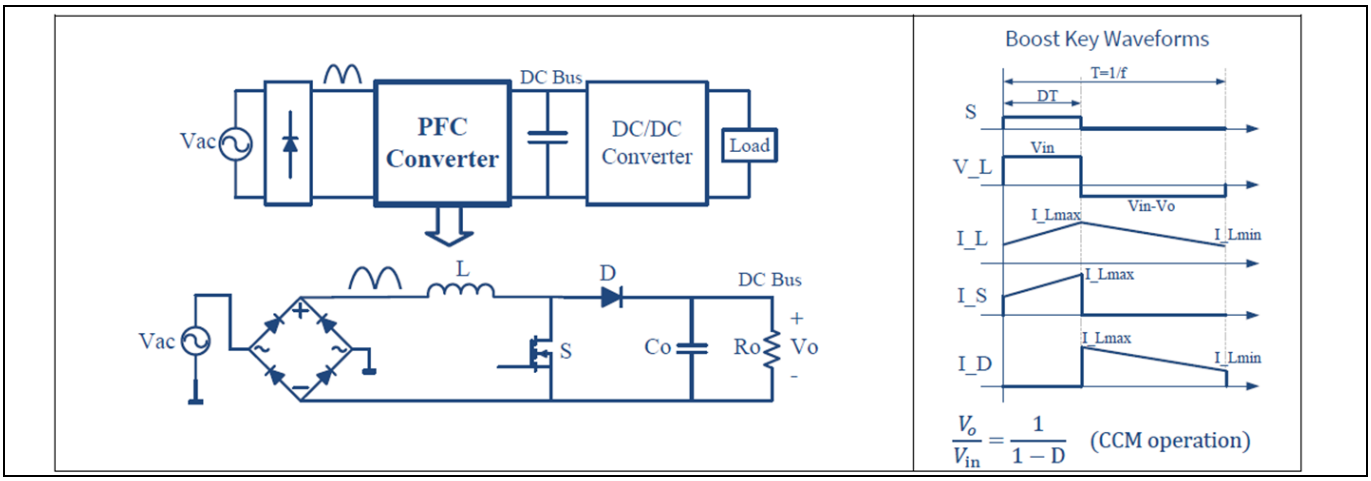


Figure 1 Schematics and key waveforms of a boost PFC converter

1.2 PFC modes of operation

The boost converter can operate in three modes: Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and Critical Conduction Mode (CrCM). Figure 2 shows modeled waveforms to illustrate the inductor and input currents in the three operating modes, for exactly the same voltage and power conditions.

By comparing DCM to the other modes, DCM operation seems simpler than CrCM, since it can operate at constant frequency; however DCM has the disadvantage that it has the highest peak current, and as a result the highest ripple current through the inductor, when compared to CrCM and also to CCM. This represents a disadvantage in performance when compared to CrCM.

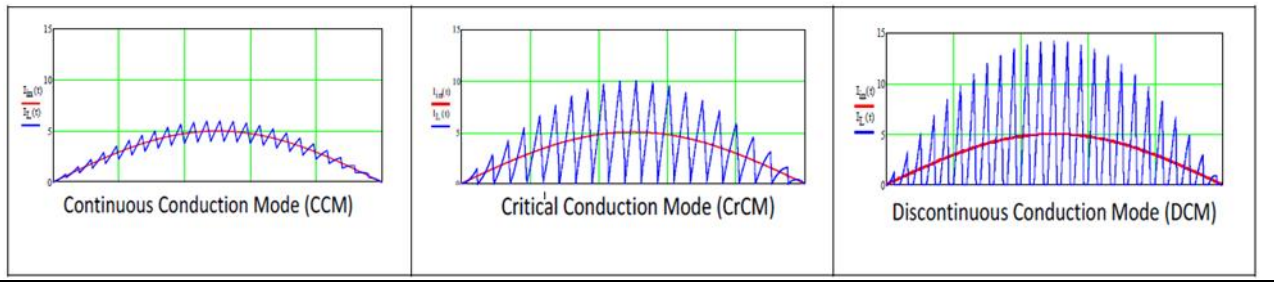


Figure 2 PFC inductor current and average input current in the three different operating modes

CrCM may be considered to be a special case of CCM, where the operation is controlled to remain at the boundary between CCM and DCM. CrCM normally uses constant on-time control; the line voltage is changing across the 50/60 Hz line cycle, the reset time for the boost inductor is varying and the operating frequency will also change in order to maintain the boundary mode operation. CrCM requires the controller to sense the inductor current zero crossing in order to trigger the start of the next switching cycle.

For fixed switching frequency operation, the input voltage and power output of the PFC will determine the operation mode. In this way we may have:

- Complete half AC cycle in CCM operation mode
- Complete half AC cycle in DCM operation mode
- DCM and CCM operation modes during half AC cycle

The boundaries between these operation modes can be calculated theoretically, as shown in Figure 3:

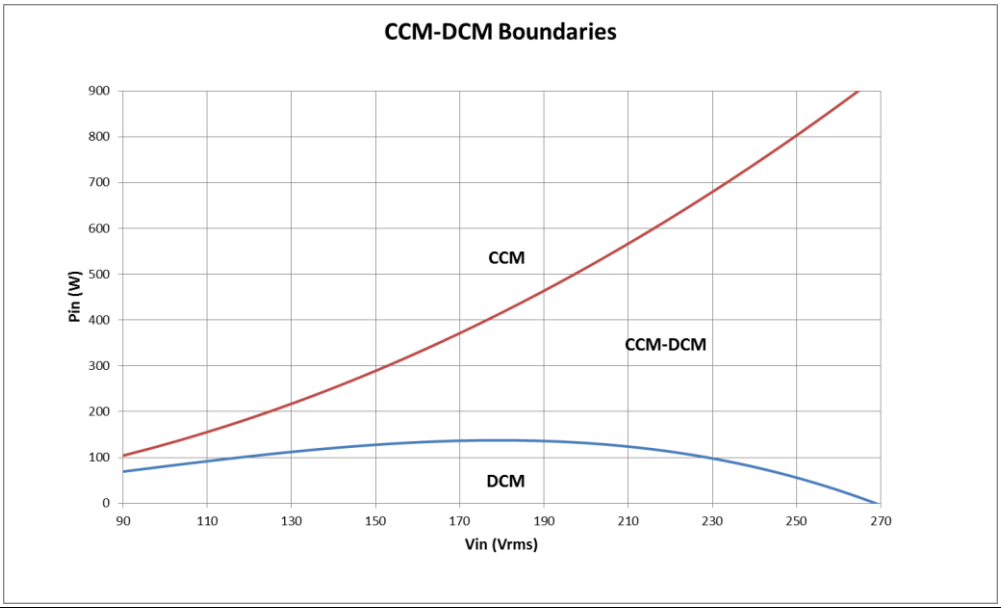


Figure 3 PFC operation mode boundaries

The control mode of the PFC topology used in this demoboard is focused on the constant switching frequency operation control mode, due to its advantage of simplified input filter. The used PFC controller handles DCM and CCM operation mode, which highly depends on the input voltage and output load conditions.

2 Power stage

2.1 Specifications

Table 1 Input requirements

Parameter	Value
Input voltage range, V_{in_range}	90 V AC – 265 V AC
Nominal input voltage, V_{in}	230 V AC
AC line frequency range, f_{AC}	47 – 63 Hz
Max peak input current, I_{in_max}	10 A_{RMS} @ 90 V AC / P_{out_max}=800 W
Turn on input voltage, V_{in_on}	80 V AC – 87 V AC, ramping up
Turn off input voltage, V_{in_off}	75 V AC – 85 V AC, ramping down
Power Factor (PF)	Greater than 0.95 from 20% rated load and above
Hold up time	10 ms after last AC zero point @ P_{out_max} = 800 W, V_{out_min} = 320 V DC
Total Harmonic Distortion (THD)	<15% from 10% load @ high line, for class A equipment

Table 2 Output requirements

Parameter	Value
Nominal output voltage, V_{out}	380 V DC
Maximum output power, P_{out}	800 W
Peak output power, P_{out_max}	1 kW
Maximum output current, I_{out_max}	2,1 A
Output voltage ripple	Max 20 V_{pk-pk} @ V_{out} and I_{out}
Maximum output overvoltage threshold	450 V DC
Minimum output overvoltage threshold	420 V DC

Table 3 Efficiency at different load conditions

Value	Conditions
> 95% @ 50% of the load	V_{IN} = 115 V AC
> 94% @ 100% of the load	V_{IN} = 115 V AC
> 97% @ from 50% of the load	V_{IN} = 230 V AC

2.2 EMI filter

The EMI filter is implemented as a two-stage filter, which provides sufficient attenuation for both Differential Mode (DM) and Common Mode (CM) noise.

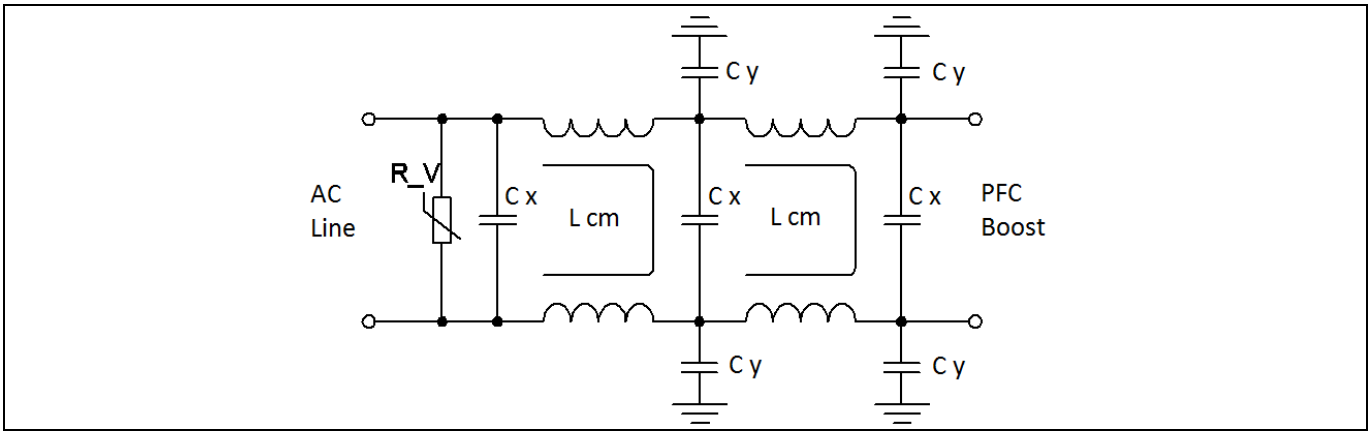


Figure 4 Two stage filter structure

The two high current CM chokes L cm are based on high permeability toroid ferrite cores.

1. 2 x 26 Turns/ 2 x 4,76 mH
2. 2 x 28 Turns/ 2 x 5,7 mH

The relatively high number of turns causes a considerable amount of stray inductance, which ensures sufficient DM attenuation

2.3 Bridge rectifier

The bridge rectifier is designed for the worst case: maximum output power and minimum input voltage. To calculate the input current, an efficiency of 94% (at V_{in} = 90 V AC) is applied.

Maximum RMS value of the input current:

$$I_{IN_RMS} = \frac{P_{OUT_MAX}}{\eta \cdot V_{IN_RMS}} = \frac{800W}{0{,}94 \cdot 90V} = 9{,}46A$$

Maximum RMS current value per diode:

$$I_{BR-D_RMS} = \frac{\sqrt{2} \cdot I_{IN_RMS}}{2} = 6{,}68\ A$$

Maximum average current value per diode:

$$I_{BR-D_avg} = \frac{\sqrt{2} \cdot I_{IN_RMS}}{\pi} = 4{,}26A$$

Due to the calculated average and effective current values, the rectifier type LVB2560 with very low forward voltage drop was selected. This 800 V device has sufficient voltage reserve with V_{in} = 265 V AC. The smaller size types GBU and KBU are only available for currents up to 10 A. For the following formula, r_D was extracted from the characteristic curve of the data sheet (T_A = 100 °C).

Conduction losses of a rectifier diode:

$$P_{BR-D} = I_{BR-D_avg} \cdot V_{BR-D} + \left(I_{BR-D_{RMS}}\right)^2 \cdot r_D = 4{,}26 \cdot 0{,}5 + (6{,}68)^2 \cdot 0{,}016 = 2{,}84\ W$$

Total losses of the rectifier:

$$P_{REC} = 4 \cdot P_{BR-D} = 4 \cdot 2{,}84\ W = 11{,}36\ W$$

2.4 PFC choke

The PFC choke design is based on a toroidal high performance magnetic powder core.

Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots. Hence they are suitable for systems that are targeting the highest power density with forced air cooling. Very small choke sizes are feasible.



Figure 5 Picture of the PFC choke

The chosen core material is HIGH FLUX from Chang Sung Corporations (CSC), which has an excellent DC bias and good core loss behavior. The part number is CH270060. The outer diameter of the core is 27 mm.

The winding was implemented using enameled copper wire AWG 19 (1 mm diameter). The winding covers approximately 2.5 layers. This arrangement allows a good copper fill factor, while still having good AC characteristics, and is a preferred fill form factor for high power toroidal inductors.

There are 90 turns, taking advantage of the high permitted DC bias. The resulting small signal bias inductance is 603 µH. The effective inductance with current bias is determined by the core material B-H characteristics and illustrated as follows:

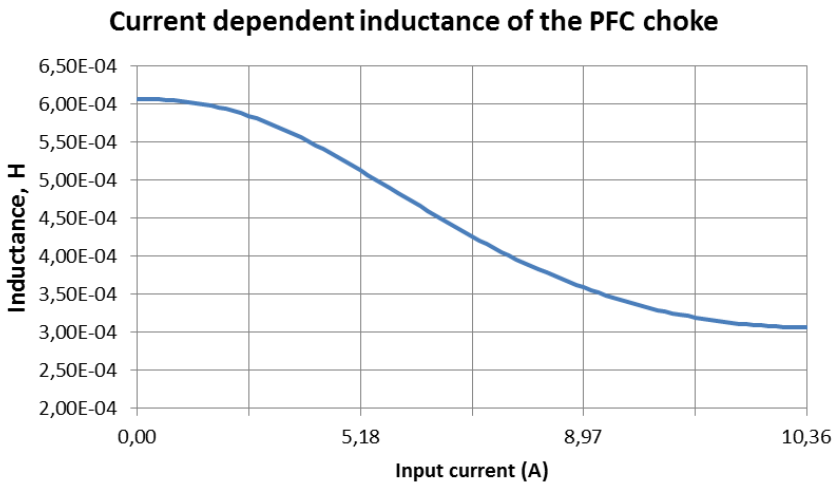


Figure 6 Input current dependency of the inductance of the PFC

The effective inductance, a current ripple ratio of 30% together with the switching frequency of 65 kHz, produce a relatively low current ripple that supports the whole system performance. The peak and RMS currents for the semiconductors and filter components are minimized. The low ripple design achieves low core losses, which is important for light load performance of the system.

Table 4 PFC choke losses at 800 W / 65 kHz (calculated results from a magnetic design tool)

Input voltage (V)	P_{CORE} (W)	$P_{WINDINGS\ @\ 100°C}$ (W)	P_{TOTAL} (W)
115	0.99	5.91	6.90
230	0.92	1.48	2.39

2.5 Infineon power semiconductors

2.5.1 600 V CooMOS™ P7

The CooMOS™ 7th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 600 V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g. very low ringing tendency, outstanding robustness of the body diode against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses make switching applications even more efficient, more compact and much cooler.

2.5.1.1 Design implementation

Based on the analysis of several current server PSUs and customer feedback, it is a common practice to implement two MOSFETs in parallel in the classic PFC topology for improving thermal performance during both normal and critical operating conditions such as AC line drop out. As a result, this demo board uses two 180 mΩ TO-220 MOSFETs working in parallel. This approach has the advantage of lowering both switching and conduction losses in both devices during the highest inductor current at low line compared to a single TO-247 approach.

2.5.2 Fast dual channel 5 A non-isolated low side gate driver

2.5.2.1 Introduction

The 2EDN7524 is a non-inverting fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure the highest flexibility and cover a wide variety of applications.

All inputs are compatible with LV TTL signal levels. The threshold voltages (with a typical hysteresis of 1 V) are kept constant over the supply voltage range.

Since the 2EDN7524 is particularly aimed at fast switching applications, signal delays and rise/fall times have been minimized. Special effort has been made towards minimizing delay differences between the two channels to very low values (typically 1 ns).

The 2EDN7524 driver used in this demo board comes in a standard PG-DSO-8 package.

2.5.2.2 Driver outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a typical 5 A of sourcing and sinking current. The on-resistance is very low with a typical value below 0.7 Ω for the sourcing p-MOS and 0.5 Ω for the sinking n-MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving real rail-to-rail behavior and not suffering from the source follower's voltage drop.

Gate drive outputs are held active low for of floating inputs (ENx, Inx) or during startup or power down once Under Voltage Lockout (UVLO) is not exceeded.

2.5.2.3 Under Voltage Lockout (UVLO)

The UVLO function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Therefore it can be guaranteed that the switch transistor is not operated if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The default UVLO level is set to a typical value of 4.2 V or 8 V (with some hysteresis). For higher levels, such as HV SJ MOSFETs, a minimum active voltage of 8 V is used.

2.5.3 CoolSiC ™ schottky diode generation 5

Selection of the boost diode is a major design decision in a CCM boost converter because the diode is hard commutated at a high current and the reverse recovery can cause significant power loss, as well as noise and current spikes. Reverse recovery can be a bottleneck for high switching frequency and high power density power supplies. Additionally, at low line, the available diode conduction duty cycle is quite low, and the forward current quite high in proportion to the average current. For that reason, the first criteria for selecting a diode in a CCM boost circuit are fast recovery with low reverse recovery charge, followed by V_f operating capability at high forward current.

Since CoolSiC™ Schottky diodes have a capacitive charge, Q_c, rather than reverse recovery charge, Q_{rr} their switching loss and recovery time are much lower than a silicon ultrafast diode leading to enhanced performance. Moreover, SiC diodes allow higher switching frequency designs. Hence, higher power density converters are achieved. The capacitive charge for SiC diodes is not only low, but also independent of di/dt, current level, and temperature; which is different from silicon diodes that have strong dependency on these conditions.

The recommended diode for CCM boost applications is the 650 V CoolSiC™ Schottky diode generation 5, which includes Infineon's leading edge technologies, such as a diffusion soldering process and wafer thinning technology. The result is a new family of products that show improved efficiency over all load conditions, resulting from the improved thermal characteristics. Even with the high surge current capability of SiC Schottky diodes, it is still preferred to use a bulk pre-charge diode. This is a low frequency standard diode with a high I^2t rating to support pre-charging the bulk capacitor to the peak of the AC line voltage; this is a high initial surge current stress (which should be limited by a series NTC) that is best avoided for the HF boost rectifier diode.

The proper current rating of the PFC diode must be calculated by considering 1,3 to 1,5 times the RMS current of the diode, which is expressed as:

$$I_{D_RMS} = \frac{P_{OUT_MAX}}{V_{IN_RMS} \cdot \eta} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{IN_RMS}}{3 \cdot \pi \cdot V_{OUT}}} = \frac{800}{90 \cdot 0{,}94} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot 90}{3 \cdot \pi \cdot 380}} = 5{,}042\ A$$

In this demo board, a 6 A IDH06G65C5 diode is used.

2.6 Output capacitor

Possible over-voltages require the selection of a 450 V (low impedance) type capacitor. The minimum capacitance is defined by the minimum hold up time and the minimum allowable DC link voltage of the system or the maximum allowable voltage from the 2x line frequency AC ripple current:

- t_{hu} = 10 ms

- V_{BULK_min} = 320 V

$$C_b \geq \frac{2 * P_{OUT_MAX} * t_{hu}}{V_{BULK}^2 - V_{BULK_min}^2} = 381\ \mu F$$

The chosen capacitor is a 470 µF @ 450 V 30 mm x 50 mm electrolytic type.

2.7 Heatsink and cooling fan

Heatsinks for the rectifier and power semiconductors are made from a 1 mm copper plate. Fan speed control operation depends on the board/heatsink temperature. There are two speed levels, the fan operates with low speed at 57°C and increases to high speed above 79°C.

3 ICE3PCS01G PFC controller

The ICE3PCS01G is a 14-pin controller IC for PFC circuits. It is suitable for wide range line input applications from 85 to 265 V AC with overall efficiency above 97%. The IC supports the converters in boost operation and operates in CCM with average current control by regulating D_{off}, without the need for input voltage sensing except for brown out detection.

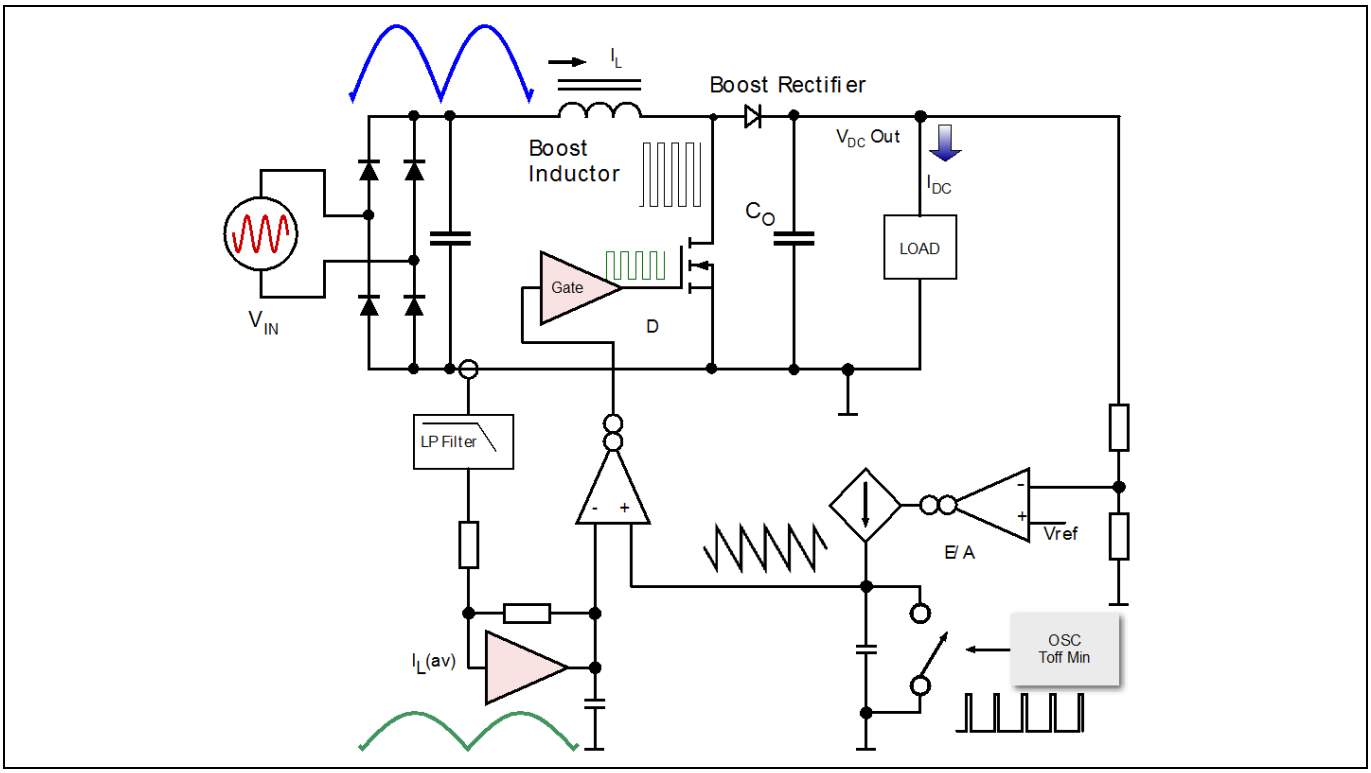


Figure 7 Simplified block diagram concept for PFC PWM modulator of the ICE3PCS0x series

The IC operates with cascaded control comprising the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load conditions, depending on the choke inductance, the system may enter DCM resulting in higher harmonics but still meeting the Class D requirement of IEC 1000-3-2 (EN 61000-3-2). The current sense amplifier filters and amplifies the I_{SENSE} signal and provides a current loop bandwidth control via the ICAP pin for the external compensation capacitor.

The outer voltage loop of the IC regulates the output bulk voltage and is realized digitally within the IC, using a delta-sigma converter operating at about 3.4 kHz to digitize the voltage feedback signal. Depending on the load condition, the PID signal is converted to an appropriate low frequency voltage that controls the amplitude of the current loop by means of a variable voltage ramp generated at the switching clock frequency, which is also sent to the PWM comparator. The current charging the ramp generator is a function of the error amplifier feedback level, plus some nonlinear block signal processing.

The digital PID has some unique features that give it some regulation advantages when compared with conventional OTA amplifiers, while still realizing low harmonic distortion and high power factor.

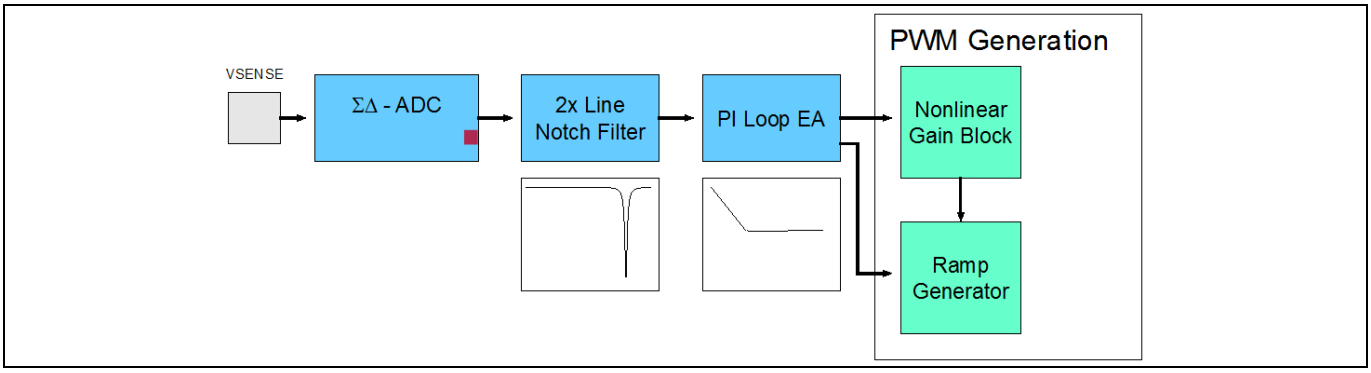


Figure 8 Digital error amplifier system concept with 2x line frequency notch filter

The self calibrating 2x line frequency notch filter greatly reduces the distortion effects from feedback of the bulk capacitor ripple, while allowing somewhat higher gain, which translates to better load step transient response.

The IC is equipped with various protection features to ensure safe operation for the system and the device.

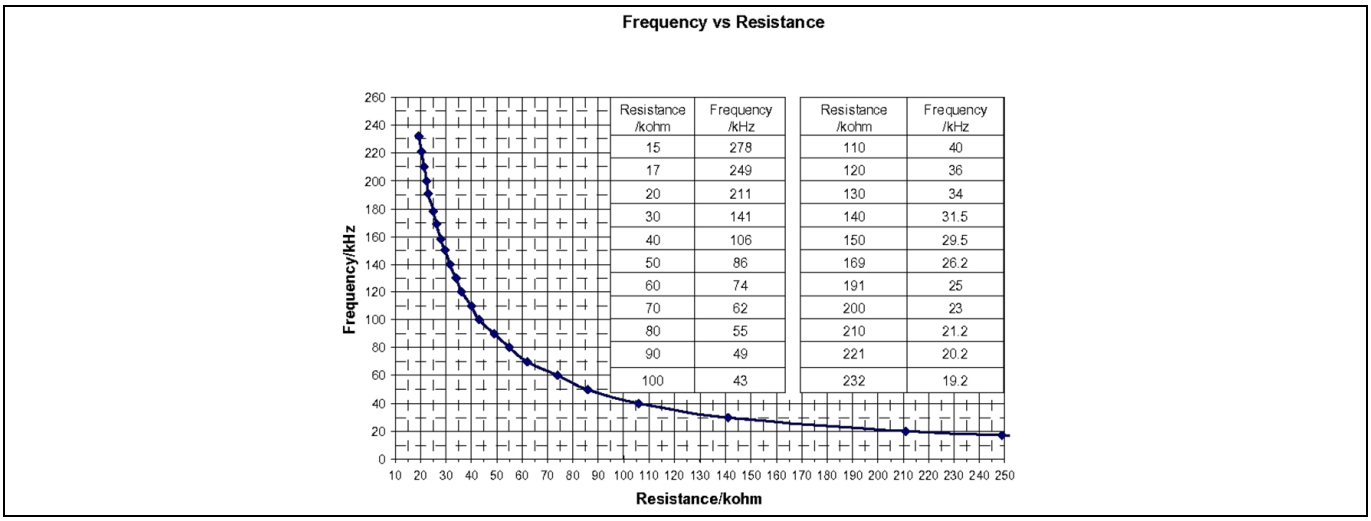
3.1 Soft start

During power-up when V_{OUT} is less than 96% of the rated level, the internal voltage loop output increases from the initial voltage under soft-start control. This results in a controlled linear increase of the input current from 0 A. This helps to reduce the current stress in power components.

Once V_{OUT} has reached 96% of the rated level, the soft-start control is released to achieve good regulation and dynamic response and the VB_OK pin is raised to 5 V indicating that the PFC output voltage is in the normal range.

3.2 Switching frequency

The switching frequency of the PFC converter can be set with an external resistor R_{FREQ} attached between the FREQ pin and SGND. The voltage on the FREQ pin is typically 1 V. The corresponding capacitor for the oscillator is integrated in the device and the R_{FREQ}/frequency is given in Figure 8. The recommended operating frequency range is from 21 kHz to 250 kHz. For this demo board, a R_{FREQ} of 68 kΩ at the FREQ pin will set a switching frequency (f_{SW}) of approximately 65 kHz (typical).



Resistance /kohm	Frequency /kHz	Resistance /kohm	Frequency /kHz
15	278	110	40
17	249	120	36
20	211	130	34
30	141	140	31.5
40	106	150	29.5
50	86	169	26.2
60	74	191	25
70	62	200	23
80	55	210	21.2
90	49	221	20.2
100	43	232	19.2

Figure 9 Frequency setting in the ICE3PCS01G IC

3.3 Protection features

3.3.1 Open loop protection

Open loop protection is available for this IC to safeguard the output and is implemented using a comparator with a threshold of 0.5 V. Whenever the voltage at the VSENSE pin falls below 0.5 V, or equally V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin is not connected). In this case, most of the blocks within the IC will be shutdown. Normally the bulk pre-charge diode will charge the bulk capacitance to a value higher than this, so this voltage range will occur.

3.3.2 Peak current limit

The IC provides a cycle-by-cycle Peak Current Limitation (PCL). It is active when the voltage at the ISENSE reaches -0.2 V. This voltage is amplified by a factor of -5 and connected to the comparator with a reference voltage of 1.0 V. A deglitcher with a value of 200 ns after the comparator improves noise immunity for the activation of this protection. In other words, the current sense resistor should be designed to be lower than the -0.2 V PCL for normal operation.

3.3.3 IC supply UVLO

When the supply voltage V_{CC} is below the under voltage lockout threshold $V_{CC,UVLO}$, (typically 11 V), the IC is turned off and the gate drive is pulled low internally to maintain the off state. The current consumption is reduced to only 1.4 mA.

3.3.4 DC link voltage monitor and enable function

The IC monitors the bulk voltage status through the VSENSE pin and outputs a TTL signal to enable the PWM IC or control the inrush relay. During soft-start once the bulk voltage is higher than 95% of the rated value, pin VB_OK is raised to a high level. The threshold to trigger the low level is determined by the externally adjustable voltage on the VBTHL pin.

When the VBTHL pin is pulled lower than 0.5 V, most functional blocks are turned off and the IC enters into standby mode for low power consumption. When the disable signal is released the IC recovers via a soft-start.

4 ICE2QR2280Z controller for the auxiliary converter

4.1 Input and output requirements

The voltages needed to supply the control circuitry and the fan is provided by the dedicated flyback DC-DC converter ICE2QR2280Z, which is assembled on the power board. The DC-link voltage supplies such converter.

Table 5

Parameter	Value
Input voltage range, $V_{aux_in_range}$	125 V_{DC} – 450 V_{DC}
Nominal primary output voltage, V_{aux_pri}	12 V_{DC} +/- 10%
Nominal secondary output voltage, V_{aux_sec}	12 V_{DC} +/- 10%
Maximum output power, P_{aux_out}	6 W

4.2 Flyback transformer

The transformer design is based on a gapped ferrite core EE 16/8/5 with a horizontal arranged bobbin. The total air gap is 0.2 mm. The selected core material is TDK N87 or equivalent.

The turn ratio was chosen to be 184:15:15, resulting in 150 V (approximately) reflected primary transformer voltage.

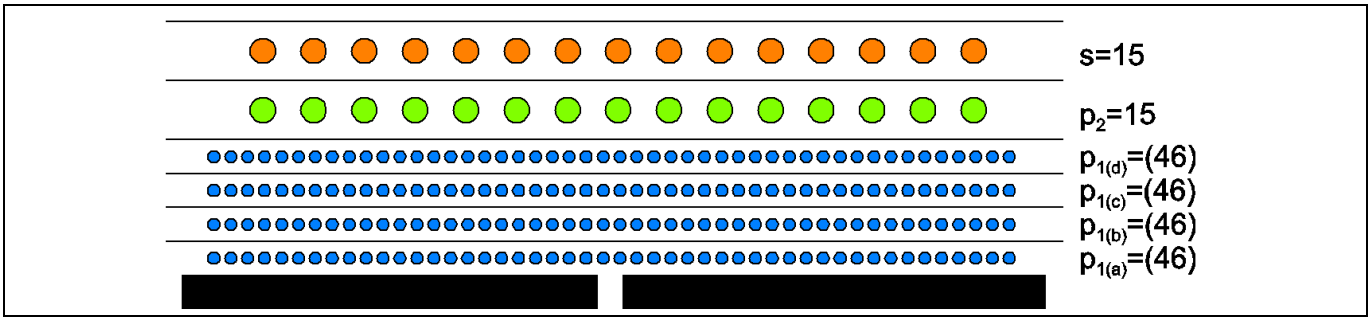


Figure 10 Winding arrangement

The secondary winding (S) has safety insulation from primary side, which is implemented using triple insulated wire. The other windings are made of standard enameled wire. The high voltage primary winding (P1) is split in to 4 layers.

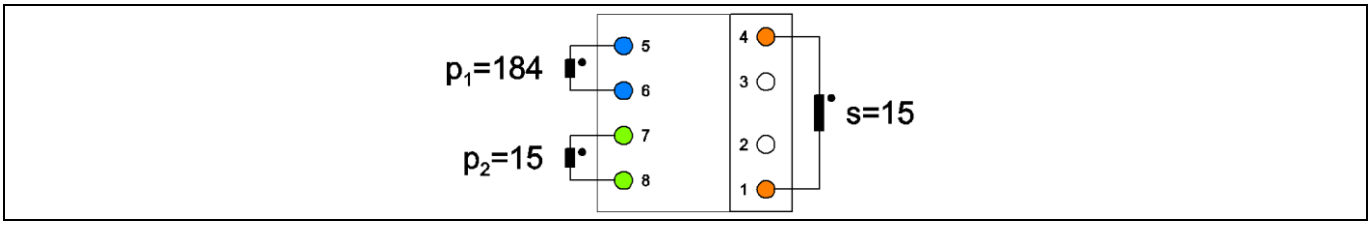
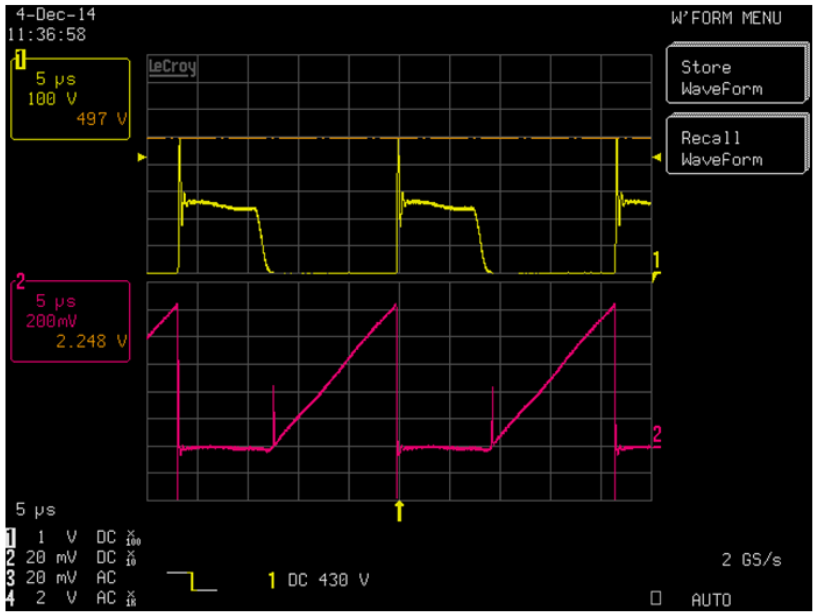


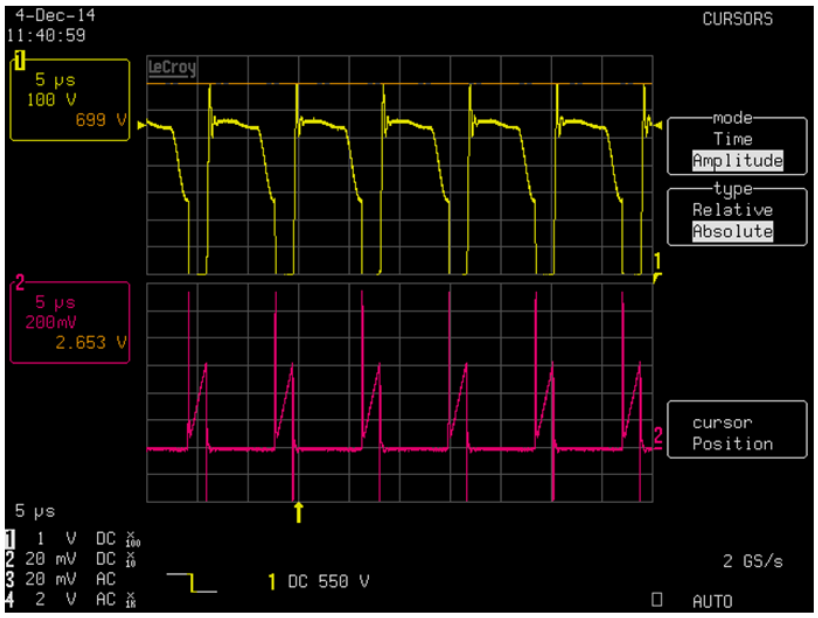
Figure 11 Pin arrangement, top view

4.3 Swiching frequency

The ICE2QR2280Z is a quasi-resonant PWM controller with integrated 800 V CoolMOS™. The switching frequency depends on load power and input voltage and is between 40 kHz and 130 kHz.



- V_{in}=100 V_{DC}
- CH1-Drain-Source Voltage
- CH2-Shuntvoltage (R3,9Ω)



- V_{in}=400 V_{DC}
- CH1-Drain-Source Voltage
- CH2-Shuntvoltage (R3,9Ω)

Figure 12 Waveforms of the auxiliary power supply

5 Experimental results

5.1 Efficiency, PF and THD measurments

Efficiency measurements were carried out with a “WT330” Yokogawa digital power meter. Losses of the EMI filter are included. The fan was supplied from an external +12 V voltage source.

Table 6 Measurements at V_{IN_AC} = 115 V AC

P_{out_load} (%)	V_{IN_AC} (V)	I_{IN_AC} (A)	P_{IN} (W)	V_{OUT} (V)	I_{IN} (A)	P_{OUT} (W)	η (%)	PF	iTHD (%)
10	115,36	0,71	80,81	379,9	0,20	76,39	94,53	0,986	7,81
20	115,32	1,43	163,57	379,9	0,41	157	95,98	0,994	8,83
30	115,28	2,15	246,66	379,9	0,63	237,82	96,42	0,997	6,71
40	115,24	2,87	329,9	379,9	0,84	318,5	96,54	0,997	5,99
50	115,20	3,60	413,7	379,9	1,05	399,4	96,54	0,998	5,97
60	115,16	4,33	497,6	379,9	1,26	479,9	96,44	0,998	5,90
70	115,12	5,07	582,2	379,9	1,48	560,6	96,29	0,998	5,56
80	115,09	5,76	661,4	379,9	1,67	635,8	96,13	0,998	5,52
90	11,05	6,50	746,8	379,9	1,89	716,1	95,89	0,998	5,47
100	115,01	7,26	833,1	379,9	2,10	796,9	95,65	0,998	5,61

Table 7 Measurements at V_{IN_AC} = 230 V AC

P_{out_load} (%)	V_{IN_AC} (V)	I_{IN_AC} (A)	P_{IN} (W)	V_{OUT} (V)	I_{IN} (A)	P_{OUT} (W)	η (%)	PF	iTHD (%)
10	230,92	0,41	79,67	379,97	0,20	76,31	95,78	0,851	14,79
20	230,9	0,73	161,71	379,96	0,41	157,03	97,11	0,958	8,82
30	230,88	1,08	243,81	379,95	0,63	237,96	97,60	0,980	5,11
40	230,86	1,43	325,72	379,96	0,84	318,66	97,83	0,989	3,47
50	230,84	1,78	407,74	379,95	1,05	399,52	97,98	0,992	2,82
60	230,83	2,14	489,74	379,94	1,26	480,19	98,05	0,994	3,66
70	230,8	2,49	571,88	379,94	1,48	560,89	98,08	0,995	3,75
80	230,79	2,82	648,5	379,94	1,67	636,2	98,10	0,996	3,73
90	230,78	3,18	730,7	379,93	1,89	716,7	98,08	0,997	3,74
100	230,77	3,54	813,1	379,96	2,10	797,5	98,08	0,996	4,35

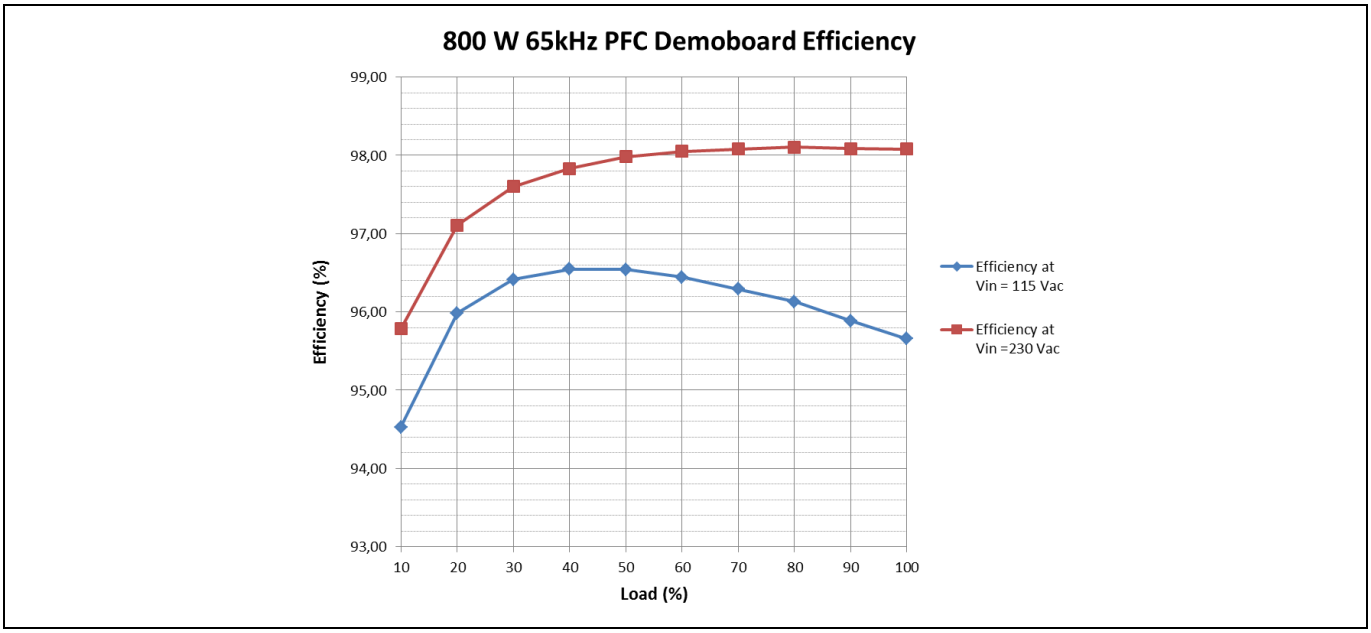


Figure 13 High and low line efficiency when R_{g_on} = 15 Ω and R_{g_off} = 2,2 Ω

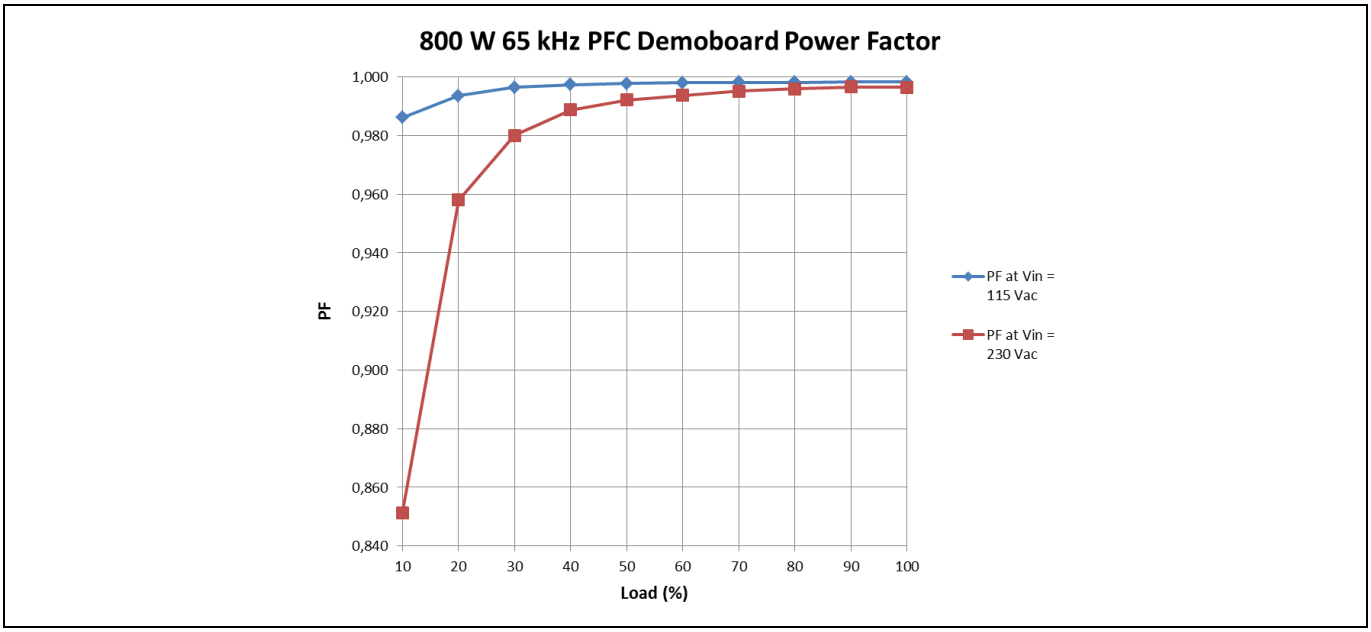


Figure 14 Power factor at high and low line

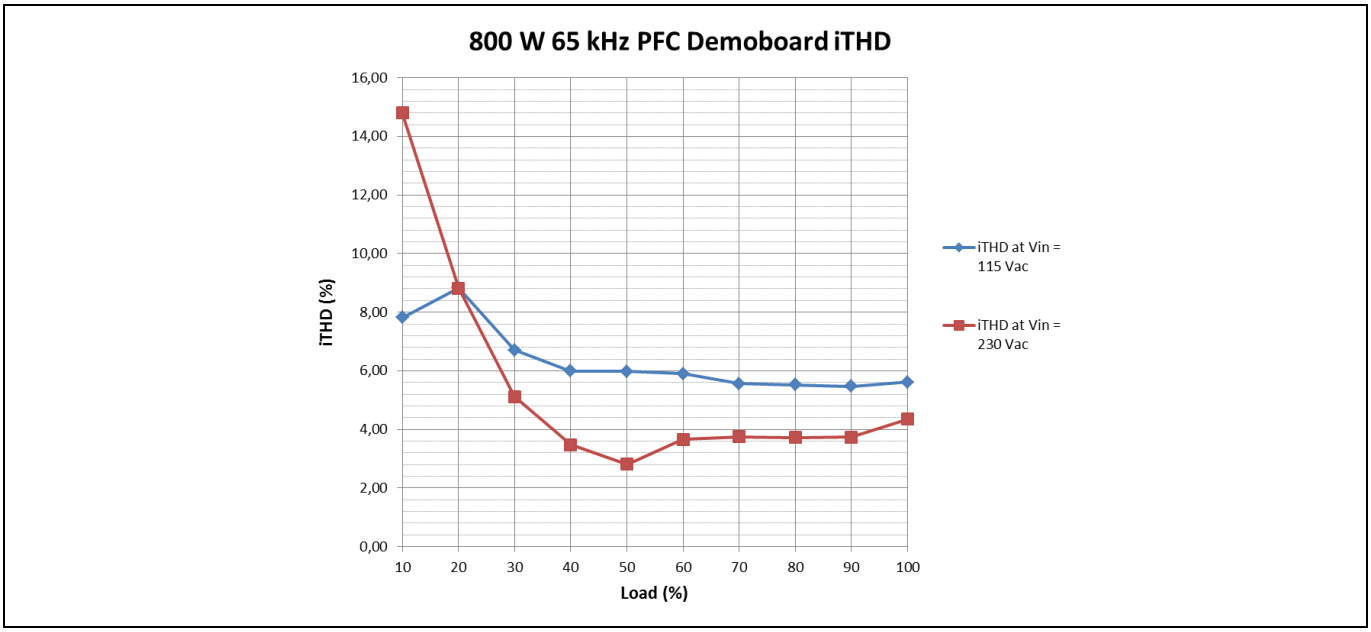


Figure 15 Input current THD at high and low line

In order to demonstrate the attractive performance of the CooMOS™ P7, additional efficiency tests were made on the demo board with previous CooMOS™ technology solutions as well as with the most commonly used competitor devices.

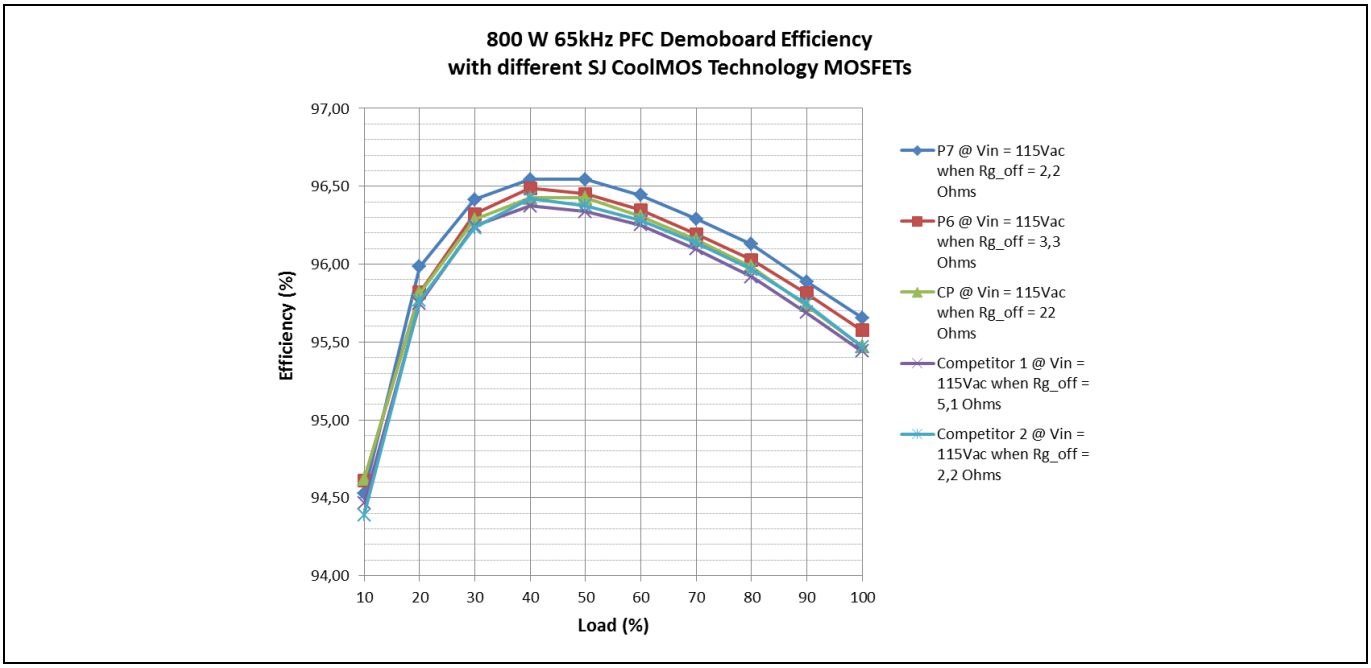


Figure 16 Efficiency comparison at V_{IN} = 115 V AC among selected SJ MOSFETs from Infineon and closest competitors with R_{DS_ON} close to 180 mΩ.

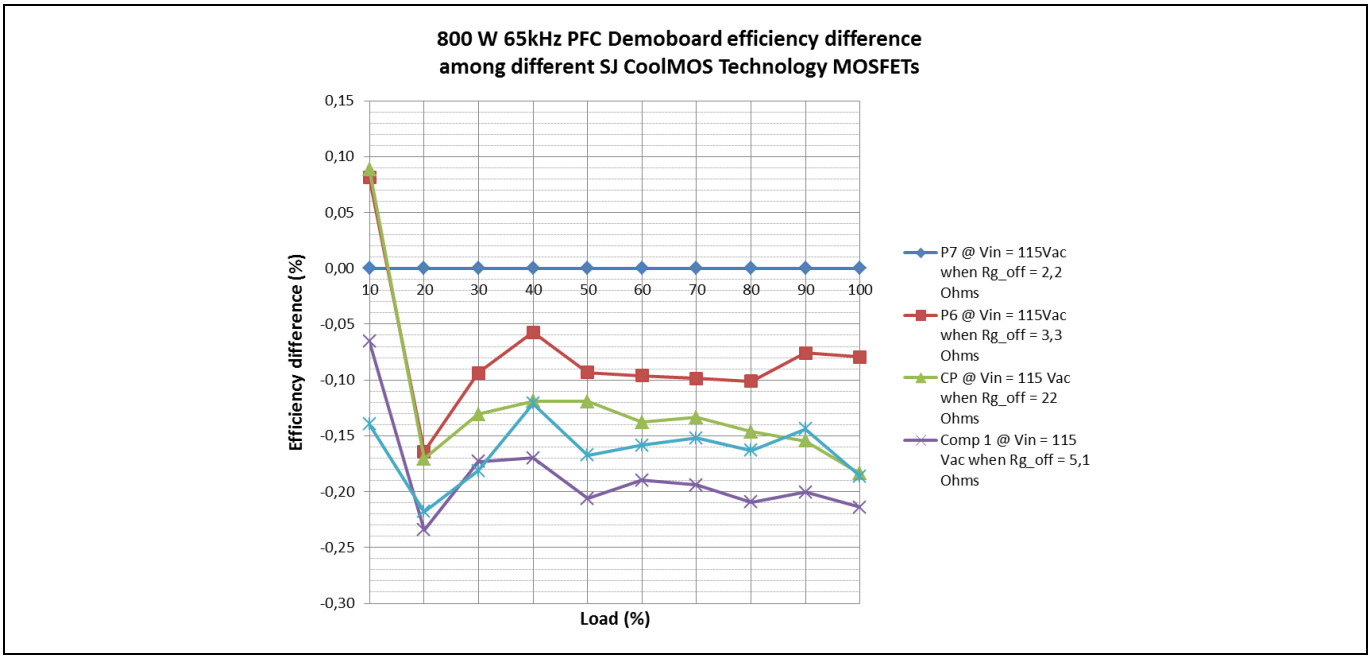


Figure 17 **Efficiency difference among selected SJ MOSFETs from Infineon and closest competitors with R_{DS_ON} close to 180 mΩ.**

5.2 Standby power consumption

Measurements performed with a “WT330” Yokogawa digital power meter showed the following results for standby power consumption of the demo board at no load:

Table 8

V_{IN} = 115 V AC	V_{IN} = 230 V AC
I_{IN} < 100 mA RMS	I_{IN} < 200 mA RMS
P_{OUT} < 1 W	P_{OUT} < 1 W

5.3 Efficiency versus MOSFETs stress

During the design process, there is always a trade-off between achieving high efficiency and semiconductor stress if the derating guidelines of IPC 9592 standard are to be fulfilled. This stress depends on drain current, drain to source voltage, stray inductances of the package and PCB as well as the switching speed (di/dt). Depending on the requirements of the application, the designer can select the proper value of turn-on and turn-off gate resistors to achieve certain efficiency at a certain stress on the MOSFET.

The design for this board is aimed at achieving high efficiency by having very low switching losses in the MOSFETs. This is achieved by using very low turn-off resistors for each of the MOSFETs with a value of 2.2 Ω. Compared to previous CooMOS™ technologies, including CP and P6, the latest P7 technology keeps the drain to source voltage below the 20% derating factor during normal operation, i.e. < 480 V DC, and shows lower ringing effects during turn-off. This gives a significant advantage to the designer when developing high efficiency PFC converters without a noticeable effect in EMI performance.

Furthermore, CoolMOS™ P7 represents our best cost/performance ratio device compared to any previous CoolMOS™ technology devices already in our portfolio.

5.4 Load steps

Key to the following figures:

- CH 2 (blue): load current
- CH2 (green): PFC output voltage (with an offset of 300 V DC)



Figure 18 Load step: 0% ➔ 100% at V_{IN} = 115 V AC



Figure 19 Load step: 0% ➔ 100% at V_{IN} = 230 V AC

Figure 18 and Figure 19 illustrate the response of the PFC converter during a load step from no load to full load with a voltage undershoot down to 325 V DC and 344 V DC, respectively. After such an abrupt load demand, the PFC controller returns to regulation in around 40 ms. Comparing both output voltage regulation responses , it

can be appreciated that, in Figure 19, the recovery is faster due to lower current demand and higher voltage availability at the input.



Figure 20 Load step: 100% ➔ 0% at V_{IN} = 115 V AC

Figure 20 illustrates the response of the voltage control loop during a load step from 100% to 10% with a voltage overshoot up to 409 V DC. A similar response can be observed at V_{IN} = 230 V AC.

5.5 Start-up

The PFC demo board has circuitry to limit the turn-on inrush current during the first half cycle to around 35 A_{peak}. After turning-on the system, the auxiliary supply will provide a stable voltage of 12 V. Once all circuits are powered and the input voltage is higher than the brown out threshold, then the PFC controller starts operating. The NTC limiter is then bypassed by the relay as long as the input current is greater than 0.2 A RMS; this precise moment can be clearly identified in the next two figures when the output voltage (blue waveform) starts to ramp up.

This timing is different for the low line and the high line situations. For further information please refer to Infineon Technologies AN-PS0052 “Design guide for boost type CCM PFC with ICE3PCS0xG” Ch. 2.14)

Key to the following two figures

- CH 1 (yellow): Input current
- CH 2 (blue): PFC output voltage
- CH 3 (magenta): 12 V DC from the auxiliary supply

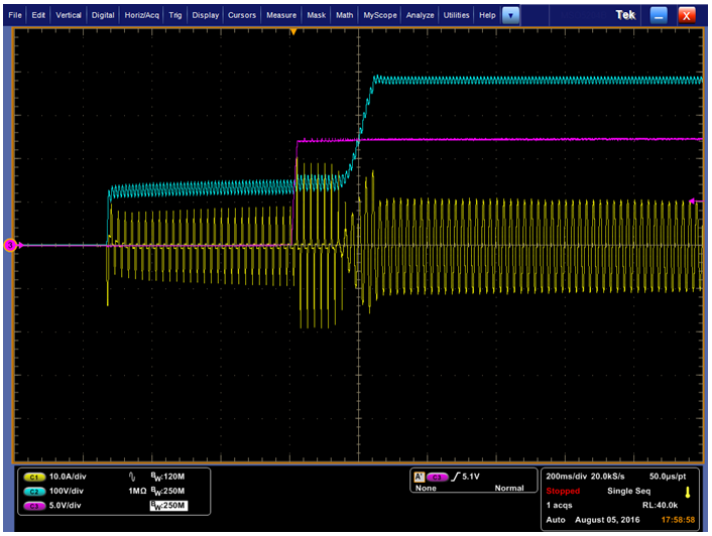


Figure 21 Star-up at V_{IN} = 115 V DC

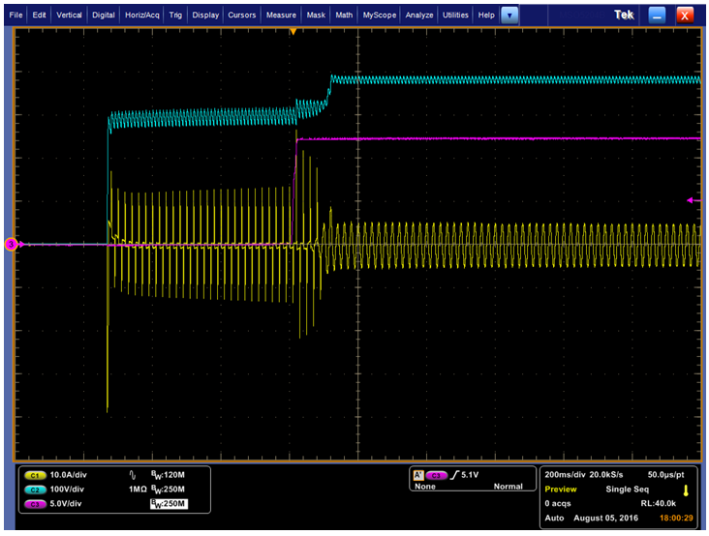


Figure 22 Start-up at V_{IN} = 230 V DC

5.6 AC line drop out

To demonstrate the robustness of the hold up time design of the PFC demo board, AC line drop out events can be tested in the worst operating conditions, i.e. no AC voltage from the grid during 10 ms working at full load.

Key to the following two figures

- CH 2 (blue): Input current of the demo board.
- CH 4 (green): PFC output voltage (with an offset of 300 V DC)



Figure 23 AC line drop out for 10 ms when V_{IN} = 115 V AC at P_{OUT} = 800 W

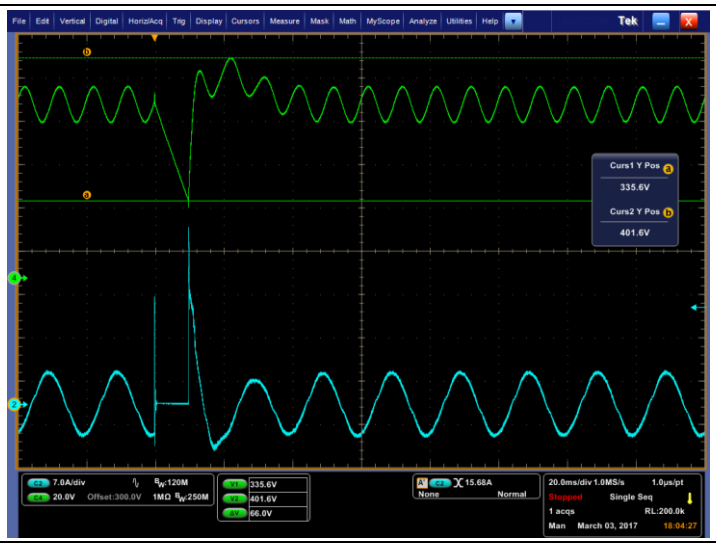


Figure 24 AC line drop out for 10 ms when V_{IN} = 230 V AC at P_{OUT} = 800 W

As can be seen in Figure 23 and Figure 24, the AC line drop out event happens at 270° with a black out of 10 ms. The return happens in the most critical point, i.e. 90°, when the current has its highest value.

In Figure 23, when the AC line voltage returns, the PFC controller boosts in current limit operating mode. This results in the sinusoidal-like truncated current waveform at the input. When the output voltage reaches the 410 V limit, then the PFC controller turns off immediately in order to avoid a higher output voltage than expected. Once the output voltage returns to the regulation level, the PFC controller starts regulating again as it does in steady state.

In the case of Figure 24, when the AC line voltage returns, the PFC controller boosts without current limit and reaches the expected regulation faster voltage due to the smaller difference between the peak input current and the output voltage. The high current spike observed when the AC line returns is due to the higher charging current of the capacitors in the EMI filter when charged at a higher input voltage, i.e. V_{IN} = 230 V AC compared to when they are charged at V_{IN} = 115 V AC.

6 Demoboard

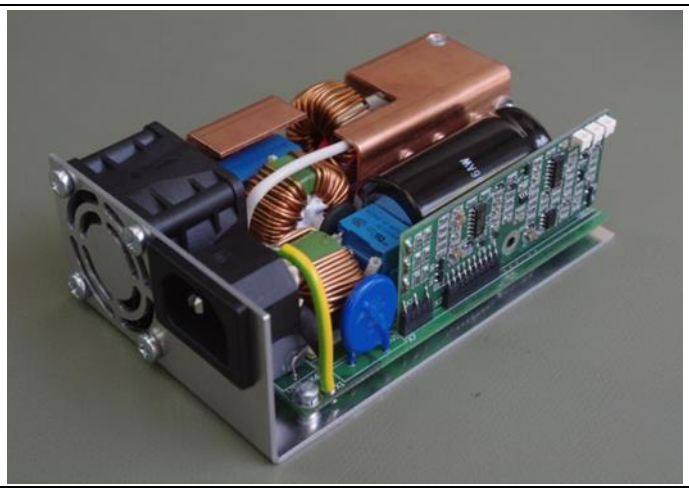


Figure 25 Picture of the 800 W 65kHz PFC demo board

6.1 Power board

6.1.1 Schematics

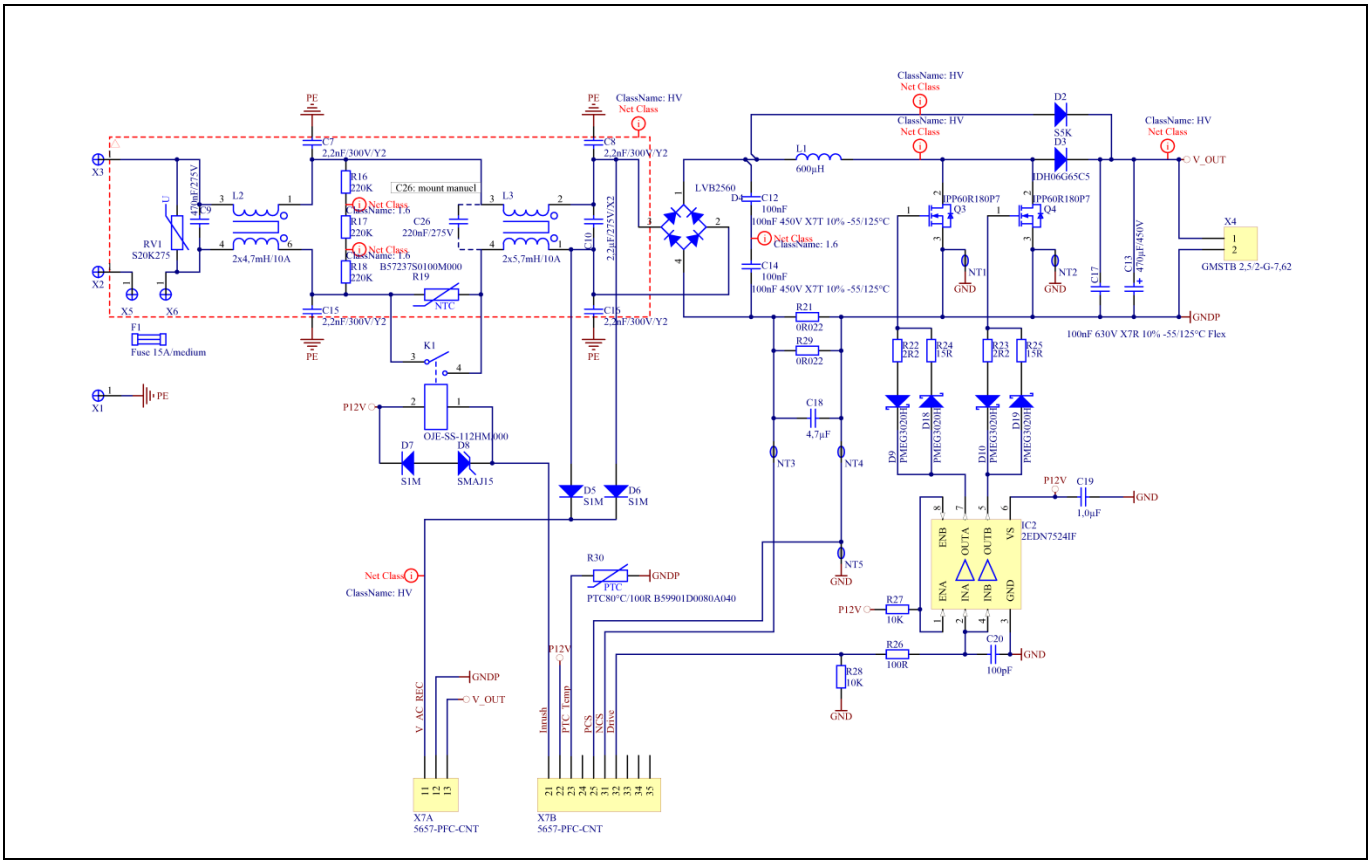


Figure 26 Schematics of the power board

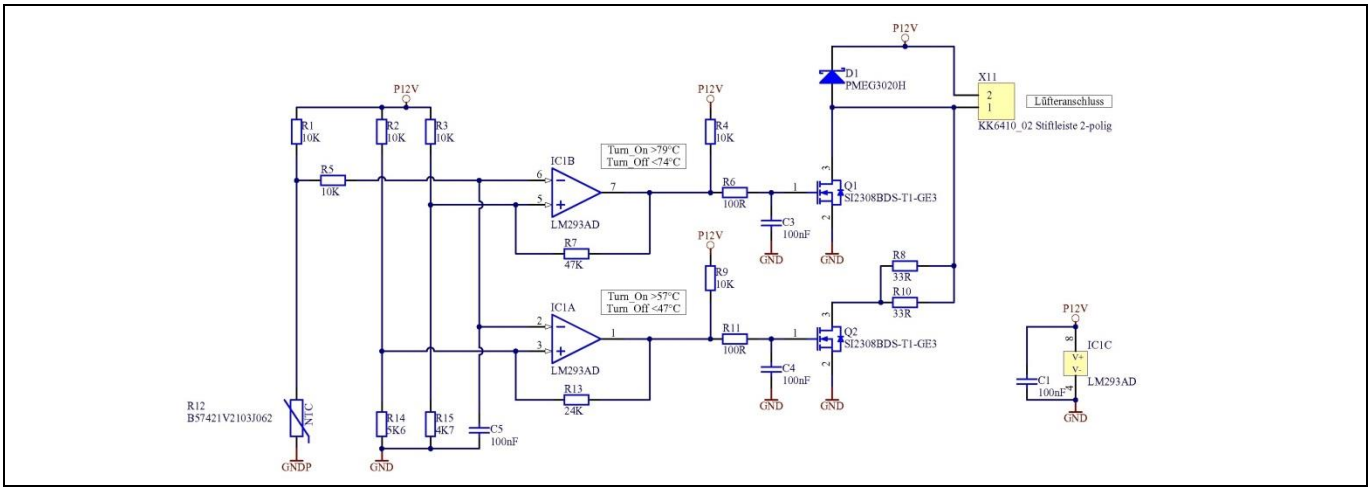


Figure 27 Schematic of fan control

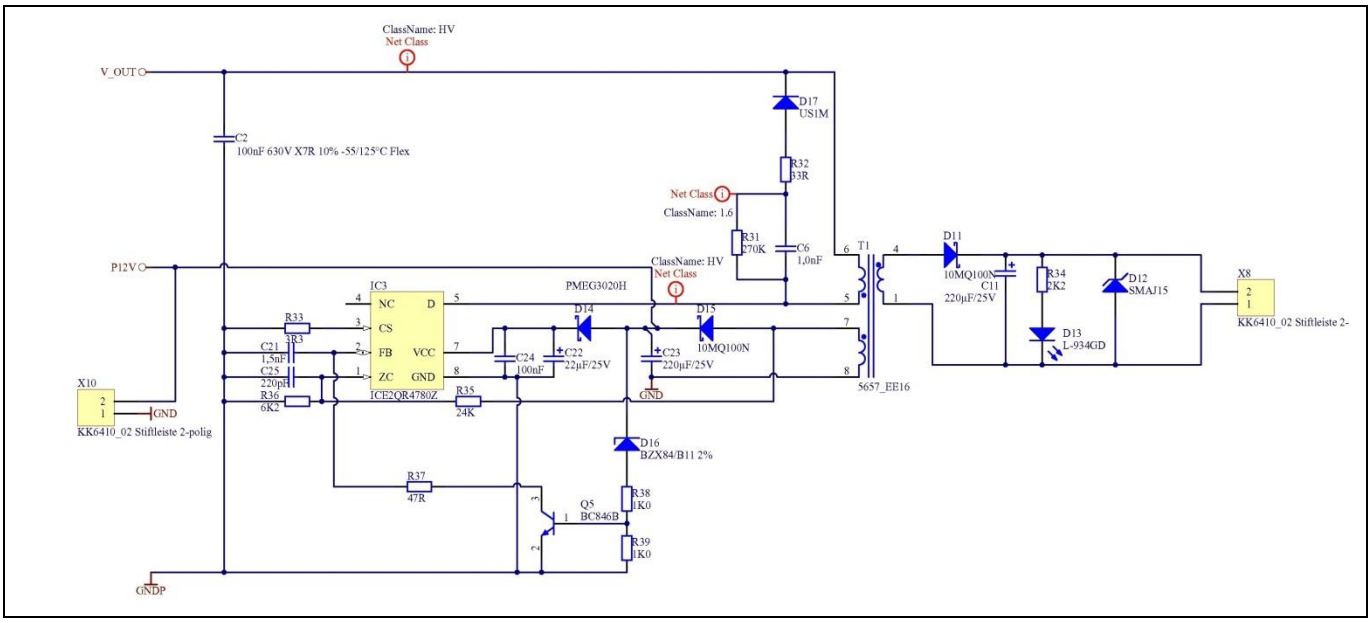


Figure 28 Schematic of auxiliary supply

6.1.2 PCB layout

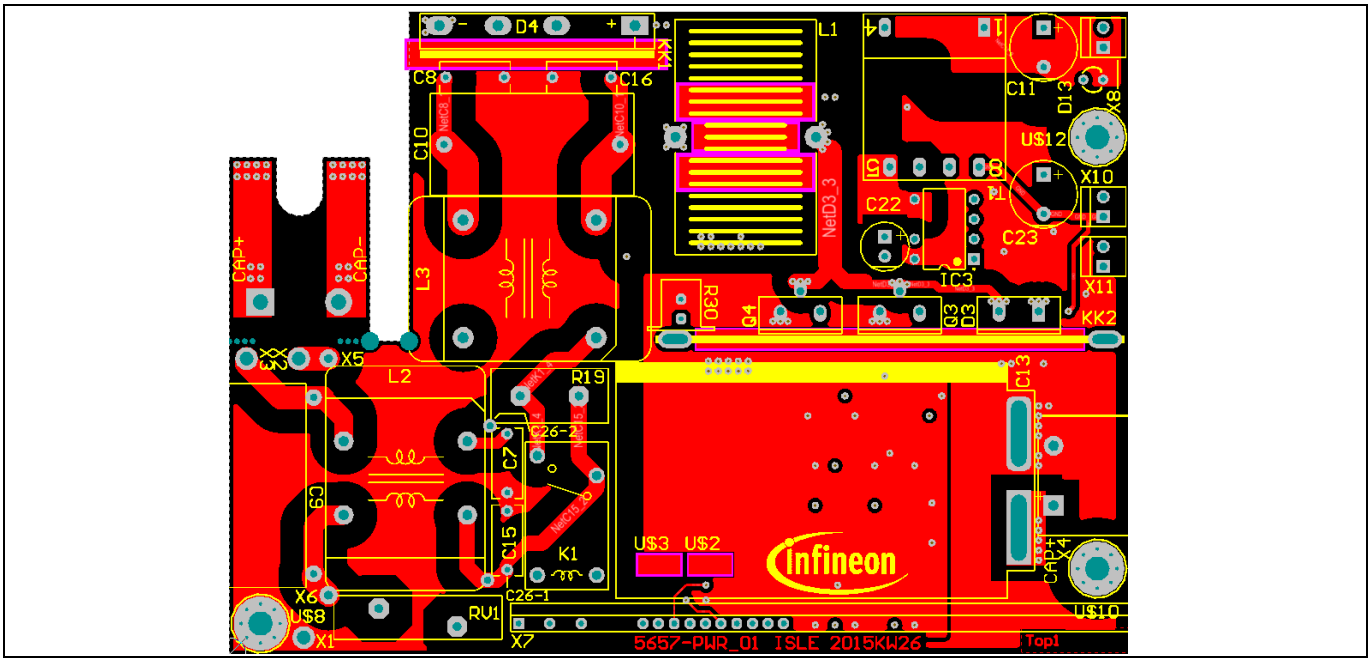


Figure 29 View of PCB top layer

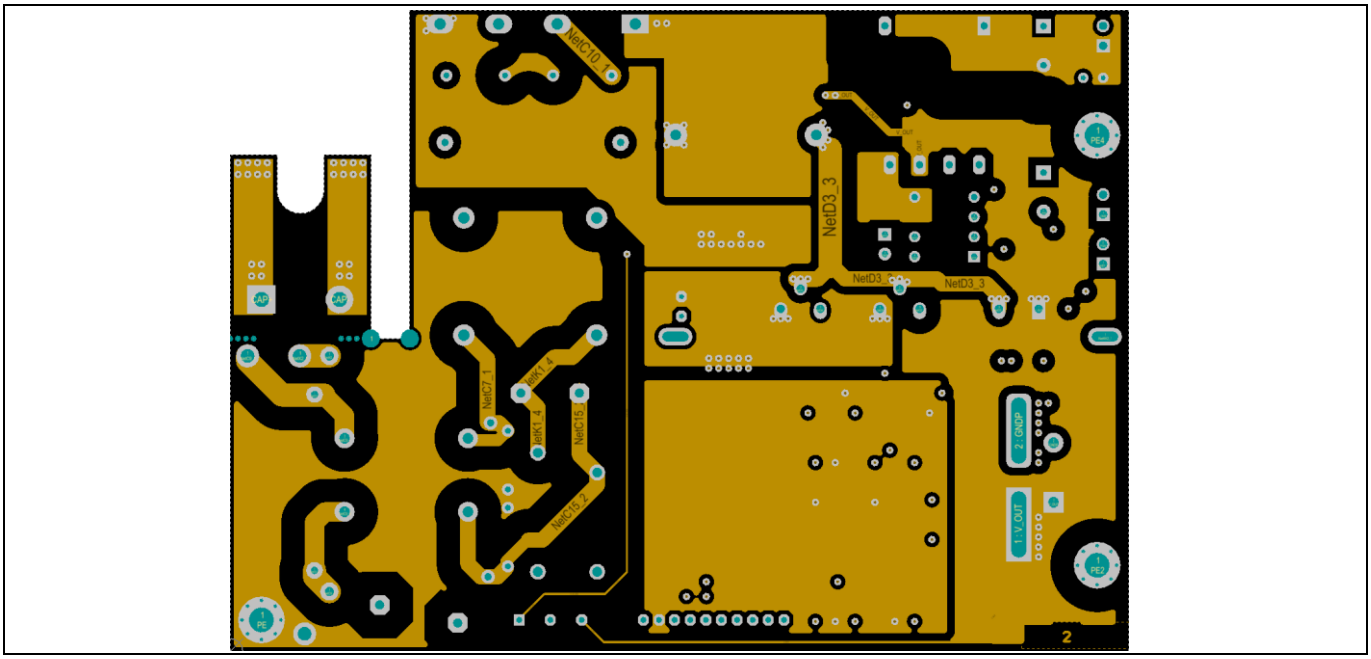


Figure 30 View of PCB inner 1 layer

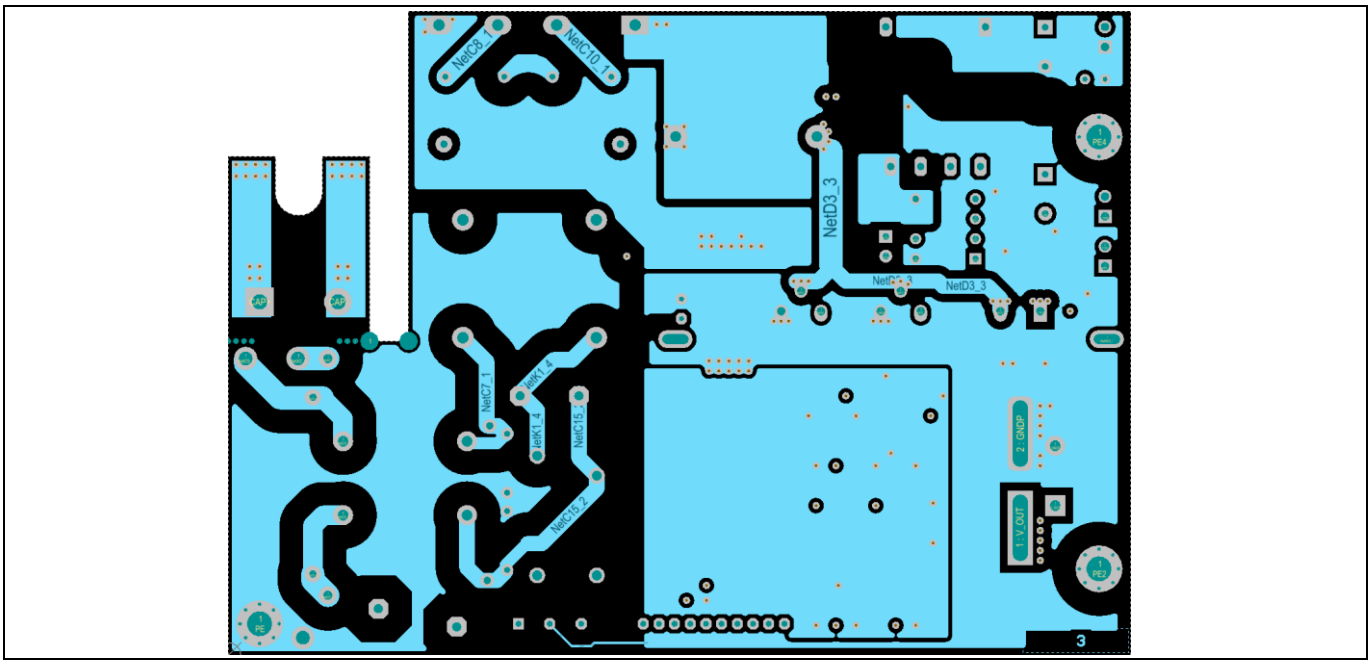


Figure 31 View of PCB inner 2 layer

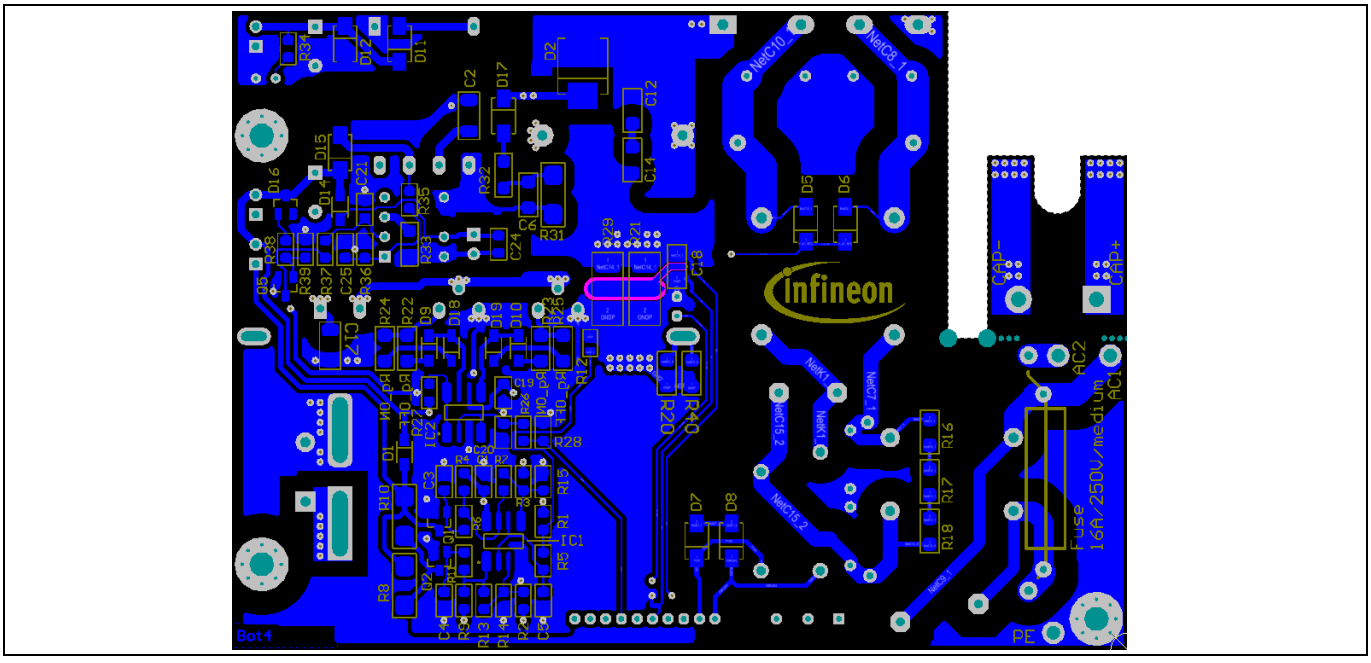


Figure 32 View of the PCB bottom layer

6.1.3 Bill of Material (BOM)

Table 9 BOM of the power board

Quantity	Comment	Description	Footprint	Designator
1	220 nF/275 V	220 nF 275 V X2		C26
1	5657-PFC-CNT		5657-CNT_Con2	X7
1	Fuse 15 A/medium	15 A Fuse		F1

1	B57237S0100M000	NTC Inrush 10R 3300 K 3,7 A 17 mW/K	B57237-Sxxx	R19
1	PTC80°C/100R B59901D0080A040	PTC	B59901-Mxxx	R30
1	1.0 µF	1.0 µF 25 V X7R 10% -55/125°C	CAPC2012M	C19
1	100 pF	100 pF 50 V C0G 5% -55/125°C	CAPC2012M	C20
1	220 pF	220 pF 50 V C0G 5% -55/125°C	CAPC2012M	C25
1	1.5 nF	1.5 nF 50 V X7R 10% -55/125°C	CAPC2012M	C21
5	100 nF	100 nF 50 V X7R 5% -55/125°C	CAPC2012M	C1, C3, C4, C5, C24
1	4.7 µF	4.7 µF 25 V X7R 10%	CAPC3216m	C18
2	100 nF	100 nF 450 V X7T 10% -55/125°C	CAPC3216M	C12, C14
1	1.0 nF	1.0 nF 630 V C0G 5%	CAPC3216M	C6
1	100 nF/630 V	100 nF 630 V X7R 10% -55/85°C	CAPC4520M	C2
1	470 µF/450 V	120 µF 450 V 105°C	CAPPA10-30x50R	C13
1	22 µF/25 V	22 µF 25 V	CAPPR2.5-6.3x11	C22
2	220 µF/25 V	220 µF 25 V	CAPPR5-8.7x12	C11, C23
4	2,2 nF/300 V/Y2		CAPR7.5-9X4	C7, C8, C15, C16
1	2,2 µF/305 V	2,2 µF 305 V X2	CAPR22.5-11X26X20	C10
1	470 nF/275 V	470 nF 275 V X2	CAPR22.5-11X26X20	C9
1	ICE2QR2280Z	PWM controller current mode QR	DIP-8_-6	IC3
1	GMSTB 2,5/2-G-7,62	Phoenix	GMSTBA2,5/2-G-7,62	X4
1	5657_EE16	EF16 bias supply	Hartu_E16-8-P2P3	T1
1	2x5,7 mH/10 A	5657 common mode choke	IFX_L-2875053801(L3)	L3
1	2x4,7 mH/10 A	5657 common mode choke	IFX_L-2875070500(L2)	L2
3	KK6410_02 Plug connector 2-pins	Molex	KK6410_2	X8, X10, X11
1	5657-KK_GL	Heatsink	KK_GL	KK1
1	5657-KK_TO220	Heatsink	KK_TO220	KK2
1	L-934GD	LED low current green	LED_5MM	D13
1	600 µH	5657 PFC choke	PFC_CHOKE-SK	L1
1	LVB2560	diode bridge 600 V 25 A	REC-GSIB-5S	D4
1	47 R		RESC2012M	R37

3	100 R		RESC2012M	R6, R11, R26
2	1K0		RESC2012M	R38, R39
1	2K2		RESC2012M	R34
1	4K7		RESC2012M	R15
1	5K6		RESC2012M	R14
1	6K2		RESC2012M	R36
8	10K		RESC2012M	R1, R2, R3, R4, R5, R9, R27, R28
2	24K		RESC2012M	R13, R35
1	47K		RESC2012M	R7
1	B57421V2103J062	NTC 10K 4000K	RESC2012N	R12
2	2R2		RESC3216M	R22, R23
2	15R		RESC3216M	R24, R25
3	220K		RESC3216M	R16, R17, R18
2	0R022	0R022 2512 RESC6330 TK75	RESC6332M	R21, R29
1	3R9		RESMELF3614M	R33
1	33R		RESMELF3614M	R32
2	33R		RESMELF5822M	R8, R10
1	270K		RESMELF5822M	R31
1	OJE-SS-112HM,000	Relay SPST-NO	RLY_TE-OJE	K1
1	S20K275	Varistor 275V 1 W	S20K275	RV1
2	SMAJ15	diode supressor	SMA_M	D8, D12
2	10MQ100N	diode schottky	SMA_M	D11, D15
3	S1M	rectifier diode	SMA_M	D5, D6, D7
1	US1M	diode ultra fast 1000 V	SMA_M	D17
1	S5K	rectifier diode	SMC_M	D2
4	PMEG3020H	diode Schottky 30 V 2 A	SOD123M	D1, D9, D10, D14
1	LM293AD	comparator	SOIC127P600-8M	IC1
1	2EDN7524IF	low side dual MOSFET driver, non-inverting	SOIC127P600-8M	IC2
1	BC846B	NPN transistor	SOT23-3M	Q5
1	BZX84/B11 2%	diode Zener	SOT23-3M	D16
2	SI2308BDS-T1-GE3	MOSFET N-Channel	SOT23-3M	Q1, Q2
2	IPP65R180P7	MOSFET N-Channel	TO220-AB_HV	Q3, Q4
1	IDH06G65C5	diode schottky 650 V	TO220-AC	D3

6.2 ICE3PCS01G daughter board

6.2.1 Schematics

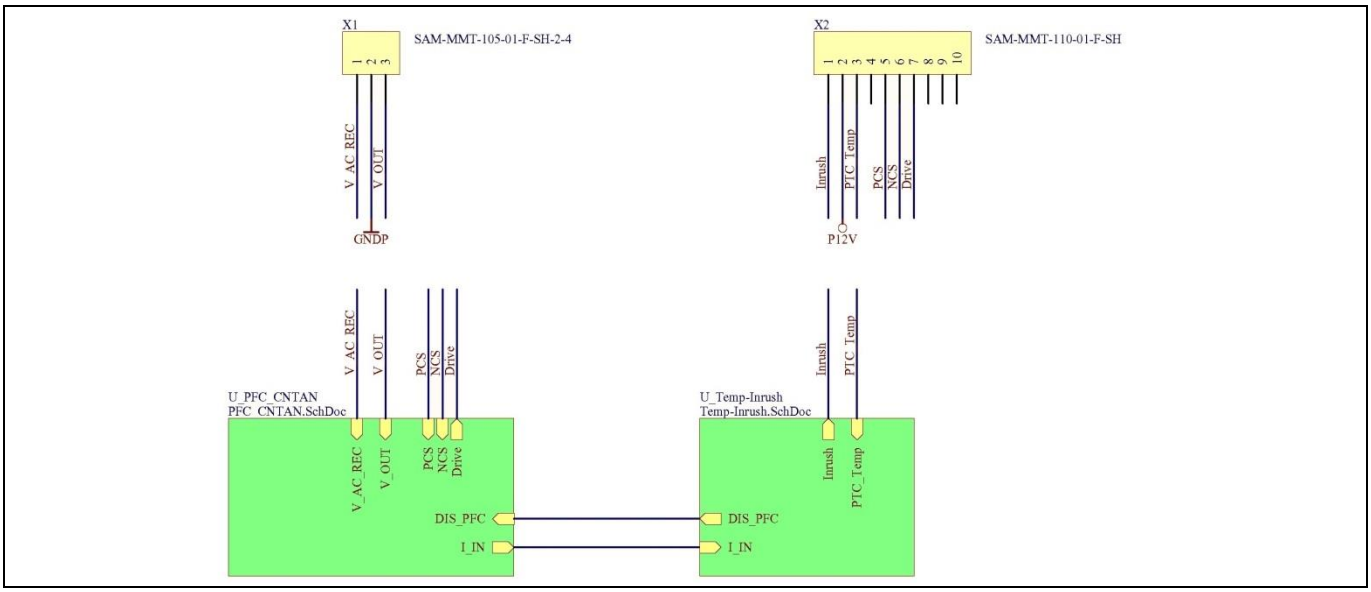


Figure 33 Schematic of the daughter card connector

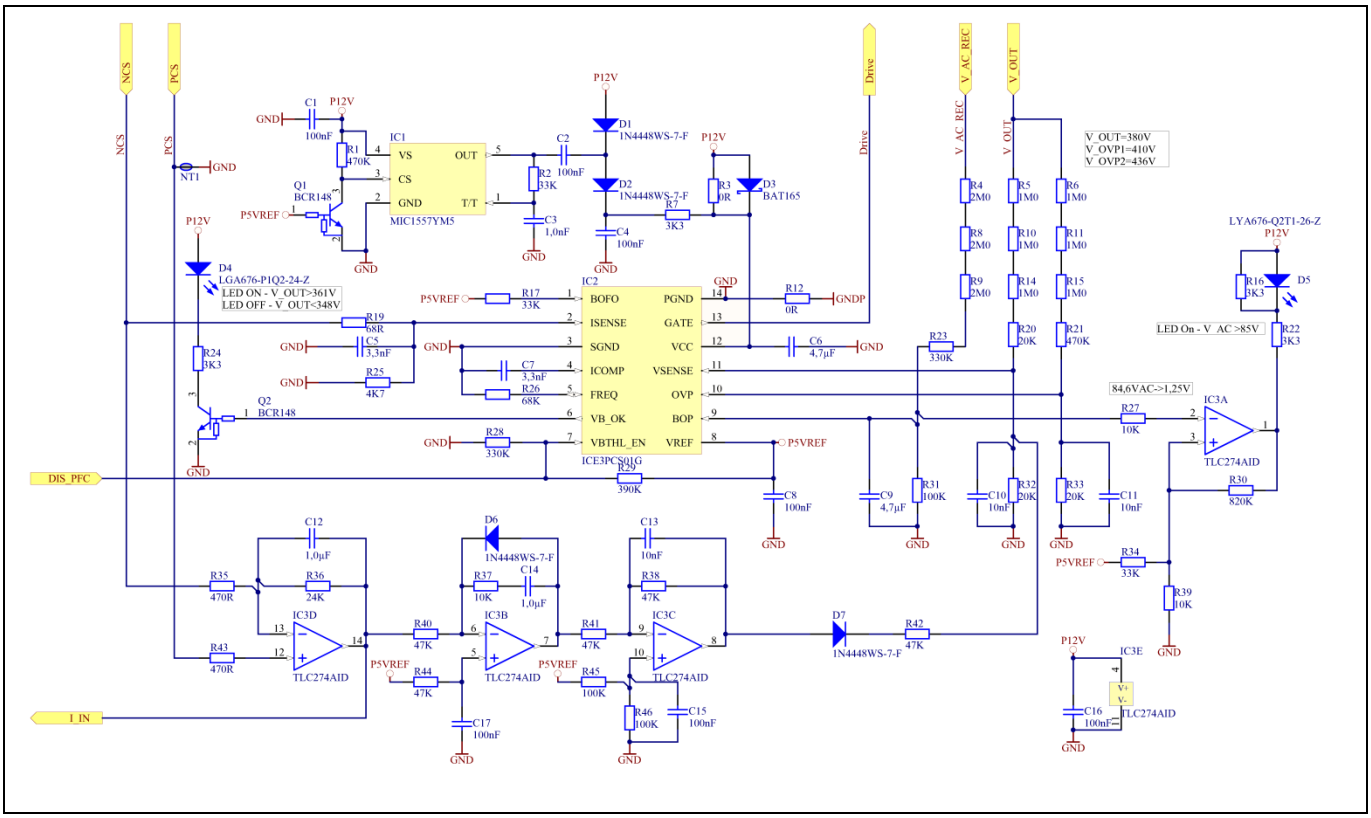


Figure 34 Schematic of PFC control

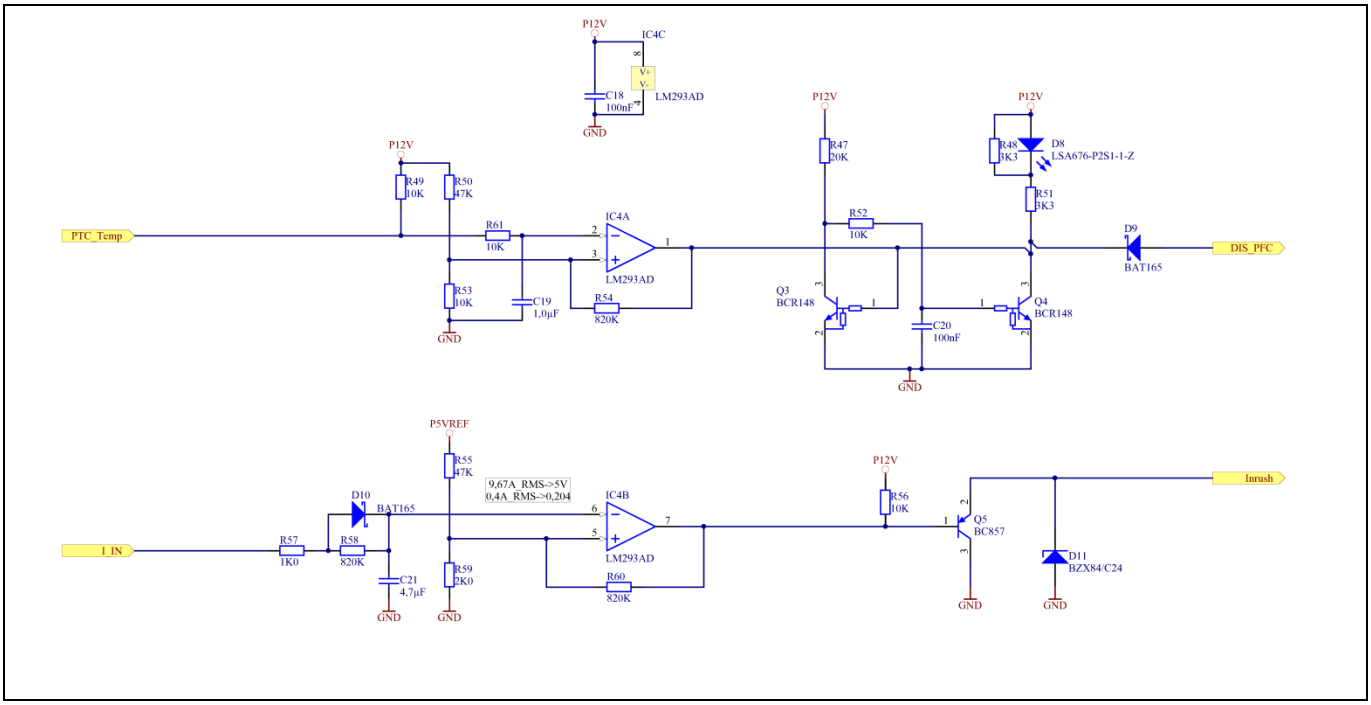


Figure 35 Schematic of temperature monitoring and inrush relay control

6.2.2 PCB layout

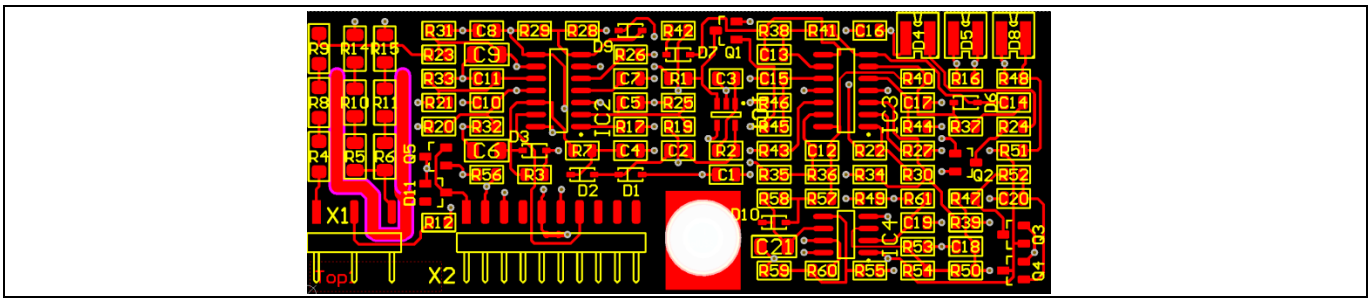


Figure 36 View of the analog control PCB top layer

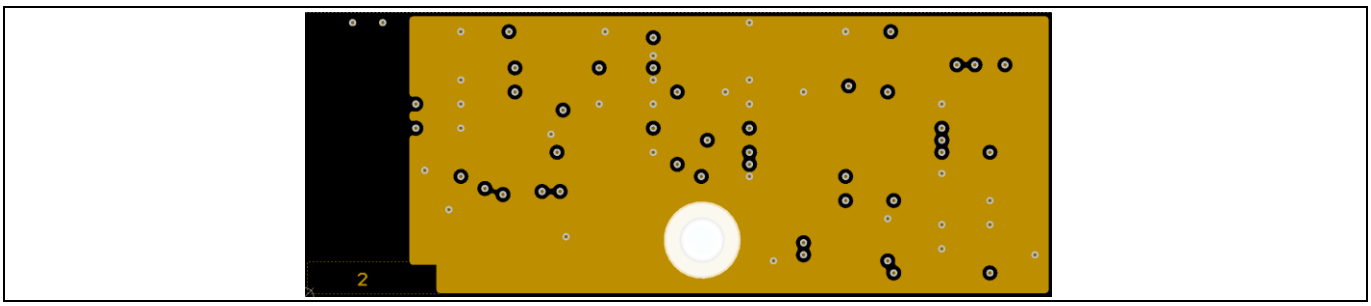


Figure 37 View of analog control PCB inner 1 layer

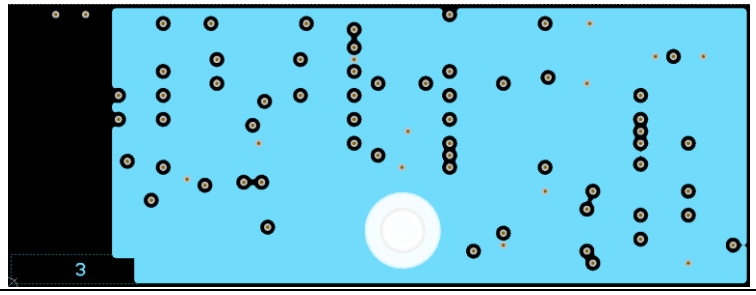


Figure 38 View of analog control PCB inner 2 layer

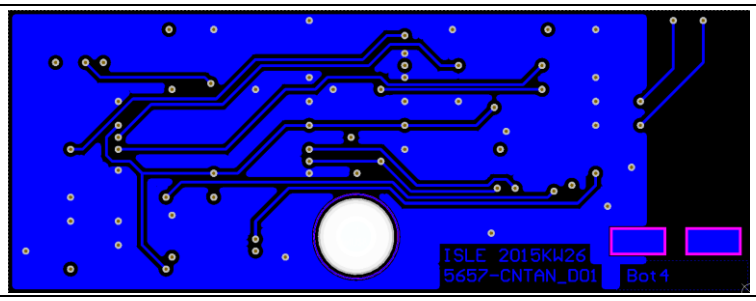


Figure 39 View of analog control PCB bottom layer

6.2.3 Bill of Material (BOM)

Table 10 BOM of the PFC control board

Quantity	Comment	Description	Footprint	Designator
3	1.0 µF	1.0 µF 25 V X7R 10% -55/125°C	CAPC2012N	C12, C14, C19
1	1.0 nF	1.0 nF 50 V C0G 5% -55/125°C	CAPC2012N	C3
2	3.3 nF	3.3 nF 50 V X7R 10% -55/125°C	CAPC2012N	C5, C7
3	10 nF	10 nF 50 V X7R 5% -55/125°C	CAPC2012N	C10, C11, C13
9	100 nF	100 nF 50 V X7R 5% -55/125°C	CAPC2012N	C1, C2, C4, C8, C15, C16, C17, C18, C20
3	4.7 µF	4.7 µF 25 V X7R 10%	CAPC3216N	C6, C9, C21
1	LSA676-P2S1-1-Z	LED hyper bright super-red	LED_LxA670	D8
1	LGA676-P1Q2-24-Z	LED hyper bright green	LED_LxA670	D4
1	LYA676-Q2T1-26-Z	LED low current yellow	LED_LxA670	D5
1	68R		RESC2012N	R19
2	470R		RESC2012N	R35, R43
2	1K0		RESC2012N	R57, R59
6	3K3		RESC2012N	R7, R16, R22, R24, R48, R51

1	4K7		RESC2012N	R25
7	10K		RESC2012N	R27, R37, R39, R52, R53, R56, R61
4	20K		RESC2012N	R20, R32, R33, R47
1	24K		RESC2012N	R36
3	33K		RESC2012N	R2, R17,R34
1	68K		RESC2012N	R26
8	47K		RESC2012N	R38, R40, R41, R42, R44, R49, R50, R55
3	100K		RESC2012N	R31, R45, R46
2	330K		RESC2012N	R23, R28
1	390K		RESC2012N	R29
2	470K		RESC2012N	R1, R21
4	820K		RESC2012N	R30, R54, R58, R60
6	1M0		RESC3216N	R5, R6, R10, R11, R14, R15
3	2M0		RESMELF3614N	R4, R8, R9
1	SAM-MMT-105-01-X-SH-2-4		SAM-MMT-105-01-X-SH-2-3	X1
1	SAM-MMT-110-01-X-SH		SAM-MMT-110-01-X-SH	X2
3	BAT165	diode schottky	SOD323	D3, D9, D10
4	1N4448WS-7-F	diode fast switching	SOD323	D1, D2, D6, D7
1	LM293AD	comparator	SOIC127P600-8N	IC4
1	TLC274AID	operational amplifier	SOIC127P600-14N	IC3
1	ICE3PCS01G	PFC controller Continuous Conduction Mode(CCM)	SOIC127P600-14N	IC2
1	BC857	pnp transistor	SOT23-3N	Q5
4	BCR148	npn transistor	SOT23-3N	Q1, Q2, Q3, Q4
1	BZX84/C24	diode Zener	SOT23-3N	D11
1	MIC1557YM5	timer	SOT23-5N	IC1

7 Useful material and links

- 600 V CooMOS™ P7 webpage
  www.infineon.com/600v-P7

- 650 V CoolSiC™ Schottky diode generation 5 webpage
  http://www.infineon.com/cms/en/product/power/sicarbide-sic/650v-thinq!-tm-sic-diode-generation-5/channel.html?channel=db3a3043399628450139b0536bed2187

- 2EDN7524F non-isolated gate driver (EICEDRIVER™)
  http://www.infineon.com/cms/en/product/power/motor-control-and-gate-driver-ics/non-isolated-gate-driver-ics-and-controllers/eicedriver-2edn-gate-driver-for-discrete-mosfets/channel.html?channel=5546d4624cb7f111014d334aeae60252

- ICE3PCS01G PFC controller webpage
  http://www.infineon.com/cms/en/product/power/ac-dc-power-conversion/ac-dc-pwm-pfc-controller/pfc-ccm-continuous-conduction-mode-ic/ICE3PCS01G/productType.html?productType=db3a304329a0f6ee0129a67b7e462b48

- ICE2QR2280Z flyback controller product webpage
  http://www.infineon.com/cms/en/product/power/ac-dc-power-conversion/ac-dc-integrated-power-stage-coolset/ac-dc-quasi-resonant-coolset/ICE2QR2280Z/productType.html?productType=db3a30432a7fedfc012a8d813a9d0477

[1] A Reference. See the code examples at **www.infineon.com**

Revision history

Major changes since the last revision

Page or reference	Description of change

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