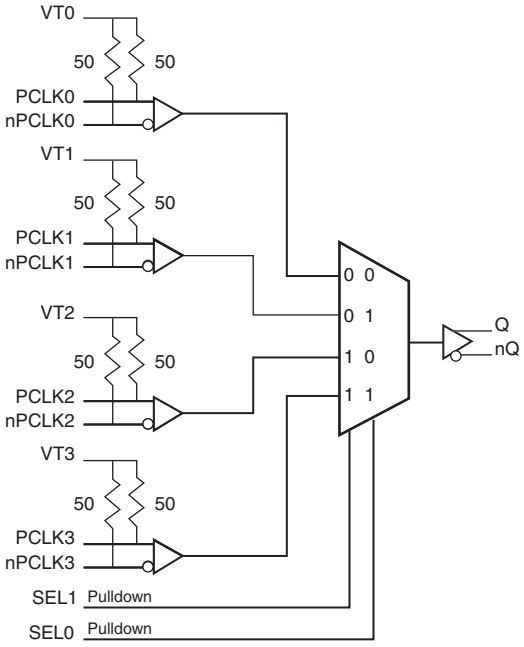
General Description

The 854S057B is a 4:1 or 2:1 LVDS Clock Multiplexer which can operate up to 2GHz. The PCLK, nPCLK pairs can accept most standard differential input levels. Internal termination is provided on each differential input pair. The 854S057B operates using a 2.5V supply voltage. The fully differential architecture and low propagation delay make it ideal for use in high speed multiplexing applications. The select pins have internal pulldown resistors. Leaving one input unconnected (pulled to logic low by the internal resistor) will transform the device into a 2:1 multiplexer. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects PCLK0, nPCLK0).

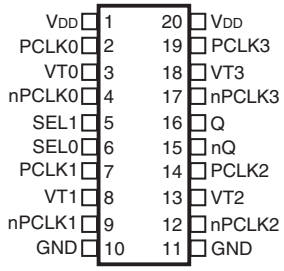
Features

- High speed differential multiplexer. The device can be configured as either a 4:1 or 2:1 multiplexer
- One LVDS output pair
- Four selectable PCLK, nPCLK inputs with internal termination
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: >2GHz
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 800ps (maximum)
- Additive phase jitter, RMS: 0.065ps (typical)
- Full 2.5V power supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



854S057B

20-Lead TSSOP
4.4mm x 6.5mm x 0.925mm package body
G Package
Top View

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Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 20	V_{DD}	Power		Power supply pins.
2	PCLK0	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to VT0.
3	VT0	Input		Termination input. For LVDS input, leave floating. R_T = 50Ω termination to VT0.
4	nPCLK0	Input		Inverting LVPECL differential clock input. R_T = 50Ω termination to VT0.
5, 6	SEL1, SEL0	Input	Pulldown	Clock select inputs. LVCMOS/LVTTL interface levels.
7	PCLK1	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to VT1.
8	VT1	Input		Termination input. For LVDS input, leave floating. R_T = 50Ω termination to VT1.
9	nPCLK1	Input		Inverting LVPECL differential clock input. R_T = 50Ω termination to VT1.
10, 11	GND	Power		Power supply ground.
12	nPCLK2	Input		Inverting LVPECL differential clock input. R_T = 50Ω termination to VT2.
13	VT2	Input		Termination input. For LVDS input, leave floating. R_T = 50Ω termination to VT2.
14	PCLK2	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to VT2.
15, 16	nQ, Q	Output		Differential output pair. LVDS interface levels.
17	nPCLK3	Input		Inverting LVPECL differential clock input. R_T = 50Ω termination to VT3.
18	VT3	Input		Termination input. For LVDS input, leave floating. R_T = 50Ω termination to VT3.
19	PCLK3	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to VT3.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
R_T	Input Termination Resistor		40	50	60	Ω

Function Table

Table 3. Control Input Function Table

Inputs		Outputs
SEL1	**SEL0**	**PCLKx, nPCLKx**
0	0	PCLK0, nPCLK0
0	1	PCLK1, nPCLK1
1	0	PCLK2, nPCLK2
1	1	PCLK3, nPCLK3

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Input Current, PCLK, nPCLK	±50mA
V_T Current, I_{VT}	±100mA
Package Thermal Impedance, θ_{JA}	92.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				50	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	SEL0, SEL1	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	SEL0, SEL1	V_{DD} = 2.625V, V_{IN} = 0V	-10			µA

Table 4C. LVPECL Differential DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IN}	Absolute Input Current; NOTE 1	V_{DD} = V_{IN} = 2.625V			35	mA
V_{PP}	Peak-to-Peak Voltage; NOTE 2		0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 2, 3		GND + 1.2		V_{DD}	V

NOTE 1: Guaranteed by design.
NOTE 2: V_{IL} should not be less than -0.3V.
NOTE 3: Common mode input voltage is defined as V_{IH}.

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Table 4D. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		225	325	425	mV
ΔV_{OD}	V_{OD} Magnitude Change			4	35	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			5	25	mV

Table 5. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

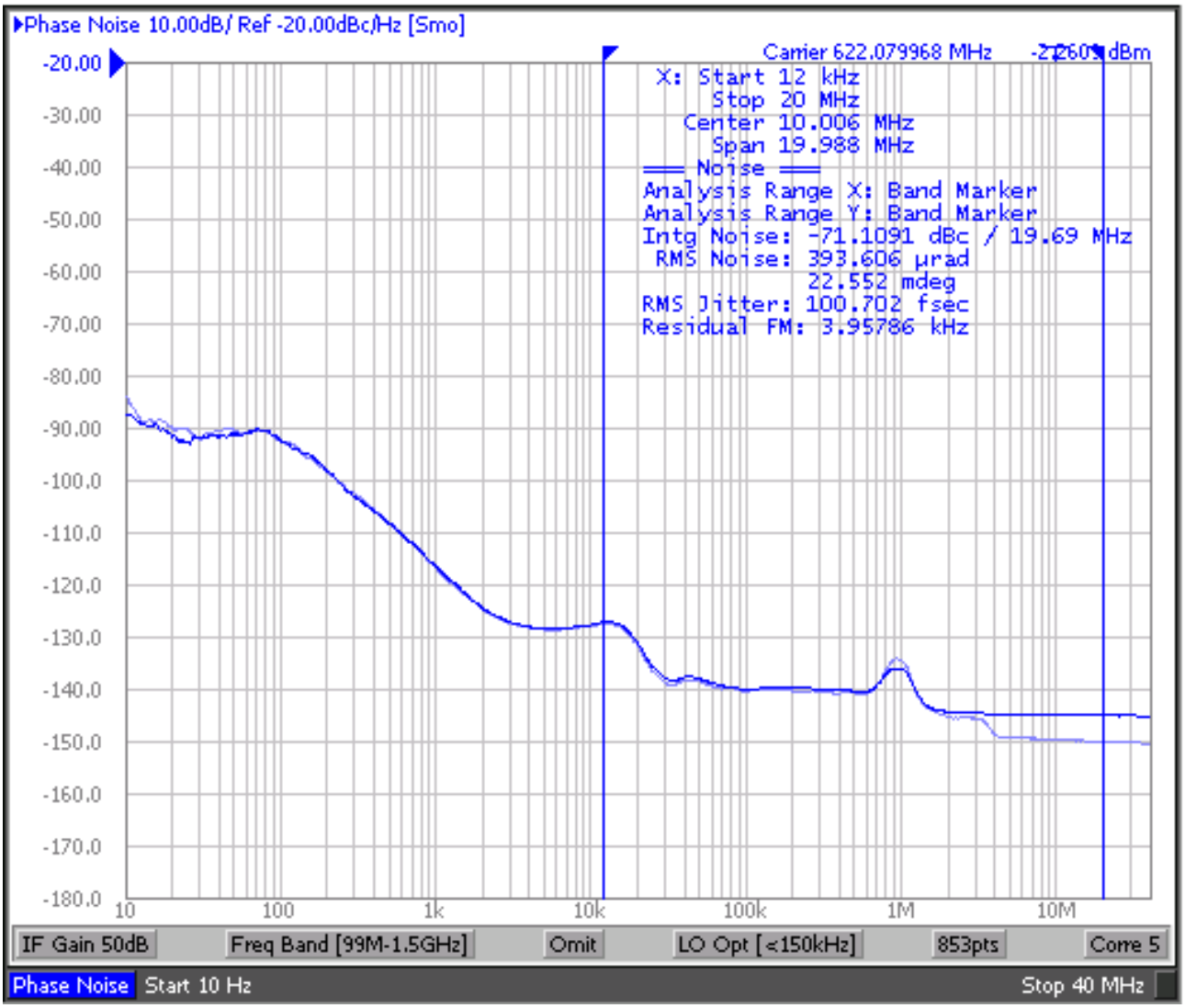
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			>2		GHz
t_{PD}	Propagation Delay; NOTE 1		300		800	ps
tsk(pp)	Part-to-Part Skew; NOTE 2, 3				200	ps
tsk(i)	Input Skew				40	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	622.08MHz, Integration Range: 12kHz – 20MHz		0.065		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
odc	Output Duty Cycle	≤ 700MHz	49		51	%
		$f \leq$ 1.1GHz	47		53	%
		$f \leq$ 2GHz	43		57	%
$MUX_{ISOLATION}$	MUX Isolation	f = 500MHz		-65		dBm

NOTE: All parameters measured at $f \leq$ 1.9GHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between different devices operating at the same supply voltage, same frequency and with equal load conditions. Using the same type of inputs on each device, the output is measured at the differential cross point.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

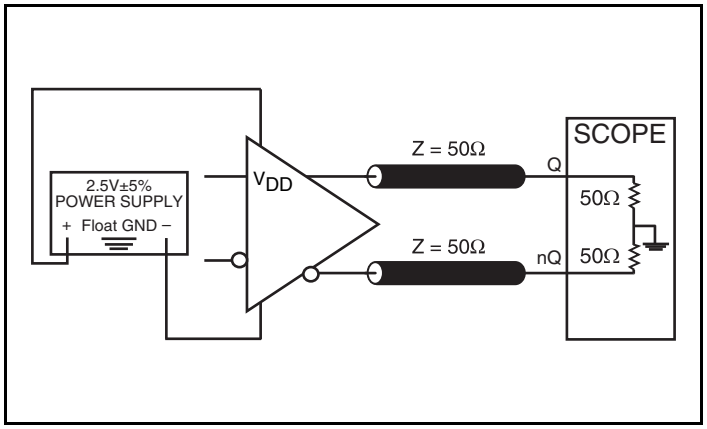


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

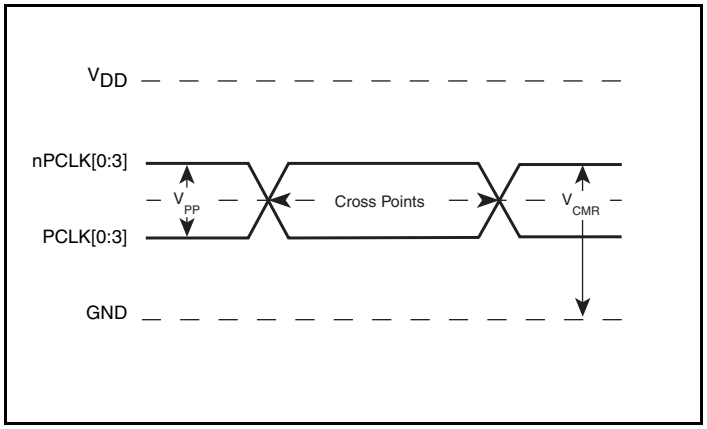
The source generator "Rohde & Schwarz SMA100A Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".

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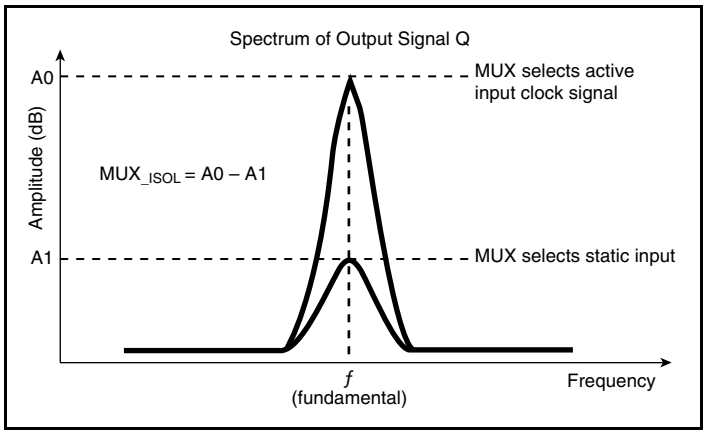
Parameter Measurement Information



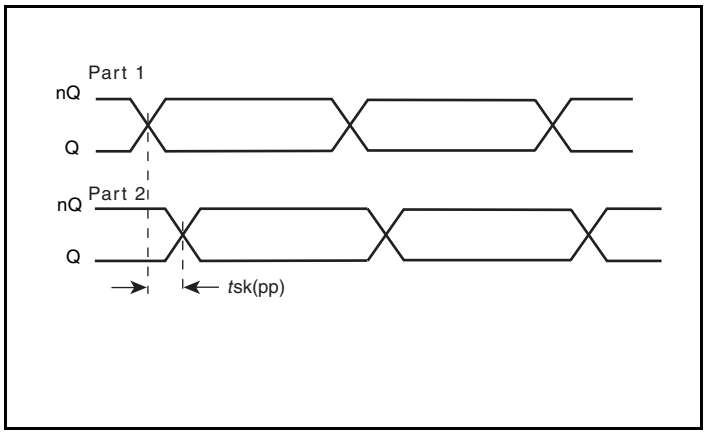
LVDS Output Load AC Test Circuit



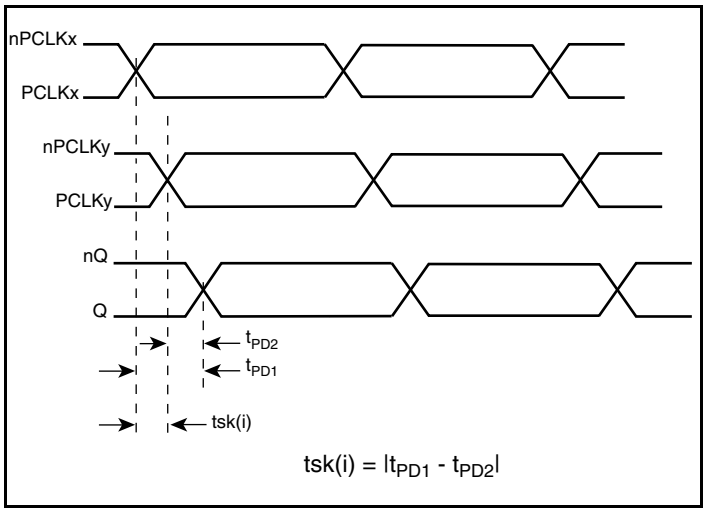
Differential Input Level



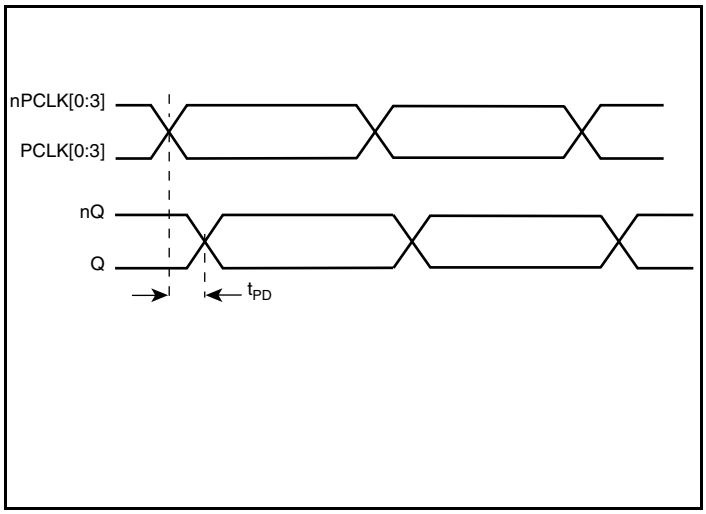
MUX Isolation



Part-to-Part Skew

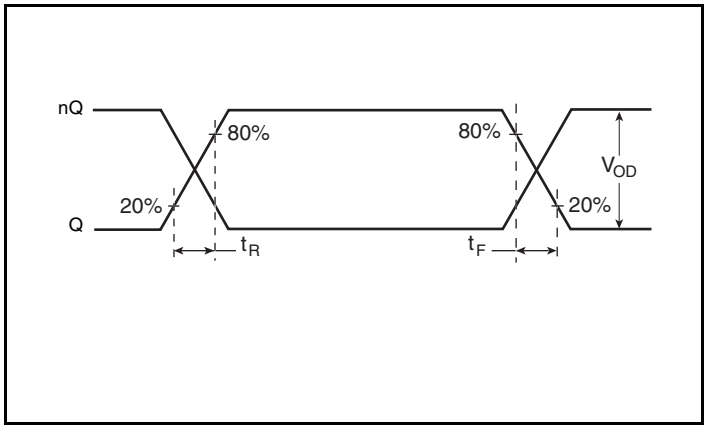


Input Skew

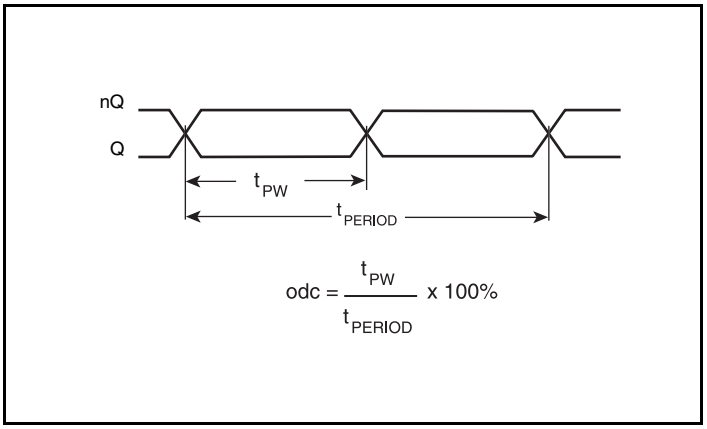


Propagation Delay

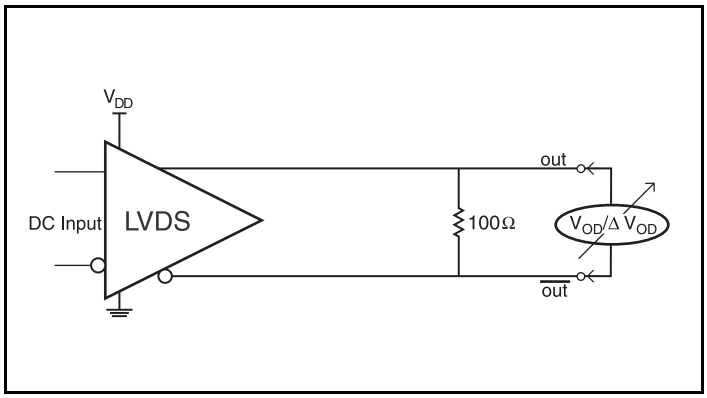
Parameter Measurement Information, continued



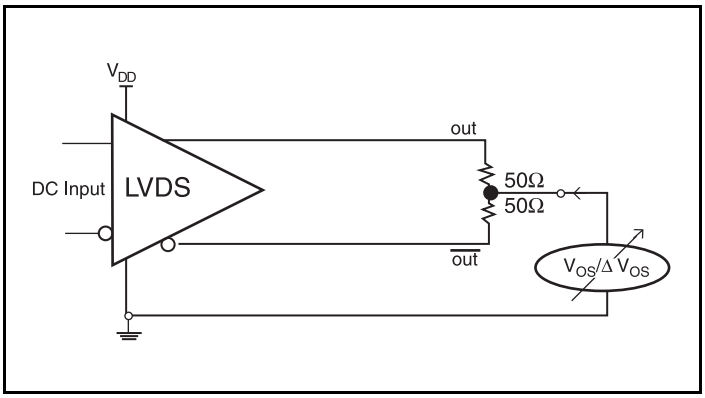
Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

2.5V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 1.*

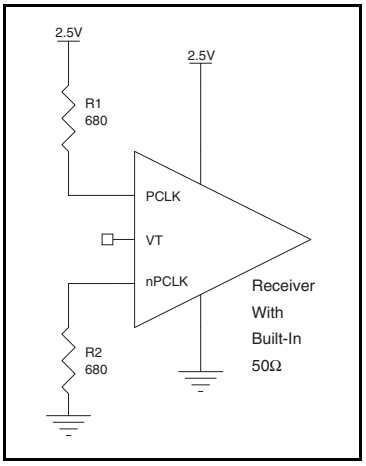


Figure 1. Unused Input Handling

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The PCLK /nPCLK with built-in 50Ω terminations accept LVDS, LVPECL, CML, SSTL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK /nPCLK with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

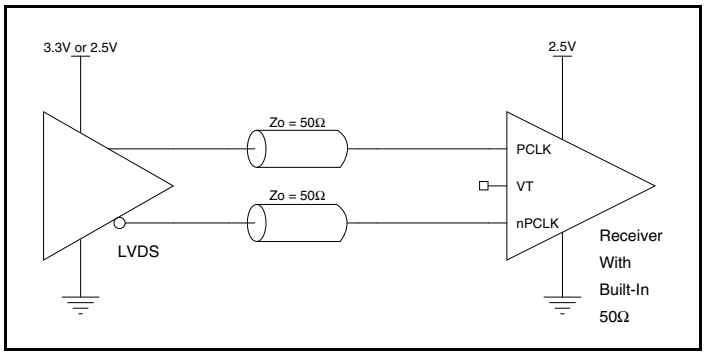


Figure 2A. PCLK/nPCLK Input with Built-In 50Ω Driven by an LVDS Driver

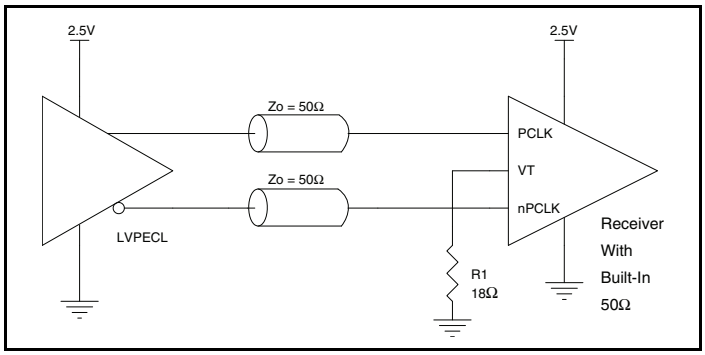


Figure 2B. PCLK/nPCLK Input with Built-In 50Ω Driven by an LVPECL Driver

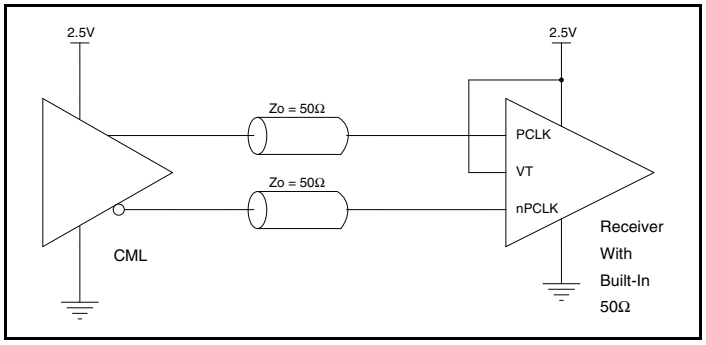


Figure 2C. PCLK/nPCLK Input with Built-In 50Ω Driven by a CML Driver

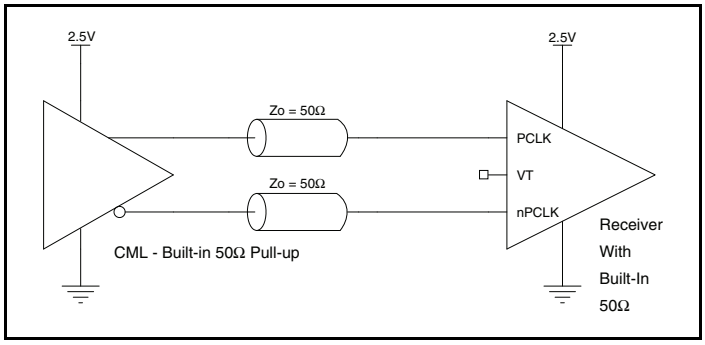


Figure 2D. PCLK/nPCLK Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

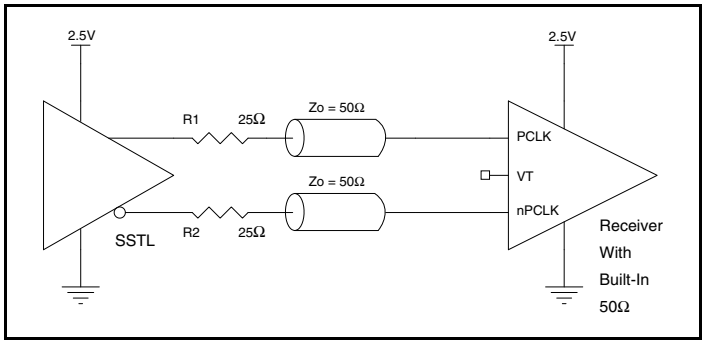


Figure 2E. PCLK/nPCLK Input with Built-In 50Ω Driven by an SSTL Driver

LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 3 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

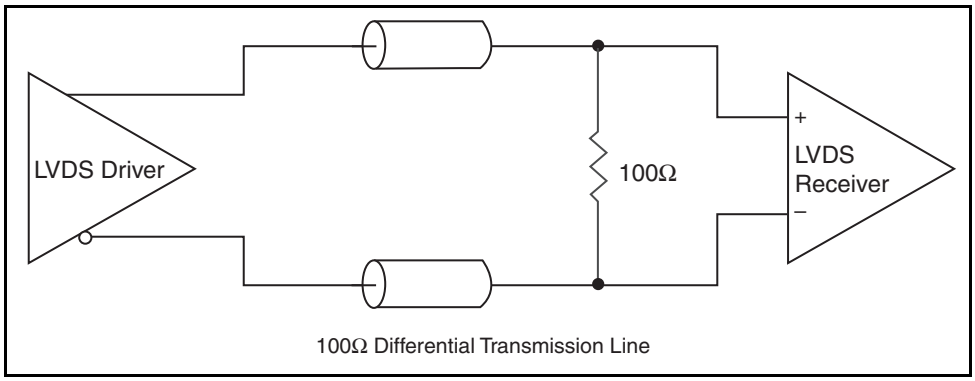


Figure 3. Typical LVDS Driver Termination

Schematic Example

Figure 4 shows a schematic example of the 854S057B. In this example, the PCLK0/nPCLK0 and PCLK1/nPCLK1 inputs are used. The decoupling capacitors should be physically located near the power pin.

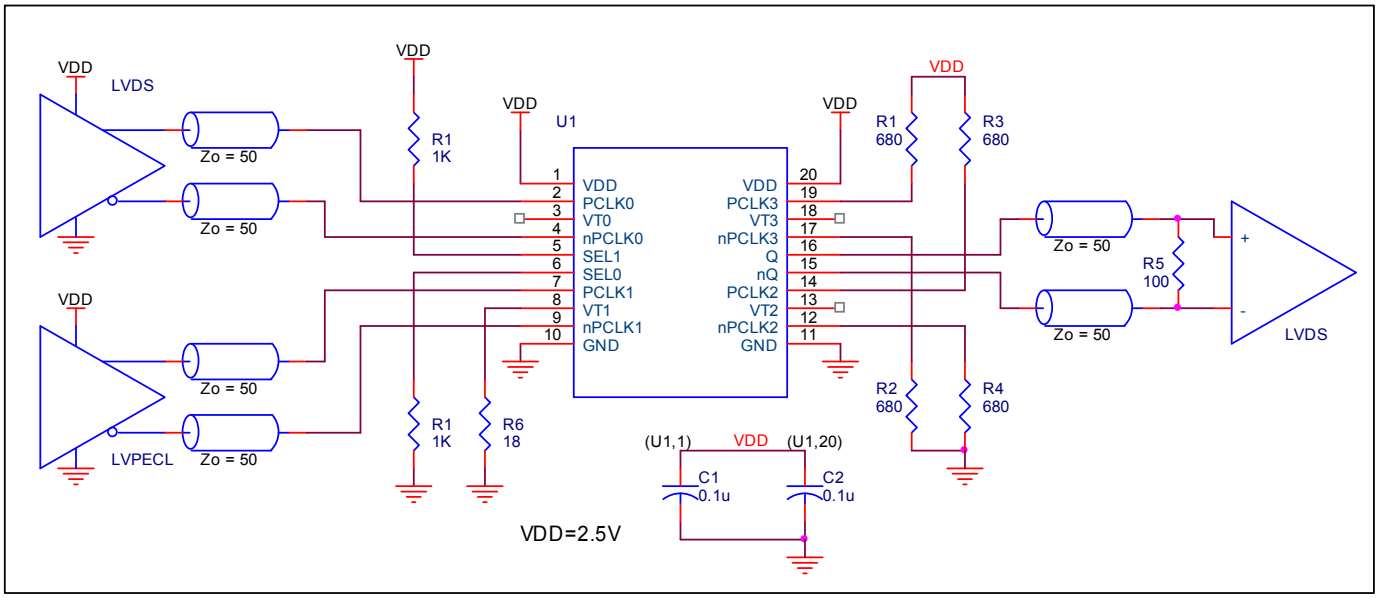


Figure 4. 854S057B LVDS Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 854S057B.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 854S057B is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD_MAX} * I_{DD_MAX}$ = 2.625V * 50mA = **131.25mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX} = 4 * (V_{PP_MAX})^2 / R_{T_MIN} = (1.2V)^2 / 80\Omega$ = **72mW**

Total Power$_{_MAX}$ = 131.25mW + 72mW = **203.25mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.203W * 92.1°C/W = 103.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.1°C/W	86.5°C/W	83.0°C/W

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.1°C/W	86.5°C/W	83.0°C/W

Transistor Count

The transistor count for 854S057B is: 375
This device is pin and function compatible and a suggested replacement for 854057.

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

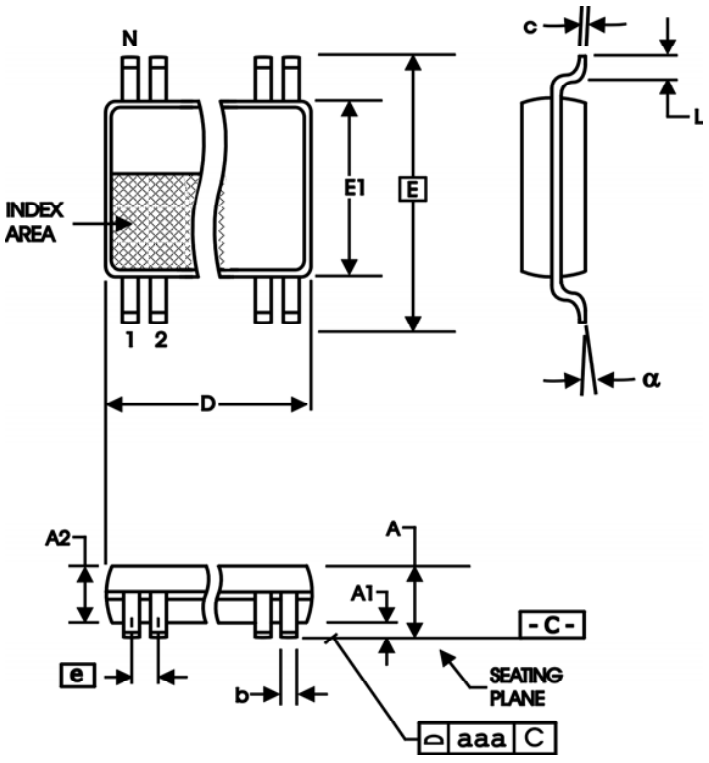


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S057BGILF	ICS54S057BIL	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
854S057BGILFT	ICS54S057BIL	“Lead-Free” 20 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		10 11	Updated LVDS Output Termination application note. Updated Power Dissipation calculation in Power Considerations Application Note.	3/26/10
A		11	Corrected Power Dissipation calculation in the Power Considerations Application Note.	3/29/10
B	T9	1 13	General Description - deleted HiperClocks logo. Ordering Information Table - deleted count for Tape & Reel. Deleted "ICS" prefix and "I" suffix in the part number throughout the datasheet.	2/10/16

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(Rev.1.0 Mar 2020)

Corporate Headquarters

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