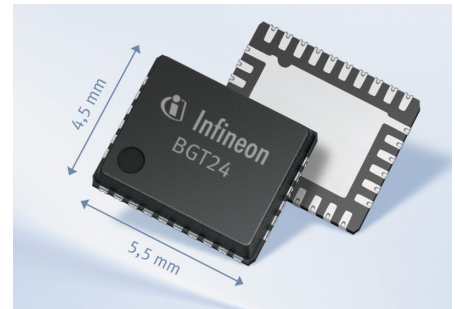


# BGT24AT2

## Silicon Germanium 24 GHz Transmitter MMIC

### Features

- 24 GHz signal source with 2 transmitter outputs and 1 local oscillator output
- External / internal phase inversion and RF pulsing capability
- Programmable gain amplifiers (PGA) with 6 bit resolution
- Fully integrated low phase noise VCO
- Frequency divider with 23.5 MHz output
- On chip RF level and temperature sensors
- Multiplexed output of analog sensor signals
- Single ended RF terminals
- Single supply voltage: 3.3 V typ.
- Low power consumption: 775 mW typ.
- 200 GHz bipolar SiGe:C technology b7hf200
- Fully ESD protected device
- VQFN-32-9 leadless plastic package including lead-tip-inspection (LTI) feature



### Description

The BGT24AT2 is a low phase noise 24 GHz ISM band multifunction signal source, manufactured in a monolithic Silicon Germanium semiconductor process technology.

It accommodates a 24 GHz fundamental voltage controlled oscillator and a frequency divider with a division ratio of 1024. The frequency divider output is differential.

The three individual RF outputs generate a typical output power of +10 dBm, adjustable via SPI-programmable 6 bit DAC's. Fast pulsing and phase inversion of the transmit signal is provided either using dedicated control inputs or the 64 bit SPI. Automatic configuration of the LO-output is possible using a dedicated logic.

RF output level sensors as well as a temperature sensor are implemented for monitoring purposes. The analog sensor signals along with an additional optional analog input are multiplexed to one common output.

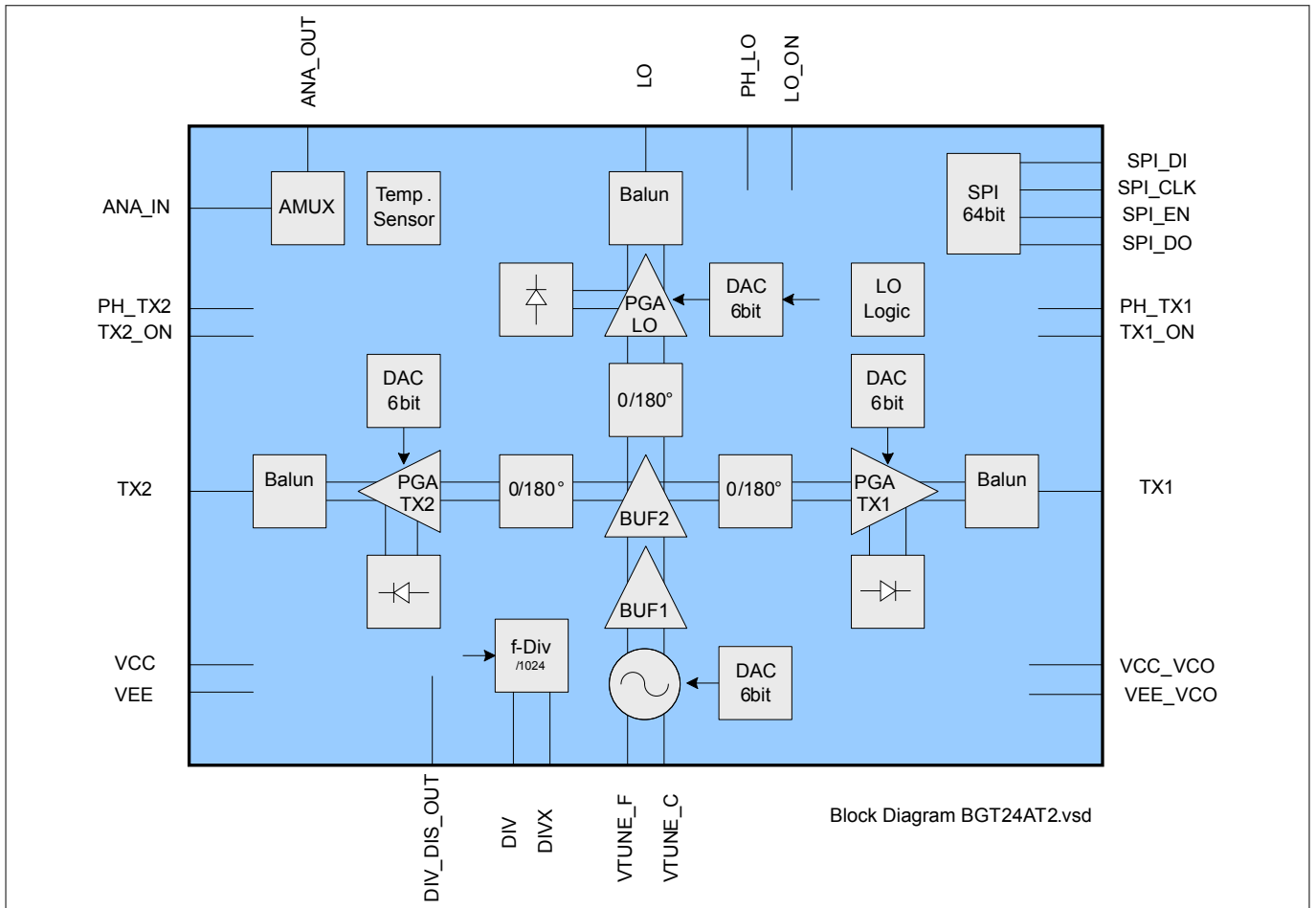
The MMIC is manufactured in a 200 GHz, 0.18µm SiGe:C technology and is packaged in a 32 pin leadless RoHS compliant VQFN package with LTI feature.

### Product Validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

Product Name	Package	Chip	Marking
BGT24AT2	VQFN32-9	T1824	BGT24AT2

**Revision History**



**Figure 1 BGT24AT2 Block Diagram**

**Revision History**

**Revision History: 2019-12-05, Revision 3.4**

**Previous Revision: 2019-10-31, Revision 3.3**

Page	Subjects (major changes since last revision)
7	VCO frequency range extended typ. and max. value
11	Output match ( $S_{22}$ ) max. value added

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**1 Electrical Characteristics**

**1 Electrical Characteristics**

**1.1 Absolute Maximum Ratings**

**Table 1 Absolute Maximum Ratings**

$T_A = -40\text{ °C}$  to  $125\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Supply voltage	$V_{CC}$	-0.3	–	$V_{CC} + 0.3$	V	■	–
Voltage applied to none-RF pins <sup>(1)</sup>	$V_{IO}$	-0.3	–	$V_{CC} + 0.3$	V	■	–
DC voltage at RF pins	$V_{DC_{RF}}$	–	–	0	V	■	MMIC provides short circuit to GND for TX1, TX2 and LO pins
DC voltage at pins VTUNE_F, VTUNE_C	$V_{TUNE}$	-0.3	–	$V_{CC} + 0.3$	V	■	–
DC voltage at pins DIV, DIVX	$V_{DIVIDER}$	2	–	$V_{CC} + 0.3$	V	■	–
Total power dissipation	$P_{DISS}$	–	–	1000	mW	■	–
Junction temperature	$T_J$	-40	–	170	°C	■	–
Ambient temperature range	$T_A$	-40	–	125	°C	■	$T_A$ = temperature at package soldering point
Storage temperature range	$T_{STG}$	-50	–	125	°C	■	–

(1) For SPI\_EN, SPI\_DI, SPI\_CLK the applied voltage may exceed given ratings as long as current into these pins is limited to  $I_{SPI} = 1\text{ mA}$

**Attention:** Stresses exceeding the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

**Attention:** Integrated protection functions are designed to prevent IC destruction under fault conditions as described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

**Note:** No permanent damage of the device is possible due to an undefined SPI state

**1 Electrical Characteristics**

**1.2 ESD Integrity**

**Table 2 ESD Integrity**

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
ESD robustness HBM <sup>(1)</sup>	V <sub>ESD-HBM</sub>	-1	-	1	kV	■	All pins
ESD robustness, CDM <sup>(2)</sup>	V <sub>ESD-CDM</sub>	-500	-	500	V	■	All pins
		-750	-	750		■	Package corner pins

(1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kOhm, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

(2) According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

Please note that this result is subject to:

- lot variations within the manufacturing process as specified by Infineon
- changes in the specific test setup

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

**1.3 Power Supply**

**Table 3 Electrical Characteristics**

T<sub>A</sub> = -40 °C ... 125 °C, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Supply voltage	V <sub>CC</sub>	3.135	3.3	3.465	V		-
Supply current nominal operation mode	I <sub>CC,ON</sub>	-	235	280	mA		nom. operation mode, SPI-state: 9F7F 2903 9F7C 10FF Hex
Supply current standby mode	I <sub>CC,STDBY</sub>	-	65	85	mA		all functional blocks disabled, SPI-state: 0000 0000 0000 Hex

**1 Electrical Characteristics**

**1.4 VCO**

**Table 4 Electrical Characteristics**

$V_{CC} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ , PGA output power =  $P_{max}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.3 GHz including matching structure and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN359)

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
VCO frequency range	$f_{VCO}$	24.00	24.15	24.3	GHz		_(1) (2)
VCO tuning voltage for VCO frequency range	$V_{TUNE\_F}$	0.1	-	0.9	V		-
Number of usable VCO coarse tune DAC states	$n$	2	-	-	-		VTUNE_F applied via series resistor $\geq 1\text{ k}\Omega$
VCO phase noise @ 1 kHz	$P_{N,P\ 1kHz}$	-	-30	-18	dBc/Hz	■	-
VCO phase noise @ 10 kHz	$P_{N,P\ 10kHz}$	-	-59	-50	dBc/Hz	■	-
VCO phase noise @ 100 kHz	$P_{N,P\ 100kHz}$	-	-82	-76.4	dBc/Hz		-
VCO phase noise @ 1 MHz	$P_{N,P\ 1MHz}$	-	-103	-97.4	dBc/Hz	■	-
VCO phase noise @ 10 MHz	$P_{N,P\ 10MHz}$	-	-123	-117.4	dBc/Hz	■	-
VCO amplitude noise @ 10 kHz	$P_{N,A\ 10kHz}$	-	-	-125	dBc/Hz	■	measured at +4 dBm output power
VCO amplitude noise @ 100 kHz	$P_{N,A\ 100kHz}$	-	-	-135	dBc/Hz	■	measured at +4 dBm output power
VCO amplitude noise @ 1 MHz	$P_{N,A\ 1MHz}$	-	-150	-145	dBc/Hz	■	measured at +4 dBm output power
VTUNE_F input resistance	$R_{VTUNE\_F}$	100	-	-	k $\Omega$	■	nonlinear, see leakage current specification
Leakage current at pin VTUNE_F	$I_{VTUNE\_F}$	-40	-	-	$\mu\text{A}$		at min. tuning voltage
VTUNE_F input capacitance	$C_{VTUNE\_F}$	-	-	10	pF	■	-
VTUNE_C input resistance	$R_{VTUNE\_C}$	1440	1800	2160	$\Omega$	■	-
VTUNE_C DAC current for PGA state 63	$I_{VTUNE\_C,DAC}$	1.2	-	-	mA	■	-
Static pulling $f_{VCO}$ change vs. load	$\Delta f_{sp}$	-1	-	+1	MHz	■	at all TX ports, 10 dB mismatch, all phases
Dynamic pulling phase and TX switch change	$\Delta f_{dp1}$	-1	-	+1	MHz	■	at all TX ports, 10 dB mismatch, all phases
Dynamic pulling TX1 to TX2 switch change	$\Delta f_{dp2}$	-1	-	+1	MHz	■	at all TX ports, 10 dB mismatch, all phases
VCO pushing	$\Delta f / \Delta V_{CC}$	-20 -60	-	+20 +60	MHz/V	■	$V_{CC} \geq 3.2\text{ V}, T_A \geq -20\text{ °C}$ (3) (3)



**1 Electrical Characteristics**

**Table 4 Electrical Characteristics (continued)**

$V_{CC} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ , PGA output power =  $P_{max}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.3 GHz including matching structure and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN359)

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Spurious level harmonics	$a_{harm}$	-	-	-32	dBc	■	at max. output power; H2 measured at SWM connector <sup>(3)</sup>
Spurious level non harmonics	$a_{nharm}$	-	-	-48	dBm	■	-
VCO tuning speed	$\Delta f / \Delta V_t$	70	-	-	MHz/ $\mu$ s	■	-
VCO tuning sensitivity	$\Delta f / \Delta f_{TUNE\_F}$	-	-	2800 2200	MHz/V	■	differential sensitivity lin. between $f_1$ 24.05 GHz and $f_2 = 24.14$ GHz
VCO frequency drift <sup>(4)</sup>	$f_{DRIFT}$	-	10	-	kHz	■	-

(1) Proper adjustment of  $V_{TUNE\_C}$  required to cover frequency band with specified  $V_{TUNE\_F}$

(2) Monotonic increasing frequency vs.  $V_{TUNE\_F}$

(3)

(4) Within 50ms and under following conditions:

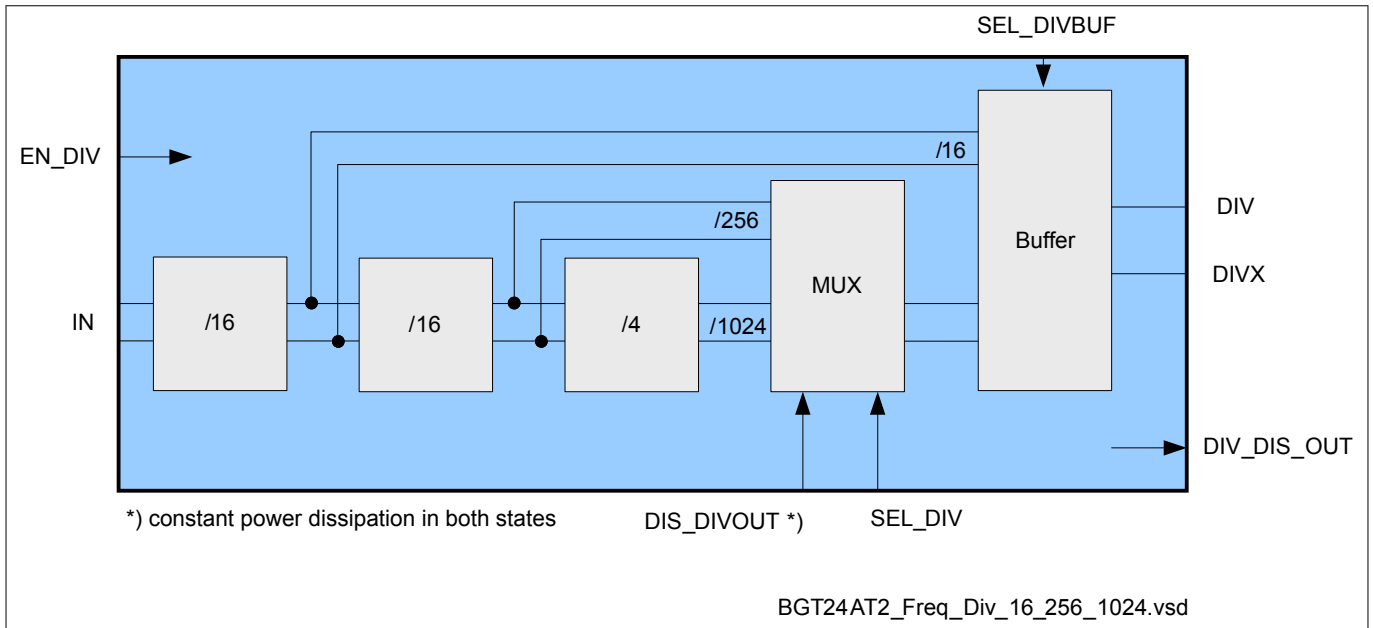
- Ambient temperature - stable
- Supply voltage - stable
- RF ports at least 50  $\mu$ s after ON/OFF or OFF/ON and phase transitions
- Divider in ON/OFF at least 50  $\mu$ s after OFF/ON transitions

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

**1.5 Frequency Divider**

The block diagram of the frequency divider is shown in [Figure 2](#), a compatible truth table is given in [Table 5](#)

**1 Electrical Characteristics**



**Figure 2** Block Diagram Frequency Divider

**Table 5** Frequency Divider Truth Table<sup>(1) (2)</sup>

EN_DIV	SEL_DIV	SEL_DIVBUF	DIS_DIVOUT	MODE
1	X	1	X	/16
1	1	0	0	/256
1	0	0	0	/1024
1	X	0	1	output disabled
0	X	X	X	shutdown

(1) deviating states not allowed, undefined divider output

(2) modes /16 and /256 for information only!

**Table 6** Electrical Characteristics

$V_{CC} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ , VCO frequency = 24.0 to 24.3 GHz, divider division ratio = 1024, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Dividing factor	$D_{DIV}$	–	256 1024	–	–	–	–
Divider output impedance	$Z_{OUT}$	240	300	360	$\Omega$	■	Into MMIC1 <sup>(1)</sup>
Output voltage	$V_{DIV,1024}$	900	1150	1400	mVpp		Into 300 $\Omega$ load <sup>(2)</sup>

## 1 Electrical Characteristics

**Table 6 Electrical Characteristics (continued)**

$V_{CC} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ , VCO frequency = 24.0 to 24.3 GHz, divider division ratio = 1024, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Common mode output voltage	$V_{DIV,CM,EN}$	2.35	2.75	3.15	V		Output enabled <sup>(2)</sup>
	$V_{DIVX,CM,EN}$	2.35	2.75	3.15			Output enabled <sup>(2)</sup>
	$V_{DIV,CM,DIS}$	–	$V_{CC}$	–			Output enabled <sup>(2)</sup>
	$V_{DIVX,CM,DIS}$	1.6	2.15	2.60			Output enabled <sup>(2)</sup>
	$V_{DIV,CM,OFF}$	–	$V_{CC}$	–		■	Shutdown <sup>(2)</sup>
	$V_{DIVX,CM,OFF}$	–	$V_{CC}$	–		■	Shutdown <sup>(2)</sup>
Duty cycle	$DC$	–	0.5	–	–	■	–

(1) Divider output stable for VSWR < 20:1

(2) Measured using T-pad-attenuator on reference PCB as provided by Infineon (see Application Note AN359)

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

## 1.6 TX and LO PGA

**Table 7 Electrical Characteristics**

$V_{CC} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ , PGA output power =  $P_{max}$ , positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.3 GHz include matching structures and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN358).

Reference board losses and 2.92 mm connector loss deembedded to outer trafo edge (reference plane).

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Output power $PGA_{min}$	$P_{min}$	–	–	-26	dBm		–
Output power $PGA_{max}$	$P_{max}$	7	10	13	dBm		–
PGA coarse resolution interval	$R_C$	–	–	8	dB/bit	■	$P_{out} \geq -26\text{ dBm}$
PGA mid resolution interval	$R_M$	–	–	3	dB/bit		$P_{out} \geq -13\text{ dBm}$
PGA fine resolution interval	$R_F$	–	–	0.6	dB/Bit		$P_{out} \geq +1\text{ dBm}$
Output power variation in temp. range	$\Delta P_{TXtemp}$	-1.25	–	0.75	dB	■	–

**1 Electrical Characteristics**

**Table 7 Electrical Characteristics (continued)**

$V_{CC} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ , PGA output power =  $P_{max}$ , positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.3 GHz include matching structures and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN358).

Reference board losses and 2.92 mm connector loss deembedded to outer trafo edge (reference plane).

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Output match	$S_{22}$	-	-	-8	dB	■	$V_{CC} = 3.3\text{ V}$ , $T_A = 25\text{ °C}^{(1)}$ PGA state $\geq 47$ PGA state $\geq 23$ PGA state $\geq 0$
Output impedance	$Z_{TX}$	-	50	-	$\Omega$	■	Single ended
TX on/off isolation	$I_{TXon/off}$	30	-	-	dB	■	$P_{out} \geq -1\text{ dBm}$
TX1/TX2 isolation	$I_{TX1/TX2}$	30	-	-	dB	■	$P_{out} \geq -1\text{ dBm}$
TX on/off switching time	$t_{ON/OFF}$	-	-	2	ns	■	-
Phase shifter phase imbalance	$\epsilon_p$	175	180	185	deg	■	-
Phase shifter amplitude imbalance	$\epsilon_A$	-0.5	0	0.5	dB		-
Phase shifter switching time	$t_{PHASE}$	-	-	100	ns	■	-

Following parameter for pins: PH\_TX1, PH\_LO, PH\_TX2, TX1\_ON, LO\_ON, TX2\_ON

High-level input voltage	$V_{I\_high}$	2.0	-	-	V	■	-
Low-level input voltage	$V_{I\_low}$	-	-	0.8	V	■	-
Input capacitance	$C_{in}$	-	-	2	pF	■	-
Pull Up resistor	$R_{PL}$	27.2	34	40.8	k $\Omega$	■	$T_A = 25\text{ °C}$
Leakage current into pins	$I_{Leakage}$	-100	-	75	$\mu\text{A}$		-

(1) SOLT calibration, reference plane at SWM connector

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

## 1 Electrical Characteristics

### 1.7 Temperature Sensor

**Table 8** Electrical Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $T_A = -40\text{ °C}$  to  $125\text{ °C}$ , application and MMIC external circuit acc. to Application Note AN359, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Temperature sensor operating range	$T_{TSENS}$	-40	-	125	°C	■	-
Output voltage	$V_{TSENSE25}$	1.4	1.5	1.6	V		at $T_{Si} = 25\text{ °C}$
Sensitivity	$S_{TSENS}$	4.3	4.7	5.1	mV/K	■	-
Setup time	$t_{TSENS}$	-	-	20	µs	■	$C_{Load} \leq 2.2\text{ nF}$ and $R_{Load} \geq 10\text{ k}\Omega$ at ANA_OUT
Power supply rejection ratio	$PSRR$	16	24	-	dB		measured at $T_{Si} = 25\text{ °C}$ and $V_{CC,MIN}/V_{CC,MAX}$

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

### 1.8 Output Level Detector

**Table 9** Electrical Characteristics

$V_{CC} = 3.3\text{ V}$  to  $3.465\text{ V}$ ,  $T_A = -40\text{ °C}$  to  $125\text{ °C}$ , application and MMIC external circuit acc. to Application Note AN359, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Output voltage	$V_{OUT}$	1.17	-	1.29	V	■	PGA state = 0, all channels RF off
Detector TX1 and TX2 absolute error	$E_{TX1, TX2}$	-2	-	+2	dB	■	at $P_{OUT} > -1\text{ dBm}$ , calculation based on equation in App. Note AN359
Detector LO absolute error	$E_{LO}$	-2	-	+2	dB	■	at $P_{OUT} > -1\text{ dBm}$ , calculation based on equation in App. Note AN359
Setup time	$t_{SENS}$	-	-	20	µs	■	$C_{LOAD} \leq 2.2\text{ nF}$ and $R_{LOAD} \geq 10\text{ k}\Omega$ at ANA_OUT

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

**1 Electrical Characteristics**

**1.9 Sensor Multiplexer**

**Table 10 Electrical Characteristics**

$V_{CC} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = -40\text{ °C to }125\text{ °C}$ , application and MMIC external circuit acc. to Application Note AN359, all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Test	Note or Test Condition
		Min.	Typ.	Max.			
Input voltage range	$V_{IN}$	1	–	2	V	■	–
Input current	$I_{IN}$	–	–	1	$\mu\text{A}$	■	–
Output impedance	$R_{OUT}$	–	20	40	$\Omega$	■	–
Offset voltage	$V_{OFFSET}$	-10	–	10	mV	■	At 10k $\Omega$ load resistance

**Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

For more information on the sensor multiplexer refer to [Chapter 4](#) and to application note AN359.

**2 Pin Description**

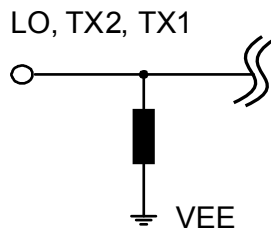
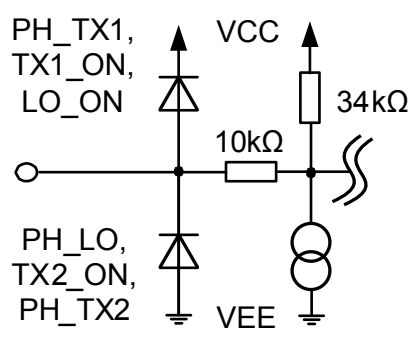
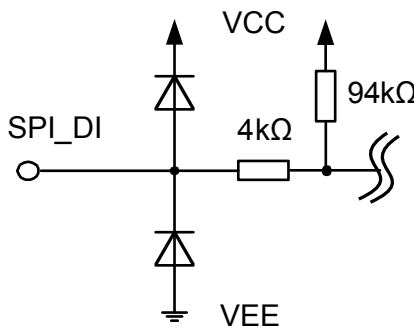
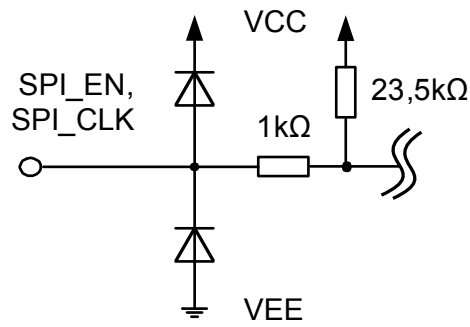
**2 Pin Description**

**Table 11 Pin Definition and Function**

Pin No.	Name	Function
1	PH_TX1	TX1 phase
2	TX1_ON	TX1 enable
3	LO_ON	LO enable
4	VEE	Ground
5	LO	LO RF output signal
6	VEE	Ground
7	VEE	Ground
8	PH_LO	LO phase
9	TX2_ON	TX2 enable
10	PH_TX2	TX2 phase
11	VEE	Ground
12	TX2	TX2 RF output signal
13	VEE	Ground
14	VCC	Supply voltage
15	DIV_DIS_OUT	Divider disable output
16	SPI_DO	SPI data output
17	DIVX	Divider output negative port
18	DIV	Divider output positive port
19	ANA_IN	Analog signal input
20	VCC_VCO	Supply voltage VCO
21	VEE	Ground
22	VTUNE_F	VCO tuning voltage (fine)
23	VTUNE_C	VCO tuning voltage (coarse)
24	VEE_VCO	Ground VCO
25	VCC	Supply voltage
26	SPI_EN	SPI enable
27	SPI_CLK	SPI clock
28	SPI_DI	SPI data input
29	ANA_OUT	Analog output signal
30	VEE	Ground
31	TX1	TX1 RF output signal
32	VEE	Ground

**2 Pin Description**

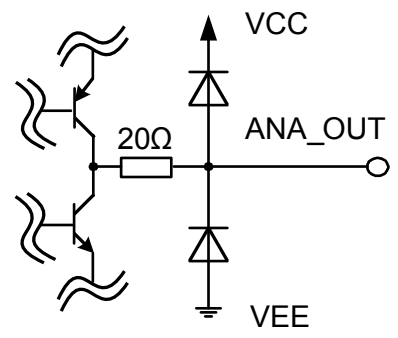
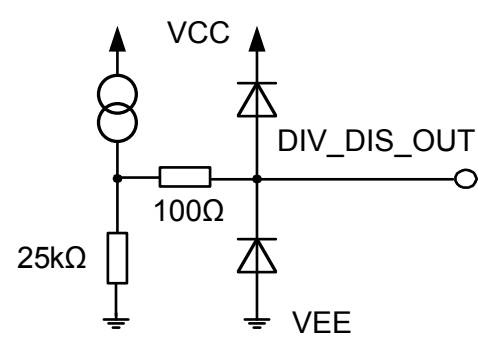
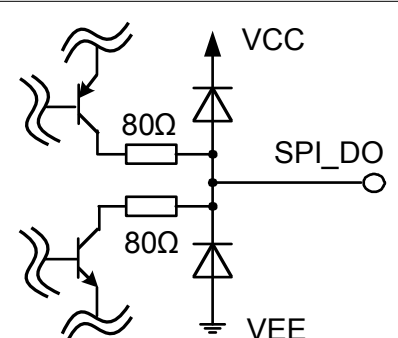
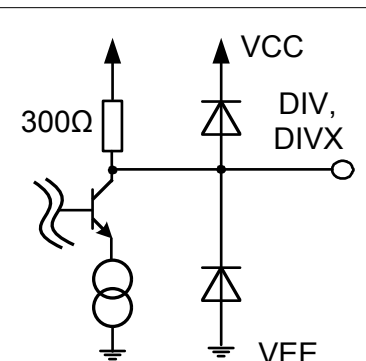
**Table 12 I/O internal circuits**

Pin No.	Name	I/O internal circuits
5, 12, 31	LO, TX2, TX1	
1, 2, 3, 8, 9, 10	PH_TX1, TX1_ON, LO_ON, PH_LO, TX2_ON, PH_TX2	
28	SPI_DI	
26, 27	SPI_EN, SPI_CLK	



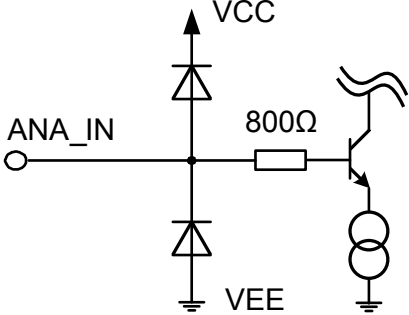
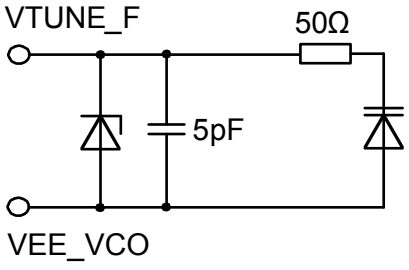
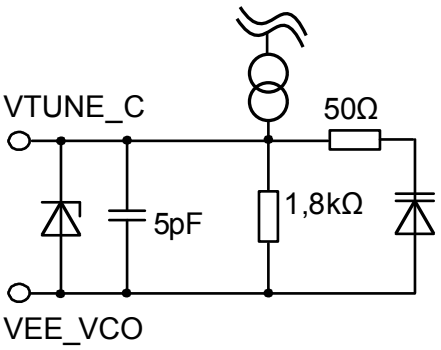
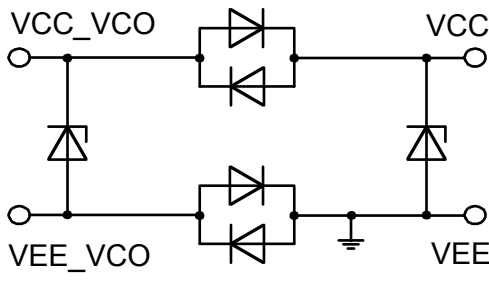
**2 Pin Description**

**Table 12 I/O internal circuits (continued)**

Pin No.	Name	I/O internal circuits
29	ANA_OUT	
15	DIV_DIS_OUT	
16	SPI_DO	
17, 18	DIVX, DIV	

**2 Pin Description**

**Table 12 I/O internal circuits (continued)**

Pin No.	Name	I/O internal circuits
19	ANA_IN	
22, 24	VTUNE_F, VEE_VCO	
23, 24	VTUNE_C, VEE_VCO	
4, 6, 7, 11, 13, 14, 20, 21, 24, 25, 30, 32	VEE, VCC, VCC_VCO, VEE_VCO,	

**3 SPI**

**3 SPI**

Communication to the transceiver is done via a Serial-Peripheral-Interface (SPI). The 32 bit SPI has a hardwired Power-On reset, which sets the output bits to a defined state after turning on the supply voltage. Data transmission is started by a negative edge on SPI\_EN. Data at SPI\_DI is then read at the falling edge of SPI\_CLK. The most significant bit (MSB) is read first.

**Table 13 SPI Data Bit Description**

Data Bit	Name	Description (Logic High)	Power ON Reset State
0 (LSB)	TX1_A5	MSB of TX1 PGA DAC output power control	0
1	TX1_A4	TX1 PGA DAC output power control	0
2	TX1_A3	TX1 PGA DAC output power control	0
3	TX1_A2	TX1 PGA DAC output power control	0
4	TX1_A1	TX1 PGA DAC output power control	0
5	TX1_A0	LSB of TX1 PGA DAC output power control	0
6	TX1_EN_DAC	TX1 PGA DAC enable	0
7	LO_EN_DAC	LO PGA DAC enable	0
8	n.c.		0
9	n.c.		0
10	n.c.		0
11	n.c.		0
12	EN_BUF1	buffer amplifier BUF1 enable	0
13	n.c.		0
14	n.c.		0
15	n.c.		0
16	VCO_A5	MSB of coarse tune DAC	0
17	VCO_A4	VCO coarse tune DAC	0
18	VCO_A3	VCO coarse tune DAC	0
19	VCO_A2	VCO coarse tune DAC	0
20	VCO_A1	VCO coarse tune DAC	0
21	VCO_A0	LSB of VCO coarse tune DAC	0
22	EN_DAC_VCO	VCO coarse tune DAC enable	0
23	PH1_SPI_ON	Phase control TX1 via SPI	0
24	TX1_SEL1	TX1 control bit (“0”=via ext. pulse pin, “1”=via SPI)	0
25	TX1_SPI_ON	TX1 enable via SPI	0
26	LO_SPI_ON	LO enable via SPI	0
27	AMUX2_SEL0	AMUX2 control bit	0

**3 SPI**

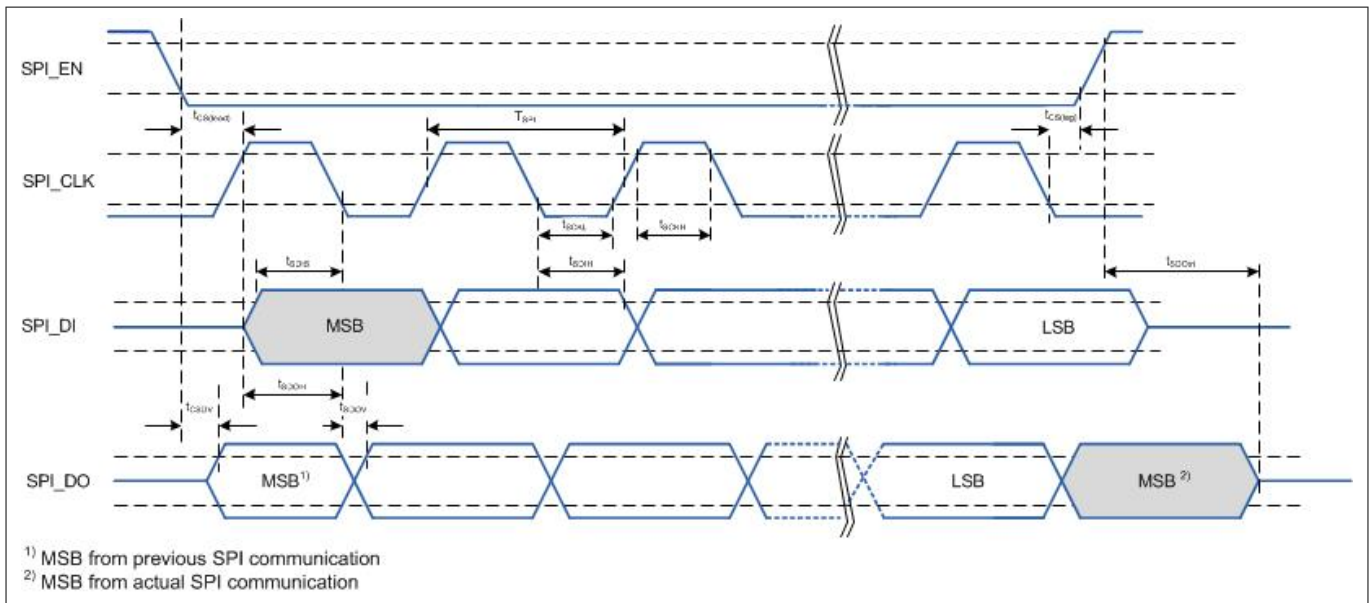
**Table 13 SPI Data Bit Description (continued)**

<b>Data Bit</b>	<b>Name</b>	<b>Description (Logic High)</b>	<b>Power ON Reset State</b>
28	AMUX2_SEL1	AMUX2 control bit	0
29	AMUX2_SEL2	AMUX2 control bit	0
30	LO_SEL1	LO logic control bit	0
31	EN_BUF2	Buffer amplifier BUF2 enable	0
32	EN_DIV	Frequency divider enable	0
33	EN_VCO	VCO enable	0
34	AMUX1_SEL0	AMUX1 control bit	0
35	AMUX1_SEL1	AMUX1 control bit	0
36	n.c.		0
37	PHLO_SPI_ON	Phase control LO via SPI	0
38	PH2_SPI_ON	Phase control TX2 via SPI	0
39	PH_SEL1	Phase control bit (“0”=via ext. pulse pin, “1”=via SPI)	0
40	TX2_SEL1	TX2 control bit (“0”=via ext. pulse pin, “1”=via SPI)	0
41	TX2_SPI_ON	TX2 enable via SPI	0
42	AMUX3_SEL1	AMUX3 control bit	0
43	AMUX3_SEL0	AMUX3 control bit	0
44	n.c		0
45	LO_SEL0	LO control bit	0
46	n.c		0
47	n.c		0
48	TX2_A5	MSB of TX2 PGA DAC output power control	0
49	TX2_A4	TX2 PGA DAC output power control	0
50	TX2_A3	TX2 PGA DAC output power control	0
51	TX2_A2	TX2 PGA DAC output power control	0
52	TX2_A1	TX2 PGA DAC output power control	0
53	TX2_A0	LSB of TX2 PGA DAC output power control	0
54	TX2_EN_DAC	TX2 PGA DAC enable	0
55	LO_A5	MSB of LO PGA DAC output power control	0
56	LO_A4	LO PGA DAC output power control	0
57	LO_A3	LO PGA DAC output power control	0
58	LO_A2	LO PGA DAC output power control	0
59	LO_A1	LO PGA DAC output power control	0

**3 SPI**

**Table 13 SPI Data Bit Description (continued)**

Data Bit	Name	Description (Logic High)	Power ON Reset State
60	LO_A0	LSB of LO PGA DAC output power control	0
61	SEL_DIVBUF	Frequency divider control bit	0
62	SEL_DIV	Frequency divider control bit	0
63 (MSB)	DIS_DIVOUT	Frequency divider output disable	0



**Figure 3 Timing Diagram of the SPI**

**Table 14 SPI Interface**

Parameter	Symbol	Values			Unit	Test
		Min.	Typ.	Max.		
SPI_CLK period	$t_{SPI}$	50	–	–	ns	
SPI_CLK low time	$t_{SCKL}$	$0.45 t_{SPI}$	$0.5 t_{SPI}$	$0.55 t_{SPI}$	ns	■
SPI_CLK high time	$t_{SCKH}$	$0.45 t_{SPI}$	$0.5 t_{SPI}$	$0.55 t_{SPI}$	ns	■
Chip select lead time	$t_{CS(lead)}$	20	–	–	ns	■
Time between falling edge of SPI_CLK and SPI_DO valid	$t_{SDOV}$	–	–	10	ns	■
Setup time of SPI_DI before falling edge of SPI_CLK	$t_{SDIS} = t_{SI(su)}$	10	–	–	ns	■
Hold time of SPI_DI after falling edge of SPI_CLK	$t_{SI(h)}$	10	–	–	ns	■
Hold time of SPI_DO after rising edge of SPI_CLK	$t_{SDOH}$	$t_{SCKH} - 10ns$	–	–	ns	■
Hold time of SPI_EN after last falling edge of SPI_CLK	$t_{CS(lag)}$	30	–	–	ns	■

**4 Sensor Multiplexer**

**Table 14**                    **SPI Interface (continued)**

Parameter	Symbol	Values			Unit	Test
		Min.	Typ.	Max.		
Delay between rising edge of SPI_EN and SPI_DO tristate (leakage current < 12μA)	$t_{SDOtri}$	–	–	100	ns	■
Delay between falling edge of SPI_EN and MSB at SPI_DO tristate valid	$t_{CSDV}$	–	–	125	ns	■
Minimum time between two SPI commands	$t_{min2SPI}$	5	–	–	μs	■

**Table 15**                    **Specification for SPI pins**

Parameter	Symbol	Values			Unit	Test
		Min.	Typ.	Max.		
High-level input voltage	$V_{I\_high}$	2.0	–	–	V	■
Low-level input voltage	$V_{I\_low}$	–	–	0.8	V	■
Input voltage hysteresis	$V_{hys}$	50	–	–	mV	■
Input current	$I_{IN}$	-190	–	150	μA	
Input capacitance (EN, CLK, DI)	$CS_{IN}$	–	–	2	pF	■
SPI_DO output high voltage (VCC=3.3V, $I_{SDO}$ =1mA)	$V_{O\_high}$	2.4	–	–	V	
SPI_DO output low voltage (VCC=3.3V, $I_{SDO}$ =1mA)	$V_{O\_low}$	–	–	0.8	V	
SPI_DO load capacitance	$CS_{L\_DO}$	–	–	30	pF	■
SPI_DO load resistance	$R_{SL\_DO}$	10	–	–	kΩ	■
Pull Up resistor (SPI_DI) $T_A = 25\text{ °C}$	RPL_SPI_DI	78	98	118	kΩ	■
Pull Up resistor (SPI_CLK, SPI_EN) $T_A = 25\text{ °C}$	RPL_SPI_CLK, RPL_SPI_EN	19.6	24.5	29.4	kΩ	■
Leakage current @ SPI_DO in high Z state (test voltage 2.4 V)	$I_{L\_DO}$	–	–	12	μA	

**Attention:** **Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.**

**4 Sensor Multiplexer**

Output signals of the temperature and output level sensors at TX1, TX2 and LO output are provided multiplexed at the output pin ANA\_OUT using an analog multiplexer (AMUX) circuit.

## 5 LO Logic

Additionally, a MMIC internal reference voltage (VBG1) can be read out and an analog input signal within 1 V and 2 V can be directed from ANA\_IN to ANA\_OUT. Tristate capability is implemented in order to combine several analog outputs in the application. In this case it has to be ensured that only one multiplexer output is activated at any time.

For more information on the sensor multiplexer refer to application note AN359.

**Table 16 Truth Table AMUX<sup>(1)</sup>**

Output at ANA_OUT	AMUX1_SEL1	AMUX1_SELO	AMUX2_SEL2	AMUX2_SEL1	AMUX2_SELO
Tristate	X	X	0	0	0
ANA_IN	X	X	0	0	1
VTEMP	X	X	0	1	1
PSENSE_TX2	0	0	1	0	0
PSENSE_TX1	0	1	1	0	0
PSENSE_LO	1	X	1	0	0
VBG1 (Bandgap output voltage)	X	X	1	0	1

(1) deviating states not allowed, undefined AMUX output

## 5 LO Logic

The BGT24AT2 accommodates a logic circuit which can be used to either activate the LO-output manually or automatically depending on the TX1/TX2 configuration.

Three operation modes are selectable:

1. manual activation / deactivation of the LO output via external pulse pin LO\_ON
2. manual activation / deactivation of the LO output via SPI bit LO\_SPI\_ON
3. automatic activation / deactivation depending on the TX1 / TX2 configuration.

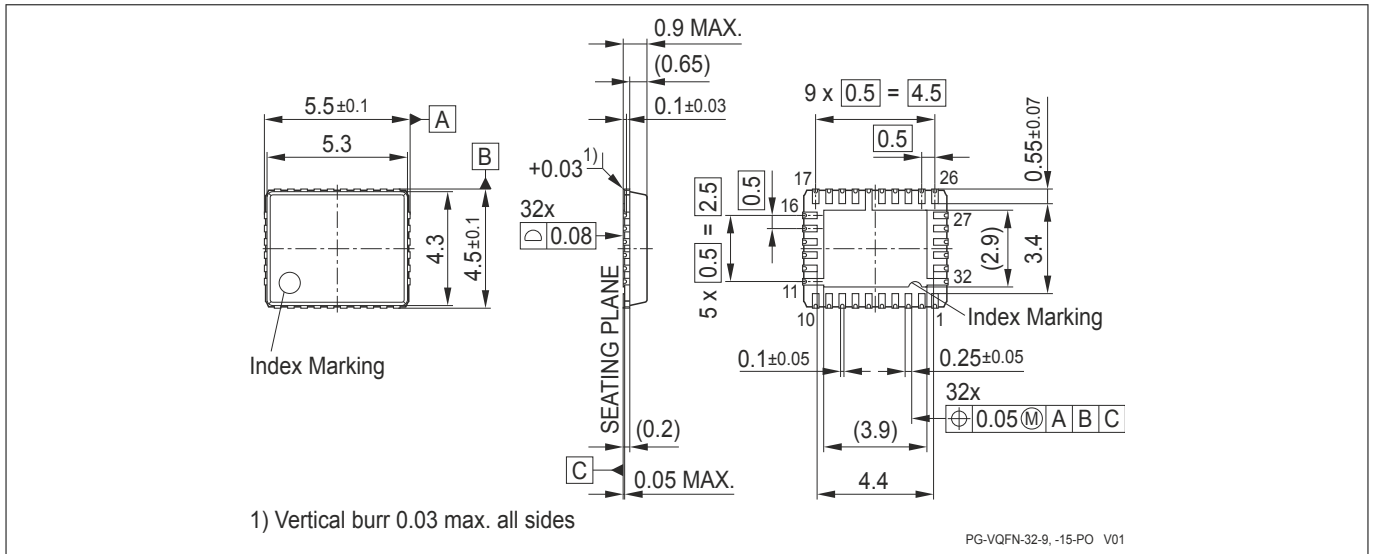
The configuration of the LO logic operation mode is shown in [Table 17](#).

**Table 17 Truth Table LO Logic**

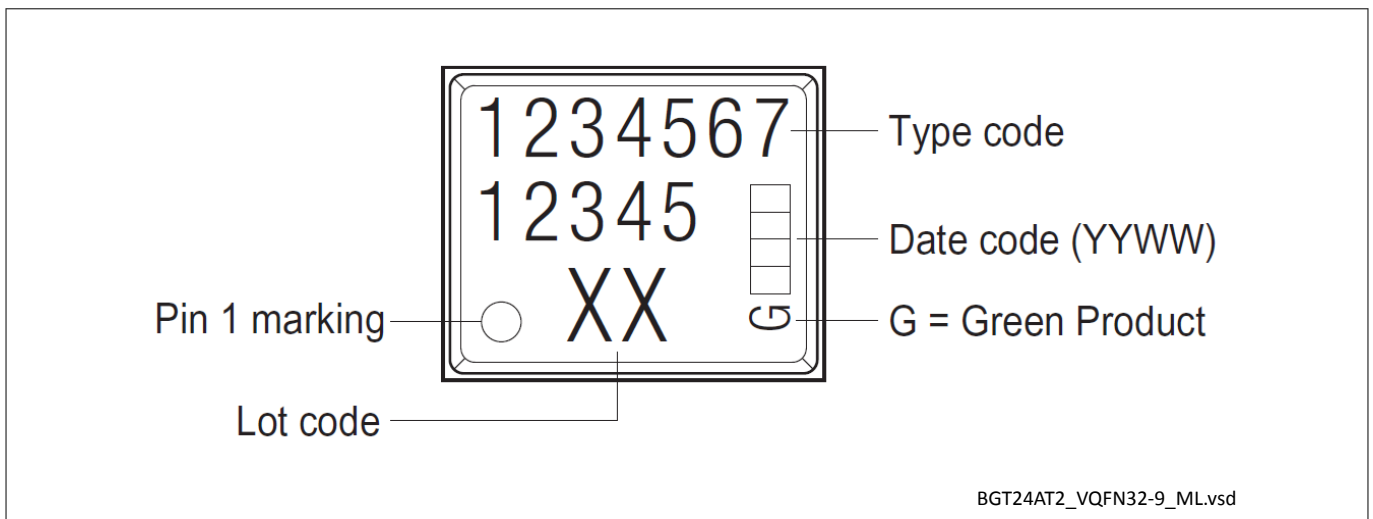
LO_SEL1	LO_SELO	Function
0	0	LO activation via external pulse pin LO_ON
0	1	LO activation via SPI bit LO_SPI_ON
1	X	Automatic LO activation via external pulse pins TX1_ON or TX2_ON

**6 Package Dimensions**

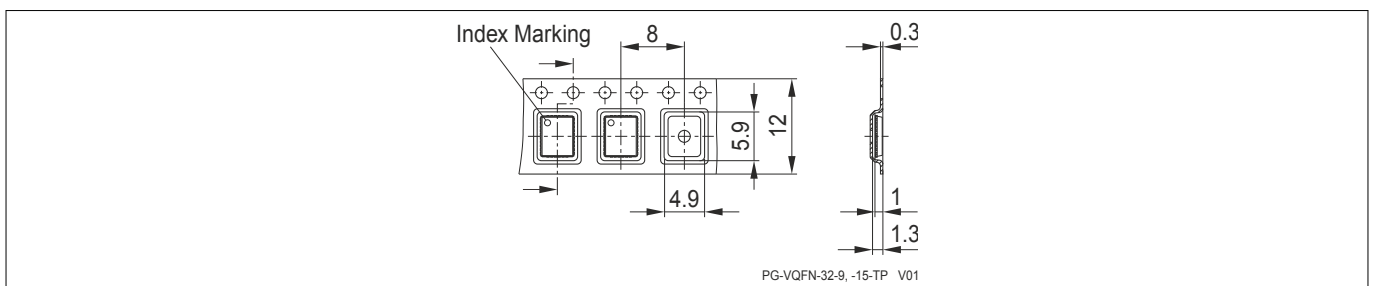
**6 Package Dimensions**



**Figure 4 Package Outline (Top, Side and Bottom View) of VQFN32-9**



**Figure 5 Marking Layout VQFN32-9 (example)**



**Figure 6 Tape of VQFN32-9, Ø Reel: 330 mm, Pieces / Reel: 3000, Reels / Box: 1**



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