

# LITIX™ Basic

TLD2326EL

3 Channel High-Side Current Source

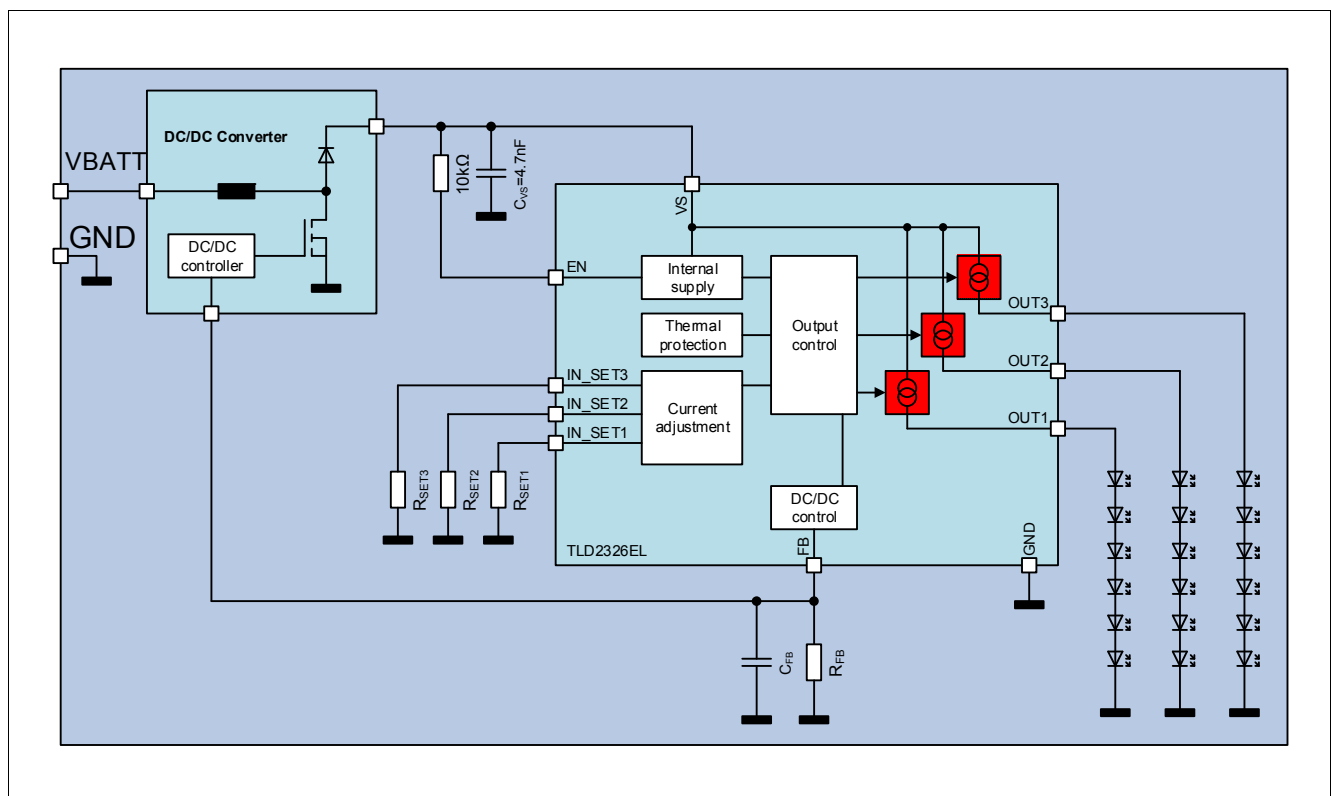
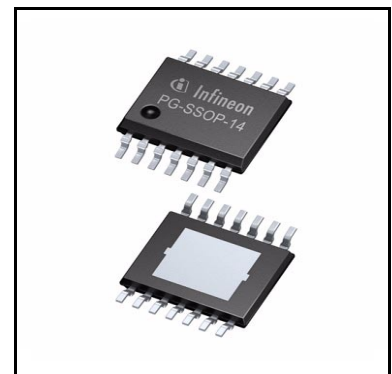


<b>Package</b>	PG-SSOP-14
<b>Marking</b>	TLD2326

## 1 Overview

### Applications

- Exterior LED lighting applications such as tail/brake light, turn indicator, position light, side marker,...
- Interior LED lighting applications such as ambient lighting (e.g. RGB), interior illumination and dash board lighting.



Application Diagram with TLD2326EL

## Overview

### Basic Features

- 3 Channel device with integrated output stages (current sources), optimized to drive LEDs with output current up to 120 mA per channel
- Low current consumption in sleep mode
- PWM-operation supported via VS- and EN-pin
- Output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during over temperature conditions
- Dynamic overhead control
- Reverse polarity protection and overload protection
- Undervoltage detection
- Open load and short circuit to GND diagnosis
- Wide temperature range:  $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$
- PG-SSOP-14 package with exposed heatslug

### Description

The LITIX™ Basic TLD2326EL is a three channel high side driver IC with integrated output stages. It is designed to control LEDs with a current up to 120 mA. In typical automotive applications the device is capable to drive i.e. 3 red LEDs per chain (total 9 LEDs) with a current up to 60 mA, which is limited by thermal cooling aspects. The output current is controlled practically independent of load and supply voltage changes.

**Table 1 Product Summary**

Parameter	Symbol	Value
Operating voltage range	$V_{S(\text{nom})}$	5.5 V ... 40 V
Maximum voltage	$V_{S(\text{max})}$ $V_{\text{OUTx}(\text{max})}$	40 V
Nominal output (load) current	$I_{\text{OUTx}(\text{nom})}$	60 mA when using a supply voltage range of 8 V - 18 V (e.g. Automotive car battery). Currents up to $I_{\text{OUT}(\text{max})}$ possible in applications with low thermal resistance $R_{\text{thJA}}$
Maximum output (load) current	$I_{\text{OUTx}(\text{max})}$	120 mA; depending on thermal resistance $R_{\text{thJA}}$
Output current accuracy at $R_{\text{SETx}} = 12 \text{ k}\Omega$	$k_{\text{LT}}$	$750 \pm 7\%$
Current consumption in sleep mode	$I_{S(\text{sleep,typ})}$	0.1 $\mu\text{A}$

### Protective Functions

- ESD protection
- Under voltage lock out
- Over Load protection
- Over Temperature protection
- Reverse Polarity protection

### Diagnostic Functions

- OL detection
- SC to Vs (indicated by OL diagnosis)
- SC to GND detection

Block Diagram

## 2 Block Diagram

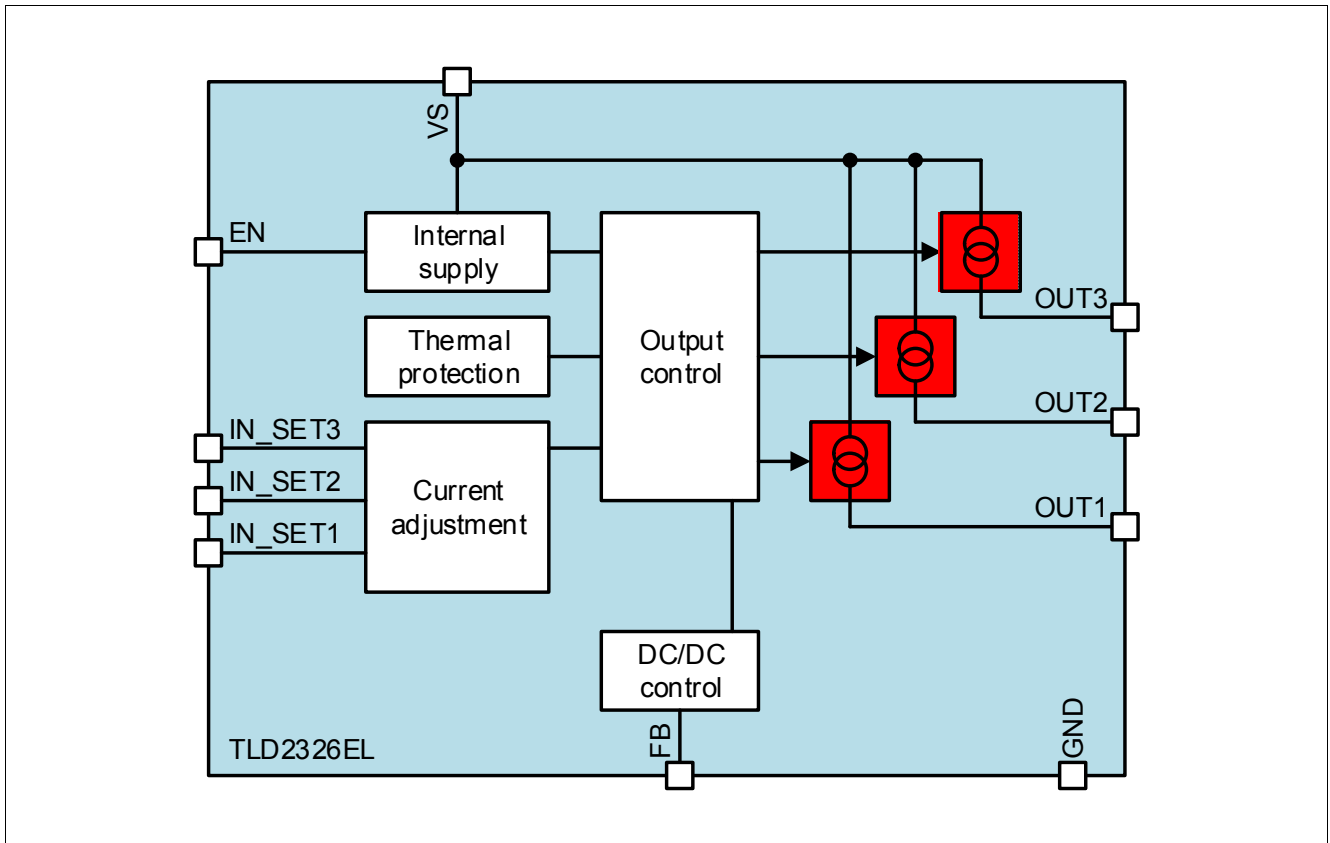


Figure 1 Basic Block Diagram

Pin Configuration

### 3 Pin Configuration

#### 3.1 Pin Assignment

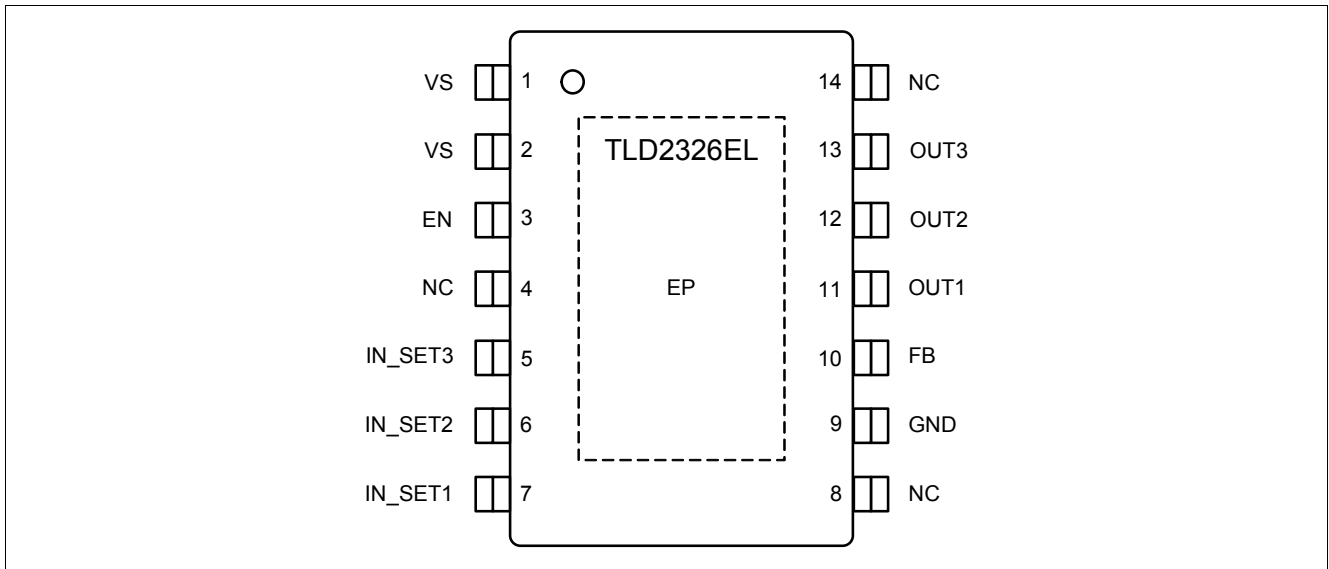


Figure 2 Pin Configuration

Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Input/ Output	Function
1, 2	VS	–	<b>Supply Voltage;</b> battery supply, connect a decoupling capacitor (100 nF - 1 µF) to GND
3	EN	I	<b>Enable pin</b>
4	NC	–	<b>Pin not connected</b>
5	IN_SET3	I/O	<b>Input / SET pin 3;</b> Connect a low power resistor to adjust the output current
6	IN_SET2	I/O	<b>Input / SET pin 2;</b> Connect a low power resistor to adjust the output current
7	IN_SET1	I/O	<b>Input / SET pin 1;</b> Connect a low power resistor to adjust the output current
8	NC	–	<b>Pin not connected</b>
9	GND	–	<sup>1)</sup> <b>Ground</b>
10	FB	O	<b>Feedback Output</b>
11	OUT1	O	<b>Output 1</b>
12	OUT2	O	<b>Output 2</b>
13	OUT3	O	<b>Output 3</b>
14	NC	–	<b>Pin not connected</b>
Exposed Pad	GND	–	<sup>1)</sup> <b>Exposed Pad;</b> connect to GND in application

1) Connect all GND-pins together.

General Product Characteristics

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>Voltages</b>						
4.1.1	Supply voltage	$V_S$	-16	40	V	-
4.1.2	Input voltage EN	$V_{EN}$	-16	40	V	-
4.1.3	Input voltage EN related to $V_S$	$V_{EN(VS)}$	$V_S - 40$	$V_S + 16$	V	-
4.1.4	Input voltage EN related to $V_{OUTx}$	$V_{EN} - V_{OUTx}$	-16	40	V	-
4.1.5	Output voltage	$V_{OUTx}$	-1	40	V	-
4.1.6	Power stage voltage	$V_{PS} = V_S - V_{OUTx}$	-16	40	V	-
4.1.7	IN_SETx voltage	$V_{IN\_SETx}$	-0.3	6	V	-
4.1.8	Feedback voltage	$V_{FB}$	-0.3	40	V	-
<b>Currents</b>						
4.1.9	IN_SETx current	$I_{IN\_SETx}$	-	2 3	mA	- Diagnosis output
4.1.10	Feedback current	$I_{FB}$	-	0.5	mA	-
4.1.11	Output current	$I_{OUTx}$	-	130	mA	-
<b>Temperatures</b>						
4.1.12	Junction temperature	$T_j$	-40	150	$^{\circ}\text{C}$	-
4.1.13	Storage temperature	$T_{stg}$	-55	150	$^{\circ}\text{C}$	-
<b>ESD Susceptibility</b>						
4.1.14	ESD resistivity to GND	$V_{ESD}$	-2	2	kV	Human Body Model (100 pF via 1.5 k $\Omega$ ) <sup>2)</sup>
4.1.15	ESD resistivity all pins to GND	$V_{ESD}$	-500	500	V	CDM <sup>3)</sup>
4.1.16	ESD resistivity corner pins to GND	$V_{ESD}$	-750	750	V	CDM <sup>3)</sup>

1) Not subject to production test, specified by design

2) ESD susceptibility, Human Body Model "HBM" according to ANSI/ESDA/JEDEC JS-001-2011

3) ESD susceptibility, Charged Device Model "CDM" according to JESD22-C101E

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

General Product Characteristics

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.17	Supply voltage range for normal operation	$V_{S(nom)}$	5.5	40	V	–
4.2.18	Power on reset threshold	$V_{S(POR)}$	–	5	V	$V_{EN} = V_S$ $R_{SETx} = 12\text{ k}\Omega$ $I_{OUTx} = 80\% I_{OUTx(nom)}$ $V_{OUTx} = 2.5\text{ V}$
4.2.19	Junction temperature	$T_j$	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	$R_{thJC}$	–	8	10	K/W	1) 2)
4.3.2	Junction to Ambient 1s0p board	$R_{thJA1}$	–	61	–	K/W	1) 3) $T_a = 85\text{ °C}$ $T_a = 135\text{ °C}$
			–	56	–		
4.3.3	Junction to Ambient 2s2p board	$R_{thJA2}$	–	45	–	K/W	1) 4) $T_a = 85\text{ °C}$ $T_a = 135\text{ °C}$
			–	43	–		

- 1) Not subject to production test, specified by design. Based on simulation results.
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature).  $T_a = 85\text{ °C}$ , Total power dissipation 1.5 W.
- 3) The  $R_{thJA}$  values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a  $76.2 \times 114.3 \times 1.5\text{ mm}^3$  board with  $70\text{ }\mu\text{m}$  Cu,  $300\text{ mm}^2$  cooling area. Total power dissipation 1.5 W distributed statically and homogeneously over all power stages.
- 4) The  $R_{thJA}$  values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a  $76.2 \times 114.3 \times 1.5\text{ mm}^3$  board with 2 inner copper layers (outside  $2 \times 70\text{ }\mu\text{m}$  Cu, inner  $2 \times 35\text{ }\mu\text{m}$  Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogeneously over all power stages.

EN Pin

## 5 EN Pin

The EN pin is a dual function pin:



**Figure 3** Block Diagram EN pin

Note: The current consumption at the EN-pin  $I_{EN}$  needs to be added to the total device current consumption. The total current consumption is the sum of the currents at the VS-pin  $I_S$  and the EN-pin  $I_{EN}$ .

### 5.1 EN Function

If the voltage at the pin EN is below a threshold of  $V_{EN(off)}$  the LITIX™ Basic IC will enter Sleep mode. In this state all internal functions are switched off, the current consumption is reduced to  $I_{S(sleep)}$ . A voltage above  $V_{EN(on)}$  at this pin enables the device after the Power on reset time  $t_{POR}$ .



**Figure 4** Power on reset



EN Pin

5.2 Internal Supply Pin

The EN pin can be used to supply the internal logic. There are two typical application conditions, where this feature can be used:

- 1) In “DC/DC control Buck” configurations, where the voltage  $V_S$  can be below 5.5V.
- 2) In configurations, where a PWM signal is applied at the Vbatt pin of a light module. The buffer capacitor  $C_{BUF}$  is used to supply the LITIX™ Basic IC during Vbatt low ( $V_S$  low) periods. This feature can be used to minimize the turn-on time to the values specified in **Pos. 9.2.11**. Otherwise, the power-on reset delay time  $t_{POR}$  (**Pos. 5.4.6**) has to be considered.

The capacitor can be calculated using the following formula:

$$C_{BUF} = t_{LOW(max)} \cdot \frac{I_{EN(LS)}}{V_S - V_{D1} - V_{S(POR)}} \tag{1}$$

See also a typical application drawing in **Chapter 10**.

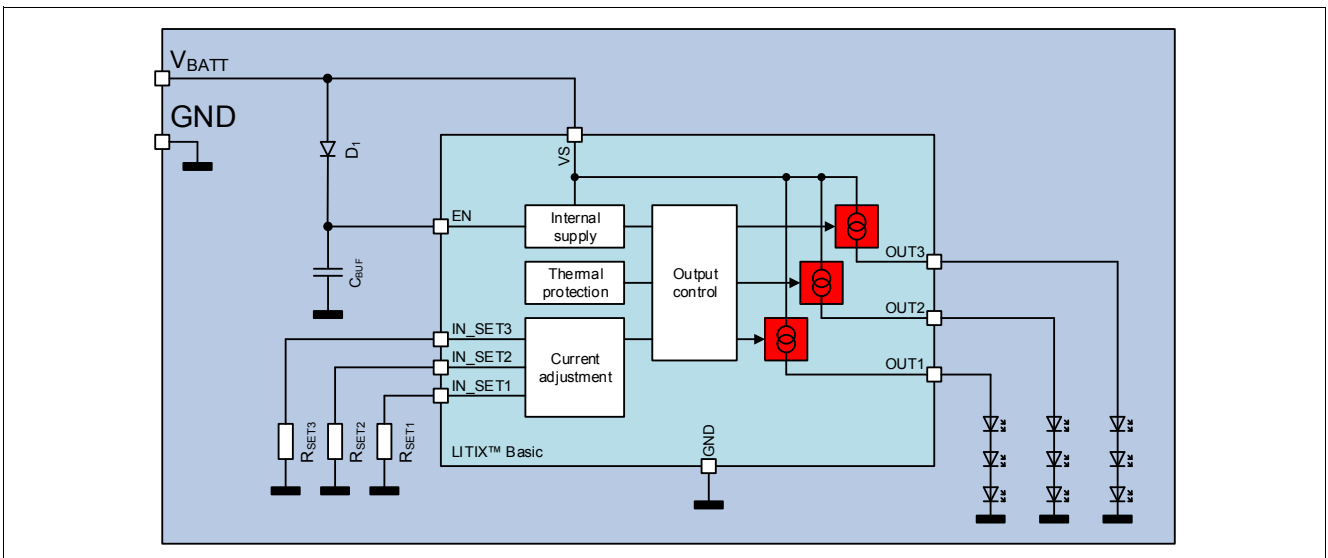


Figure 5 External circuit when applying a fast PWM signal on  $V_{BATT}$

EN Pin



**Figure 6** Typical waveforms when applying a fast PWM signal on  $V_{BATT}$

The parameter  $t_{ON(VS)}$  is defined at [Pos. 9.2.11](#). The parameter  $t_{OFF(VS)}$  depends on the load and supply voltage  $V_{BATT}$  characteristics.

### 5.3 EN Unused

In case of an unused EN pin, there are two different ways to connect it:

#### 5.3.1 EN - Pull Up to VS

The EN pin can be connected with a pull up resistor (e.g. 10 k $\Omega$ ) to  $V_s$  potential. In this configuration the LITIX™ Basic IC is always enabled.

#### 5.3.2 EN - Direct Connection to VS

The EN pin can be connected directly to the VS pin (IC always enabled). This configuration has the advantage (compared to the configuration described in [Chapter 5.3.1](#)) that no additional external component is required.

## 5.4 Electrical Characteristics Internal Supply / EN Pin

### Electrical Characteristics Internal Supply / EN pin

Unless otherwise specified:  $V_S = 5.5\text{ V to }40\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $R_{SETx} = 12\text{ k}\Omega$  all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Current consumption, sleep mode	$I_{S(\text{sleep})}$	-	0.1	2	$\mu\text{A}$	<sup>1)</sup> $V_{EN} = 0.5\text{ V}$ $T_j < 85^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUTx} = 3.6\text{ V}$
5.4.2	Current consumption, active mode	$I_{S(\text{on})}$	-	-	1.7	$\text{mA}$	<sup>2)</sup> $I_{IN\_SET} = 0\ \mu\text{A}$ $T_j < 105^\circ\text{C}$ $V_S = 18\text{ V}$ $V_{OUTx} = 3.6\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{EN} = 18\text{ V}$ <sup>1)</sup> $R_{EN} = 10\text{ k}\Omega$ between VS and EN-pin
5.4.3	Current consumption, device disabled via IN_SETx	$I_{S(\text{dis,IN\_SET})}$	-	-	1.65	$\text{mA}$	<sup>2)</sup> $V_S = 18\text{ V}$ $T_j < 105^\circ\text{C}$ $V_{IN\_SETx} = 5\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{EN} = 18\text{ V}$ <sup>1)</sup> $R_{EN} = 10\text{ k}\Omega$ between VS and EN-pin
5.4.4	Current consumption, active mode in single fault detection condition	$I_{S(\text{fault})}$	-	-	6.0	$\text{mA}$	<sup>2)</sup> $V_S = 18\text{ V}$ $T_j < 105^\circ\text{C}$ $R_{SET1} = 12\text{ k}\Omega$ $R_{SET2,3} = \text{unconnected}$ $V_{OUTx} = 18\text{ V or }0\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{EN} = 18\text{ V}$ <sup>1)</sup> $R_{EN} = 10\text{ k}\Omega$ between VS and EN-pin
5.4.5	Current consumption, active mode in double fault detection condition and one output disabled via IN_SETx	$I_{S(\text{dfault})}$	-	-	9.0	$\text{mA}$	<sup>2)</sup> $V_S = 18\text{ V}$ $T_j < 105^\circ\text{C}$ $R_{SET1,2} = 12\text{ k}\Omega$ $R_{SET3} = \text{unconnected}$ $V_{OUTx} = 18\text{ V or }0\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{EN} = 18\text{ V}$ <sup>1)</sup> $R_{EN} = 10\text{ k}\Omega$ between VS and EN-pin

EN Pin

Electrical Characteristics Internal Supply / EN pin (cont'd)

Unless otherwise specified:  $V_S = 5.5\text{ V}$  to  $40\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $R_{SETx} = 12\text{ k}\Omega$  all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.6	Power-on reset delay time <sup>3)</sup>	$t_{POR}$	-	-	25	$\mu\text{s}$	<sup>1)</sup> $V_S = V_{EN} = 0 \rightarrow 13.5\text{ V}$ $V_{OUTx(nom)} = 3.6 \pm 0.3\text{ V}$ $I_{OUTx} = 80\% I_{OUTx(nom)}$
5.4.7	Required supply voltage for output activation	$V_{S(on)}$	-	-	4	V	$V_{EN} = 5.5\text{ V}$ $V_{OUTx} = 3\text{ V}$ $I_{OUTx} = 50\% I_{OUTx(nom)}$
5.4.8	Required supply voltage for current control	$V_{S(CC)}$	-	-	5.2	V	$V_{EN} = 5.5\text{ V}$ $V_{OUTx} = 3.6\text{ V}$ $I_{OUTx} \geq 90\% I_{OUTx(nom)}$
5.4.9	EN turn on threshold	$V_{EN(on)}$	-	-	2.5	V	-
5.4.10	EN turn off threshold	$V_{EN(off)}$	0.8	-	-	V	-
5.4.11	EN input current during low supply voltage	$I_{EN(LS)}$	-	-	2.4	mA	<sup>1)</sup> $V_S = 4.5\text{ V}$ $T_j < 105^\circ\text{C}$ $V_{EN} = 5.5\text{ V}$
5.4.12	EN high input current	$I_{EN(H)}$	-	-	0.1 0.1 2.05 0.45	mA	$T_j < 105^\circ\text{C}$ $V_S = 13.5\text{ V}, V_{EN} = 5.5\text{ V}$ $V_S = 18\text{ V}, V_{EN} = 5.5\text{ V}$ $V_S = V_{EN} = 18\text{ V}$ <sup>1)</sup> $V_S = 18\text{ V}, R_{EN} = 10\text{ k}\Omega$ between VS and EN-pin

1) Not subject to production test, specified by design

2) The total device current consumption is the sum of the currents  $I_S$  and  $I_{EN(H)}$ , please refer to **Pos. 5.4.12**

3) See also **Figure 4**

## 6 FB Pin

The following block diagram shows the feedback pin functionality.

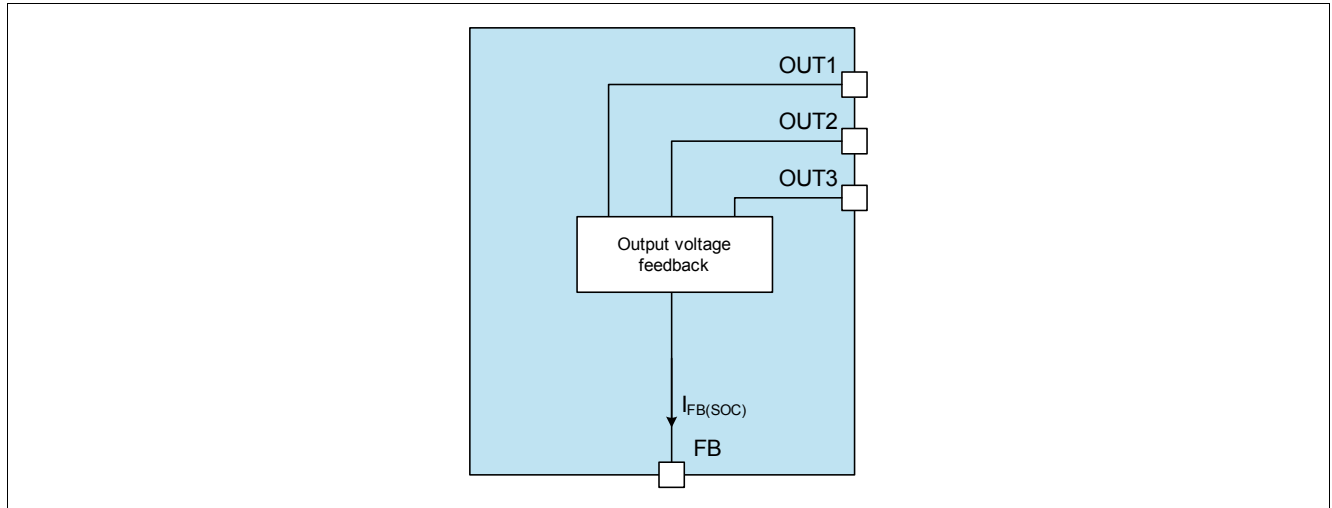


Figure 7 Block Diagram FB pin

### 6.1 DC/DC Control

With the FB pin the LITIX™ Basic IC realizes the dynamic overhead control. The IC provides a voltage feedback to an external DC/DC converter. Using the circuit shown in **Figure 17** it is possible to adjust the DC/DC output voltage in a way that the voltage drop over the output stages of the LITIX™ Basic IC is minimized - dynamic overhead control. This leads to a significant reduction of the overall driver's power dissipation and an increased system efficiency. **Figure 17** gives an application example, how different light functions can be controlled using a  $\mu\text{C}$ , if an open load diagnosis per LED chain is required.

*Note: For correct output current control and dynamic overhead control the parameters as specified in **Pos. 6.2.1** and **Pos. 6.2.2** need to be considered. FB source currents higher than given in **Pos. 6.2.1** lead to a drop of the FB regulation voltage  $V_{\text{FB(nom)}}$ .*

The resistor  $R_{\text{FB(PD)}}$  can be dimensioned by applying equations **Equation (2)** and **Equation (3)**. The following parameters are required:

- $V_{\text{OUT}}$  represents the maximum LED loads forward voltage, i.e. number of LEDs multiplied with the maximum LED forward voltage. Temperature drifts of the LED's forward voltage needs to be considered!
- $V_{\text{BO}}$  represents the DC/DC output voltage, which is predefined by the feedback resistors (**Figure 17**:  $R_{\text{FB1}}$ ,  $R_{\text{FB2}}$ ,  $R_{\text{FB3}}$ ). Please refer to the according DC/DC device data sheet for the dimensioning of those resistors.
- $n_{\text{len}}$  represents the numbers of LITIX™ Basics using the longest LED-chains (e.g. if there are 3 devices connected to one DC/DC converter and two devices using LED chains with 7 LEDs and one device is used with LED chain lengths of 6 LEDs the according  $n_{\text{len}} = 2$ .)
- $\beta$  represents the DC gain of the external bipolar transistor, which is connected to the DC/DC's feedback pin.

$$R_{\text{FB(PD,min)}} = \min \left\{ \frac{V_{\text{OUT}} - 0.5 \text{ V}}{4 \cdot 10^{-5} \text{ A}} \cdot \frac{1}{n_{\text{len}}}, \frac{V_{\text{OUT}} - 1.1 \text{ V}}{V_{\text{BO}} - V_{\text{OUT}} - 1.1 \text{ V}} \cdot \frac{1.7 \cdot 10^5 \Omega}{n_{\text{len}}} \right\} \quad (2)$$

$$R_{\text{FB(PD,max)}} = \frac{V_{\text{OUT}} - 1.1 \text{ V}}{V_{\text{BO}} - V_{\text{OUT}}} \cdot \frac{1}{R_{\text{FB1}} \cdot \beta + 1} \quad (3)$$

FB Pin

## 6.2 Electrical Characteristics FB Pin

### Electrical Characteristics FB pin

Unless otherwise specified:  $V_S = 5.5\text{ V to }40\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $R_{SET} = 12\text{ k}\Omega$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

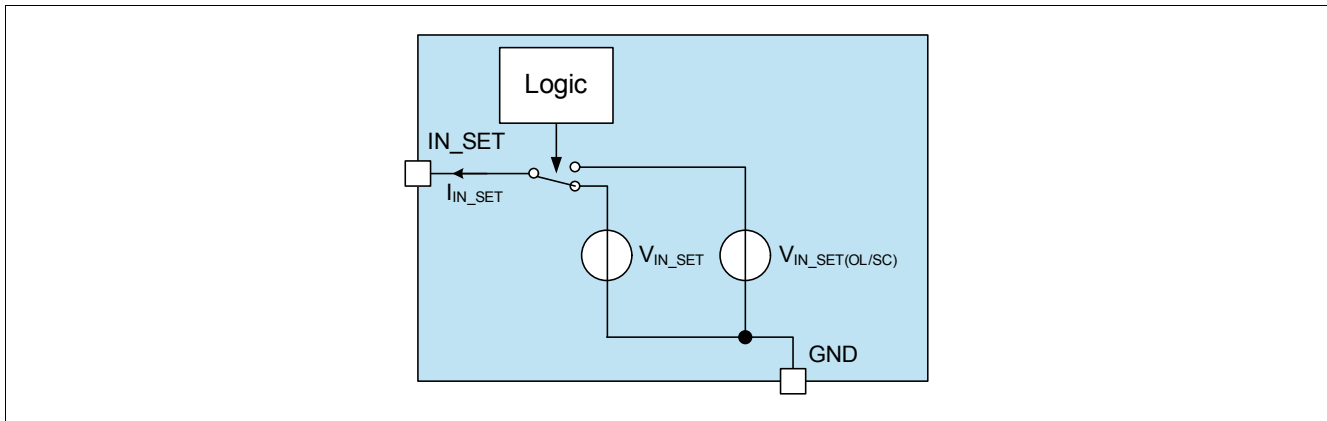
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.2.1	FB regulation voltage	$V_{FB(nom)}$	$(V_{OUT} - 1) * 0.9$	$V_{OUT} - 1$	-	V	$I_{FB(SOC)} = 25\ \mu\text{A}$
6.2.2	FB operating voltage at power stage $V_{PS(FB)} = V_S - V_{OUTx}$	$V_{PS(FB)}$	-	-	10	V	<sup>1)</sup>

1) Not subject to production test, specified by design

IN\_SETx Pin

## 7 IN\_SETx Pin

The IN\_SET pin is a multiple function pin for output current definition, input and diagnostics:



**Figure 8** Block Diagram IN\_SET pin

### 7.1 Output Current Adjustment via RSET

The output current of each channel can be adjusted independently. The current adjustment can be done by placing a low power resistor ( $R_{SET}$ ) at the IN\_SETx pin to ground. The dimensioning of the resistor can be done using the formula below:

$$R_{SET} = \frac{k}{I_{OUT}} \quad (4)$$

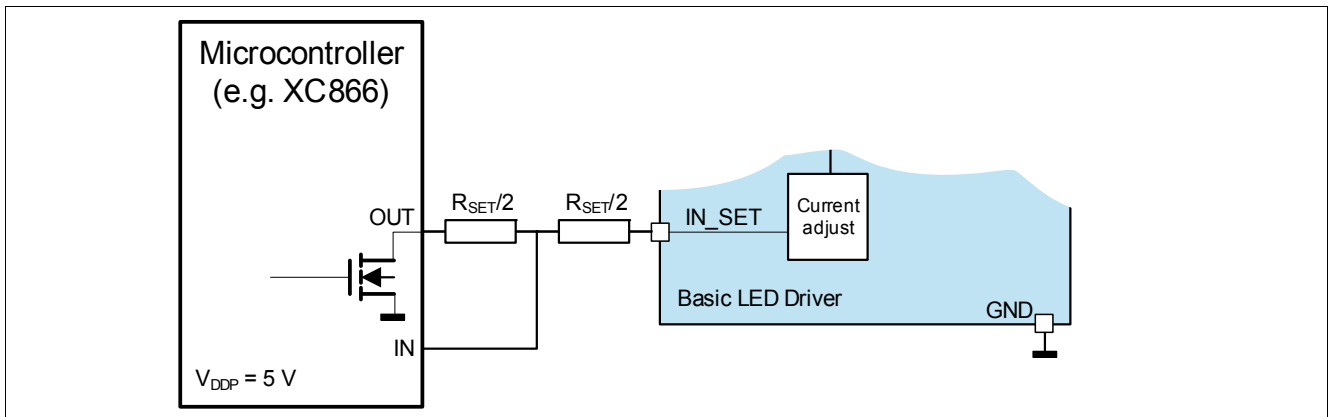
The gain factor  $k$  ( $R_{SET}$  \* output current) is specified in **Pos. 9.2.4** and **Pos. 9.2.5**. The current through the  $R_{SET}$  is defined by the resistor itself and the reference voltage  $V_{IN\_SET(ref)}$ , which is applied to the IN\_SET during supplied device.

### 7.2 Smart Input Pin

The IN\_SETx pin can be connected via  $R_{SET}$  to the open-drain output of a  $\mu C$  or to an external NMOS transistor as described in **Figure 9**. This signal can be used to turn off the output stages of the IC. A minimum IN\_SET current of  $I_{IN\_SET(act)}$  is required to turn on the output stages. This feature is implemented to prevent glimmering of LEDs caused by leakage currents on the IN\_SET pin, see **Figure 11** for details. In addition, the IN\_SET pin offers the diagnostic feedback information. In case of a fault event the IN\_SET voltage is increased to  $V_{IN\_SET(OL/SC)}$  **Pos. 8.4.2**. Therefore, the device has two voltage domains at the IN\_SET-pin, which is shown in **Figure 12**.

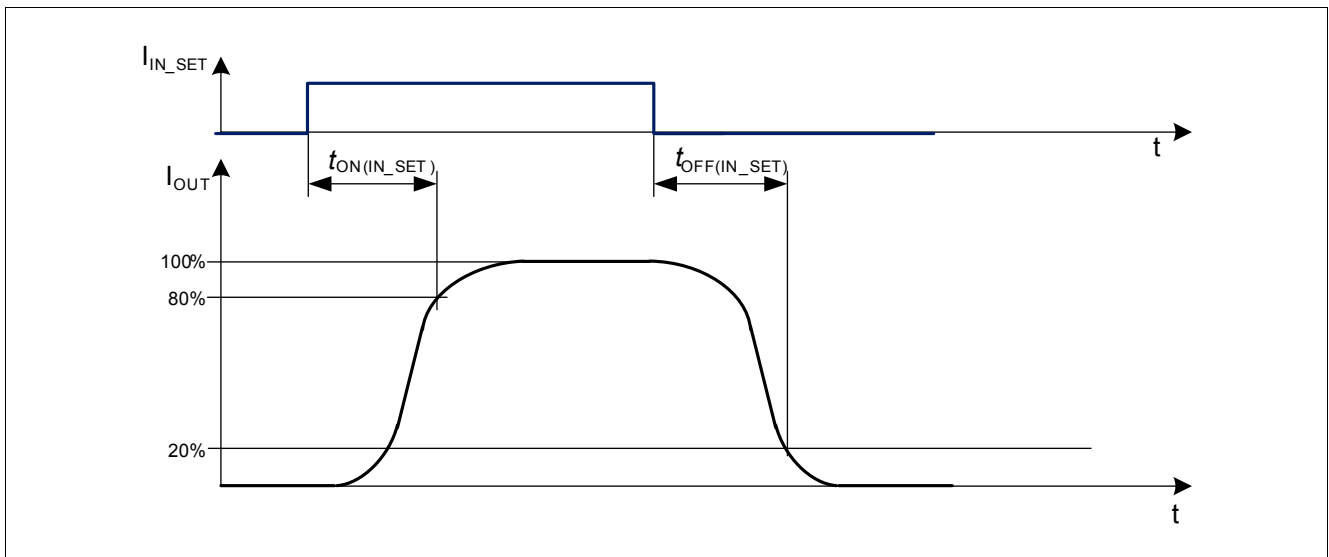
*Note: If one output has a present fault (open load or short circuit) and one or both of the other channels are dimmed via PWM at the IN\_SET-pins a short spike to  $V_{IN\_SET(OL/SC)}$  is possible. Please refer to **Chapter 8.3**.*

IN\_SETx Pin



**Figure 9 Schematics IN\_SET interface to  $\mu$ C**

The resulting switching times are shown in [Figure 10](#):



**Figure 10 Switching times via IN\_SET**



IN\_SETx Pin

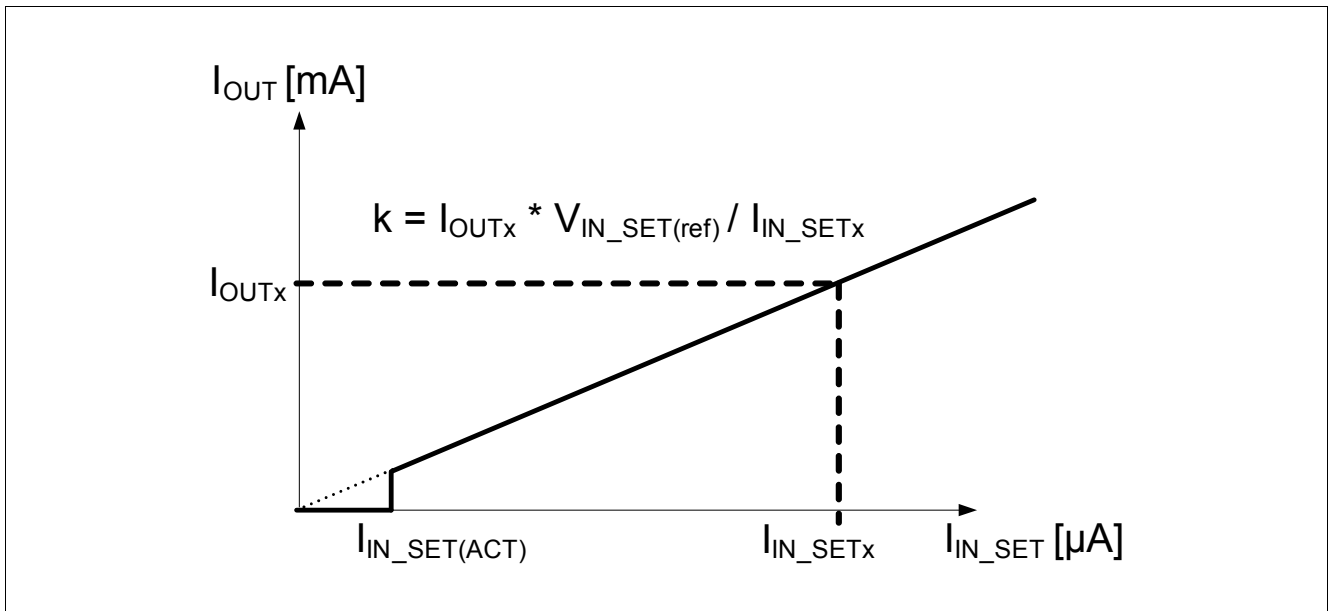


Figure 11  $I_{OUT}$  versus  $I_{INSET}$

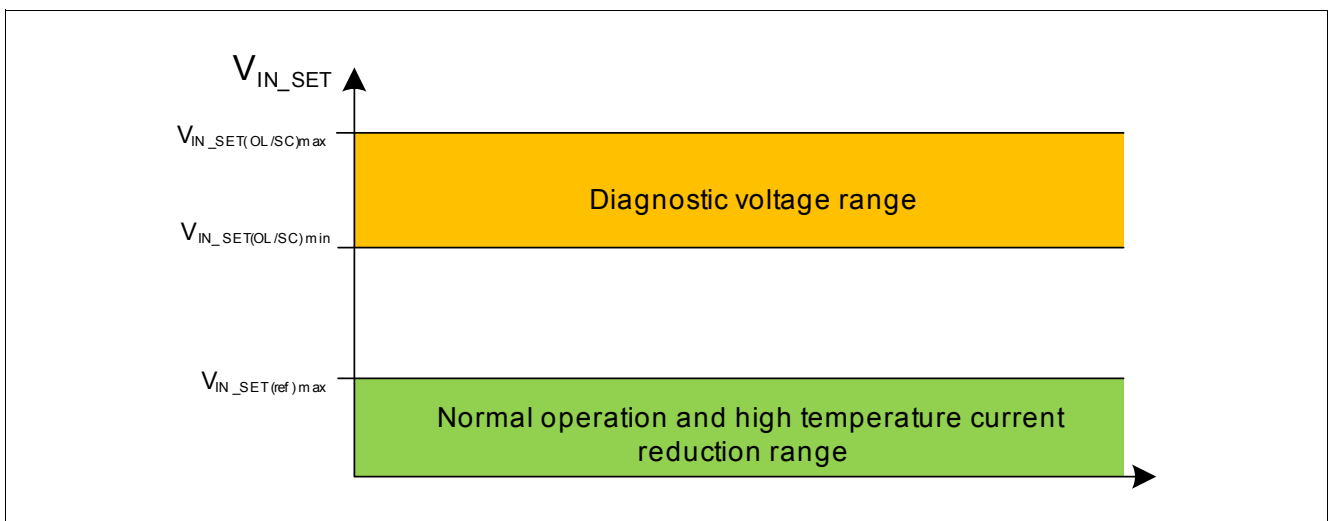
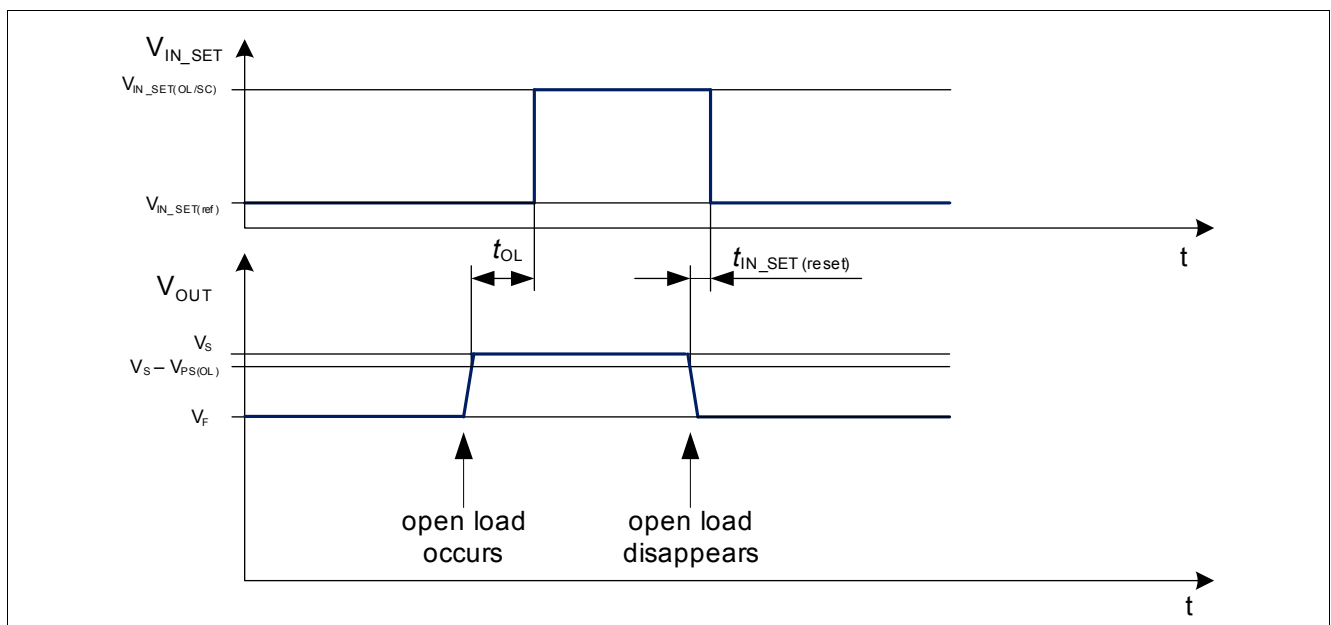


Figure 12 Voltage domains for IN\_SET pin, if ST pin is connected to GND

## 8 Load Diagnosis

### 8.1 Open Load

An open load diagnosis feature is integrated in the TLD2326EL driver IC. If there is an open load on one of the outputs, the respective output is turned off. The potential on the IN\_SET pin rises up to  $V_{IN\_SET(OL/SC)}$ . This high voltage can be used as input signal for an  $\mu C$  as shown in **Figure 9**. The open load status is not latched, as soon as the open load condition is no longer present, the output stage will be turned on again. An open load condition is detected, if the voltage drop over the output stage  $V_{PS}$  is below the threshold according **Pos. 8.4.6** and a filter time of  $t_{OL}$  is passed.



**Figure 13** IN\_SET behavior during open load condition

### 8.2 Short Circuit to GND detection

The TLD2326EL has an integrated SC to GND detection. If the output stage is turned on and the voltage at the output falls below  $V_{OUT(SC)}$  the potential on the IN\_SET pin is increased up to  $V_{IN\_SET(OL/SC)}$  after  $t_{SC}$ . This condition is not latched. For detecting a normal condition after a short circuit detection an output current according to  $I_{OUT(SC)}$  is driven by the channel.

Load Diagnosis

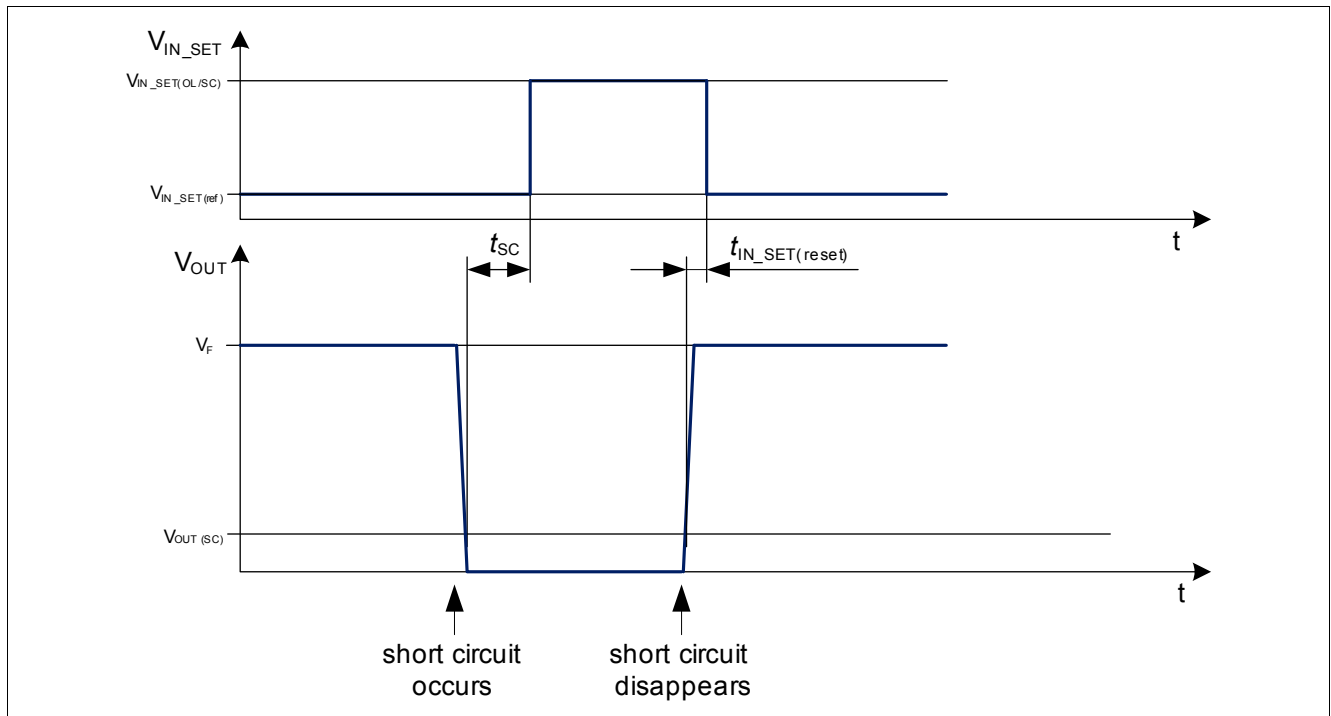


Figure 14 **IN\_SET** behavior during short circuit to GND condition with ST connected to GND and  $V_{DEN} > V_{DEN(act)}$

8.3 Double Fault Conditions

The TLD2326EL allows the diagnosis of each channel separately. The diagnosis filter times  $t_{OL}$  and  $t_{SC}$  (Pos. 8.4.5 and Pos. 8.4.8) are valid only for the channel, which diagnoses first the fault condition. For the other channel or channels with a subsequential fault the diagnosis is reported immediately without the diagnosis filter time, if the filter time  $t_{OL}$  has been elapsed for the channel with the first fault. During activation via IN\_SET of a non-faulty output, where one channel has already a fault detected, a short spike to  $V_{IN\_SET(OL/SC)}$  could occur on the channel, which should be activated. Therefore, in general a diagnosis should be done earliest after the diagnosis filter times  $t_{OL}$  and  $t_{SC}$  to avoid any incorrect diagnosis readout. In the scenario mentioned above the turn on time  $t_{ON(IN\_SET)}$  could be extended. The following figure shows the example behavior, if OUT1 has a fault and OUT2 is operated in PWM-mode. OUT3 is disabled.

Load Diagnosis

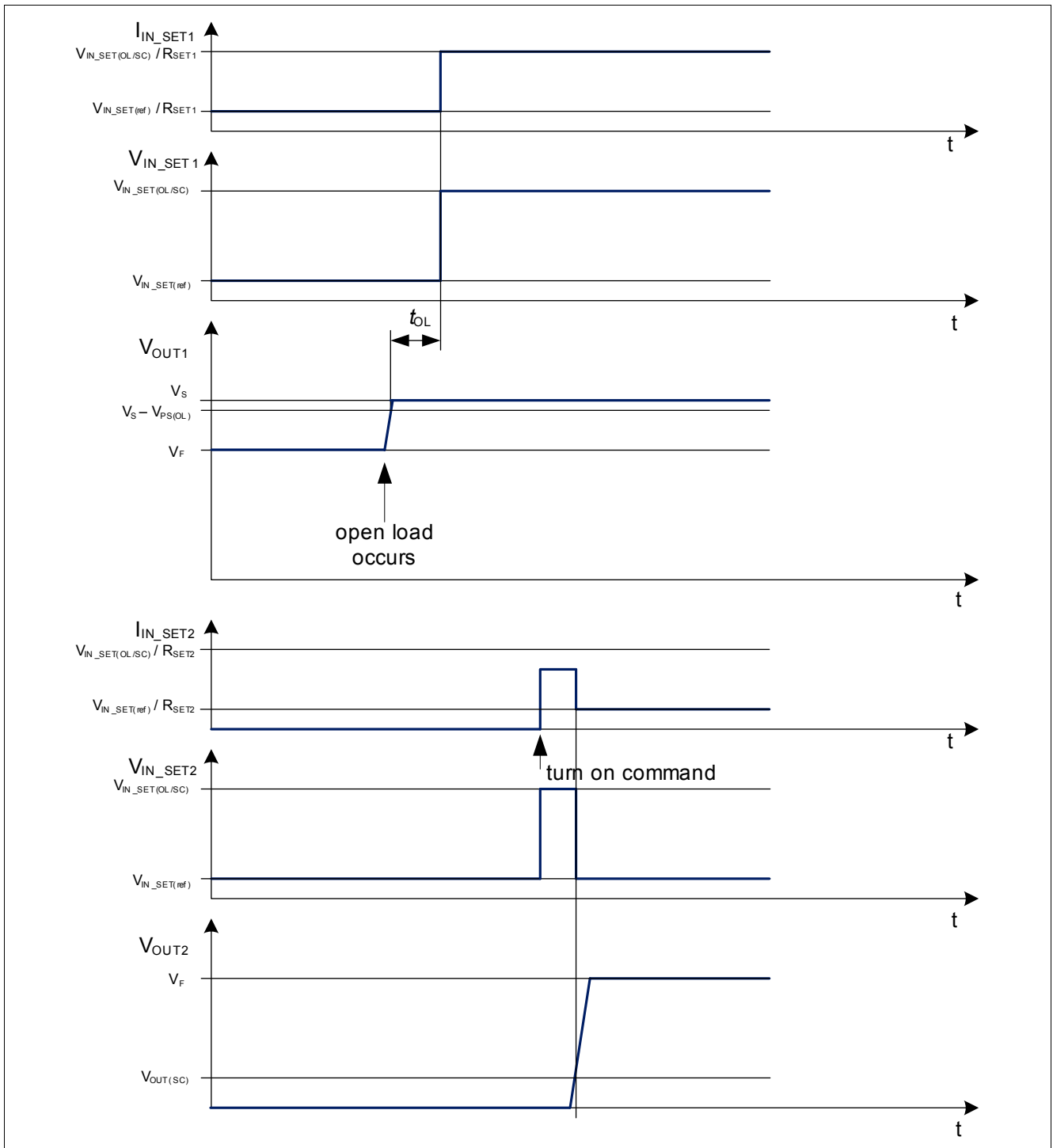


Figure 15 Example single channel fault on OUT1 and PWM-operation on OUT2

Load Diagnosis

8.4 Electrical Characteristics IN\_SET Pin and Load Diagnosis

Electrical Characteristics IN\_SET pin and Load Diagnosis

Unless otherwise specified:  $V_S = 5.5 \text{ V to } 40 \text{ V}$ ,  $T_j = -40^\circ\text{C to } +150^\circ\text{C}$ ,  $R_{SETx} = 12 \text{ k}\Omega$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.1	IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.19	1.23	1.27	V	<sup>1)</sup> $V_{OUTx} = 3.6 \text{ V}$ $T_j = 25...115 \text{ }^\circ\text{C}$
8.4.2	IN_SET open load/short circuit voltage	$V_{IN\_SET(OL/SC)}$	4	–	5.5	V	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150 \text{ }^\circ\text{C}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.3	IN_SET open load/short circuit voltage	$V_{IN\_SET(OL/SC)}$	3.2	–	5.5	V	<sup>1)</sup> $V_S = 5.5 \text{ V}$ $T_j = 25...150 \text{ }^\circ\text{C}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.4	IN_SET open load/short circuit current	$I_{IN\_SET(OL/SC)}$	0.5	–	2.5	mA	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150 \text{ }^\circ\text{C}$ $V_{IN\_SET} = 4 \text{ V}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.5	OL detection filter time	$t_{OL}$	10	22	35	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.6	OL detection voltage $V_{PS(OL)} = V_S - V_{OUTx}$	$V_{PS(OL)}$	0.2	–	0.4	V	$V_S > 8 \text{ V}$
8.4.7	Short circuit to GND detection threshold	$V_{OUT(SC)}$	0.8	–	1.4	V	$V_S > 8 \text{ V}$
8.4.8	SC detection filter time	$t_{SC}$	10	22	35	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.9	IN_SET diagnosis reset time	$t_{IN\_SET(reset)}$	–	5	20	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.10	SC detection current	$I_{OUT(SC)}$	0.1	2	4.75	mA	$V_S > 8 \text{ V}$ $V_{OUTx} = 0 \text{ V}$
8.4.11	IN_SET activation current without turn on of output stages	$I_{IN\_SET(act)}$	2	–	15	$\mu\text{A}$	See <b>Figure 11</b>

1) Not subject to production test, specified by design

## 9 Power Stage

The output stages are realized as high side current sources with a current of 120 mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED. To increase the overall output current for high brightness LED applications it is possible to connect two or all three output stages in parallel.

The maximum current of each channel is limited by the power dissipation and used PCB cooling areas (which results in the applications  $R_{thJA}$ ).

For an operating current control loop the supply and output voltages according to the following parameters have to be considered:

- Required supply voltage for current control  $V_{S(CC)}$ , **Pos. 5.4.8**
- Voltage drop over output stage during current control  $V_{PS(CC)}$ , **Pos. 9.2.6**
- Required output voltage for current control  $V_{OUTx(CC)}$ , **Pos. 9.2.7**

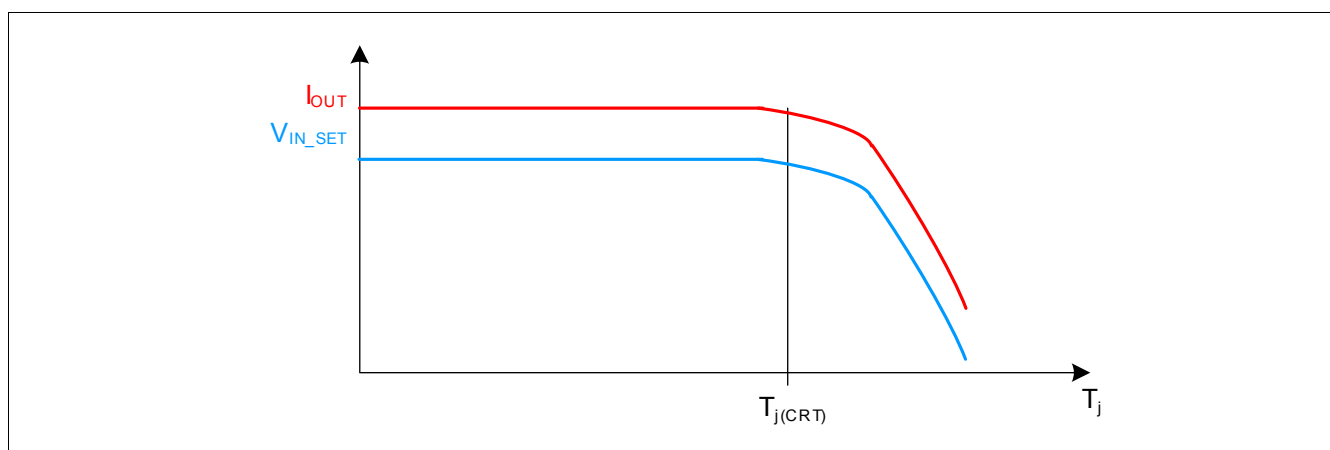
### 9.1 Protection

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

#### 9.1.1 Over Load Behavior

An over load detection circuit is integrated in the LITIX™ Basic IC. It is realized by a temperature monitoring of the output stages (OUTx).

As soon as the junction temperature exceeds the current reduction temperature threshold  $T_{j(CRT)}$  the output current will be reduced by the device by reducing the IN\_SET reference voltage  $V_{IN\_SET(ref)}$ . This feature avoids LED’s flickering during static output overload conditions. Furthermore, it protects LEDs against over temperature, which are mounted thermally close to the device. If the device temperature still increases, the three output currents decrease close to 0 A. As soon as the device cools down the output currents rise again.



**Figure 16 Output current reduction at high temperature**

*Note: This high temperature output current reduction is realized by reducing the IN\_SET reference voltage (Pos. 8.4.1). In case of very high power loss applied to the device and very high junction temperature the output current may drop down to  $I_{OUTx} = 0$  mA, after a slight cooling down the current increases again.*

## Power Stage

### 9.1.2 Reverse Battery Protection

The TLD2326EL has an integrated reverse battery protection feature. This feature protects the driver IC itself, but also connected LEDs. The output reverse current is limited to  $I_{OUTx(rev)}$  by the reverse battery protection.

*Note: Due to the reverse battery protection a reverse protection diode for the light module may be obsolete. In case of high ISO-pulse requirements and only minor protecting components like capacitors a reverse protection diode may be reasonable. The external protection circuit needs to be verified in the application.*

## 9.2 Electrical Characteristics Power Stage

### Electrical Characteristics Power Stage

Unless otherwise specified:  $V_S = 5.5\text{ V to }18\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $V_{OUTx} = 3.6\text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.1	Output leakage current	$I_{OUTx(leak)}$	-	-	7 3	$\mu\text{A}$	$V_{EN} = 5.5\text{ V}$ $I_{IN\_SET} = 0\ \mu\text{A}$ $V_{OUTx} = 2.5\text{ V}$ $T_j = 150^\circ\text{C}$ 1) $T_j = 85^\circ\text{C}$
9.2.2	Output leakage current in boost over battery setup	- $I_{OUTx(leak,B2B)}$	-	-	50	$\mu\text{A}$	1) $V_{EN} = 5.5\text{ V}$ $I_{IN\_SET} = 0\ \mu\text{A}$ $V_{OUTx} = V_S = 40\text{ V}$
9.2.3	Reverse output current	$-I_{OUTx(rev)}$	-	-	1	$\mu\text{A}$	1) $V_S = -16\text{ V}$ Output load: LED with break down voltage < -0.6 V
9.2.4	Output current accuracy limited temperature range	$k_{LT}$	697 645	750 750	803 855		1) $T_j = 25\dots115^\circ\text{C}$ $V_S = 8\dots18\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{SETx} = 6\dots12\text{ k}\Omega$ $R_{SETx} = 30\text{ k}\Omega$
9.2.5	Output current accuracy over temperature	$k_{ALL}$	697 645	750 750	803 855		1) $T_j = -40\dots115^\circ\text{C}$ $V_S = 8\dots18\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{SETx} = 6\dots12\text{ k}\Omega$ $R_{SETx} = 30\text{ k}\Omega$
9.2.6	Voltage drop over power stage during current control $V_{PS(CC)} = V_S - V_{OUTx}$	$V_{PS(CC)}$	0.75	-	-	V	1) $V_S = 13.5\text{ V}$ $R_{SETx} = 12\text{ k}\Omega$ $I_{OUTx} \geq 90\%$ of $(k_{LT(typ)}/R_{SETx})$
9.2.7	Required output voltage for current control	$V_{OUTx(CC)}$	2.3	-	-	V	1) $V_S = 13.5\text{ V}$ $R_{SETx} = 12\text{ k}\Omega$ $I_{OUTx} \geq 90\%$ of $(k_{LT(typ)}/R_{SETx})$

Power Stage

Electrical Characteristics Power Stage (cont'd)

Unless otherwise specified:  $V_S = 5.5\text{ V to }18\text{ V}$ ,  $T_j = -40^\circ\text{C to }+150^\circ\text{C}$ ,  $V_{OUTx} = 3.6\text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.8	Maximum output current	$I_{OUT(max)}$	120	–	–	mA	$R_{SETx} = 4.7\text{ k}\Omega$ The maximum output current is limited by the thermal conditions. Please refer to <b>Pos. 4.3.1 - Pos. 4.3.3</b>
9.2.9	IN_SET turn on time	$t_{ON(IN\_SET)}$	–	–	15	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $I_{IN\_SET} = 0 \rightarrow 100\text{ }\mu\text{A}$ $I_{OUTx} = 80\%$ of $(k_{LT(typ)}/R_{SETx})$ No OL or SC at other channels
9.2.10	IN_SET turn off time	$t_{OFF(IN\_SET)}$	–	–	10	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $I_{IN\_SET} = 100 \rightarrow 0\text{ }\mu\text{A}$ $I_{OUTx} = 20\%$ of $(k_{LT(typ)}/R_{SETx})$
9.2.11	VS turn on time	$t_{ON(VS)}$	–	–	20	$\mu\text{s}$	<sup>1) 2)</sup> $V_{EN} = 5.5\text{ V}$ $R_{SETx} = 12\text{ k}\Omega$ $V_S = 0 \rightarrow 13.5\text{ V}$ $I_{OUTx} = 80\%$ of $(k_{LT(typ)}/R_{SETx})$
9.2.12	Current reduction temperature threshold	$T_{j(CRT)}$	–	140	–	$^\circ\text{C}$	<sup>1)</sup> $I_{OUTx} = 95\%$ of $(k_{LT(typ)}/R_{SETx})$
9.2.13	Output current during current reduction at high temperature	$I_{OUT(CRT)}$	85% of $(k_{LT(typ)}/R_{SETx})$	–	–	A	<sup>1)</sup> $R_{SETx} = 12\text{ k}\Omega$ $T_j = 150\text{ }^\circ\text{C}$

1) Not subject to production test, specified by design

2) see also **Figure 6**



Application Information

10 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

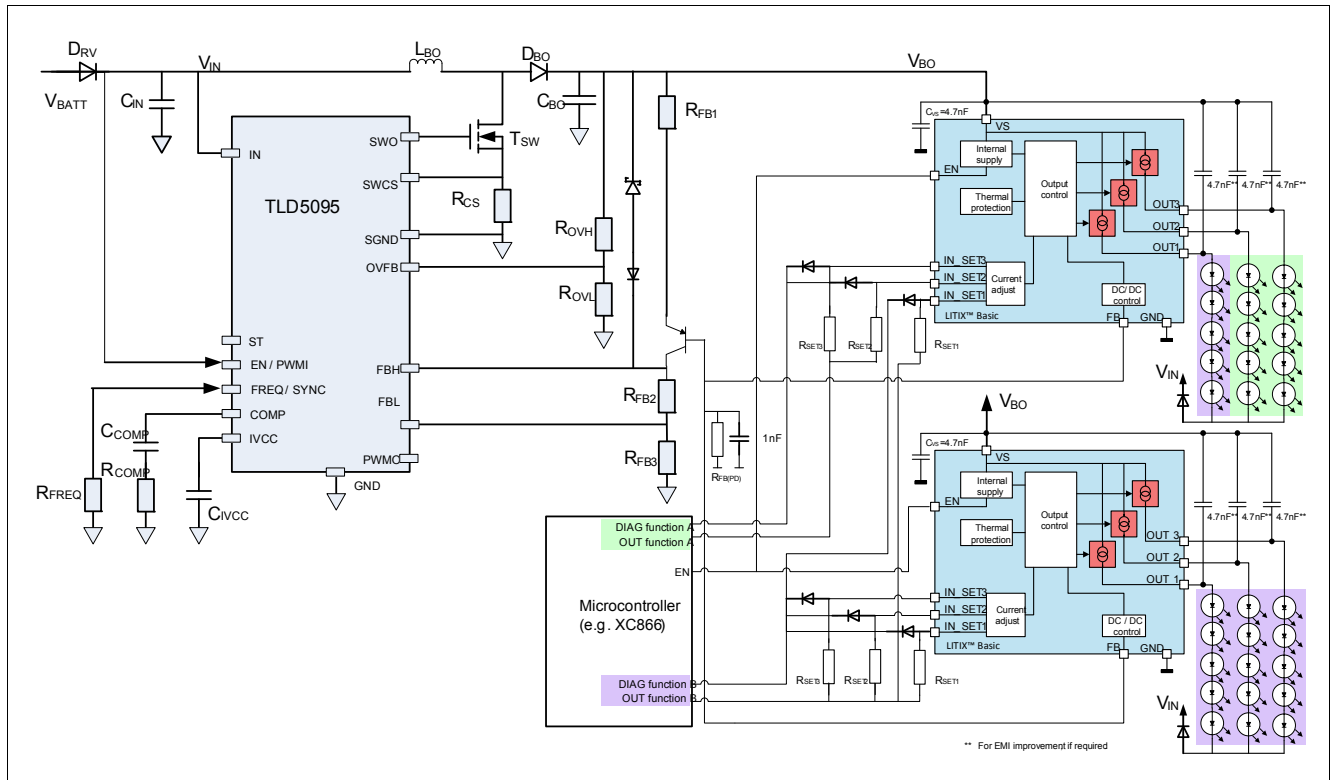


Figure 17 System diagram DC/DC control Boost using 3 IN\_SET pins

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

10.1 Further Application Information

- For further information you may contact <http://www.infineon.com/>

## 11 Package Outlines

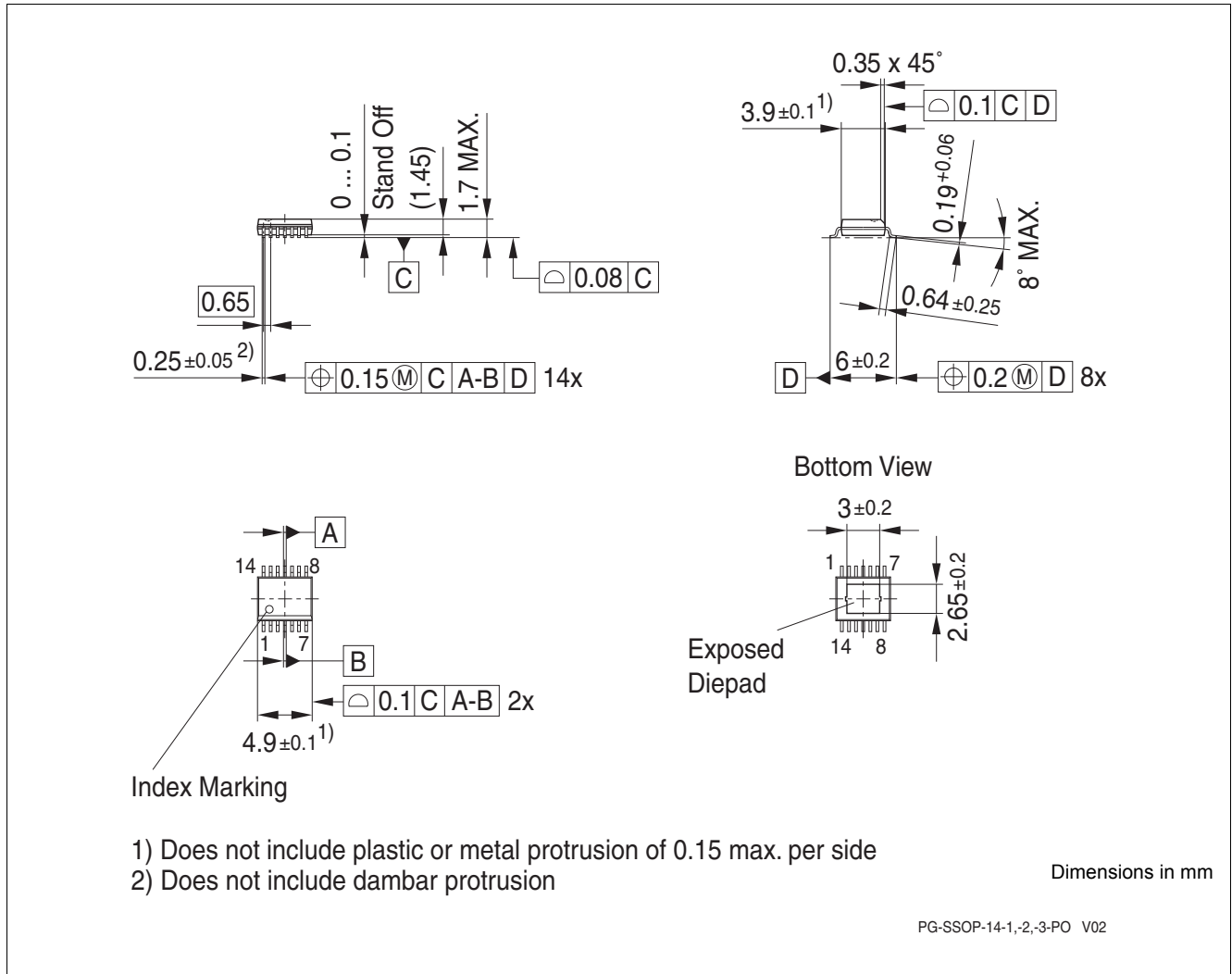


Figure 18 PG-SSOP-14

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision History

## 12 Revision History

Revision	Date	Changes
1.0	2013-08-08	Initial revision of data sheet
1.1	2015-03-19	Updated parameters $K_{LT}$ and $K_{ALL}$ in the chapter Power Stage
1.2	2018-04-26	Updated to latest template
1.2	2018-04-26	Updated application drawing
1.2	2018-04-26	Updated package marking
1.2	2018-04-26	Updated package figure

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