User's Guide

TPS54394 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS54394EVM-057 evaluation module as well as for the TPS54394. Included are the performance specifications, schematic, and the bill of materials of the TPS54394 EVM.

Table of Contents

1 Introduction ... 3
2 Performance Specification Summary ... 4
3 Modifications ... 5
3.1 Output Voltage Setpoint ... 5
3.2 Output Filter and Closed-Loop Response ... 5
4 Test Setup and Results ... 6
4.1 Input/Output Connections ... 6
4.2 Start-Up Procedure ... 6
4.3 Efficiency ... 7
4.4 Load Regulation ... 9
4.5 Line Regulation ... 10
4.6 Load Transient Response ... 11
4.7 Output Voltage Ripple ... 12
4.8 Input Voltage Ripple ... 14
4.9 Start-Up ... 15
5 Board Layout ... 17
5.1 Layout ... 17
6 Schematic, Bill of Materials, and Reference ... 21
6.1 Schematic ... 21
6.2 Bill of Materials ... 22
6.3 Reference ... 22
7 Revision History ... 23

List of Figures

Figure 4-1. TPS54394EVM Converter 1 Efficiency ... 7
Figure 4-2. TPS54394EVM Converter 1 Light Load Efficiency ... 7
Figure 4-3. TPS54394EVM Converter 2 Efficiency ... 8
Figure 4-4. TPS54394EVM Converter 2 Light Load Efficiency ... 8
Figure 4-5. TPS54394EVM Converter 1 Load Regulation ... 9
Figure 4-6. TPS54394EVM Converter 2 Load Regulation ... 9
Figure 4-7. TPS54394EVM Converter 1 Line Regulation ... 10
Figure 4-8. TPS54394EVM Converter 2 Line Regulation ... 10
Figure 4-9. TPS54394EVM Converter 1 Load Transient Response ... 11
Figure 4-10. TPS54394EVM Converter 2 Load Transient Response ... 11
Figure 4-11. TPS54394EVM Converter 1 Output Voltage Ripple ... 12
Figure 4-12. TPS54394EVM Converter 1 Eco-mode Output Voltage Ripple at No Load ... 12
Figure 4-13. TPS54394EVM Converter 2 Output Voltage Ripple ... 13
Figure 4-14. TPS54394EVM Converter 2 Eco-mode Output Voltage Ripple at No Load ... 13
Figure 4-15. TPS54394EVM Input Voltage Ripple ... 14
Figure 4-16. TPS54394EVM Converter 1 Start-Up Relative to V_{IN} ... 15
Figure 4-17. TPS54394EVM Start-Up Relative to EN1 ... 15
Figure 4-18. TPS54394EVM Converter 2 Start-Up Relative to V_{IN} ... 16

Copyright © 2022 Texas Instruments Incorporated

Figure 4-19. TPS54394EVM Start-Up Relative to EN2 16
Figure 5-1. Top Assembly 17
Figure 5-2. Top Layer 18
Figure 5-3. Internal 1 Layer 18
Figure 5-4. Internal 2 Layer 19
Figure 5-5. Bottom Layer 19
Figure 5-6. Bottom Assembly 20
Figure 6-1. TPS54394EVM Schematic Diagram 21

List of Tables

Table 1-1. Input Voltage, Output Voltage and Output Current Summary 3
Table 2-1. TPS54394EVM Performance Specifications Summary 4
Table 3-1. Output Voltages 5
Table 4-1. Connection and Test Points 6
Table 6-1. Bill of Materials 22

Trademarks

D-CAP2™, and Eco-mode™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

Copyright © 2022 Texas Instruments Incorporated

1 Introduction

The TPS54394 is a dual, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a low, external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal of 700 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS54394 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFETs allows the TPS54394 to achieve high efficiencies and helps keep the junction temperature low at high-output currents. The TPS54394 also features auto-skip Eco-mode™ operation for improved light-load efficiency. The TPS54394 dual DC/DC synchronous converter is designed to provide up to 3-A output on CH1 and CH2 from an input voltage source of 4.5 V to 18 V. The output voltage range is from 0.76 V to 7 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1.

The TPS54394 EVM evaluation module is a dual, synchronous buck converter providing 3.3 V at 3 A on CH1 and 1.5 V at 3 A on CH2 from 5-V to 18-V input. This user's guide describes the TPS54394 EVM performance.

Note

Throughout the document, x means 1 or 2, for example, VFBx means VFB1 or VFB2.

Table 1-1. Input Voltage, Output Voltage and Output Current Summary

TPS54394EVM	INPUT VOLTAGE RANGE	OUTPUT VOLTAGE	OUTPUT CURRENT RANGE
CH1	V_{IN1} = 6 V to 18 V	3.3 V	0 A to 3 A
CH2	V_{IN2} = 5 V to 18 V	1.5 V	0 A to 3 A

Copyright © 2022 Texas Instruments Incorporated

2 Performance Specification Summary

A summary of the TPS54394EVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{INx} = 12 V and an output voltage of 3.3 V and 1.5 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS54394EVM Performance Specifications Summary

SPECIFICATIONS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range (V_{INx})			(1)	12	18	V
Output voltages	V_{OUT1}			3.3		V
	V_{OUT2}			1.5		
Operating frequency		V_{IN1}, V_{IN2} = 12 V, I_{OUT1}, I_{OUT2} = 1.5 A		700		kHz
Output current range	CH1		0		3	A
	CH2		0		3	
Line regulation, V_{OUT1}		I_{OUT1} = 1.5 A, I_{OUT2} = 0 A, V_{IN1}, V_{IN2}= 6 V to 18 V		+0.3 , – 0.5%		
Line regulation, V_{OUT2}		I_{OUT2} = 1.5 A, I_{OUT1} = 0 A, V_{IN1}, V_{IN2}= 5 V to 18 V		+0.2, – 0.4%		
Load regulation, V_{OUT1}		V_{IN1}, V_{IN2} = 12 V, I_{OUT1} = 0 A to 3 A		+0.65, – 0.05%		
Load regulation, V_{OUT2}		V_{IN1}, V_{IN2} = 12 V, I_{OUT2} = 0 A to 3 A		+0.6, – 0.05%		
Over current limit, V_{OUT1}		V_{IN1} = 12 V, L_1 = 2.2 µH	3.5	4.7	6.5	A
Over current limit, V_{OUT2}		V_{IN2} = 12 V, L_1 = 2.2 µH	3.5	4.7	6.5	A
Output ripple voltage, V_{OUT1}		V_{IN1} = 12 V, I_{OUT1} = 3 A		15		mV_{PP}
Output ripple voltage, V_{OUT2}		V_{IN2} = 12 V, I_{OUT2} = 3 A		25		mV_{PP}
Maximum efficiency, V_{OUT1}		V_{IN1} = 6 V, I_{OUT1}= 0.7 A		94.9%		
Maximum efficiency, V_{OUT2}		V_{IN2} = 5 V, I_{OUT2}= 0.7 A		90.3%		

(1) See Table 1-1

Copyright © 2022 Texas Instruments Incorporated

3 Modifications

This evaluation module is designed to provide access to the features of the TPS54394. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltages of the EVM, it is necessary to change the value of the top resistor of the feedback divider, R1 or R3. Please refer to the top assembly in Figure 5-1 to locate the resistors close to the output connectors. Changing the value of R1 or R3 can change the output voltage above 0.765 V. The value of R1 or R3 for a specific output voltage can be calculated using Equation 1.

For output voltage from 0.76 V to 7 V:

$$V_{OUT1} = 0.765\ V \times \left(1 + \frac{R1}{R2}\right);\ V_{OUT2} = 0.765\ V \times \left(1 + \frac{R3}{R4}\right) \quad (1)$$

Table 3-1 lists the R1 or R3 values for some common output voltages. For output voltages of 1.8 V or above, a feedforward capacitor (C21 or C20) can be required to improve the phase margin. Pads for this component (C21 or C20) are provided on the printed-circuit board. Note that the resistor values given in Table 3-1 are standard values and not the exact values calculated using Equation 1.

Table 3-1. Output Voltages

Output Voltage (V)	R1, R3 (kΩ)	R2, R4 (kΩ)	C21, C20 (pF)	L1, L2 (µH)	C14, C15, C18 TOTAL CAPACITANCE, C16, C17, C19 TOTAL CAPACITANCE (µF)
1	6.81	22.1		1.5 – 2.2	22 – 68
1.05	8.25	22.1		1.5 – 2.2	22 – 68
1.2	12.7	22.1		1.5 – 2.2	22 – 68
1.5	21.5	22.1		1.5 – 2.2	22 – 68
1.8	30.1	22.1	5 – 22	2.2 – 3.3	22 – 68
2.5	49.9	22.1	5 – 22	2.2 – 3.3	22 – 68
3.3	73.2	22.1	5 – 22	2.2 – 3.3	22 – 68
5	124	22.1	5 – 22	4.7	22 – 68
6.5	165	22.1	5 – 22	4.7	22 – 68

3.2 Output Filter and Closed-Loop Response

The TPS54394 relies on the output filter characteristics to ensure stability of the control loop. The recommended output filter components for common output voltages are given in Table 3-1. It may be possible for other output filter component values to provide acceptable closed-loop characteristics. R11 and R12 are provided for convenience in breaking the control loop and measuring the closed-loop response.

Copyright © 2022 Texas Instruments Incorporated

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54394EVM. The section also includes test results typical for the following:

- Evaluation modules and efficiency
- Output load regulation
- Output line regulation
- Load transient response
- Output voltage ripple
- Input voltage ripple
- Start-up
- Switching frequency

4.1 Input/Output Connections

The TPS54394EVM is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The loads must be connected to J3 and/or J2 through a pair of 20 AWG wires. The maximum load current capability is two times 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the input voltage (V_{IN}) with TP7 providing a convenient ground reference. TP4 and TP3 are used to monitor the output voltages with TP5 and TP6 as the ground references.

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT2}, 1.5 V at 3-A maximum
J3	V_{OUT1}, 3.3 V at 3-A maximum
J4	EN1 control. Connect EN1 to off to disable converter 1; connect EN1 to on to enable converter 1.
J5	EN2 control. Connect EN2 to off to disable converter 2; connect EN2 to on to enable converter 2.
JP1	Jumper to give the possibility to use another input voltage for converter 2
TP1	V_{IN} test point at V_{IN} connector
TP2	V_{IN2} test point after JP1
TP3	Output voltage test point for converter 2
TP4	Output voltage test point for converter 1
TP5, TP6, TP7	Ground test points at input and output connectors
TP8	EN2 test point
TP9	EN1 test point
TP10	Switch node test point of converter
TP11	Switch node test point of converter 2
TP12	VREG5 test point
TP13	PG1 test point
TP14	PG2 test point
TP15	Analog ground test point

4.2 Start-Up Procedure

1. Ensure that the jumper at J4, J5 (Enable control), or both are set from ENx to off.
2. Apply appropriate V_{IN} voltage to VIN and PGND terminals at J1.
3. Move the jumper at J4, J5 (Enable control), or both to cover ENx and on. The EVM enables the according output voltage.

Copyright © 2022 Texas Instruments Incorporated

4.3 Efficiency

4.3.1 Efficiency of Converter 1

Figure 4-1 shows the efficiency for converter 1 on the TPS54394EVM at an ambient temperature of 25°C.

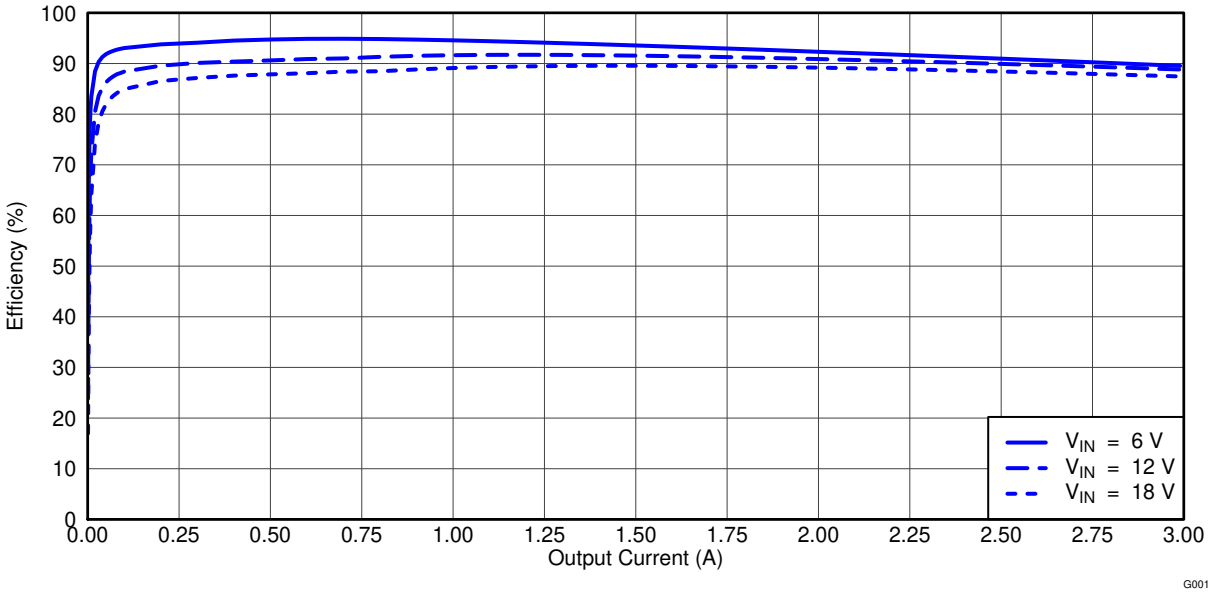


Figure 4-1. TPS54394EVM Converter 1 Efficiency

Figure 4-2 shows the light load efficiency for converter 1 on the TPS54394EVM at an ambient temperature of 25°C.

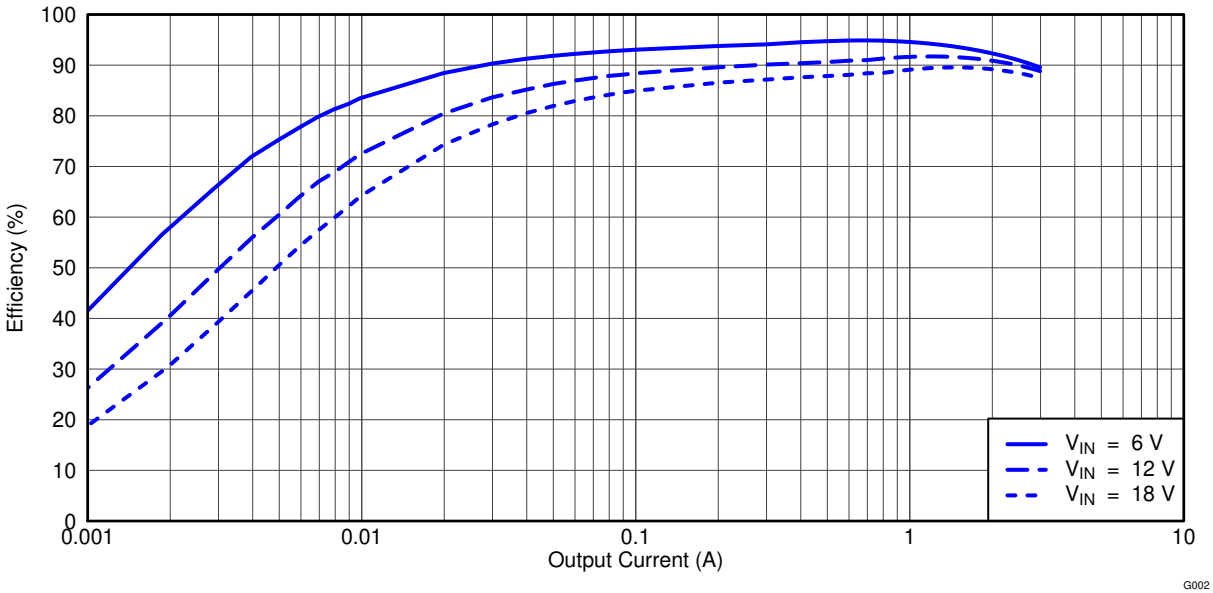


Figure 4-2. TPS54394EVM Converter 1 Light Load Efficiency

Copyright © 2022 Texas Instruments Incorporated

4.3.2 Efficiency of Converter 2

Figure 4-3 shows the efficiency for converter 2 on the TPS54394EVM at an ambient temperature of 25°C.

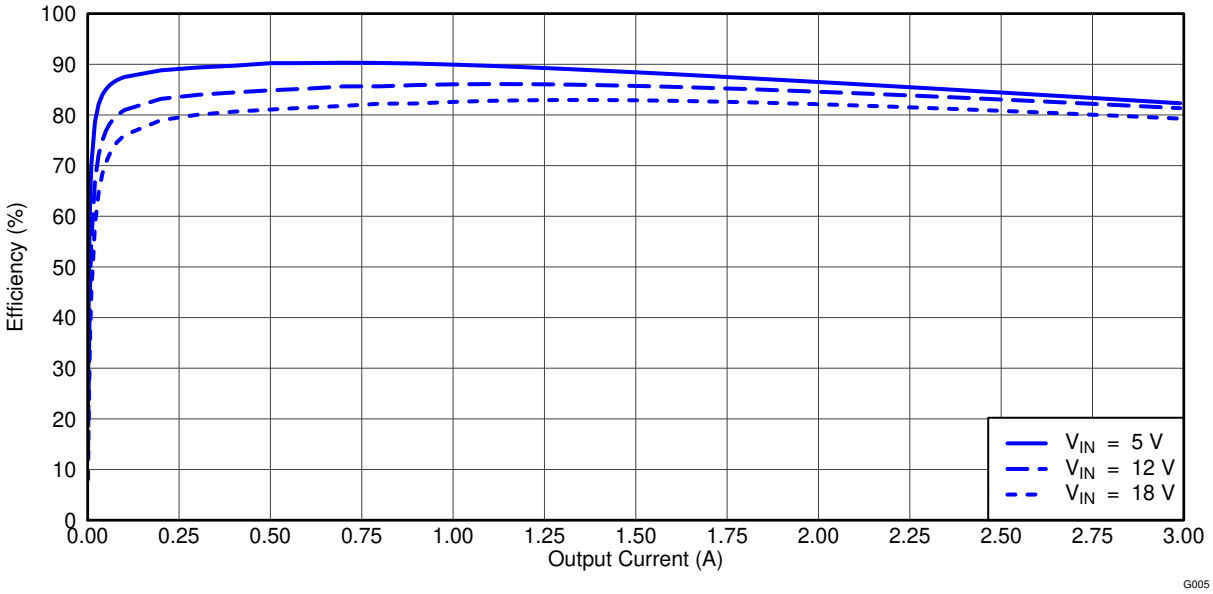


Figure 4-3. TPS54394EVM Converter 2 Efficiency

Figure 4-4 shows the light load efficiency for converter 2 on the TPS54394EVM at an ambient temperature of 25°C.

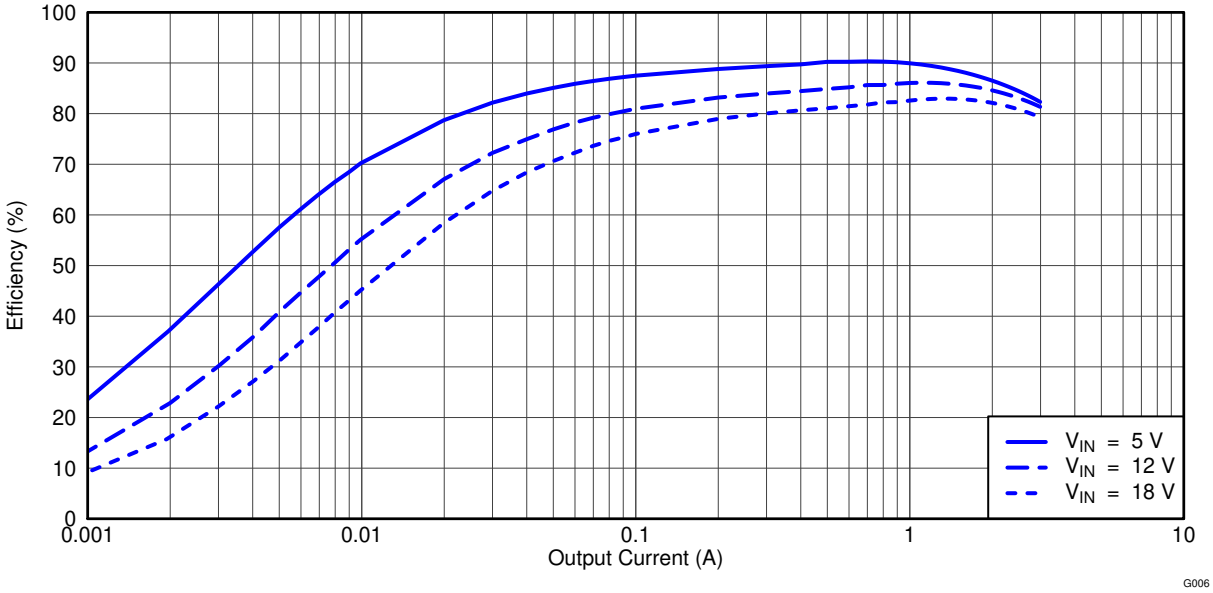


Figure 4-4. TPS54394EVM Converter 2 Light Load Efficiency

Copyright © 2022 Texas Instruments Incorporated

4.4 Load Regulation

4.4.1 Load Regulation of Converter 1

The load regulation for converter 1 on the TPS54394EVM is shown in Figure 4-5. On the EVM, the load regulation of converter 1 is independent on the load of converter 2.

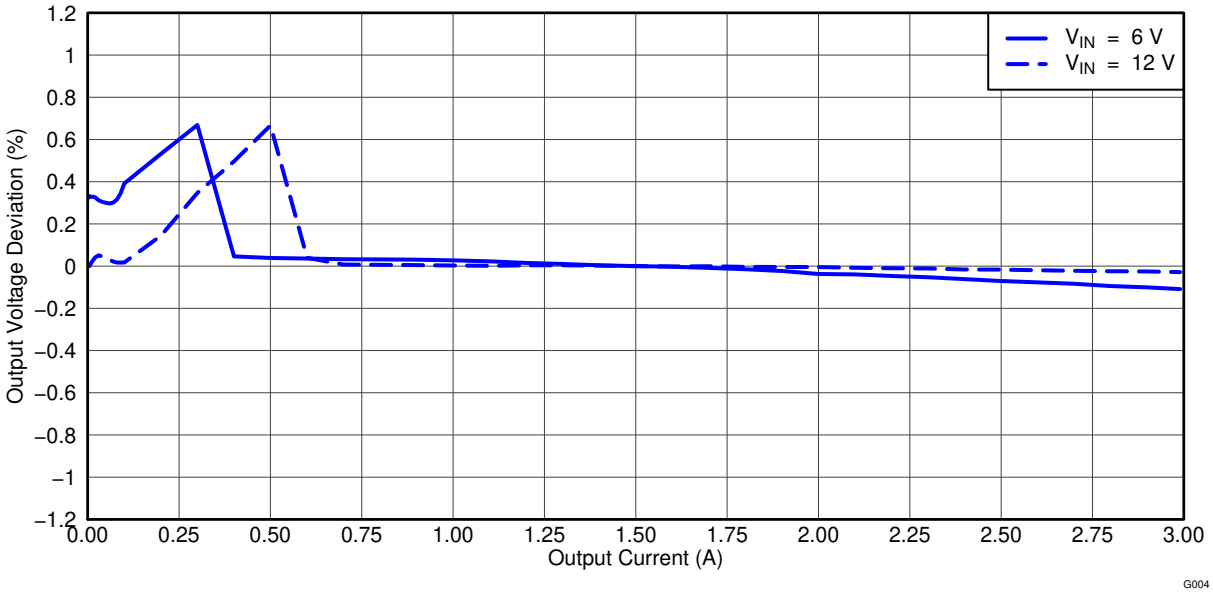


Figure 4-5. TPS54394EVM Converter 1 Load Regulation

4.4.2 Load Regulation of Converter 2

The load regulation for converter 2 on the TPS54394EVM is shown in Figure 4-6. For 5-V input voltage, converter 2 shows on the EVM some dependency on the load of converter 1.

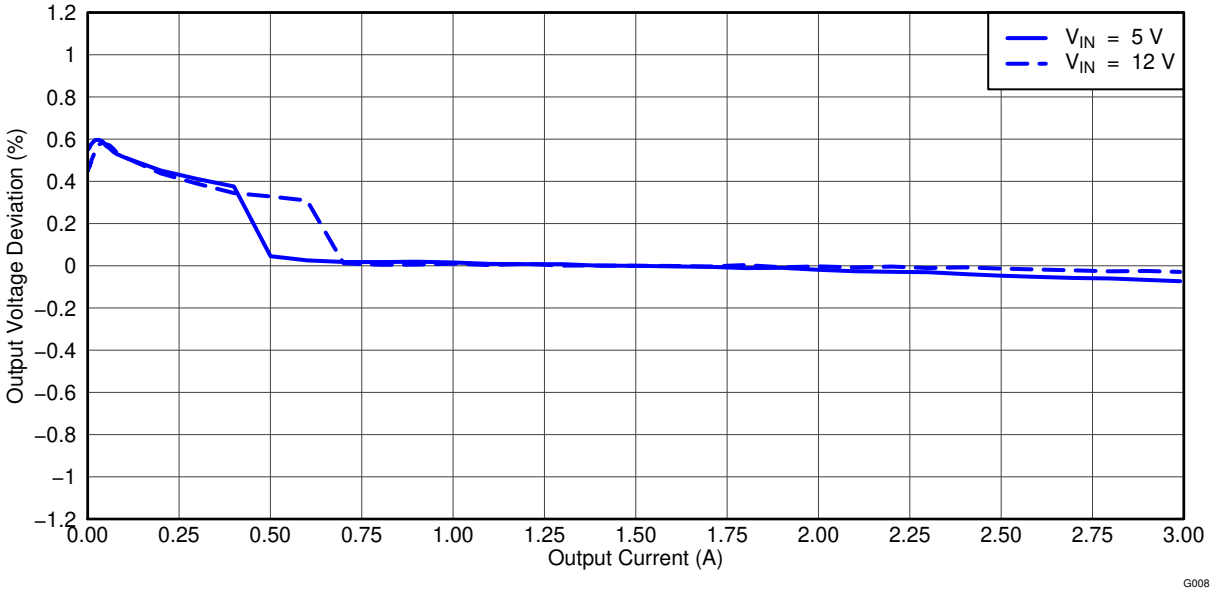


Figure 4-6. TPS54394EVM Converter 2 Load Regulation

Copyright © 2022 Texas Instruments Incorporated

4.5 Line Regulation

4.5.1 Line Regulation Converter 1

The line regulation of converter 1 on the TPS54394EVM is shown in Figure 4-7.

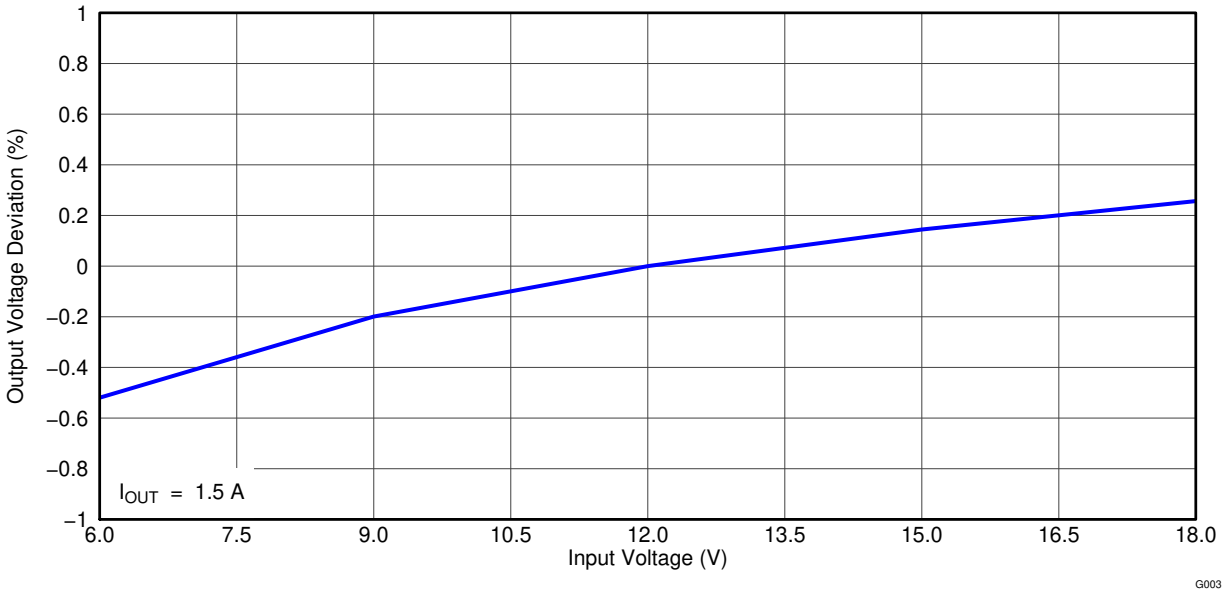


Figure 4-7. TPS54394EVM Converter 1 Line Regulation

4.5.2 Line Regulation Converter 2

The line regulation of converter 2 on the TPS54394EVM is shown in Figure 4-8.

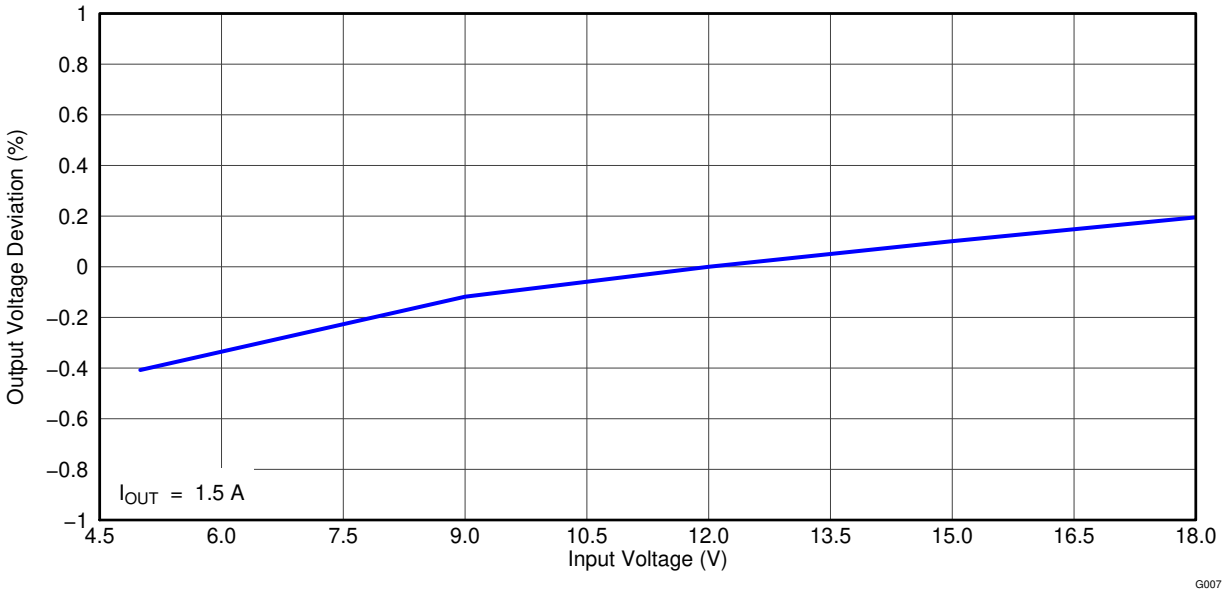


Figure 4-8. TPS54394EVM Converter 2 Line Regulation

Copyright © 2022 Texas Instruments Incorporated

4.6 Load Transient Response

4.6.1 Load Transient Response Converter 1

The response of converter 1 on the TPS54394EVM to a load transient is shown in Figure 4-9.

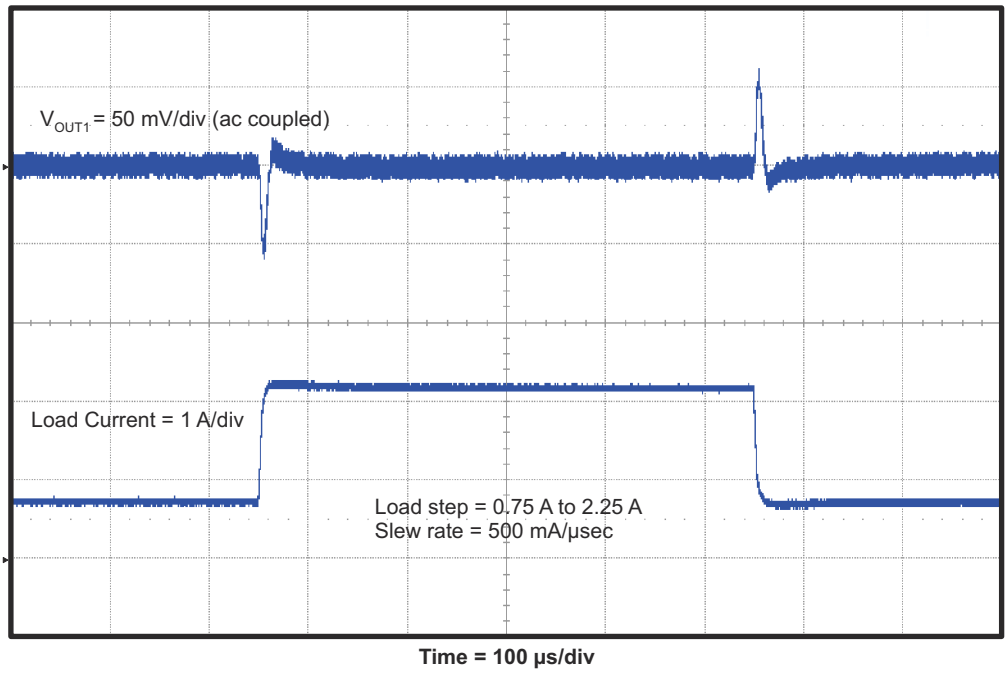


Figure 4-9. TPS54394EVM Converter 1 Load Transient Response

4.6.2 Load Transient Response Converter 2

The response of converter 2 on the TPS54394EVM to a load transient is shown in Figure 4-10.

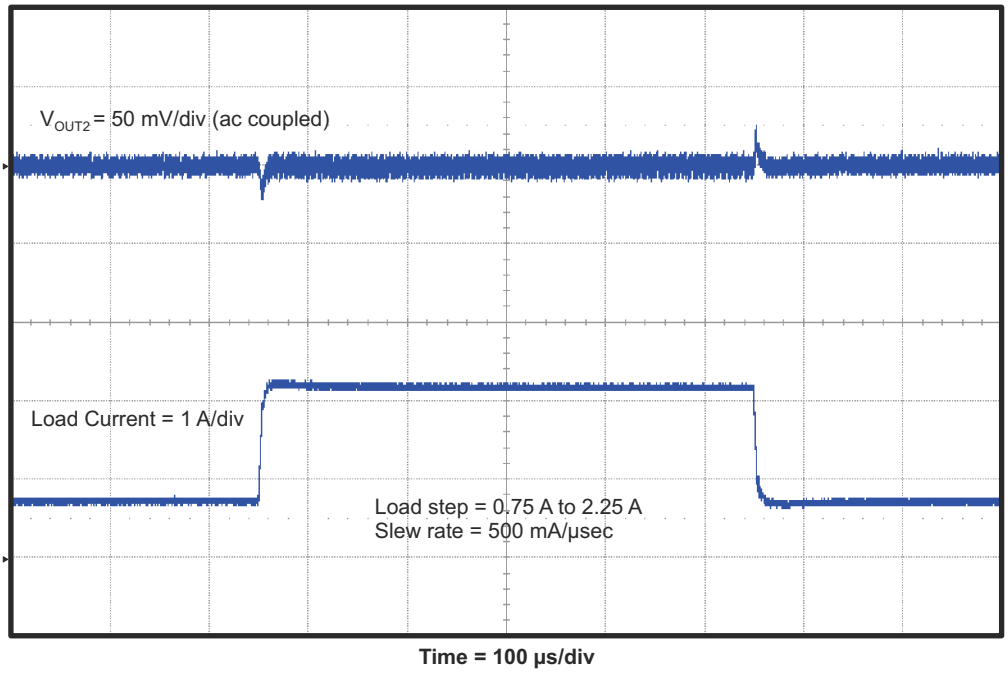


Figure 4-10. TPS54394EVM Converter 2 Load Transient Response

Copyright © 2022 Texas Instruments Incorporated

4.7 Output Voltage Ripple

4.7.1 Output Voltage Ripple Converter 1

The output voltage ripple of converter 1 on the TPS54394EVM is shown in Figure 4-11. The output current is the rated full load of 3 A.

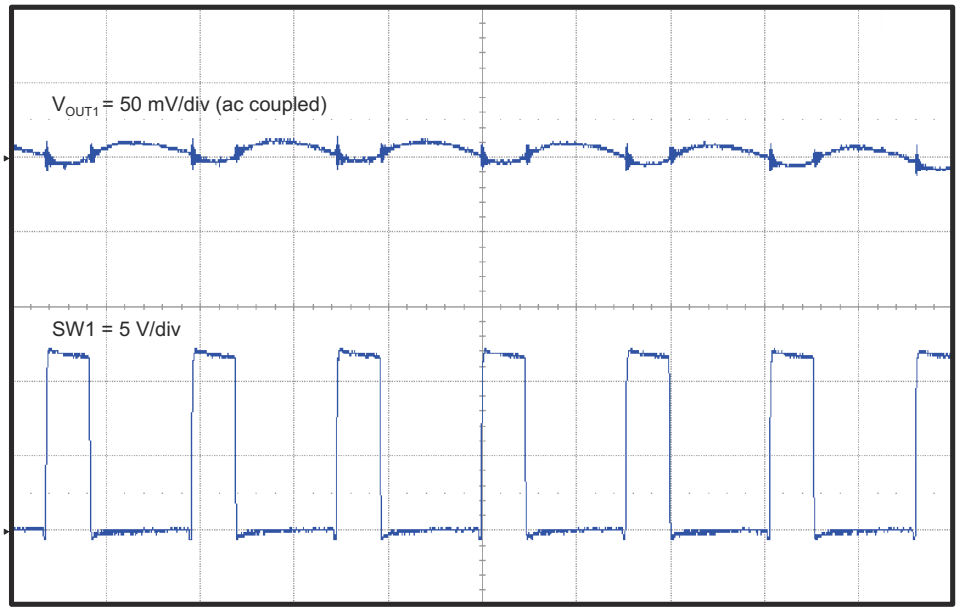


Figure 4-11. TPS54394EVM Converter 1 Output Voltage Ripple

The output voltage ripple of converter 1 on the TPS54394EVM during Eco-mode operation at no load is shown in Figure 4-12.

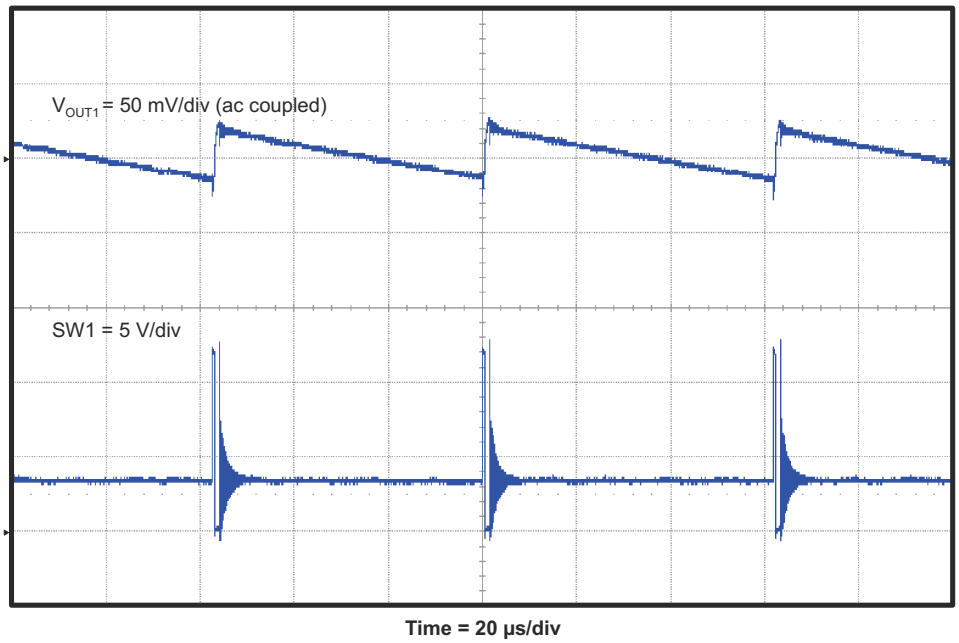


Figure 4-12. TPS54394EVM Converter 1 Eco-mode Output Voltage Ripple at No Load

Copyright © 2022 Texas Instruments Incorporated

4.7.2 Output Voltage Ripple Converter 2

The output voltage ripple of converter 2 on the TPS54394EVM is shown in Figure 4-13. The output current is the rated full load of 3 A.

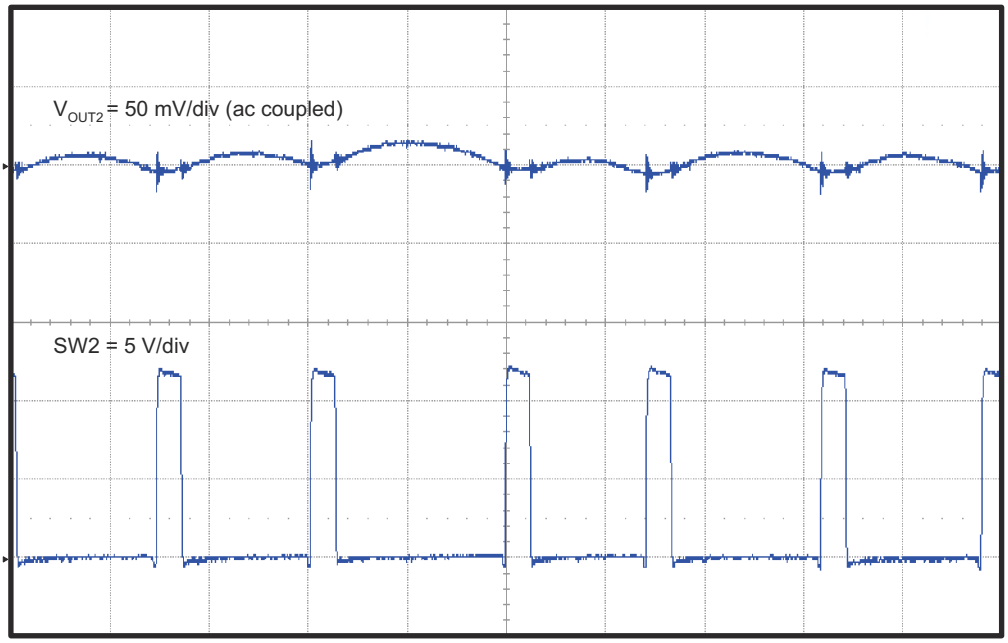


Figure 4-13. TPS54394EVM Converter 2 Output Voltage Ripple

The output voltage ripple of converter 2 on the TPS54394EVM during Eco-mode operation at no load is shown in Figure 4-14.

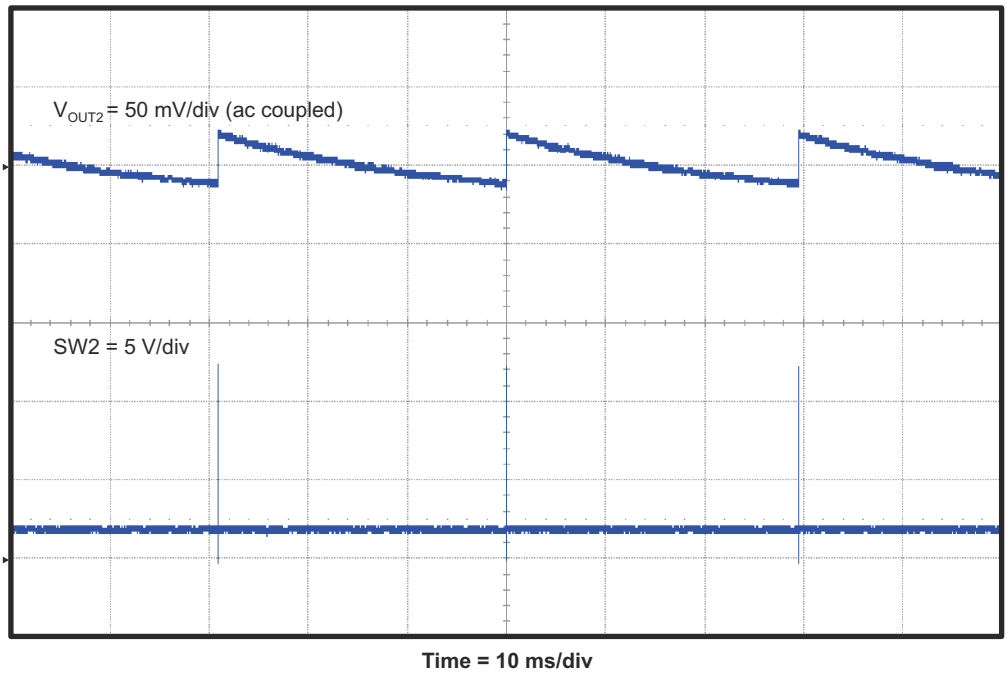


Figure 4-14. TPS54394EVM Converter 2 Eco-mode Output Voltage Ripple at No Load

Copyright © 2022 Texas Instruments Incorporated

4.8 Input Voltage Ripple

The TPS54394EVM input voltage ripple is shown in Figure 4-15. The output currents are the rated full load currents of 3-A each channel.

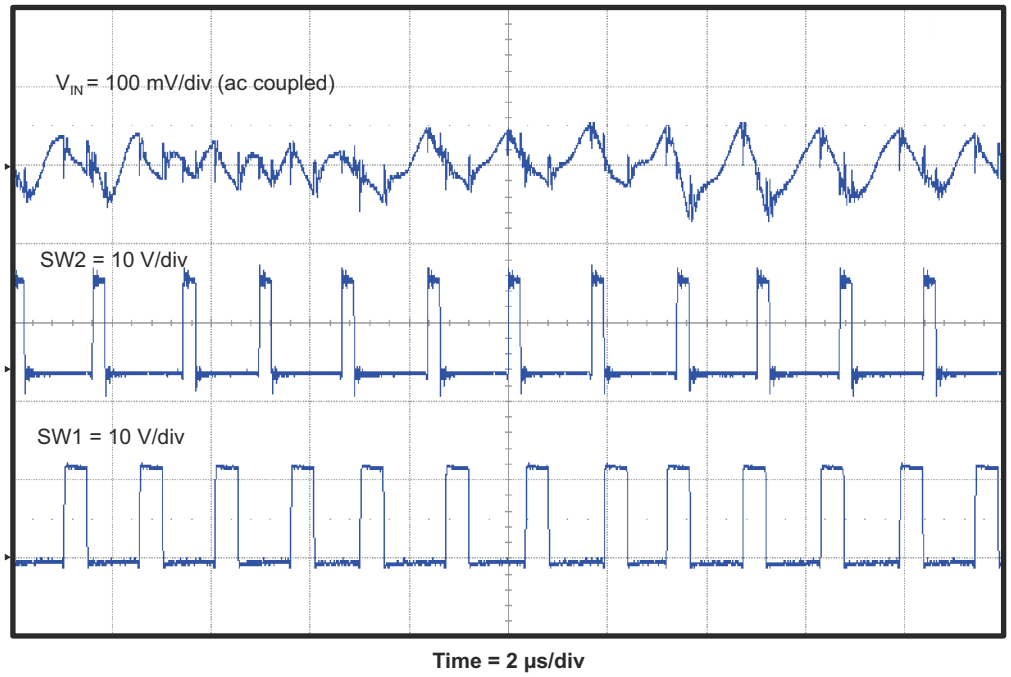


Figure 4-15. TPS54394EVM Input Voltage Ripple

Copyright © 2022 Texas Instruments Incorporated

4.9 Start-Up

4.9.1 Converter 1 Start-Up

The TPS54394EVM start-up waveform of converter 1 relative to V_{IN} is shown in Figure 4-16.

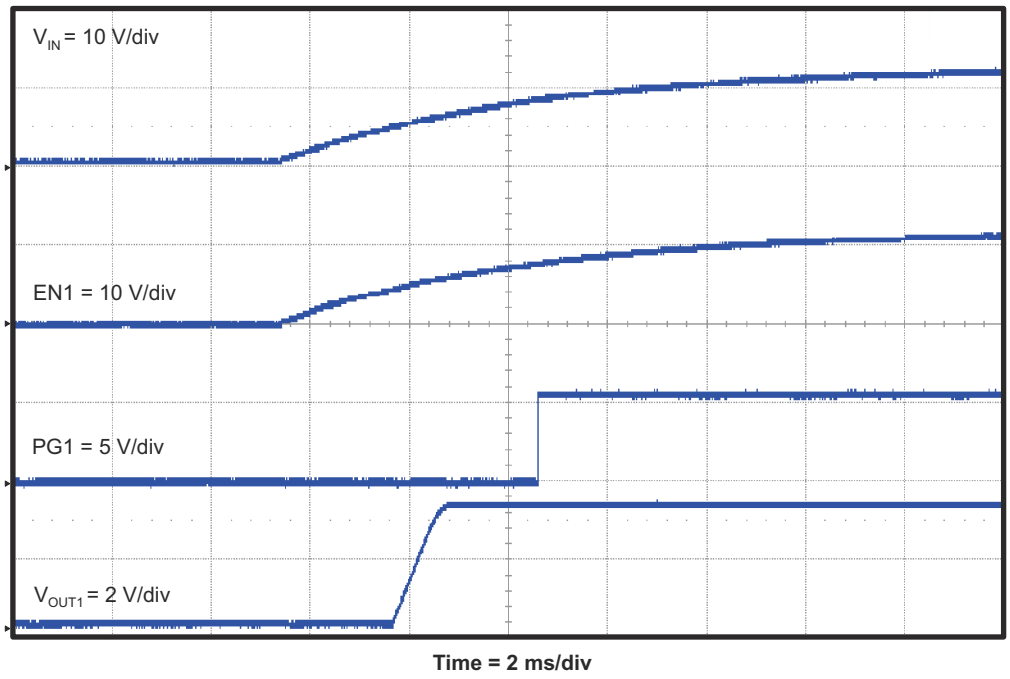


Figure 4-16. TPS54394EVM Converter 1 Start-Up Relative to V_{IN}

The TPS54394EVM start-up waveform of converter 1 relative to EN1 is shown in Figure 4-17.

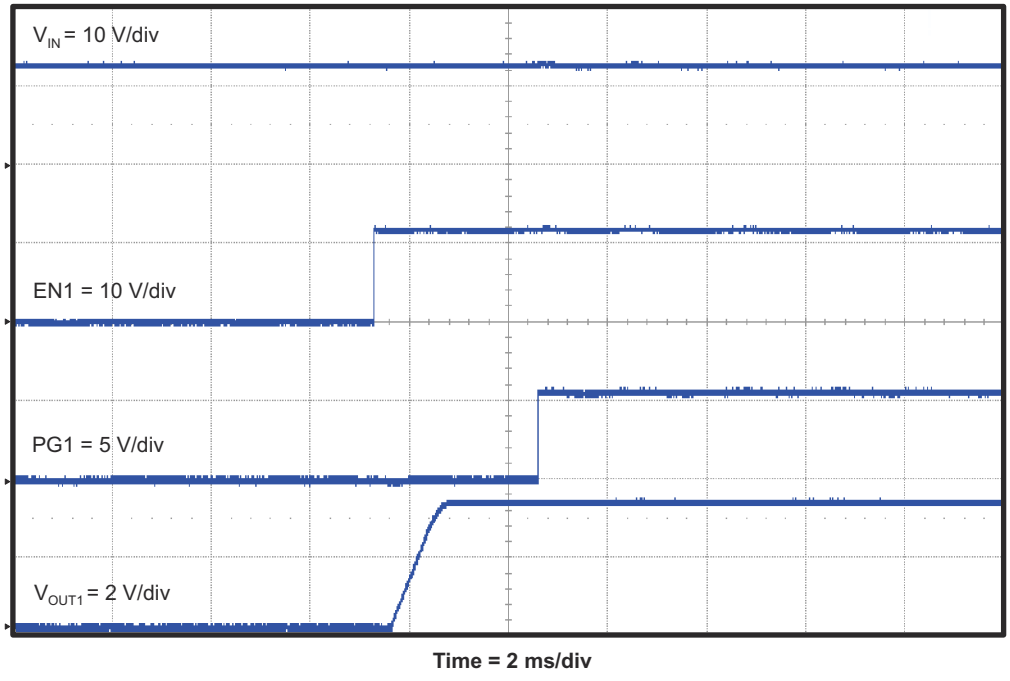


Figure 4-17. TPS54394EVM Start-Up Relative to EN1

Copyright © 2022 Texas Instruments Incorporated

4.9.2 Converter 2 Start-Up

The TPS54394EVM start-up waveform of converter 2 relative to V_{IN} is shown in Figure 4-18.

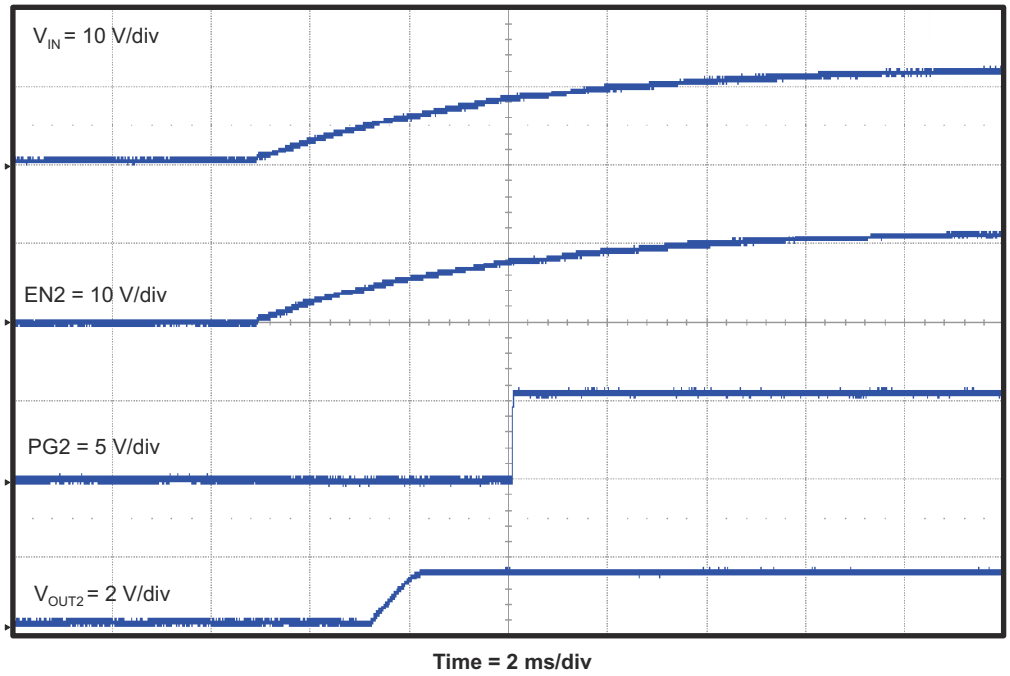


Figure 4-18. TPS54394EVM Converter 2 Start-Up Relative to V_{IN}

The TPS54394EVM start-up waveform of converter 2 relative to EN2 is shown in Figure 4-19.

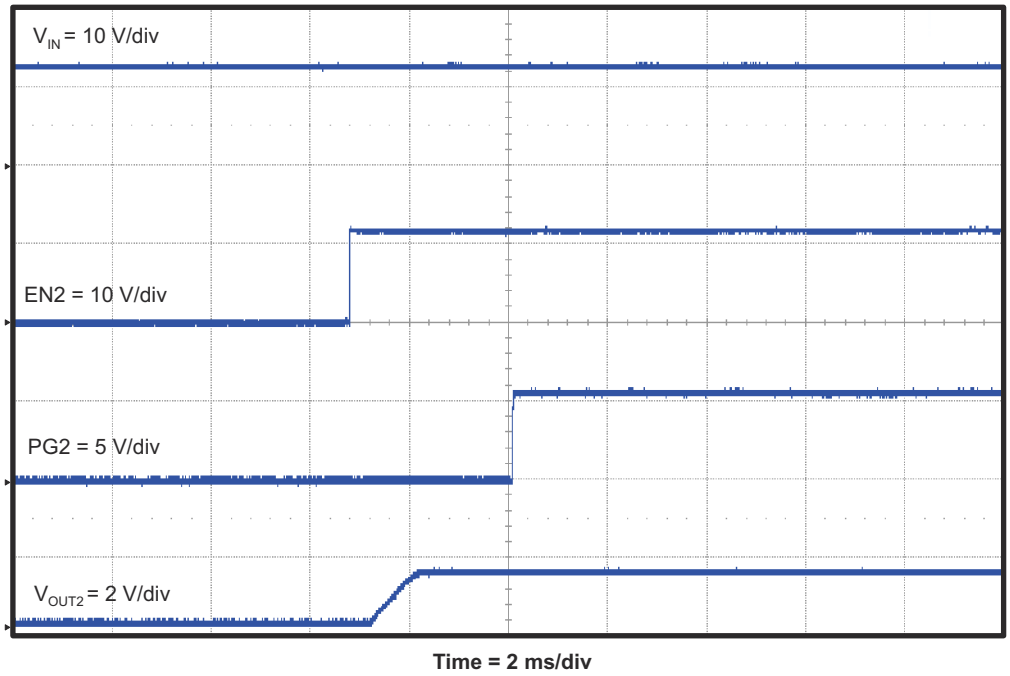


Figure 4-19. TPS54394EVM Start-Up Relative to EN2

Copyright © 2022 Texas Instruments Incorporated

5 Board Layout

This section provides a description of the TPS54394EVM, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS54394EVM is shown in Figure 5-1 through Figure 5-6. The top layer contains the main power traces for VIN and VOUTx. Also on the top layer are connections for the pins of the TPS54394 and a large area filled with ground. Many of the signal traces also are located on the top side. The input decoupling capacitors are located as close to the IC as possible. The input and output connectors, test points, and all of the assembled components are located on the top side. An analog ground (GND) area is provided on the top side. Analog ground (GND) and power ground (PGND) are connected at a single point on the top layer near the IC. The other layers are primarily power ground but the bottom layer has some traces to connect the test points for SSx and ENx.

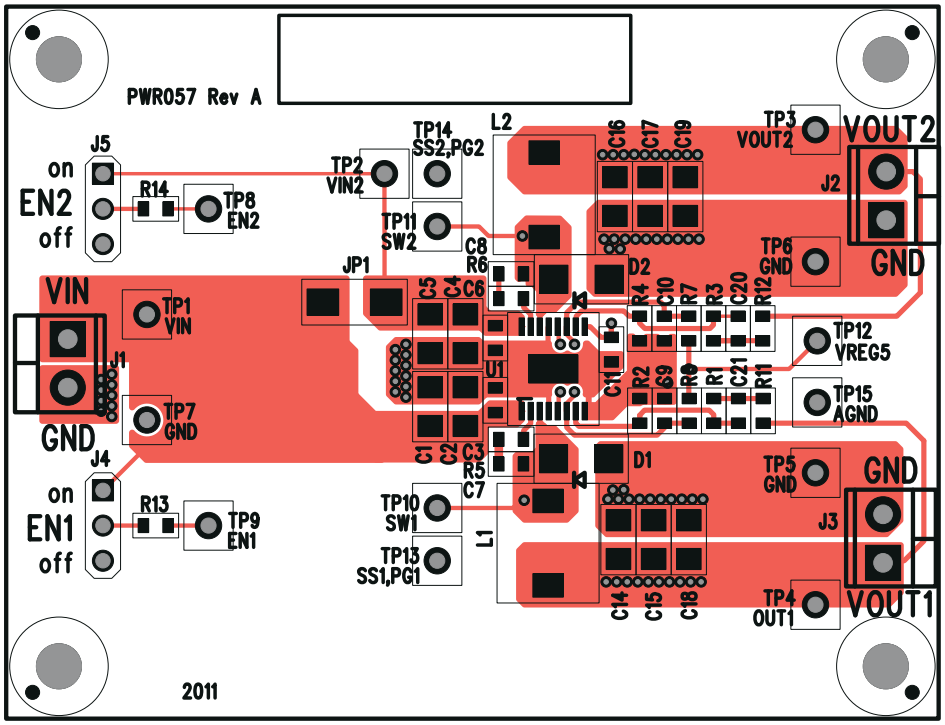


Figure 5-1. Top Assembly

Copyright © 2022 Texas Instruments Incorporated

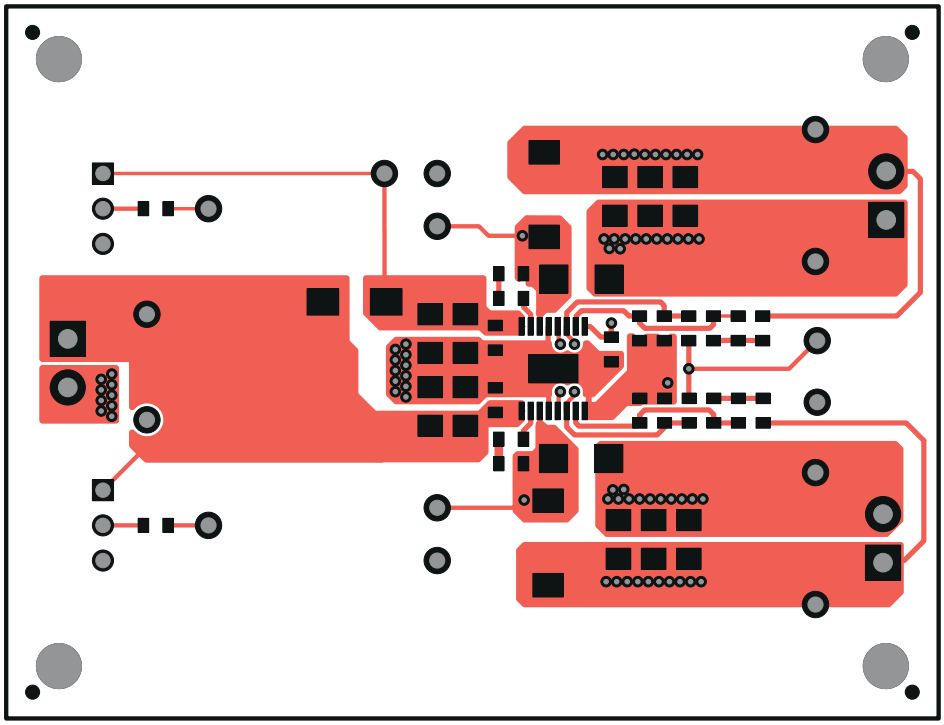


Figure 5-2. Top Layer

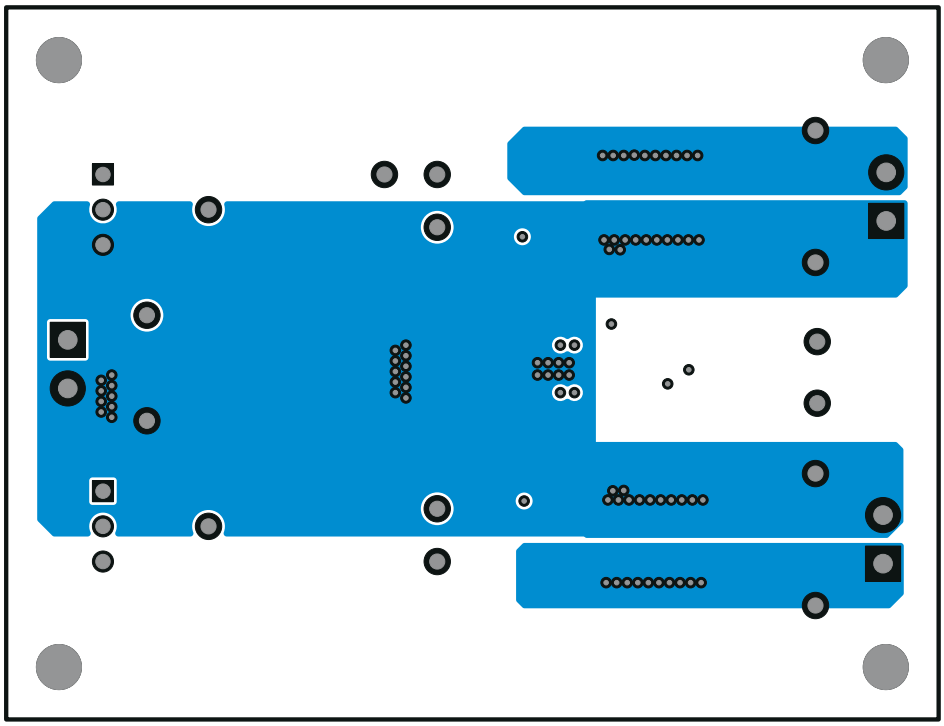


Figure 5-3. Internal 1 Layer

Copyright © 2022 Texas Instruments Incorporated

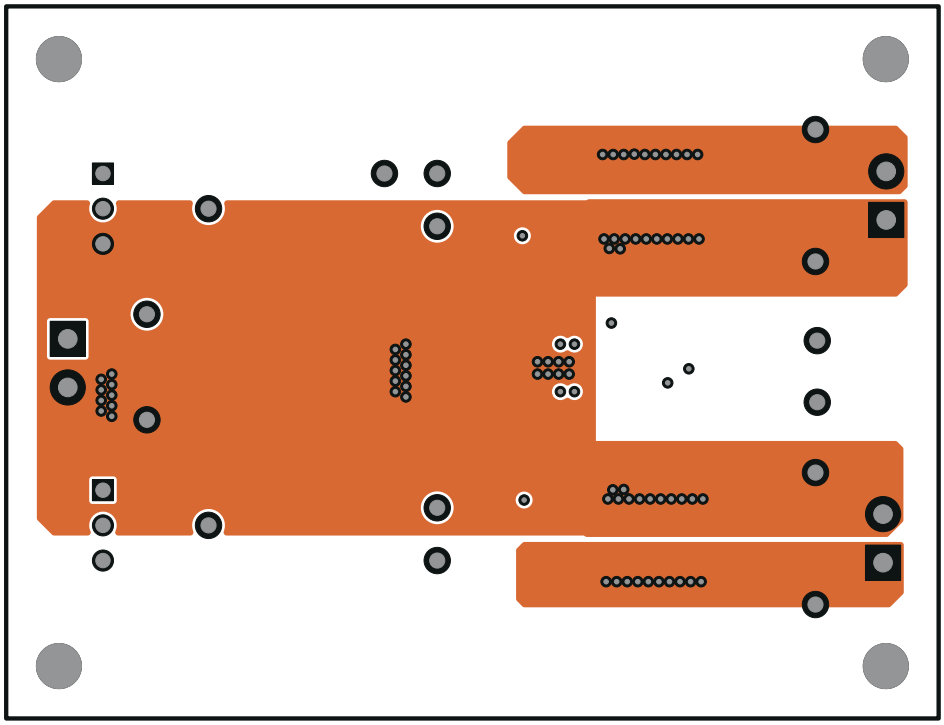


Figure 5-4. Internal 2 Layer

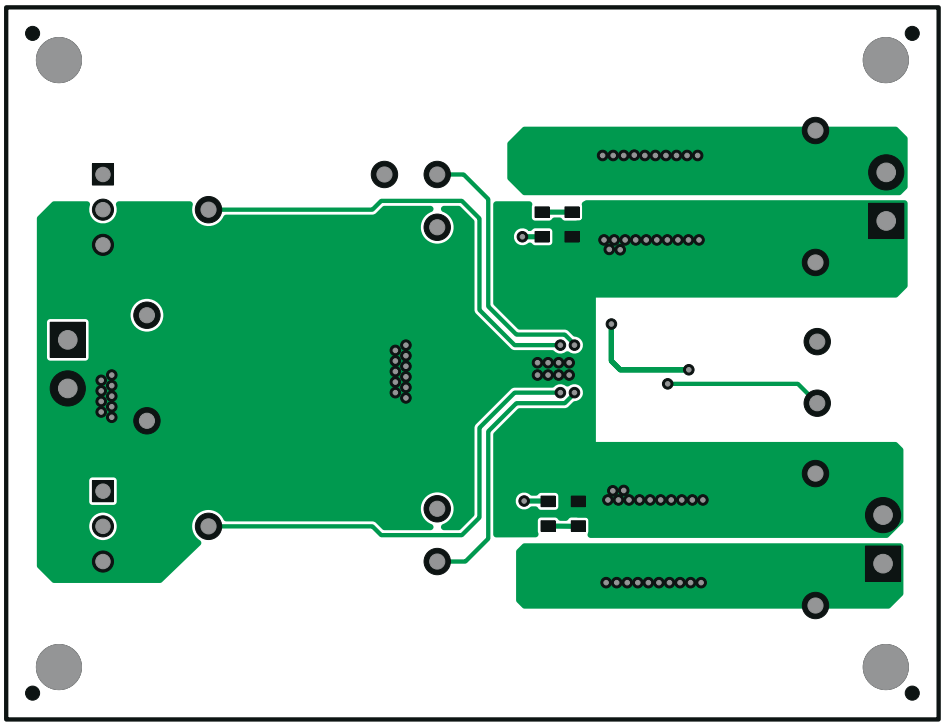


Figure 5-5. Bottom Layer

Copyright © 2022 Texas Instruments Incorporated

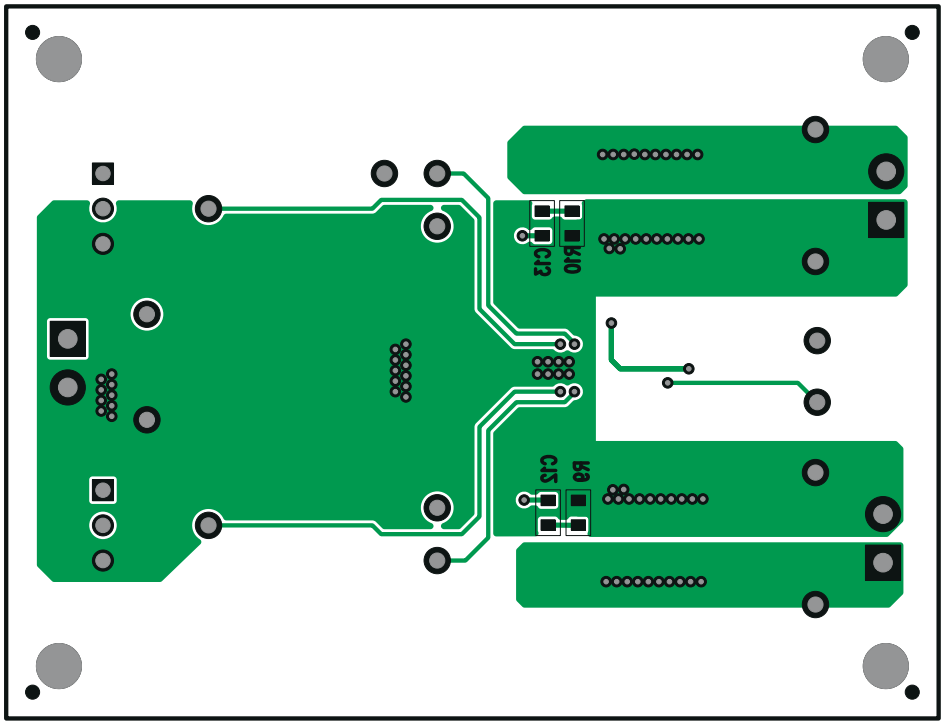


Figure 5-6. Bottom Assembly

Copyright © 2022 Texas Instruments Incorporated

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS54394EVM.

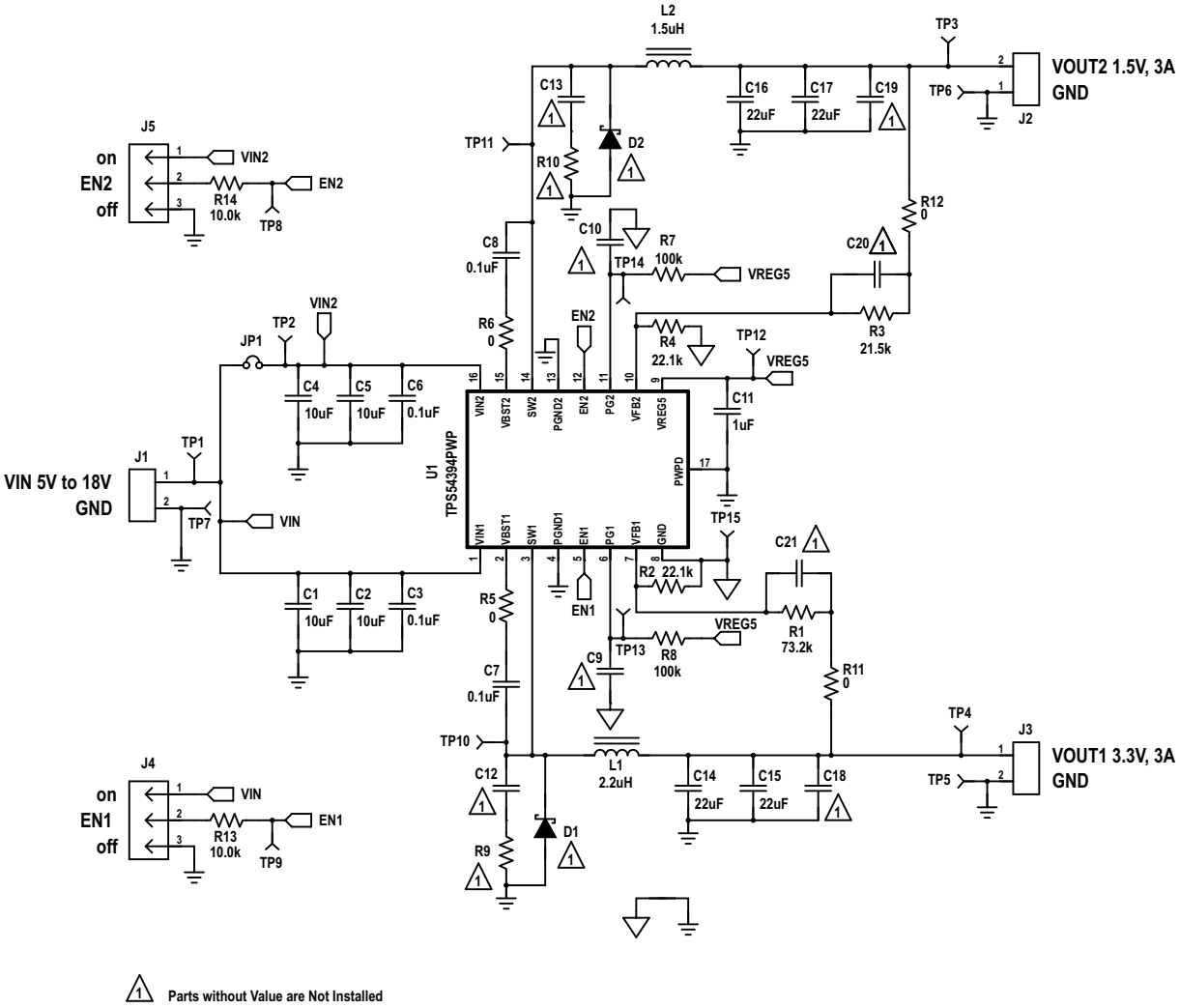


Figure 6-1. TPS54394EVM Schematic Diagram

Copyright © 2022 Texas Instruments Incorporated

6.2 Bill of Materials

Table 6-1. Bill of Materials

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
1	C11	1 µF	Capacitor, ceramic, 16 V, X7R, 10%	0603	GRM188R71C105KA12	Murata
4	C1–2, C4–5	10 µF	Capacitor, ceramic, 25 V, X7R, 10%	1206	GRM31CR71E106KA12	Murata
0	C12–13	open	Capacitor, ceramic, 50 V, X7R, 10%	0603	GRM188R71H104KA93	Murata
4	C14–17	22 µF	Capacitor, ceramic, 6.3 V, X7R, 10%	1206	GRM31CR70J226KE19	Murata
0	C18–19	open	Capacitor, ceramic, 6.3 V, X7R, 10%	1206		
0	C20–21	open	Capacitor, ceramic, 50 V, X7R, 10%	0603	Std	Std
4	C3, C6–8	0.1 µF	Capacitor, ceramic, 50 V, X7R, 10%	00603	GRM188R71H104KA93	Murata
0	C9–10	open	Capacitor, ceramic, 50 V, X7R, 10%	0603	Std	Std
0	D1–2	open	Diode, Schottky	SMA	STD	STD
1	L1	2.2 µH	Inductor, power line, magnetic shielded, ±30%, 4.3 A	6.9 × 7.2 mm	SPM6530-2R2M	TDK
1	L2	1.5 µH	Inductor, power line, magnetic shielded, ±30%, 4.1 A	6.9 × 7.2 mm	SPM6530-1R5M	TDK
1	R1	73.2 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R11–12	0 Ω	Resistor, chip, 1/16W, 5%	0603	STD	STD
2	R13–14	10.0 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R2, R4	22.1 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
1	R3	21.5 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R5–6	0 Ω	Resistor, chip, 1/16W, 1%	0603	STD	STD
2	R7–8	100 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
0	R9–10	open	Resistor, chip, 1/16W, 1%	0603	STD	STD
1	U1	TPS54394PWP	IC, 3A/3A , dual output fully synchronous buck converter with integrated FET	TSSOP	TPS54394PWP	TI

C14-C19 must be replaced with capacitors which have a higher voltage rating when the output voltage is set above 4V.

6.3 Reference

1. Texas Instruments, *TPS54394, 3-A Dual Channel Synchronous Step-Down Switcher With Integrated FETs Data Sheet*

Copyright © 2022 Texas Instruments Incorporated

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2012) to Revision A (September 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title.	3
• Edited the user's guide for clarity.	3

Copyright © 2022 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated