General Description

The 8741004I is a high performance Differential-to-LVDS/0.7V Differential Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 8741004I has 3 PLL bandwidth modes: 200kHz, 600kHz and 2MHz. The 200kHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 600kHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. The 2MHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. Because some 2.5Gb serdes have x20 multipliers while others have x25 multipliers, the 8741004I can be set for 1:1 mode or 5/4 multiplication mode (i.e. 100MHz input/125MHz output) using the F_SEL pins.

The 8741004I uses IDT's 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 24 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

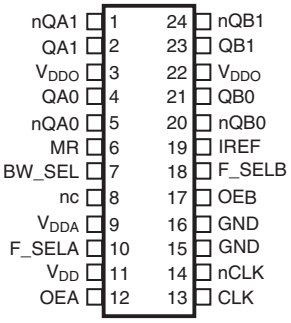
PLL Bandwidth

BW_SEL
0 = PLL Bandwidth: ~200kHz
Float = PLL Bandwidth: ~600kHz (default)
1 = PLL Bandwidth: ~2MHz

Features

- Two LVDS and two 0.7V differential output pairs
  Bank A has two LVDS output pairs and
  Bank B has two 0.7V differential output pairs
- One differential clock input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 160MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 35ps (maximum)
- Full 3.3V operating supply
- Three bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- -40°C to 85°C ambient operating temperature
- Available in lead-free packages

Pin Assignment



24-Lead TSSOP, E-Pad
4.40mm x 7.8mm x 0.925mm
package body
G Package
Top View

Block Diagram

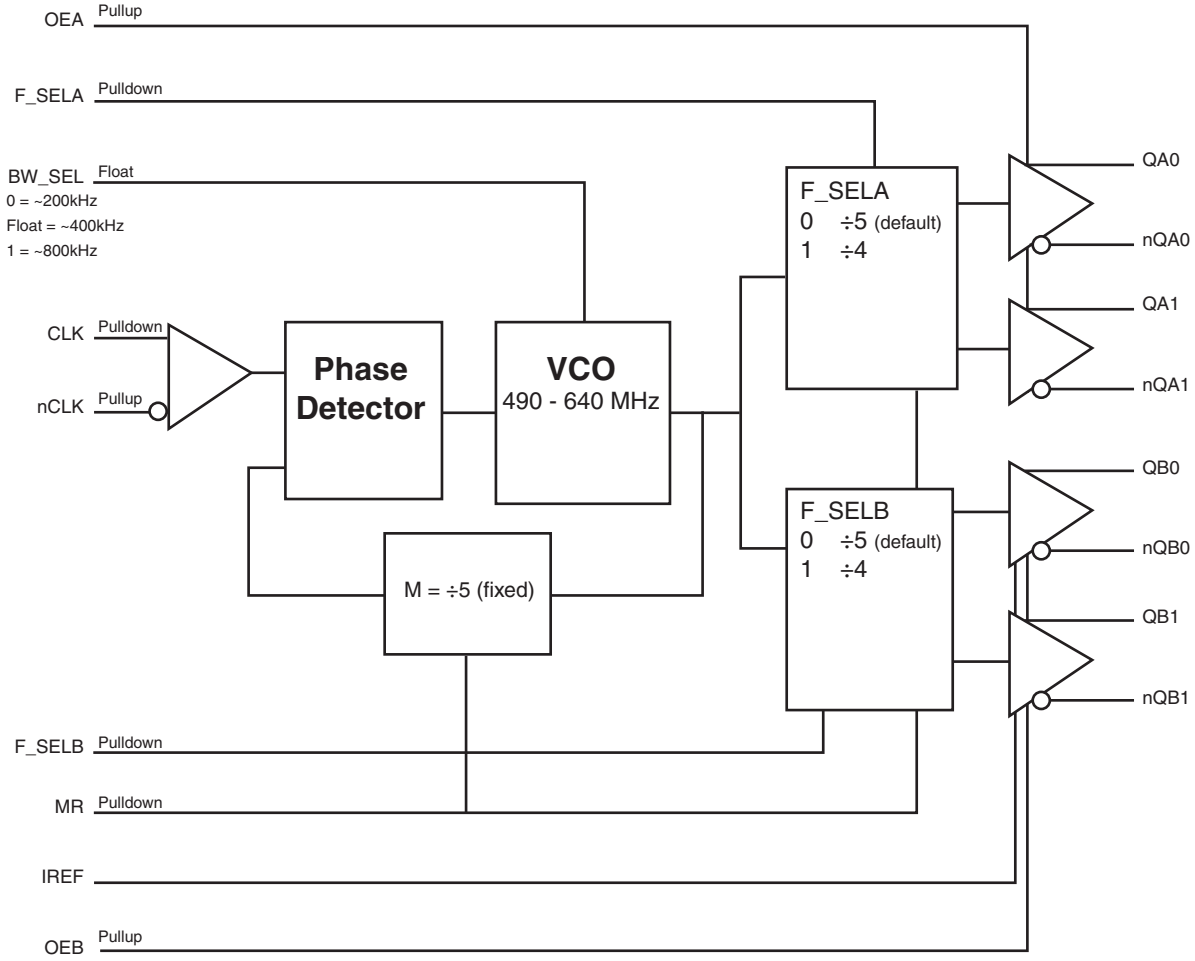


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQA1, QA1	Output		Differential output pair. LVDS interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
6	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Q[Ax:Bx] to go LOW and the inverted outputs nQ[Ax:Bx] to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	BW_SEL	Input	Pullup/ Pulldown	PLL Bandwidth input. LVCMOS/LVTTL interface levels. See Table 3B.
8	nc	Unused		No connect.
9	V_{DDA}	Power		Analog supply pin.
10	F_SELA	Input	Pulldown	Frequency select pins for QAx/nQAx outputs. LVCMOS/LVTTL interface levels. See Table 3C.
11	V_{DD}	Power		Core supply pin.
12	OEA	Input	Pullup	Output enable for QAx pins. When HIGH, QAx/nQAx outputs are enabled. When LOW, the QAx/nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
13	CLK	Input	Pulldown	Non-inverting differential clock input.
14	nCLK	Input	Pullup	Inverting differential clock input.
15, 16	GND	Power		Power supply ground.
17	OEB	Input	Pullup	Output enable for QBx pins. When HIGH, QBx/nQBx outputs are enabled. When LOW, the QBx/nQBx outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
18	F_SELB	Input	Pulldown	Frequency select pins for QBx/nQBx outputs. LVCMOS/LVTTL interface levels. See Table 3C.
19	IREF	Input		A fixed precision resistor (RREF = 475Ω) from this pin to ground provides a reference current used for differential current-mode QB0/nQB0 clock outputs.
20, 21	nQB0, QB0	Output		Differential output pair. HCSL interface levels.
23, 24	QB1, nQB1	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Enable Function Table

Inputs		Outputs	
OEA	**OEB**	**QA[0:1]/nQA[0:1]**	**QB[0:1]/nQB[0:1]**
0	0	Hi-Z	Hi-Z
1	1	Enabled	Enabled

Table 3B. PLL Bandwidth Function Table

Input	
BW_SEL	**PLL Bandwidth**
0	~200kHz
Float	~600kHz (default)
1	~2MHz

Table 3C. Frequency Select Table

Inputs	
F_SEL[A, B]	**Divider**
0	÷5 (default)
1	÷4

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	32.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				45	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				80	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OEA, OEB, MR, F_SELA, F_SELB		2		V_{DD} + 0.3	V
		BW_SEL		V_{DD} – 0.3		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OEA, OEB, MR, F_SELA, F_SELB		-0.3		0.8	V
		BW_SEL		-0.3		+0.3	V
V_{IM}	Input Mid Voltage	BW_SEL		V_{DD}/2 – 0.1		V_{DD}/2 + 0.1	V
I_{IH}	Input High Current	F_SELA, F_SELB, MR, BW_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
		OEA, OEB	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	MR, F_SELA, F_SELB,	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		OEA, OEB, BW_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V			150	µA
		nCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, NOTE 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		290	390	490	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2	1.35	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

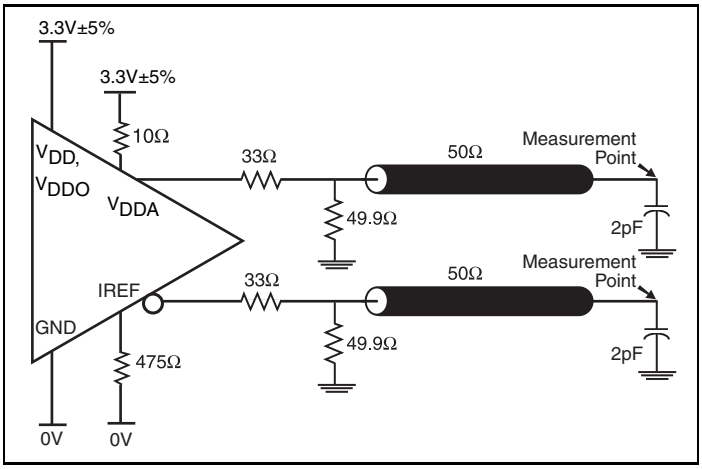
AC Electrical Characteristics

Table 5. 0.7V Differential AC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

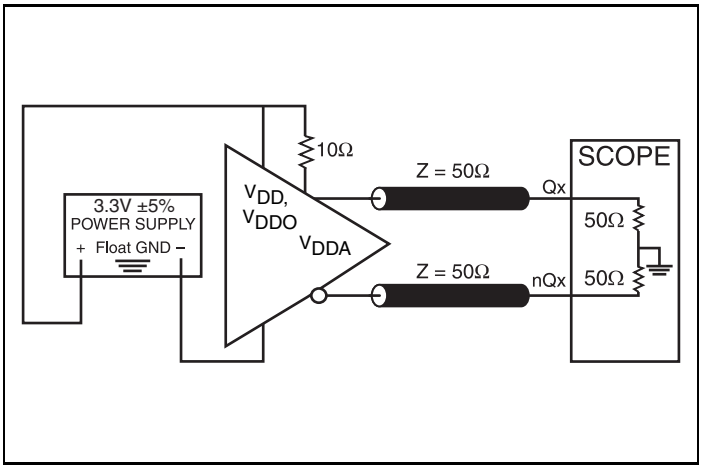
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			98		160	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1					35	ps
*t*sk(b)	Bank Skew, NOTE 2					30	ps
V_{HIGH}	Output Voltage High	QBx/nQBx		530		870	mV
V_{LOW}	Output Voltage Low	QBx/nQBx		-150			mV
V_{OVS}	Max. Voltage, Overshoot	QBx/nQBx				V_{HIGH} + 0.35	V
V_{UDS}	Min. Voltage, Undershoot	QBx/nQBx		-0.3			V
V_{rb}	Ringback Voltage	QBx/nQBx				0.2	V
V_{CROSS}	Absolute Crossing Voltage	QBx/nQBx	@ 0.7V Swing	250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges	QBx/nQBx	@ 0.7V Swing			140	mV
t_R / t_F	Output Rise/Fall Time	QBx/nQBx	measured between 0.175V to 0.525V	175		700	ps
		QAx/nQAx	20% to 80%	250		600	ps
Δt_R / Δt_F	Rise/Fall Time Variation	QBx/nQBx				125	ps
t_{RFM}	Rise/Fall Matching	QBx/nQBx				20	%
odc	Output Duty Cycle			48		52	%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

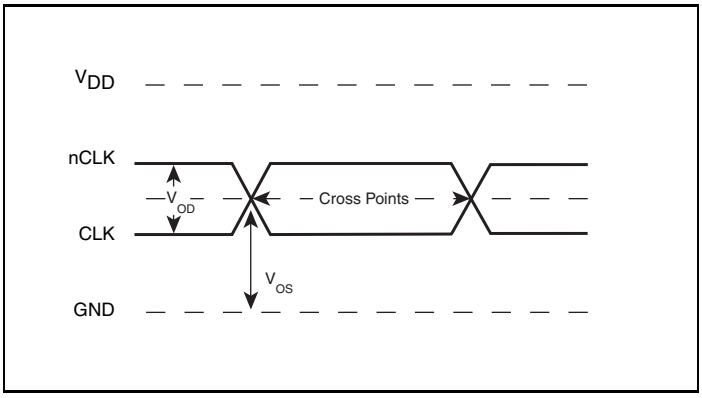
Parameter Measurement Information



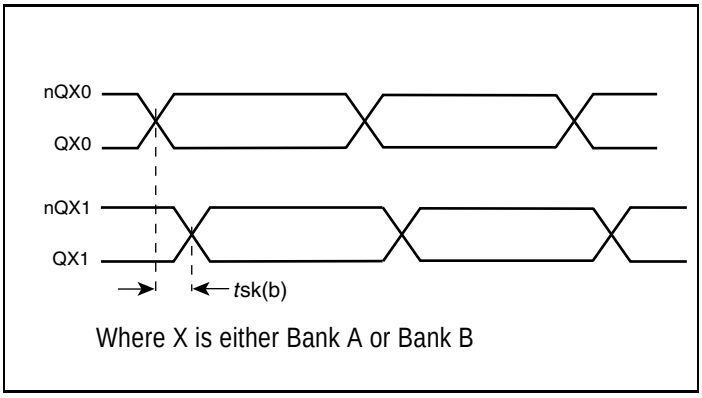
3.3V HCSL Output Load AC Test Circuit



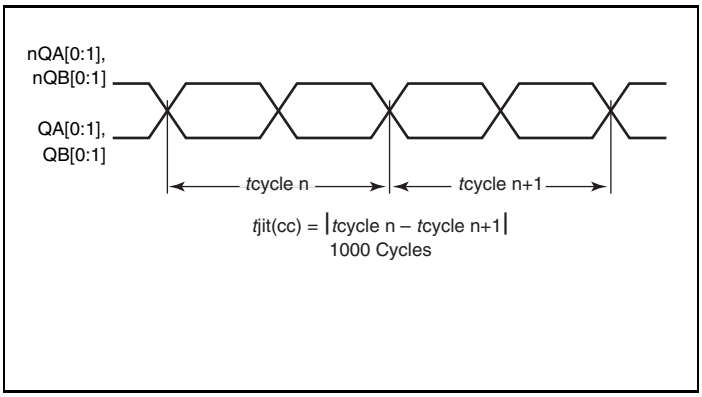
3.3V LVDS Output Load AC Test Circuit



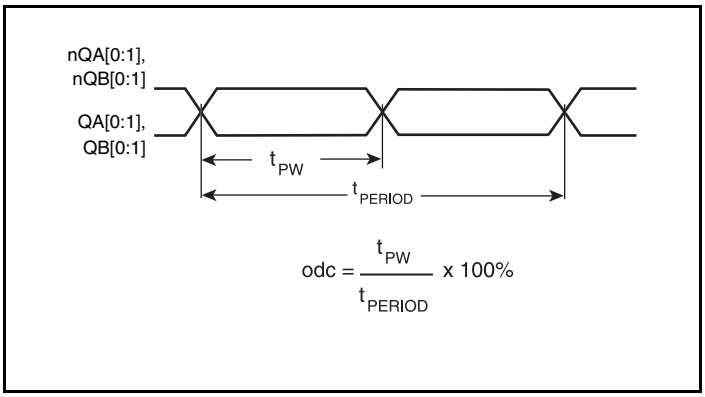
Differential Input Level



Bank Skew

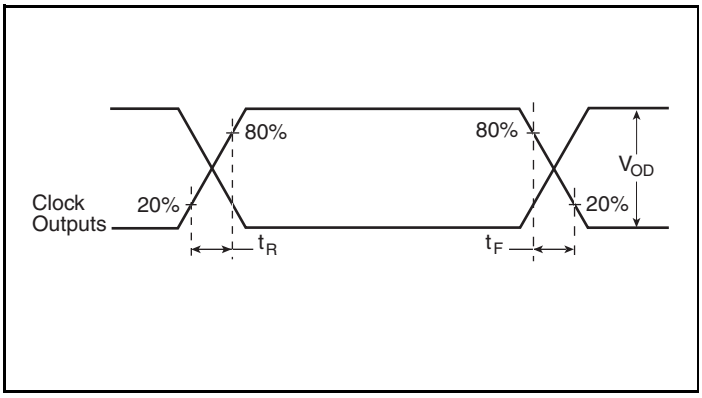


Cycle-to-Cycle Jitter

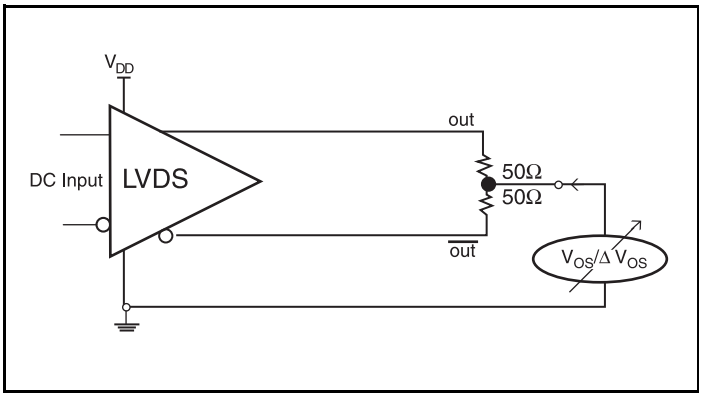


LVDS Output Duty Cycle/Pulse Width/Period

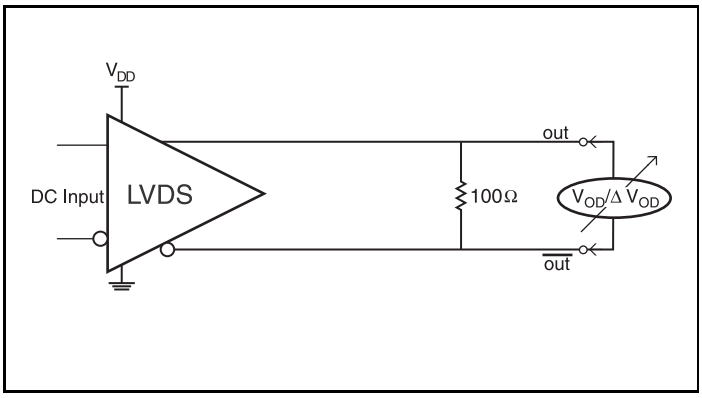
Parameter Measurement Information, continued



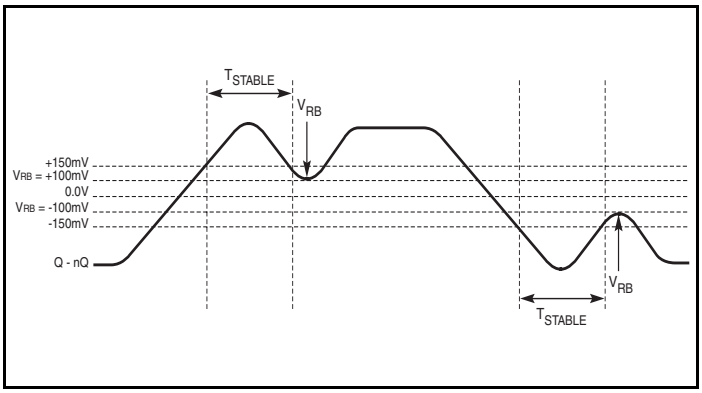
LVDS Output Rise/Fall Time



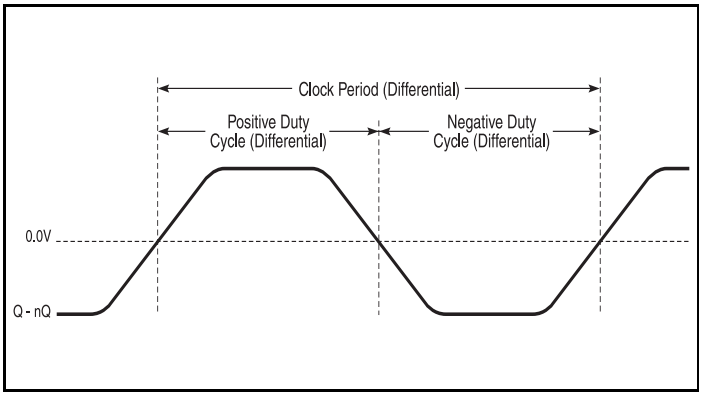
Offset Voltage Setup



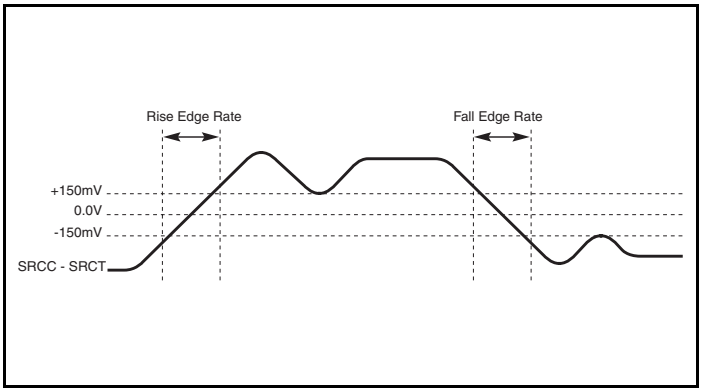
Differential Output Voltage Setup



Differential Measurement Points for Ringback

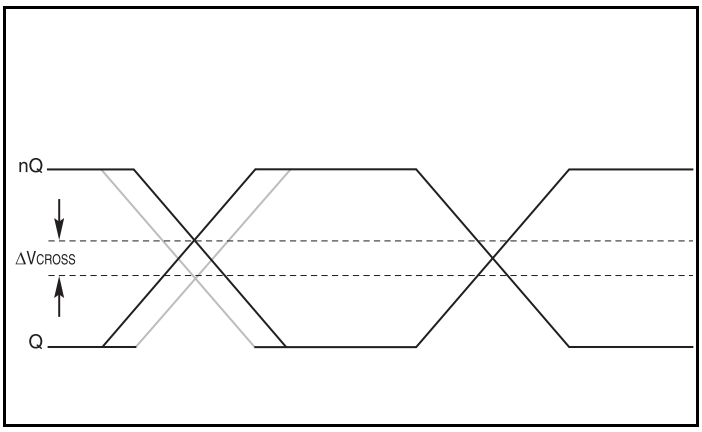


Differential Measurement Points for Duty Cycle/Period

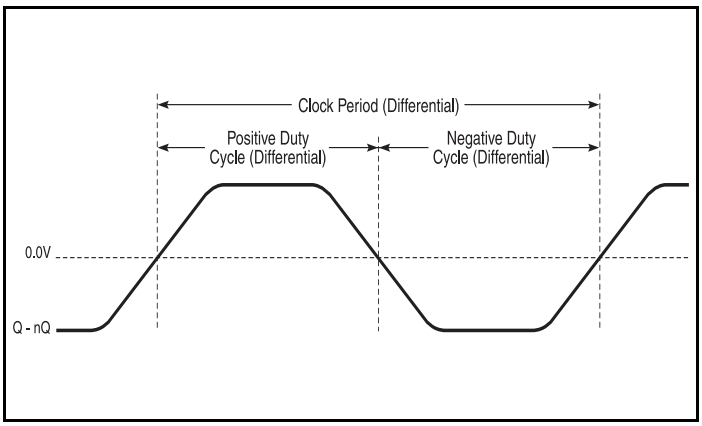


HCSL Differential Measurement Points for Rise/Fall Time

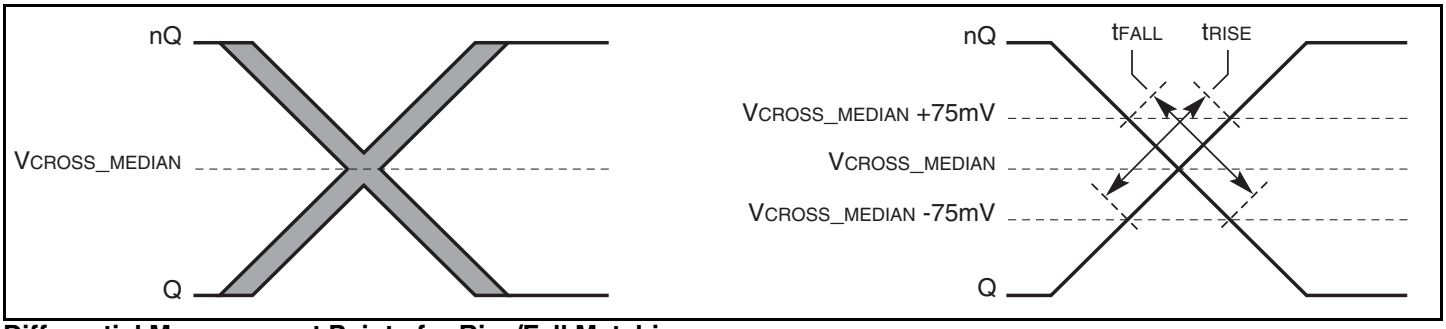
Parameter Measurement Information, continued



Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Duty Cycle/Period



Differential Measurement Points for Rise/Fall Matching

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8741004I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

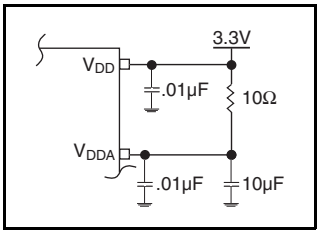


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

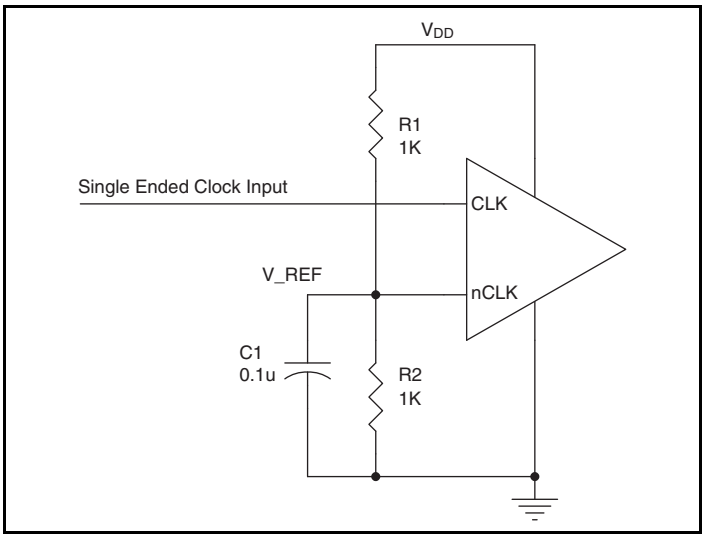


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

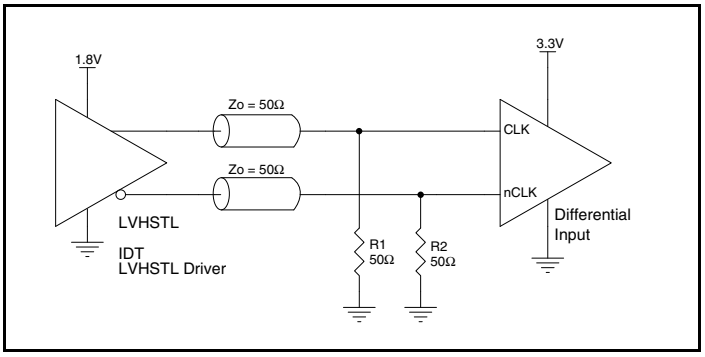


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

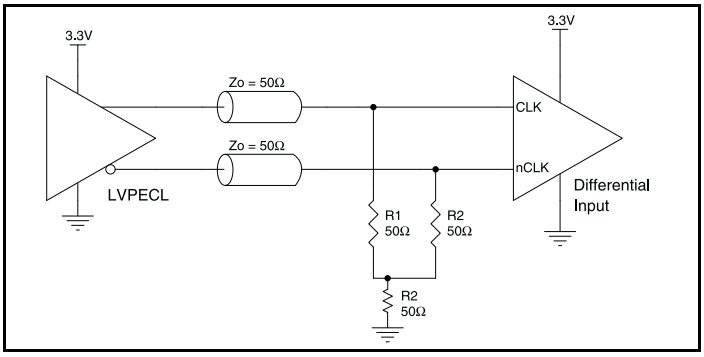


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

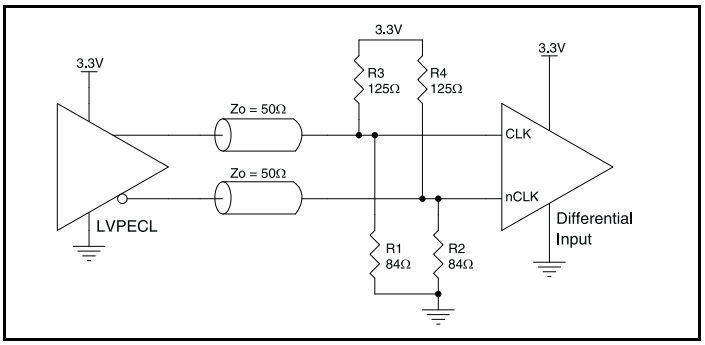


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

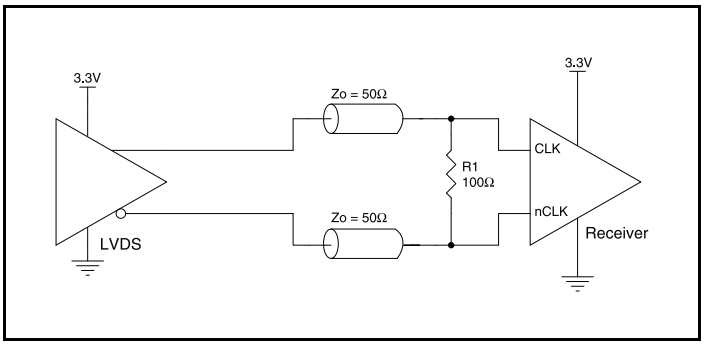


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

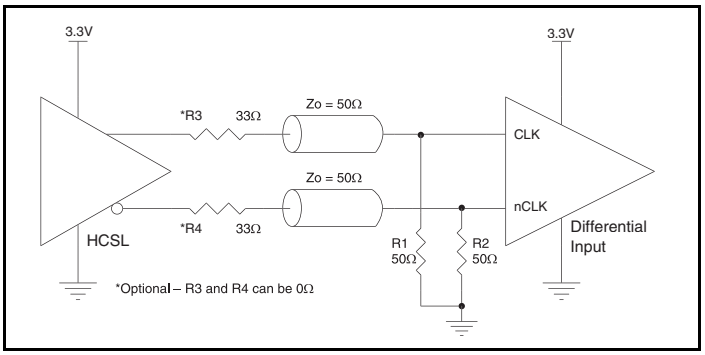


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

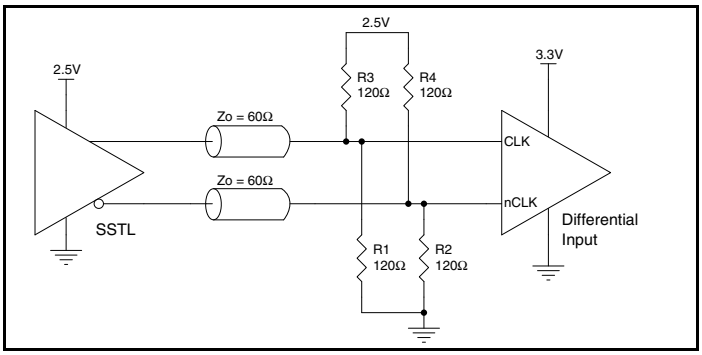


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

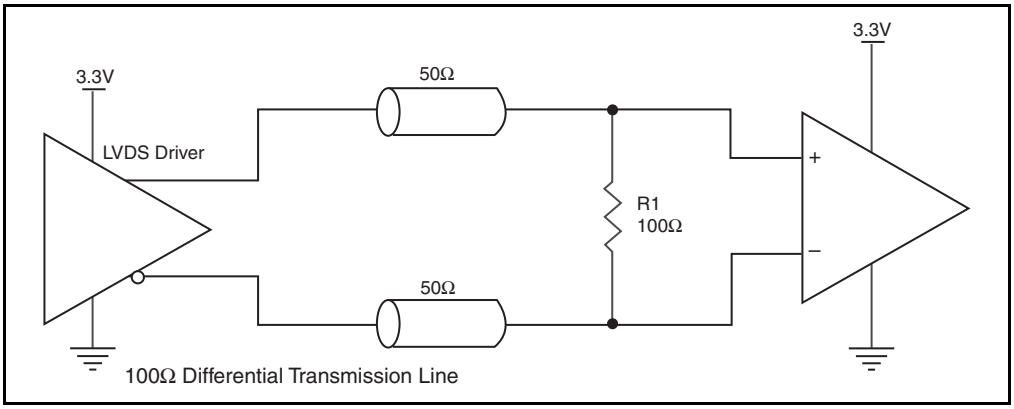


Figure 4. Typical LVDS Driver Termination

Recommended Termination

Figure 5A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ù impedance.

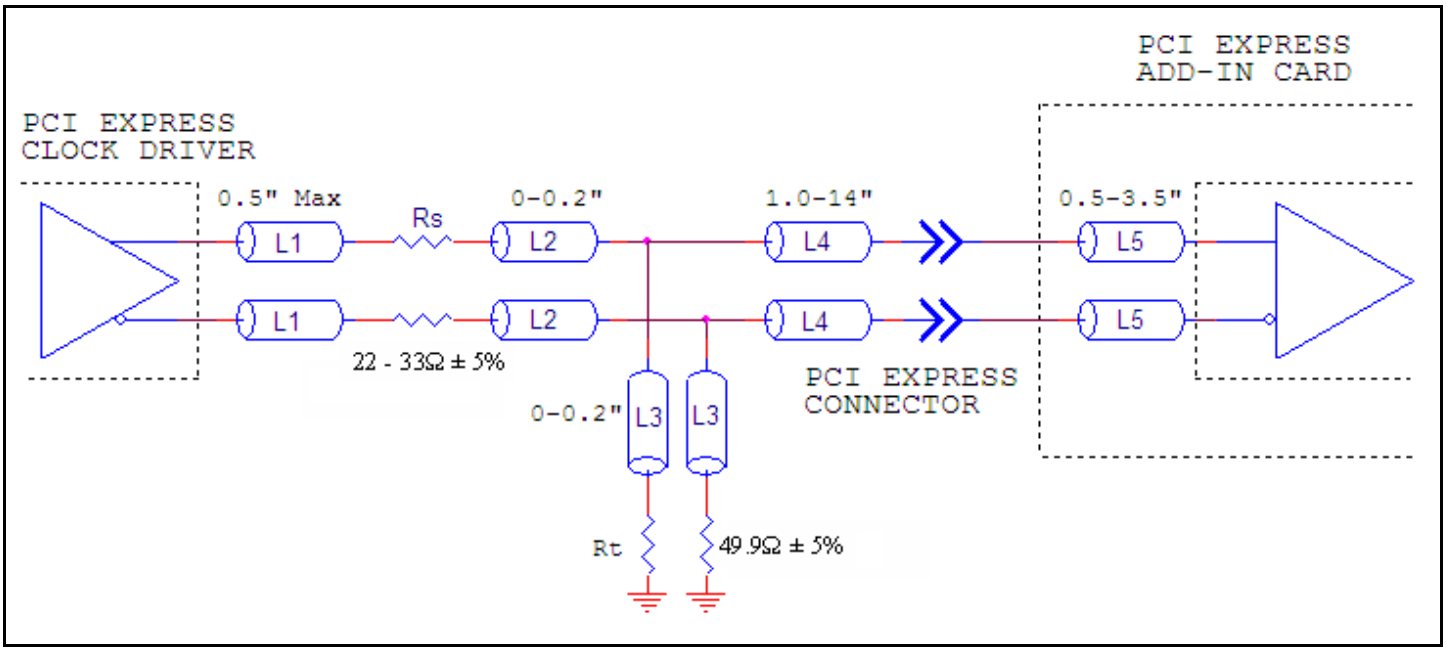


Figure 5A. Recommended Termination

Figure 5B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ù impedance.

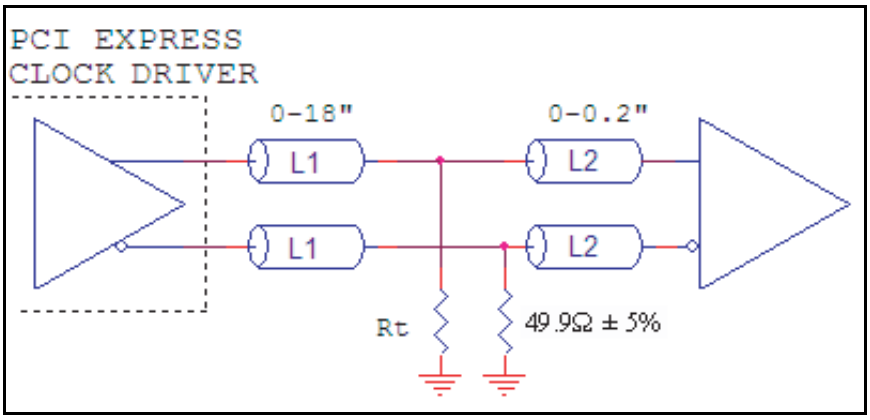


Figure 5B. Recommended Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

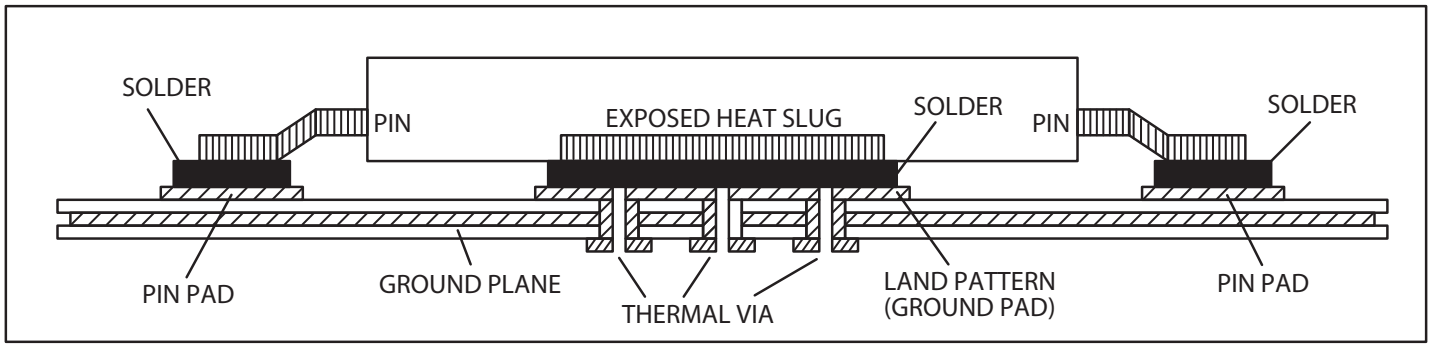


Figure 6. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Example

Figure 7 shows an example of 8741004I application schematic. In this example, the device is operated at V_{DD} = V_{DDO} = 3.3V. Two examples of LVDS terminations and two examples of HCSL terminations are shown in this schematic. The input is driven by a 3.3V LVPECL driver. The decoupling capacitors should be located as close as possible to the power pin.

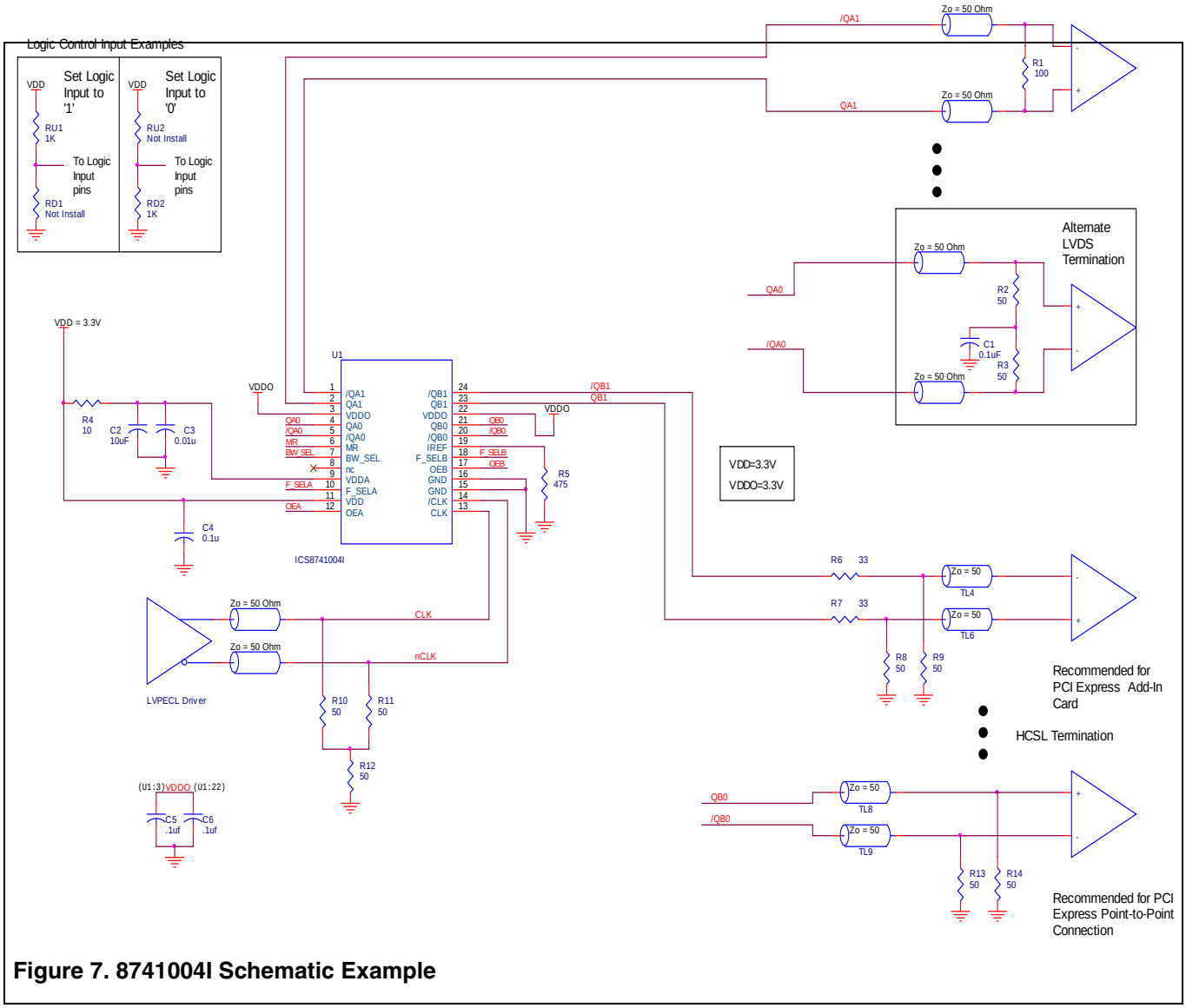


Figure 7. 8741004I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8741004I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 741004I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (45mA + 12mA) = **197.5mW**
- Power (LVDS_output)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 80mA = **277.2mW**
- Power (HCSL_output)$_{MAX}$ = 44.5mW * 2 = **89mW**

Total Power$_{_MAX}$ = (3.465V, with all outputs switching) = 197.5mW + 277.2mW + 89mW = **563.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.564W * 32.1°C/W = 103.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, E-Pad, Forced Convection

θ_{JA} **Vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 8*.

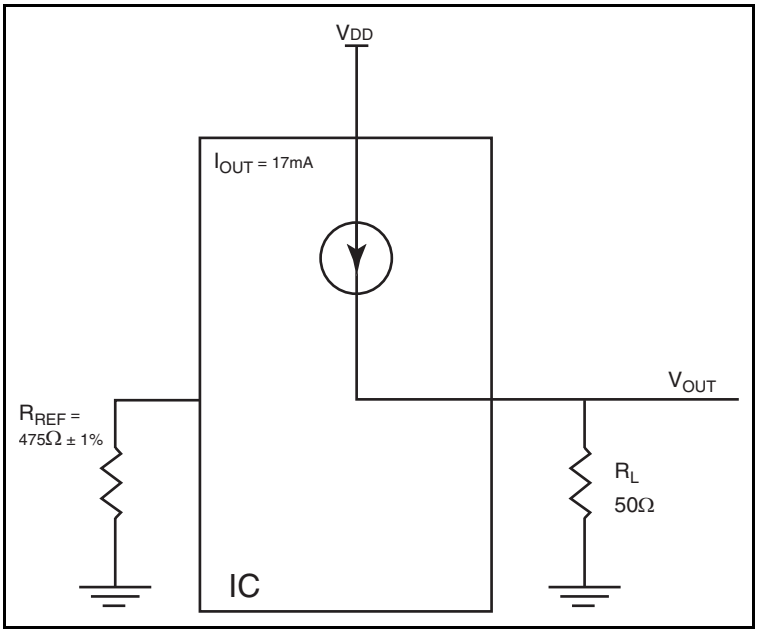


Figure 8. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power $= (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$, since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP, E-Pad

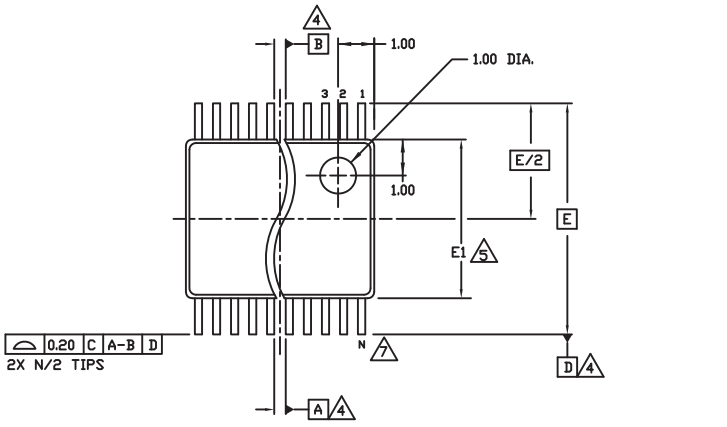
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24.0°C/W

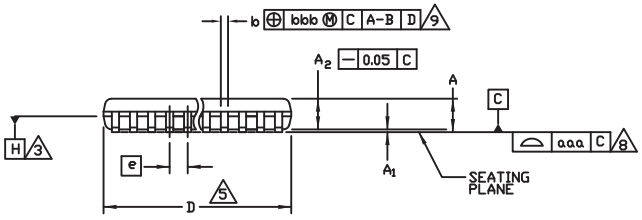
Transistor Count

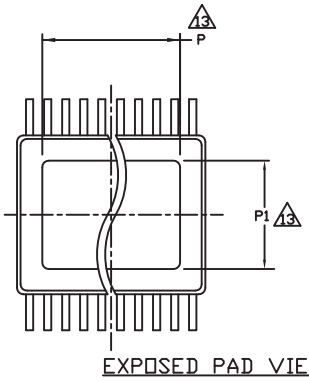
The transistor count for 8741004I is: 1318

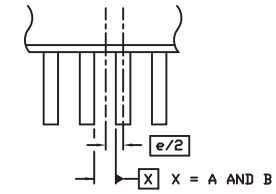
Package Outline and Package Dimension

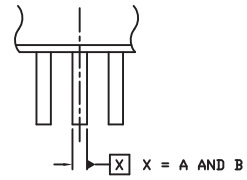
Package Outline - G Suffix for 24 Lead TSSOP, E-Pad

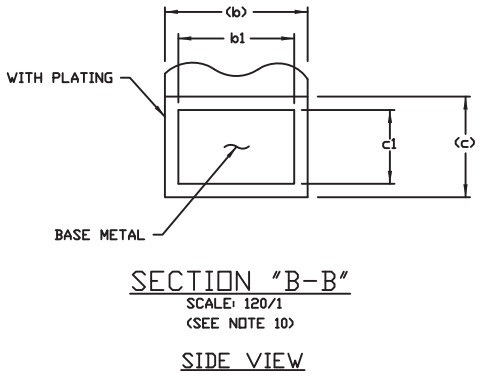


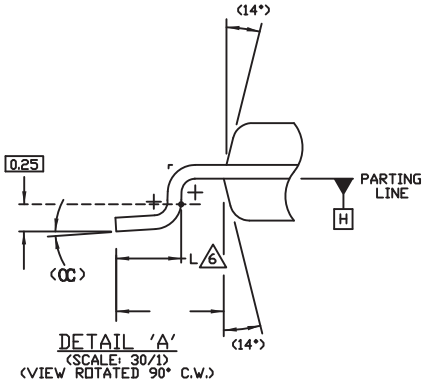












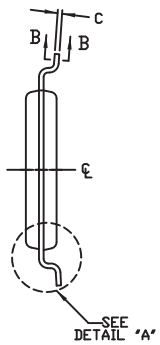


Table 8. Package Dimensions

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		24	
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
b1	0.19	0.22	0.25
c	0.09		0.20
c1	0.09	0.127	0.16
D	7.70		7.90
E		6.40 Basic	
E1	4.30	4.40	4.50
e		0.65 Basic	
L	0.50	0.60	0.70
P	5.0		5.5
P1	3.0		3.2
α	0°		8°
ααα		0.076	
bbb		0.10	

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8741004BGILF	ICS8741004BIL	“Lead-Free” 24 Lead TSSOP, E-Pad	Tray	-40°C to 85°C
8741004BGILFT	ICS8741004BIL	“Lead-Free” 24 Lead TSSOP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T3C	4 16 & 17	Added F_SEL Function Table. Power Considerations - updated Power Dissipation section to coincide with updates to the Calculations & Equations section on page 17.	5/29/08
A	T9	20	Removed leaded parts from Ordering Information table	11/15/12
A	T9	1 11	Removed ICS from part numbers where needed. General Description - Deleted ICS chip. Ordering Information - Deleted quantity from tape and reel. Deleted LF note below table. Updated header and footer.	1/27/16

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