# MP2491C

## 32V, 6A, Step-Down Converter with Programmable Current Limit and Output Voltage Scaling Control

## DESCRIPTION

The MP2491C is a fully integrated, high-voltage, step-down converter. The MP2491C can achieve 6A of continuous output current with excellent load and line regulation over a wide input supply range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include over-current protection (OCP), hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MP2491C requires a minimal number of readily available, standard, external components and is available in a QFN-13 (2.5mmx3mm) package.

## FEATURES

- Wide 4.0V to 32V Operating Input Range
- 0.5V to 30V Output Voltage Range
- 6A Output Current
- Constant-on-Time (COT) Control
- Two Dedicate Voltage Scaling Control Pins
- Slew Rate Control during DVS
- Low Dropout Mode Operation
- 33mΩ/22mΩ Internal MOSFET Switches
- 450μA $I_Q$
- Fixed 490kHz Switching Frequency
- Output Line Drop Compensation when $V_{FB}$ = 0.5V
- EN Shutdown Discharge
- Output Over-Voltage Protection (OVP)
- Adjustable Auto-PFM/PWM Mode or Forced PWM Mode
- Adjustable Current Limit
- Power Good (PG) Indication
- Available in a QFN-13 (2.5mmx3mm) Package

## APPLICATIONS

- TVs, Monitors
- MFP Power Supplies
- USB Power Supplies with PD
- Automotive Cigarette Lighter Adapters

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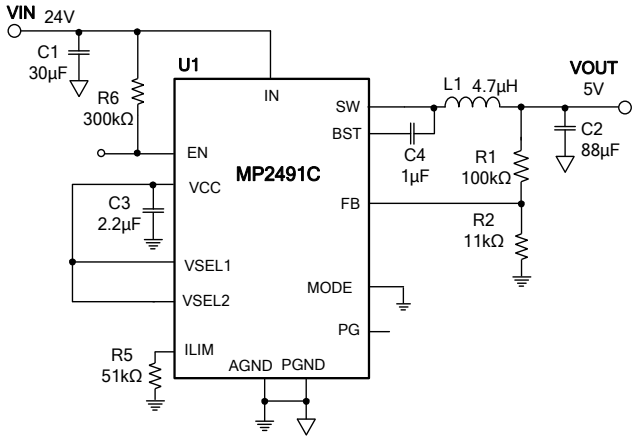
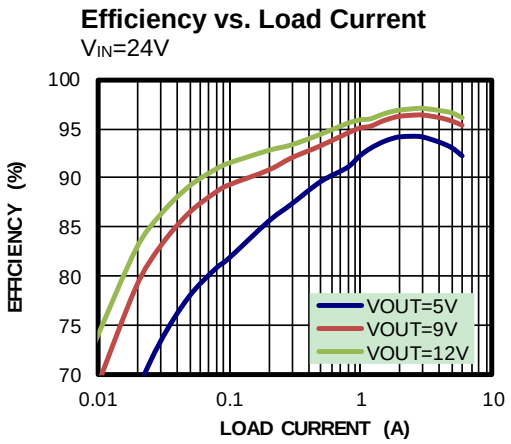
## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP2491CGQB | QFN-13 (2.5mmx3mm) | *See Below* |

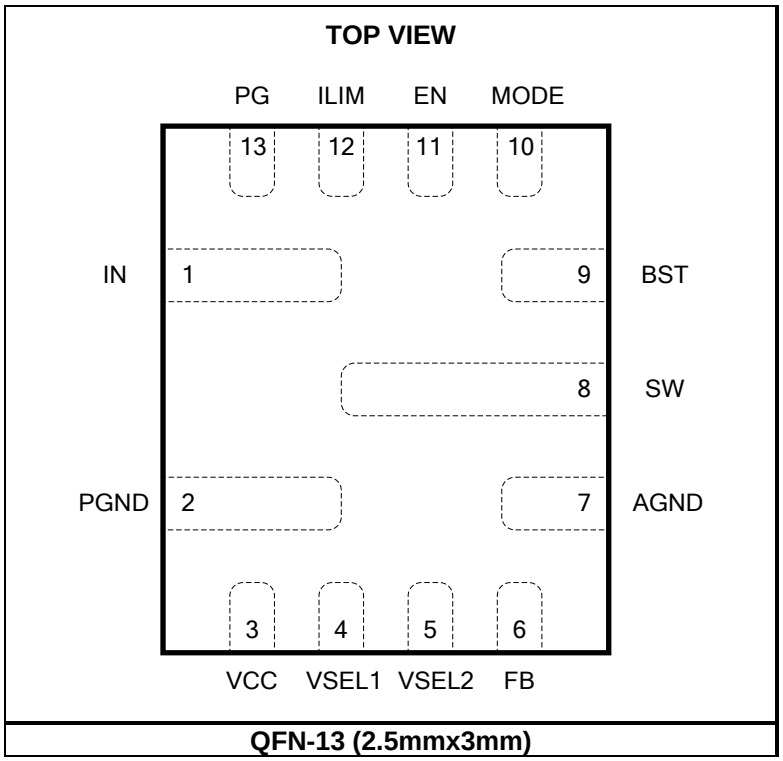
* For Tape & Reel, add suffix –Z (e.g. MP2491CGQB–Z).

## TOP MARKING

BAX
YWW
LLL

BAX: Product code of MP2491CGQB
Y: Year code
WW: Week code
LLL: Lot number

## PACKAGE REFERENCE




QFN-13 (2.5mmx3mm)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## PIN FUNCTIONS

| QFN-13 Pin # | Name | Description |
|---|---|---|
| 1 | IN | **Supply voltage.** IN is the drain of the internal power device and power supply for the entire chip. The MP2491C operates from a 4V to 32V unregulated input. Place a capacitor ($C_{IN}$) as close to the IC as possible to prevent large voltage spikes from appearing at the input. |
| 2 | PGND | **Power ground.** Place the PGND node outside of the $C_{IN}$ ground path to prevent switching current spikes from inducing voltage noise into the part. |
| 3 | VCC | **Internal 5V LDO regulator output.** Decouple VCC with a 2.2µF capacitor. The VCC LDO is active even if EN is pulled low. |
| 4 | VSEL1 | **Select the FB reference voltage 1.** Connect VSEL1 to VCC, AGND, or a 1/2 VCC divider. VSEL1 cannot be left floating. |
| 5 | VSEL2 | **Select the FB reference voltage 2.** Connect VSEL2 to VCC or AGND. VSEL2 cannot be left floating. |
| 6 | FB | **Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. |
| 7 | AGND | **Analog ground.** Connect AGND to PGND. |
| 8 | SW | **Switch output.** SW is the source of the high-side power device. |
| 9 | BST | **Bootstrap.** A BST capacitor is needed to drive the power switch's gate above the supply voltage. Connect this capacitor between SW and BST to form a floating supply across the power switch driver. An on-chip regulator is used to charge up the external bootstrap capacitor. |
| 10 | MODE | **Buck operation mode set.** Connect MODE to VCC or AGND to set auto-PFM/PWM mode or forced PWM mode. MODE cannot be left floating. |
| 11 | EN | **Enable control.** Drive EN high to enable the MP2491C. EN has a 2MΩ pull-down resistor to GND. |
| 12 | ILIM | **Buck current limit set.** Connect a resistor from ILIM to ground to program the output current limit. ILIM cannot be left floating. |
| 13 | PG | **Power good output.** PG is an open drain and indicates both output UV and OV. PG does not respond for BST low or UV conditions. When the VSEL1/VSEL2 voltage changes, PG switches low. After the output voltage settles, PG goes high again. |


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## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{IN}$) ..... 34V
$V_{SW}$ ..... -0.3V (-7V for <10ns) to $V_{IN}$ + 0.3V
$V_{BST}$ ..... $V_{SW}$ + 6V
$V_{EN}$ ..... 6V (<100μA when >6V)
All other pins ..... -0.3V to +6V
Continuous power dissipation ($T_A$ = +25°C) (2)
QFN-13 (2.5mmx3mm) ..... 3.9W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

### *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 4V to 32V
Output voltage ($V_{OUT}$) ..... 0.5V to 30V
Output current ..... 6A
Operating junction temp. ($T_J$)... -40°C to +125°C

| *Thermal Resistance* | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| QFN-13 (2.5mmx3mm) | | | |
| EV2491C-QB-00A (4) | 32 | 8 | °C/W |
| JESD51-7 (5) | 60 | 13 | °C/W |

**NOTES:**

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on an EV2491C-QB-00A evaluation board for MP2491CGQB, four-layer PCB, 2Oz per layer, 8.5cmx8.5cm.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on an EV2491C-QB-00A, four-layer PCB, 2Oz per layer, 8.5cmx8.5cm.
5) The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 24V, $V_{EN}$ = 5V, $T_J$ = -40°C to +125°C [6], unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply current (shutdown) | $I_{IN}$ | $V_{EN}$ = 0V, $T_J$ = +25°C | | 100 | 200 | μA |
| | | $V_{EN}$ = 0V, $T_J$ = -40°C to +125°C | | | 700 | |
| Supply current (quiescent) | $I_Q$ | No switching, $T_J$ = +25°C | | 450 | 600 | μA |
| | | No switching, $T_J$ = -40°C to +125°C | | | 1000 | |
| EN rising threshold | $V_{EN_Rising}$ | | -5% | 1.24 | +5% | V |
| EN hysteresis | $V_{EN_HYS}$ | | | 280 | | mV |
| EN input current | $I_{EN}$ | $V_{EN}$ = 2V | | 1 | | μA |
| | | $V_{EN}$ = 0V | | 0 | | |
| Feedback voltage | $V_{FB1}$ | VSEL1 = VCC, VSEL2 = VCC, $T_J$ = +25°C | -1% | 0.5 | +1% | V |
| | $V_{FB2}$ | VSEL1 = 0, VSEL2 = VCC, $T_J$ = +25°C | -1.5% | 0.9 | +1.5% | V |
| | $V_{FB3}$ | VSEL1 = 1/2*VCC, VSEL2 = 0, $T_J$ = +25°C | -1.5% | 1.2 | +1.5% | V |
| | $V_{FB4}$ | VSEL1 = VCC, VSEL2 = 0, $T_J$ = +25°C | -1.5% | 1.5 | +1.5% | V |
| | $V_{FB5}$ | VSEL1 = 0, VSEL2 = 0, $T_J$ = +25°C | -1% | 2.0 | +1% | V |
| Thermal shutdown [7] | $T_{STD}$ | | | 150 | | °C |
| Thermal hysteresis [7] | $T_{HYS}$ | | | 20 | | °C |
| VCC regulator | $V_{CC}$ | | 4.8 | 5.05 | 5.3 | V |
| VCC load regulation | $V_{CC_RG}$ | $I_{CC}$ = 0 - 10mA | | | 3 | % |
| $V_{IN}$ under-voltage lockout threshold rising | $INUV_{Vth}$ | | 3.6 | 3.8 | 4.0 | V |
| $V_{IN}$ under-voltage lockout threshold hysteresis | $INUV_{HYS}$ | | | 250 | | mV |
| HS switch on resistance | $R_{DSON_HS}$ | | | 33 | | mΩ |
| LS switch on resistance | $R_{DSON_LS}$ | | | 22 | | mΩ |
| Output over-voltage rising | $V_{OVP_R}$ | | 110 | 115 | 120 | $\%V_{FB}$ |
| OVP recovery threshold | $V_{OVP_F}$ | | 105 | 110 | 115 | $\%V_{FB}$ |
| PG UV rising | $V_{PG_UV_R}$ | | 88% | 93% | 98% | Vref |
| PG UV falling | $V_{PG_UV_F}$ | | | 87% | | Vref |
| PG OV rising | $V_{PG_OV_R}$ | | 108% | 113% | 118% | Vref |
| PG OV falling | $V_{PG_OV_F}$ | | | 107% | | Vref |
| PG rise delay | $t_{PG_R_DLY}$ | | | 250 | | μs |
| PG falling delay | $t_{PG_F_DLY}$ | | | 50 | | μs |
| Power good sink current capability | $V_{PG_Sink}$ | Sink 1mA | | | 0.4 | V |
| Output voltage change slew rate | $V_{SLEW}$ | Both ramp up and down | 10 | 14 | 18 | mV/μs |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{EN}$ = 5V, $T_J$ = -40°C to +125°C [6], unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Line drop compensation | $V_{LINE_DROP}$ | $I_{OUT}$ = 3A, $V_{FB1}$ = 0.5V, $V_{OUT}$ = 5V, $T_J$ = +25°C | | 220 | | mV |
| Switch leakage | $SW_{LKG}$ | $V_{EN}$ = 0V, $V_{SW}$ = 32V, $T_J$ = +25°C | | | 1 | μA |
| | | $V_{EN}$ = 0V, $V_{SW}$ = 32V, $T_J$ = -40°C to +125°C | | | 3 | μA |
| MODE pin voltage threshold 1 | $V_{MODE_1}$ | Forced PWM mode | | | 0.12 | VCC |
| MODE pin voltage threshold 2 | $V_{MODE_2}$ | Auto PFM/PWM | 0.9 | | | VCC |
| Negative current limit [7] | $I_{LIMITN}$ | PWM mode, OVP or EN shutdown | | -3 | | A |
| AAM threshold | $I_{AAM}$ | Inductor peak current, $V_{OUT}$ = 5V, 12V | 100 | 400 | 700 | mA |
| Output current limit | $I_{LIMI_TH1}$ | ILIM = 51kΩ, $T_J$ = +25°C | -15% | 7.19 | +15% | A |
| | $I_{LIMI_TH2}$ | ILIM = 64.9kΩ, $T_J$ = +25°C | -15% | 5.6 | +15% | A |
| | $I_{LIMI_TH3}$ | ILIM = 95.3kΩ, $T_J$ = +25°C | -15% | 3.6 | +15% | A |
| | $I_{LIMI_TH4}$ | ILIM = 110kΩ, $T_J$ = +25°C | -20% | 3.11 | +20% | A |
| Hiccup duty cycle [7] | $D_{HICP}$ | | | 0.2 | | % |
| Oscillator frequency | $f_{SW}$ | MODE/FREQ = 0V, $T_J$ = +25°C | 400 | 490 | 580 | kHz |
| Maximum on time [7] | $T_{ON_MAX}$ | | | 10 | | μs |
| Minimum on time [7] | $T_{ON_MIN}$ | | | 60 | | ns |
| Minimum off time [7] | $T_{OFF_MIN}$ | | | 180 | | ns |
| Soft-start time | $t_{SS}$ | $V_{OUT}$ = 5V, output is from 0% to 100% | | 1 | 1.7 | ms |

**NOTES:**
6) Not tested in production, guaranteed by over-temperature correlation.
7) Guaranteed by design and characterization test.


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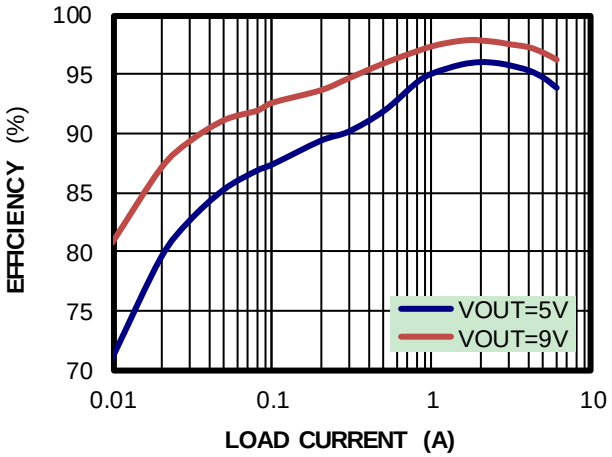
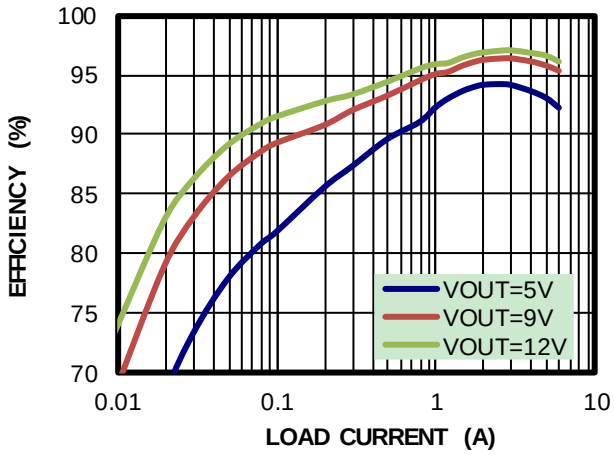
## TYPICAL PERFORMANCE CHARACTERISTICS

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, Fs = 490kHz, L = 4.7μH, PFM mode, $T_A$ = +25°C, unless otherwise noted.**

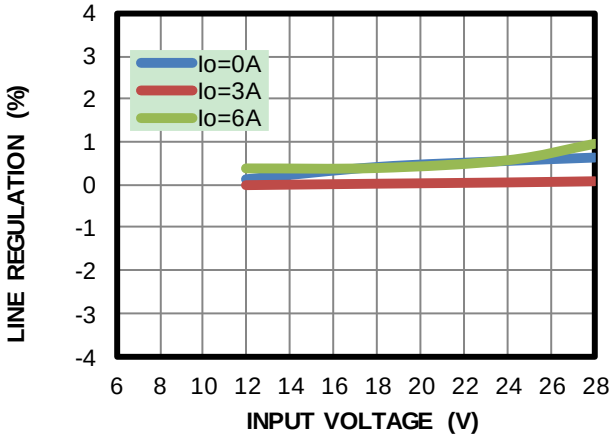
**Efficiency vs. Load Current**
$V_{IN}$ = 12V



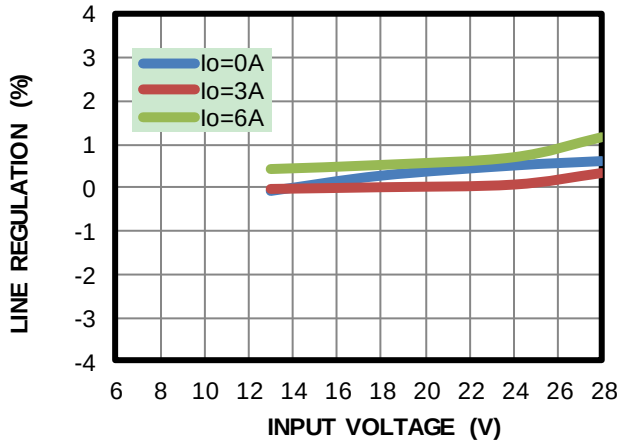

**Efficiency vs. Load Current**
$V_{IN}$ = 24V



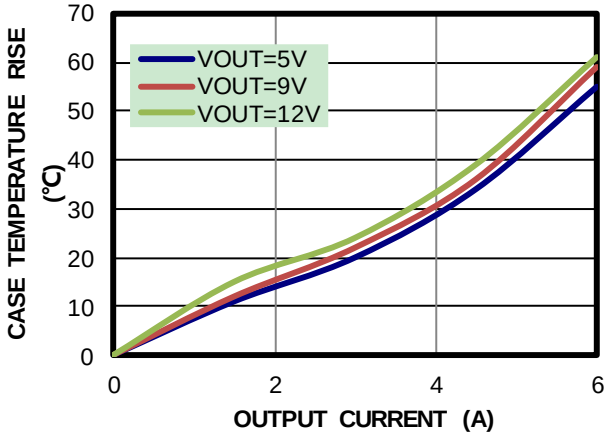

**Line Regulation**
$V_{OUT}$ = 9V



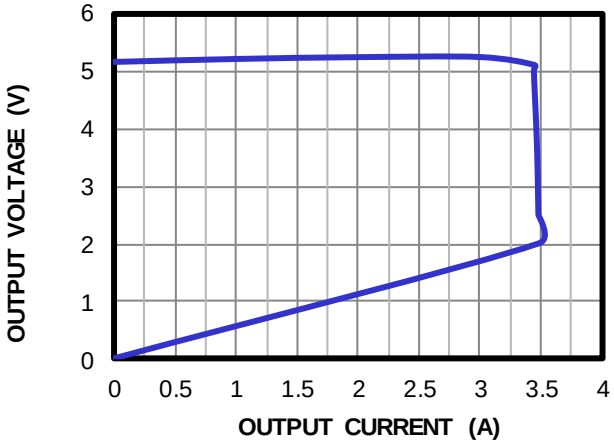

**Line Regulation**
$V_{OUT}$ = 12V




**Case Temperature Rise vs. Output Current, Four-Layer PCB**




**CC/CV Mode Curve**
$R_{LIMIT}$ = 100kΩ





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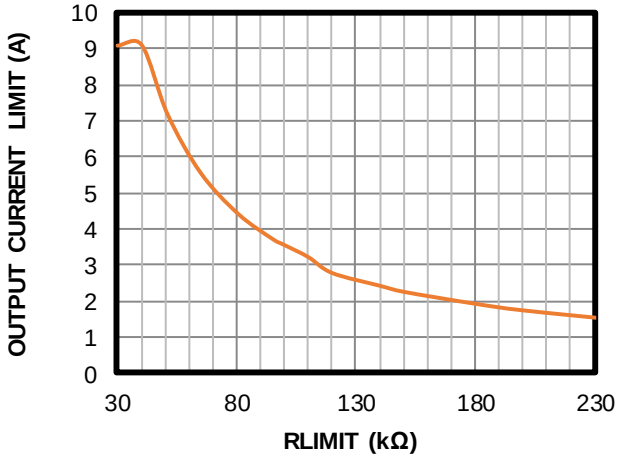
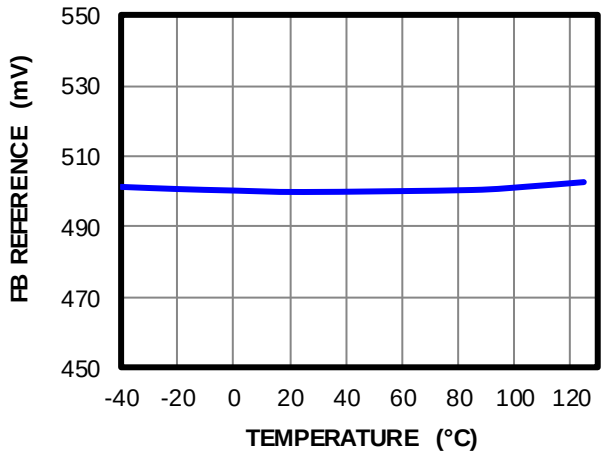
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, Fs = 490kHz, L = 4.7μH, PFM mode, $T_A$ = +25°C, unless otherwise noted.**

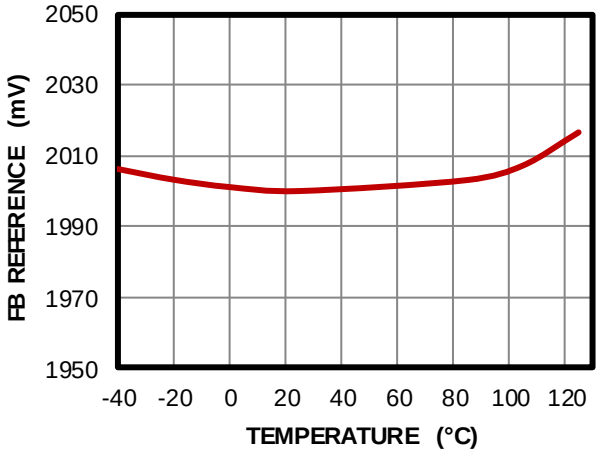
**Current Limit vs. $R_{LIMIT}$ Resistor**




**$V_{FB}$ = 0.5V vs. Temperature**

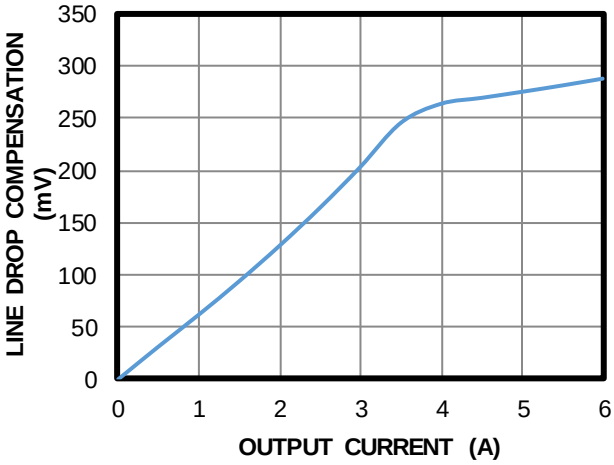



**$V_{FB}$ = 2V vs. Temperature**




**Line Drop Compensation vs. Output Current**

$V_{FB}$ = 0.5V, $V_{OUT}$ = 5V





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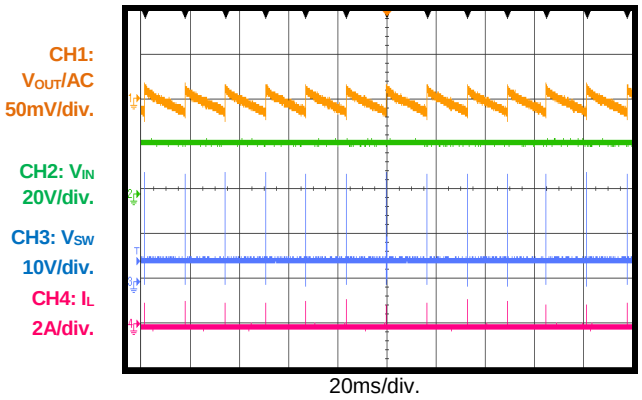
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, Fs = 490kHz, L = 4.7µH, $T_A$ = +25°C, unless otherwise noted.**

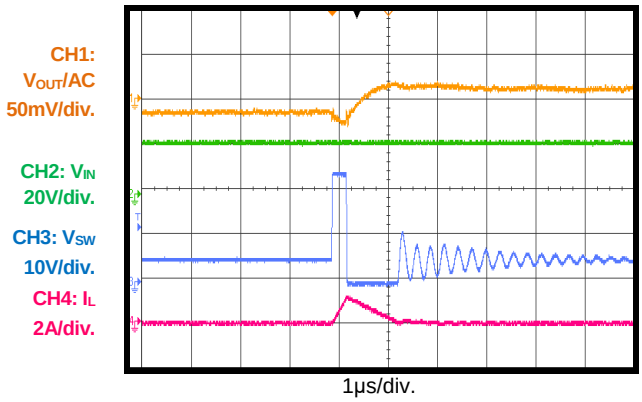
### Output Ripple

$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A



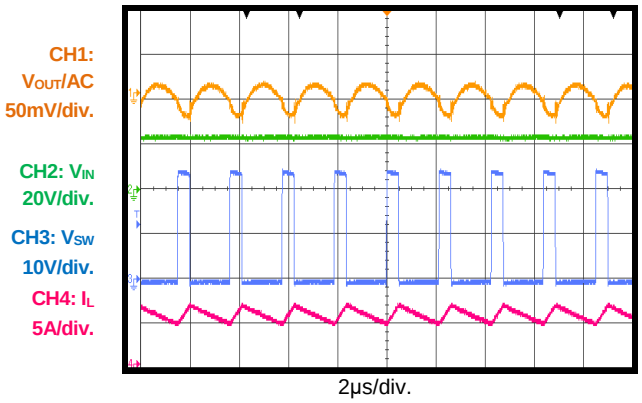

### Output Ripple

$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A



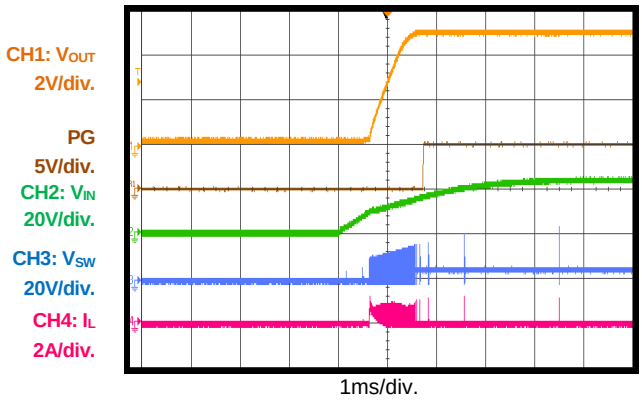

### Output Ripple

$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 6A



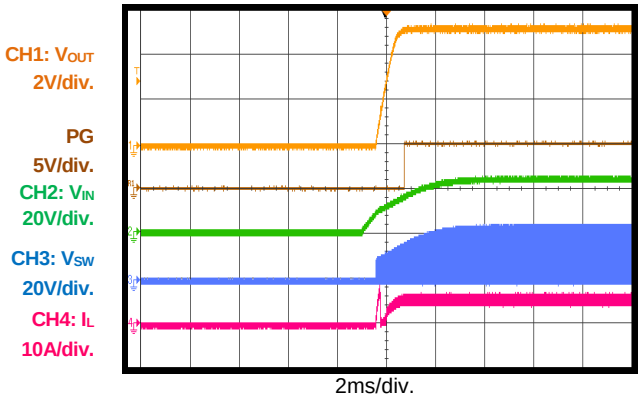

### Power Start-Up

$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A



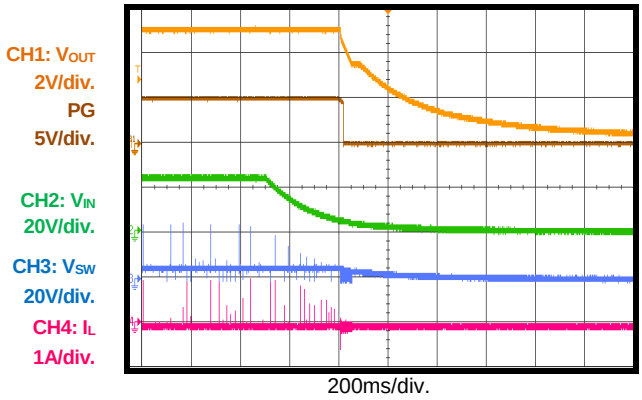

### Power Start-Up

$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 6A




### Power Shutdown

$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A





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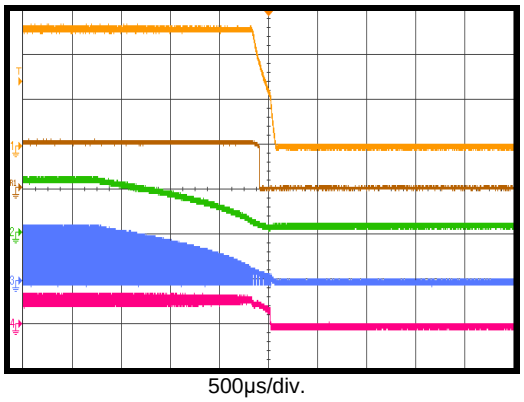
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, Fs = 490kHz, L = 4.7μH, $T_A$ = +25°C, unless otherwise noted.**

### Power Shutdown

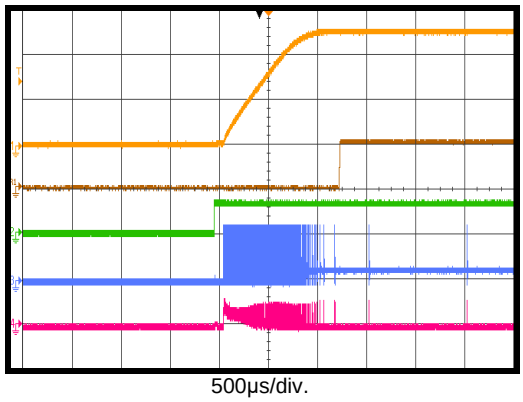
$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 6A




500μs/div.

### EN Start-Up

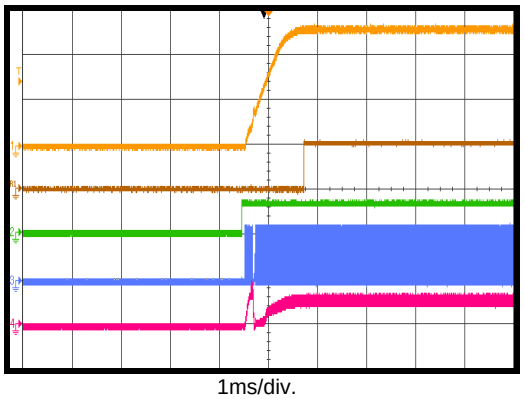
$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A




500μs/div.

### EN Start-Up

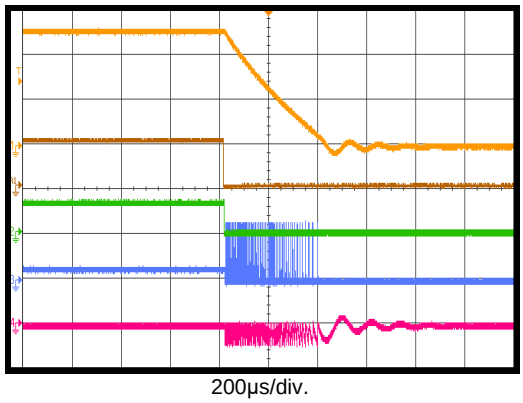
$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 6A




1ms/div.

### EN Shutdown

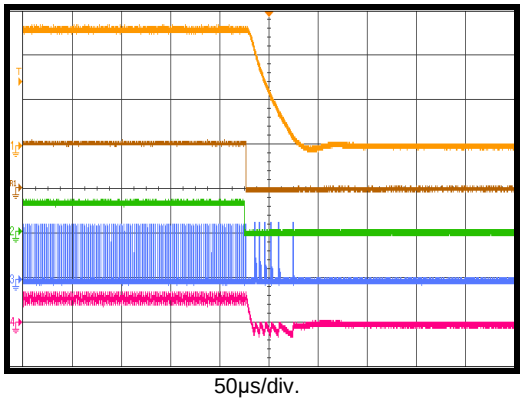
$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A




200μs/div.

### EN Shutdown

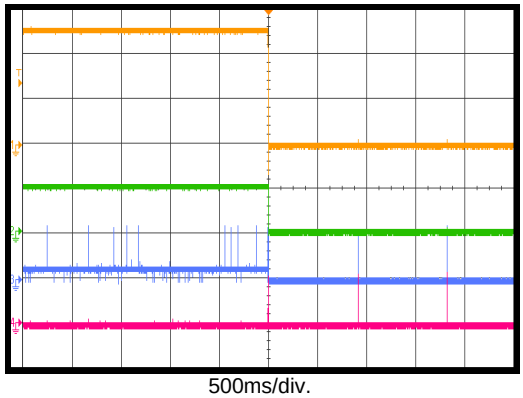
$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 6A




50μs/div.

### SCP Entry

$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A




500ms/div.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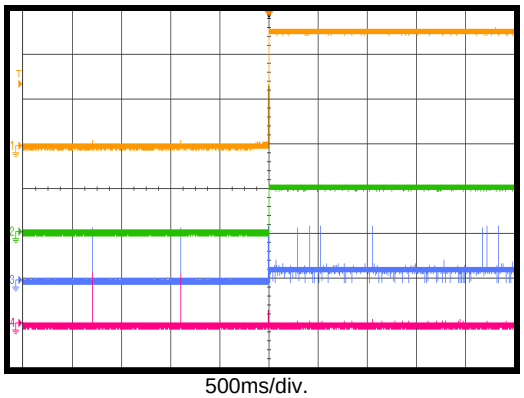
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 24V, $V_{OUT}$ = 5V, Fs = 490kHz, L = 4.7μH, $T_A$ = +25°C, unless otherwise noted.**

### SCP Recovery

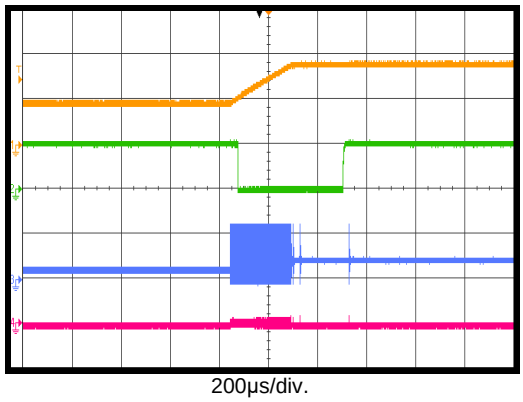
$V_{IN}$ = 24V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A




500ms/div.

### Output Voltage Scaling Up

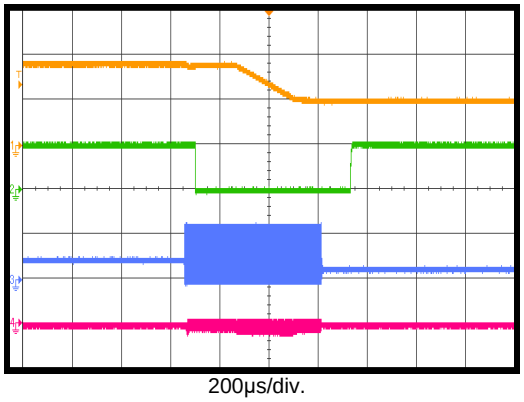
$V_{IN}$ = 24V, $I_{OUT}$ = 0A, $V_{OUT}$ = 5 - 9V




200μs/div.

### Output Voltage Scaling Down

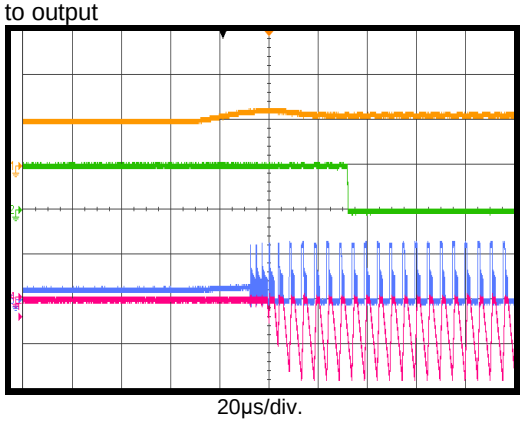
$V_{IN}$ = 24V, $I_{OUT}$ = 0A, $V_{OUT}$ = 9 - 5V




200μs/div.

### Output Over-Voltage Protection

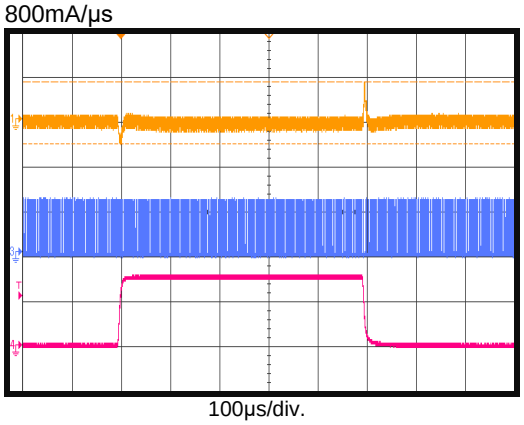
$V_{IN}$ = 24V, $I_{OUT}$ = 0A, add external DC voltage to output




20μs/div.

### Load Transient

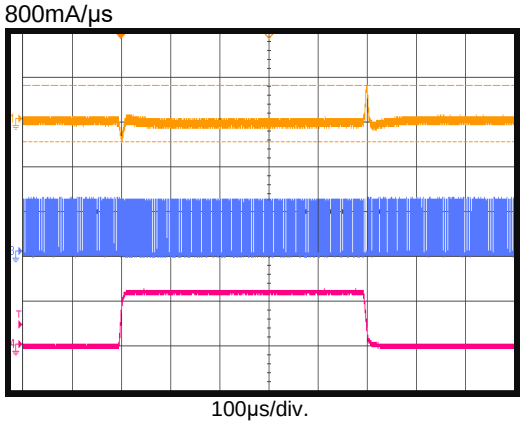
$V_{IN}$ = 24V, $V_{FB}$ = 1.2V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0 - 3A, 800mA/μs




100μs/div.

### Load Transient

$V_{IN}$ = 24V, $V_{FB}$ = 1.2V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0 - 6A, 800mA/μs




100μs/div.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## BLOCK DIAGRAM

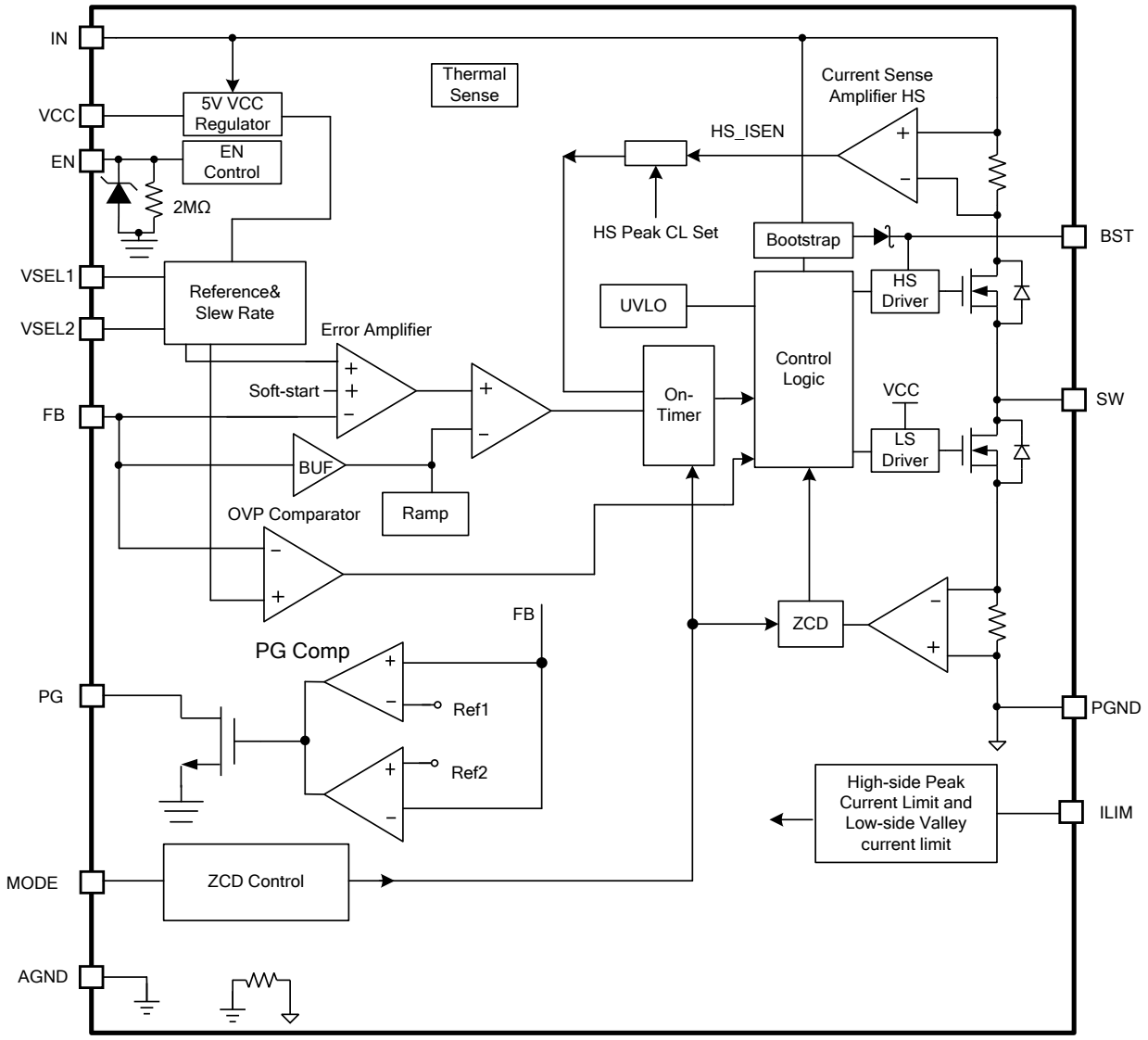


**Figure 1: Functional Block Diagram**


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## OPERATION

The MP2491C is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. Figure 2 shows the simplified ramp compensation block in MP2491C. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage ($V_{RAMP}$) is lower than the error amplifier output voltage ($V_{EAO}$), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off and turns on again when $V_{RAMP}$ drops below $V_{EAO}$. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting line or load regulation.

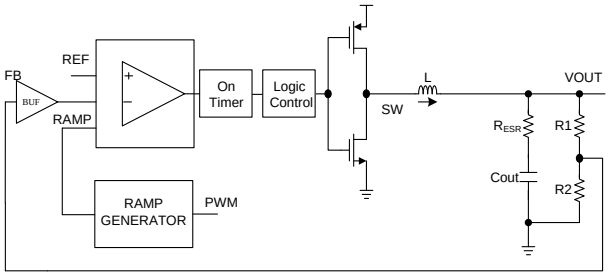


**Figure 2: Simplified Ramp Compensation Block**

### Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps (see Figure 3). When $V_{RAMP}$ is below $V_{EAO}$, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period.

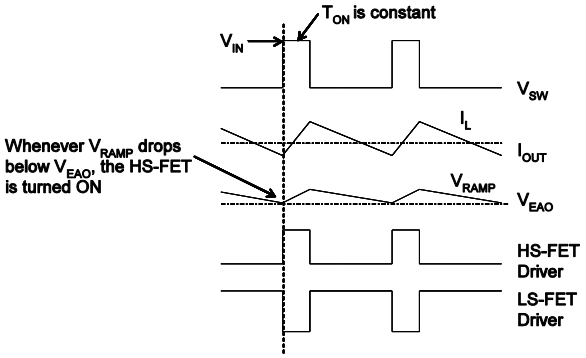


**Figure 3: Heavy Load Operation**

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

### Light-Load Operation

When the MP2491C works in pulse-frequency modulation (PFM) mode during light-load operation, the MP2491C reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. The HS-FET turns on when $V_{RAMP}$ is below $V_{EAO}$. The HS-FET turns off when the on-timer elapses and the inductor current is higher than its given threshold. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 4). Therefore, the output capacitors discharge slowly to GND through the LS-FET and the resistors R1 and R2. This operation improves device efficiency greatly when the output current is low.


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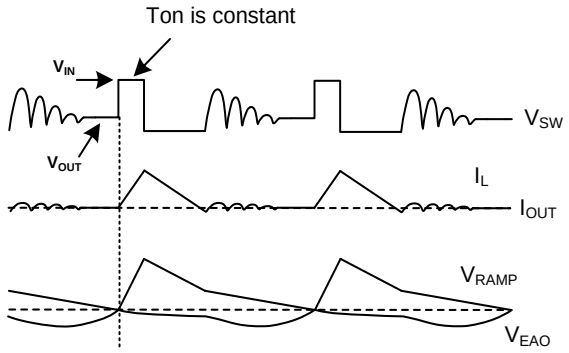


**Figure 4: Light-Load Operation**

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The HS-FET turn-on frequency is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

### Low Dropout Mode Operation

The MP2491C supports low dropout mode. When VIN is close to the output voltage and the minimum off time is triggered, the switching on-timer is extended to avoid output voltage drops. The switching frequency decreases accordingly. After the maximum on time is triggered (typically 10μs), SW enters max duty cycle operation (typically 98%).

### 5V Internal VCC Regulator

The 5V internal regulator powers most of the internal logic circuitries. This regulator takes the VIN input and operates in the full VIN range. When VIN exceeds 5V, the output of the regulator is in full regulation. When VIN is less than 5V, the output decreases with VIN. The VCC regulator is active, even if EN is pulled low. This pin requires a 2.2μF ceramic decoupling capacitor. VCC can supply 20mA of current (4.6 - 5V) for the external USB charger protocol controller.

### Over-Current Protection (OCP)

The MP2491C senses the high-side and low-side currents and uses this information to protect the output from an over-current (OC) condition. If the high-side current exceeds the set current-limit threshold, the HS-FET turns off to limit the increasing current. The LS-FET monitors the current flowing through it. The HS-FET waits until the valley current limit is removed before turning on again. As the load resistance reduces, the output voltage drops until the feedback voltage falls below the under voltage (UV) threshold (typically 40% below the reference). Once UV is triggered, the MP2491C enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This reduces the average short-circuit current greatly, alleviating thermal issues and protecting the regulator. The MP2491C exits hiccup mode once the OC condition is removed.

### Current Limit Set (ILIM)

The MP2491C has a programmable current-limit pin (ILIM). Connect a resistor from ILIM to ground to adjust the output current limit continuously through the high-side peak current limit and low-side valley current limit. Refer to the Current Limit vs. $R_{LIMIT}$ curve on page 8 for the current limit setting. $R_{LIMIT}$ can range from 30 - 230kΩ.

### Mode Selection (MODE)

The MP2491C's MODE pin offers two different programmable states to set the buck operation mode: forced PWM or auto PFM/PWM (see Figure 5).

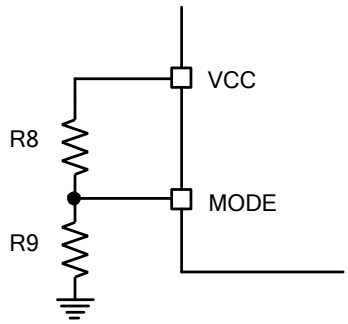


**Figure 5: MODE Configuration**


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Table 1 lists detail information according to different pin voltages.

**Table 1: MODE Truth Table**

| Resistor Value | Pin Voltage | Buck Operation Mode |
|---|---|---|
| R8 = NS, R9 = 0 | 0 | Forced PWM |
| R8 = 0, R9 = NS | VCC | Auto PFM/PWM |

MODE supports dynamic adjustment with a glitch time. MODE cannot be left floating during normal operation.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2491C's UVLO comparator monitors the input voltage.

### Enable Control (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN above 1.24V to turn on the regulator. Drive EN below 0.96V to turn off the regulator. EN has a 2MΩ pull-down resistor to GND.

EN is clamped internally using a 7V series Zener diode (see Figure 6). Connecting the EN input through a pull-up resistor to VIN limits the EN input current below 100μA, preventing damage to the Zener diode.

For example, if connecting 24V to VIN, then $R_{PULL_UP}$ ≥ (24V - 7V)/100μA - 3kΩ = 167kΩ.

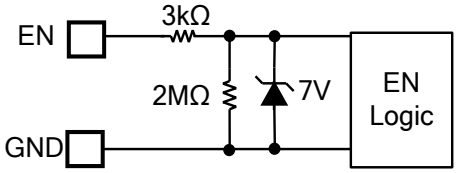


**Figure 6: Zener Diode between EN and GND**

### Internal Soft Start (SS)

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 5.05V. When SS is below REF, the error amplifier uses SS as the reference. When SS rises above REF, the error amplifier uses REF as the reference. The SS time is set to 1ms internally from a 0 - 100% output when REF is 0.5V.

For different REF voltages ($V_{REF}$), calculate the SS time with Equation (2):

$$SS(ms) = 2 \times V_{REF}(V) \quad (2)$$

If the output of the MP2491C is pre-biased to a certain voltage during start-up, the MP2491C disables the switching of both the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the internal feedback voltage.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C4, L1, and C2 (see Figure 7). If $V_{IN}$ - $V_{SW}$ exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4.

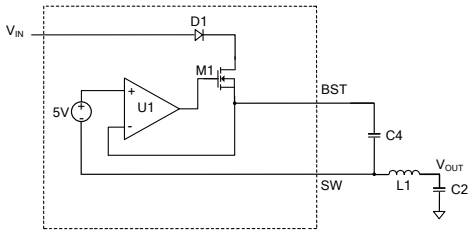


**Figure 7: Internal Bootstrap Charging Circuit**

### Output Discharge

An active discharge path turns on when EN is low or during output over-voltage protection (OVP). The low-side switch turns on until the negative inductor current reaches its current limit. The low-side switch then turns off for a fixed period. The low-side switch turns on again after a fixed delay and the on/off cycles are repeated. The discharge function is turned off when VOUT is fully discharged or the 10ms maximum passes.

During a negative output voltage transition (such as 20V to 15V, 15V to 12V, 15V to 9V, 9V to 5V, or 5V to 0), the MP2491C enters forced PWM mode to ensure that the output voltage can be discharged.

### Output Over-Voltage Protection (OVP)

To protect the downstream device from an over-voltage (OV) condition, the MP2491C provides an output OVP discharge function.


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If the FB voltage ($V_{FB}$) is higher than 115%$V_{REF}$ with a 5µs deglitch time, the low-side switch repeats the turn-on process to discharge the output voltage until the output decreases to 110%$V_{REF}$. Then the chip resumes normal operation.

If the input voltage is charged above 33V while $V_{OUT}$ OVP is discharging, the output OVP function is disabled. The output OVP discharge function is enabled again when VIN falls below 31V. The OVP function is blanked during a high-to-low voltage mode change period.

### Output Line Drop Compensation

The MP2491C is capable of compensating for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant 5V load-side voltage.

Long traces to the circuit load induce a voltage drop between $V_{OUT}$ and $V_{LOAD}$, which can be calculated with Equation (3):

$$V_{DROP} = I_{OUT} \cdot R_{TRACE} \quad (3)$$

Since the trace resistance ($R_{TRACE}$) varies for different cables, the MP2491C uses linear line drop compensation. If the output current is 0A, there is no compensation. If the output current is 3A, the line drop compensation voltage is 220mV@5$V_{OUT}$. Refer to the Line Drop Compensation vs. Output Current curve on page 8 for details. The output line drop compensation works only for a 0.5V FB reference voltage condition. It is not active for 0.9V, 1.2V, 1.5V, 2.0V, or other reference voltage cases.

### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

### Output Voltage Selection (VSEL1, VSEL2)

The MP2491C has two pins to adjust the internal feedback reference voltage (VSEL1, VSEL2). Use a resistor divider from VCC to AGND to connect to VSEL1/VSEL2. An external open-drain GPIO or other logic control signal can be used to change the output voltage dynamically (see Figure 8).

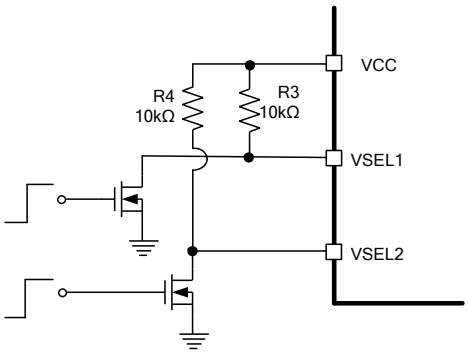


**Figure 8: Output Adjust Configuration**

Table 2 shows details for the reference voltage setting.

**Table 2: VSEL1, VSEL2 Truth Table**

| VSEL1 | VSEL2 | $V_{REF}$ | $V_{OUT}$ |
|---|---|---|---|
| 0 | 0 | 2V | 20V |
| VCC | 0 | 1.5V | 15V |
| 0 | VCC | 0.9V | 9V |
| 1/2*VCC | 0 | 1.2V | 12V |
| VCC | VCC | 0.5V | 5V |

There is a 20µs deglitch time for each VSEL pin logic voltage change.

### Power Good (PG)

The power good pin (PG) indicates whether the output voltage is in the normal range or not compared to the internal reference voltage. PG is an open-drain structure and requires an external pull-up supply. During power-up, the power good output is driven low. This tells the system to remain off and keep the load on the output to a minimum. This helps reduce inrush current during a start-up condition.

When the output voltage is higher than the PG UV and lower than the PG OV of the internal reference voltage and the soft start is finished, the PG signal is open drain output. When the output voltage is lower than the PG UV or higher than the PG OV of the internal reference, PG is switched low.

PG uses a deglitch time for both the rising and falling edge whenever $V_{OUT}$ crosses the UV/OV rising and falling thresholds. The PG output is pulled low immediately when EN is below its threshold or input UVLO is triggered.

During VSEL1/VSEL2 logic changes, PG switches low. After the output voltage is settled, PG goes open drain again.


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# APPLICATION INFORMATION

## Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Use an inductor with a DC resistance less than 15mΩ for the best efficiency. For most designs, the inductor value can be calculated with Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where $\Delta I_L$ is the inductor ripple current.

Set the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Under light-load conditions (below 100mA), use a larger inductor for improved efficiency.

## Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

## Selecting the Output Capacitor

Considering the inrush and discharge current during a voltage change, the maximum output capacitance is recommended less than 330µF. The MP2491C requires an output capacitor (C2) to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where $L_1$ is the inductor value, and $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulatory system. The MP2491C can be optimized for a wide range of capacitance and ESR values.


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## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. Use a 4-layer PCB for better thermal performance. For best results, refer to Figure 9 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input decoupling capacitor as close to the VIN and GND pins as possible.
3. Place the VCC decoupling capacitor as close to the VCC pin as possible.
4. Add multiple vias on the ground side of the VCC decoupling capacitor and the GND pins to connect to the inner and bottom ground plane.
5. Place the external feedback resistors next to the FB pin.

## Design Example

Table 3 shows a design example when ceramic capacitors are applied.

**Table 3: Design Example**

| | |
|---|---|
| $V_{IN}$ | 24V |
| $V_{OUT}$ | 5V |
| $I_{OUT}$ | 6A |

Detailed application schematics are shown in Figure 10 and Figure 11. The typical performance waveforms are shown in the Typical Performance Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

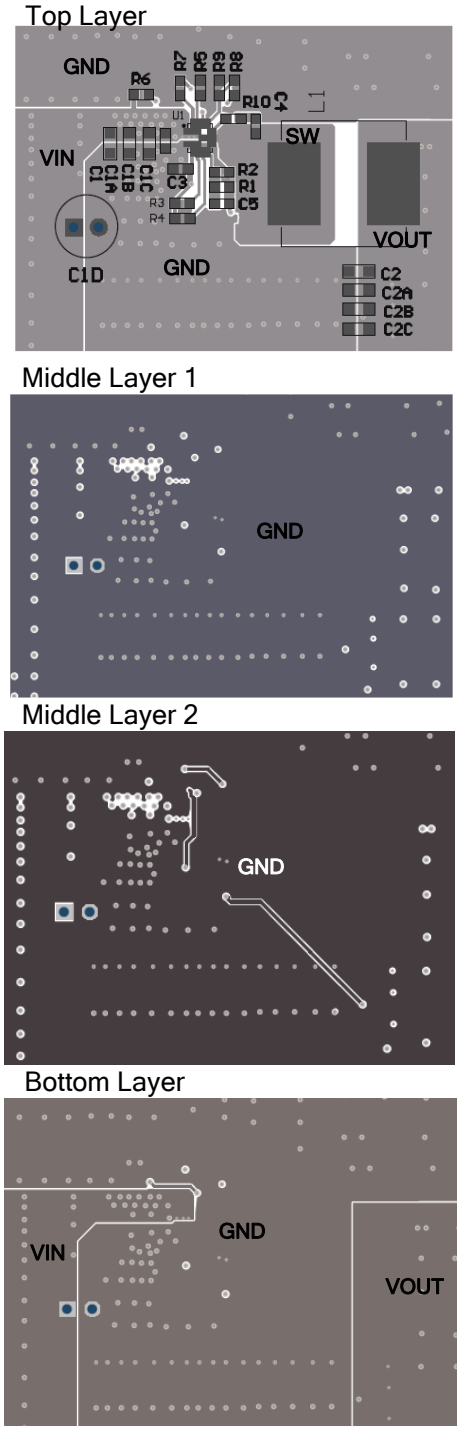


**Figure 9: Recommended Layout**


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## TYPICAL APPLICATION CIRCUITS

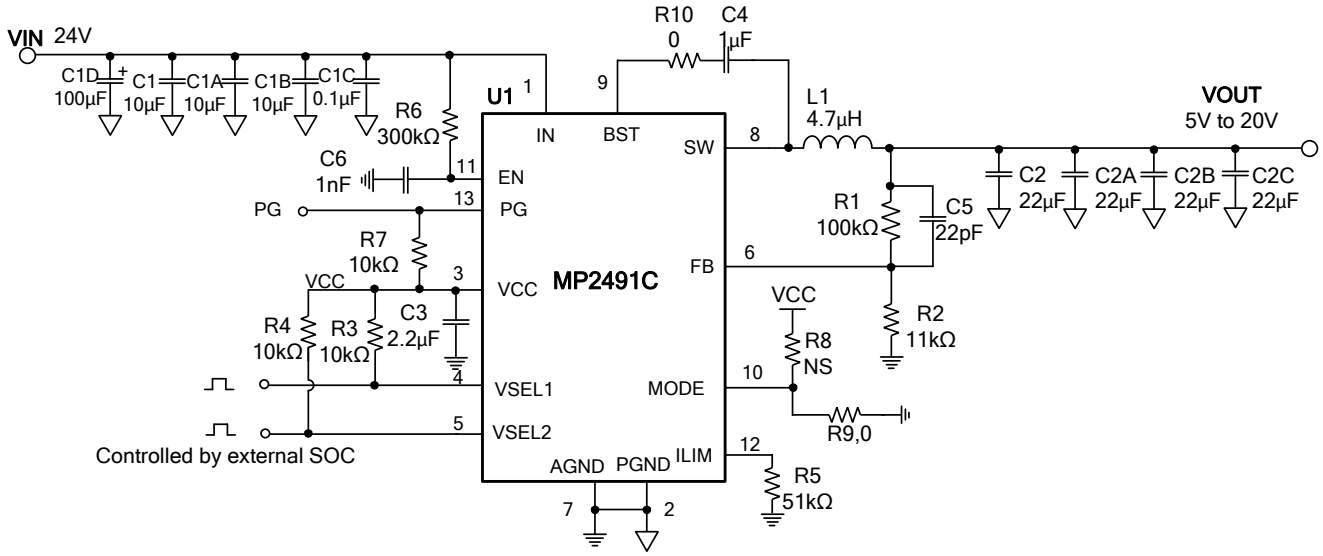


**Figure 10: USB PD Typical Application, $V_{IN}$ = 24V, $V_{OUT}$ = 5V to 20V**

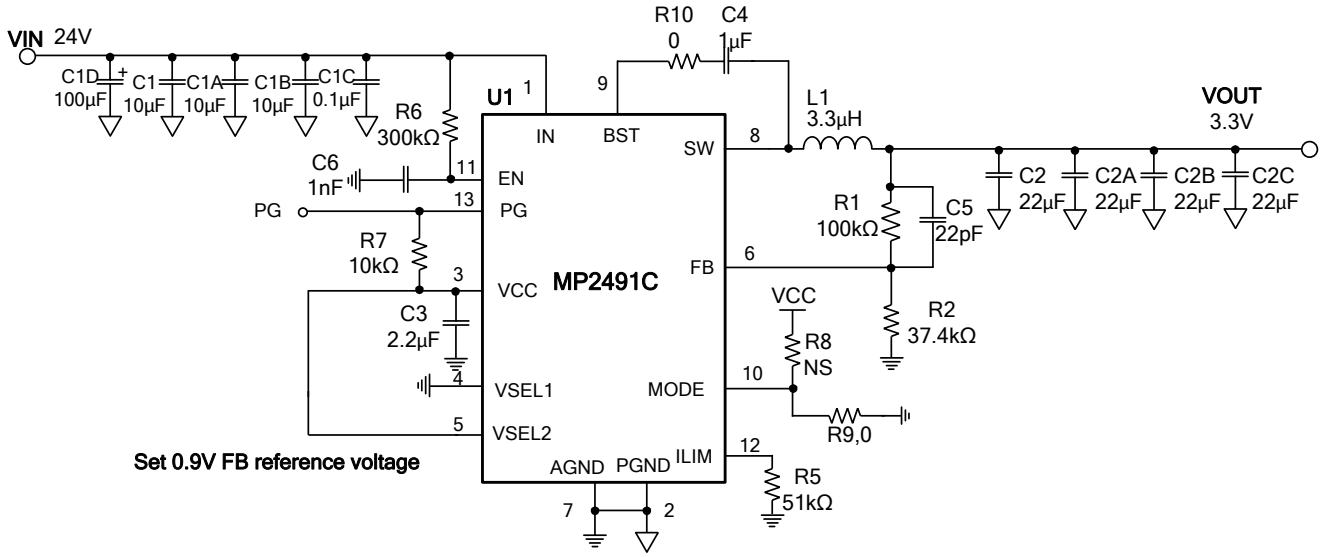


**Figure 11: $V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A**


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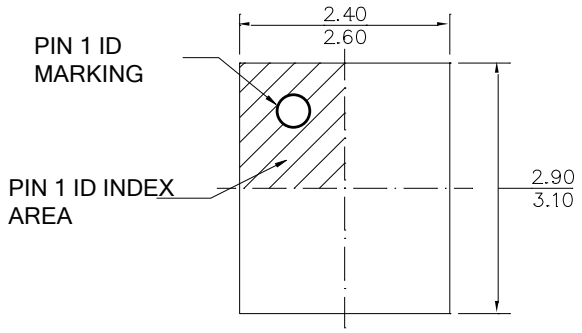
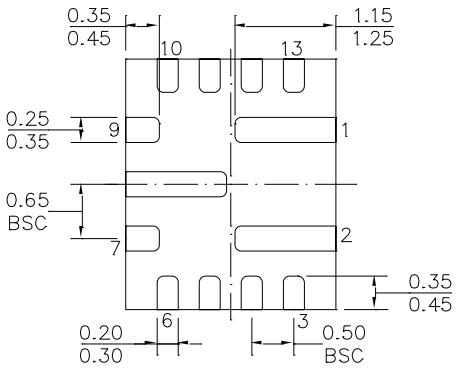
# PACKAGE INFORMATION

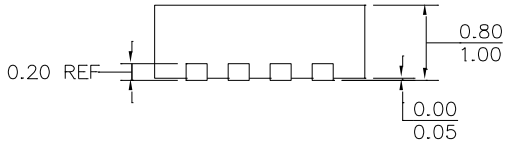
## QFN-13 (2.5mmx3.0mm)



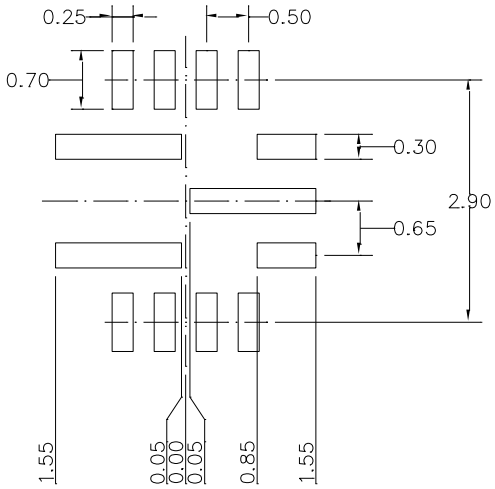

TOP VIEW




BOTTOM VIEW




SIDE VIEW




RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,PIN2,PIN8 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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