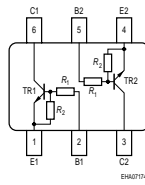
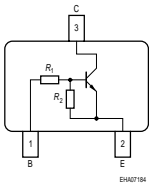


NPN Silicon Digital Transistor

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ($R_1=4.7\text{ k}\Omega$, $R_2=47\text{ k}\Omega$)
- BCR116S: Two internally isolated transistors with good matching in one multichip package
- BCR116S: For orientation in reel see package information below


**BCR116/F/L3
BCR116T/W**
BCR116S


Type	Marking	Pin Configuration						Package
BCR116	WG _s	1=B	2=E	3=C	-	-	-	SOT23
BCR116F	WG _s	1=B	2=E	3=C	-	-	-	TSFP-3
BCR116L3	WG	1=B	2=E	3=C	-	-	-	TSLP-3-4
BCR116S	WG _s	1=E1	2=B1	3=C2	4=E2	5=B2	6=C1	SOT363
BCR116T	WG	1=B	2=E	3=C	-	-	-	SC75
BCR116W	WG _s	1=B	2=E	3=C	-	-	-	SOT323

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	30	
Input reverse voltage	$V_{i(rev)}$	5	
Collector current	I_C	100	mA
Total power dissipation- BCR116, $T_S \leq 102^\circ\text{C}$ BCR116F, $T_S \leq 128^\circ\text{C}$ BCR116L3, $T_S \leq 135^\circ\text{C}$ BCR116S, $T_S \leq 115^\circ\text{C}$ BCR116T, $T_S \leq 109^\circ\text{C}$ BCR116W, $T_S \leq 124^\circ\text{C}$	P_{tot}	200 250 250 250 250 250	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}		K/W
BCR116		≤ 240	
BCR116F		≤ 90	
BCR116L3		≤ 60	
BCR116S		≤ 140	
BCR116T		≤ 165	
BCR116W		≤ 105	

¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

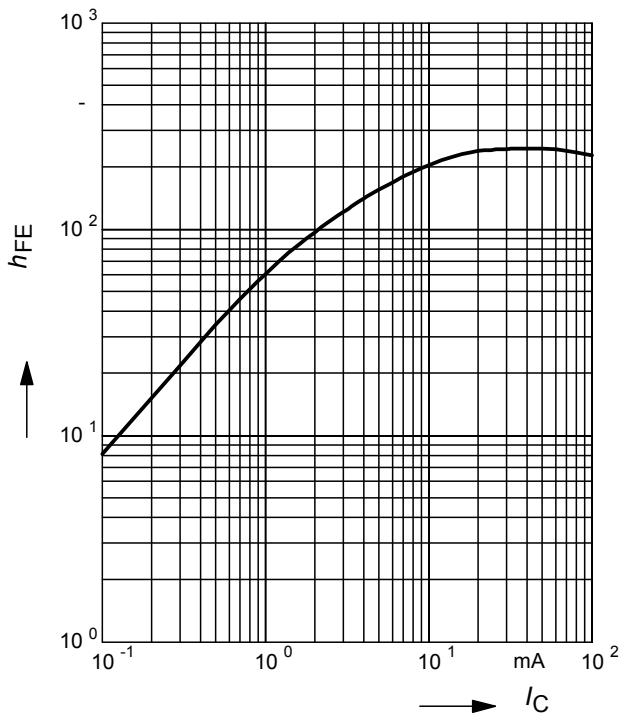
Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_E = 0$	$V_{(BR)CBO}$	50	-	-	
Collector-base cutoff current $V_{CB} = 40 \text{ V}, I_E = 0$	I_{CBO}	-	-	100	nA
Emitter-base cutoff current $V_{EB} = 5 \text{ V}, I_C = 0$	I_{EBO}	-	-	155	μA
DC current gain ¹⁾ $I_C = 5 \text{ mA}, V_{CE} = 5 \text{ V}$	h_{FE}	70	-	-	-
Collector-emitter saturation voltage ¹⁾ $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$	$V_{i(off)}$	0.4	-	0.8	
Input on voltage $I_C = 2 \text{ mA}, V_{CE} = 0.3 \text{ V}$	$V_{i(on)}$	0.5	-	1.4	
Input resistor	R_1	3.2	4.7	6.2	$\text{k}\Omega$
Resistor ratio	R_1/R_2	0.09	0.1	0.11	-
AC Characteristics					
Transition frequency $I_C = 10 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	f_T	-	150	-	MHz
Collector-base capacitance $V_{CB} = 10 \text{ V}, f = 1 \text{ MHz}$	C_{cb}	-	3	-	pF

¹Pulse test: $t < 300 \mu\text{s}$; $D < 2\%$

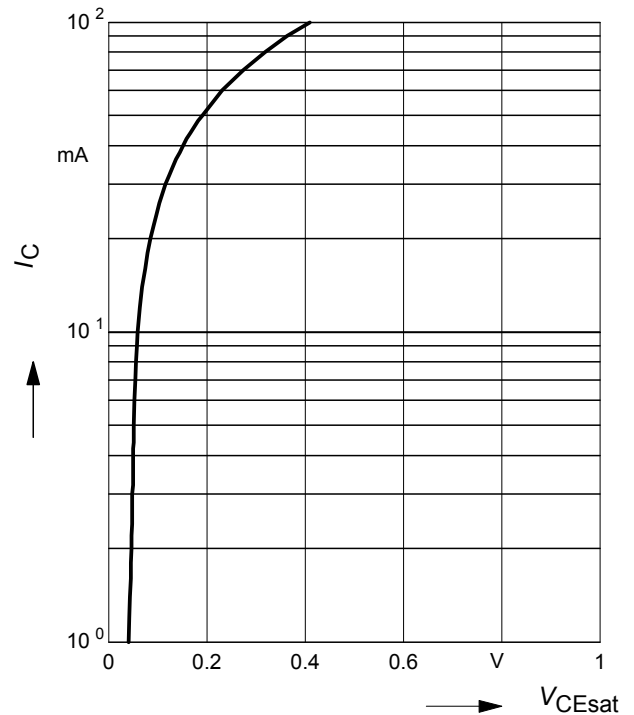
DC current gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



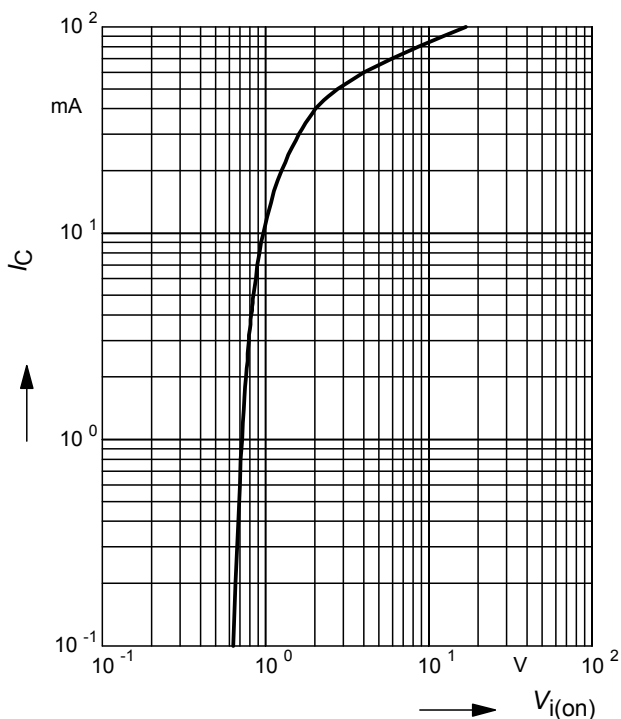
Collector-emitter saturation voltage

$V_{CEsat} = f(I_C), h_{FE} = 20$



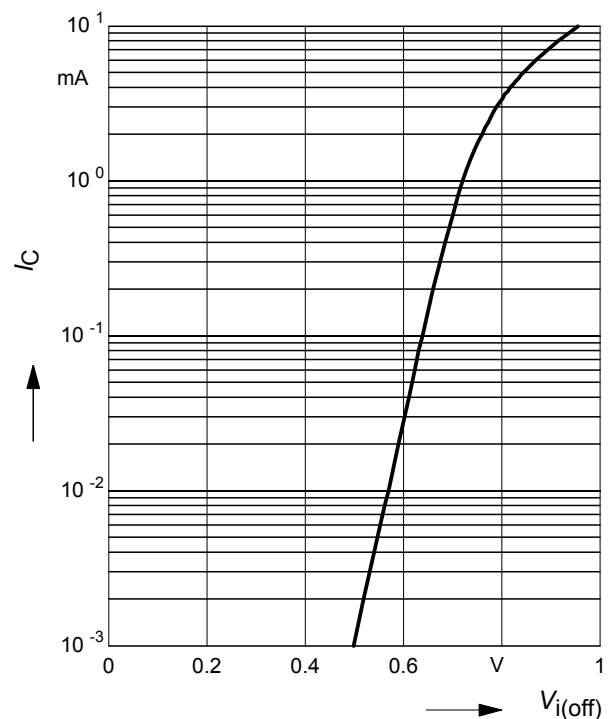
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)



Input off voltage $V_{i(off)} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



Total power dissipation $P_{tot} = f(T_S)$

BCR116



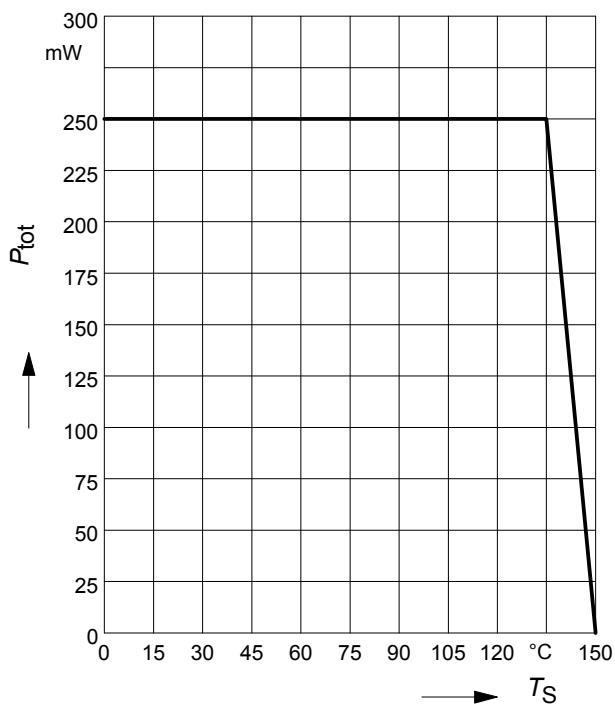
Total power dissipation $P_{tot} = f(T_S)$

BCR116F



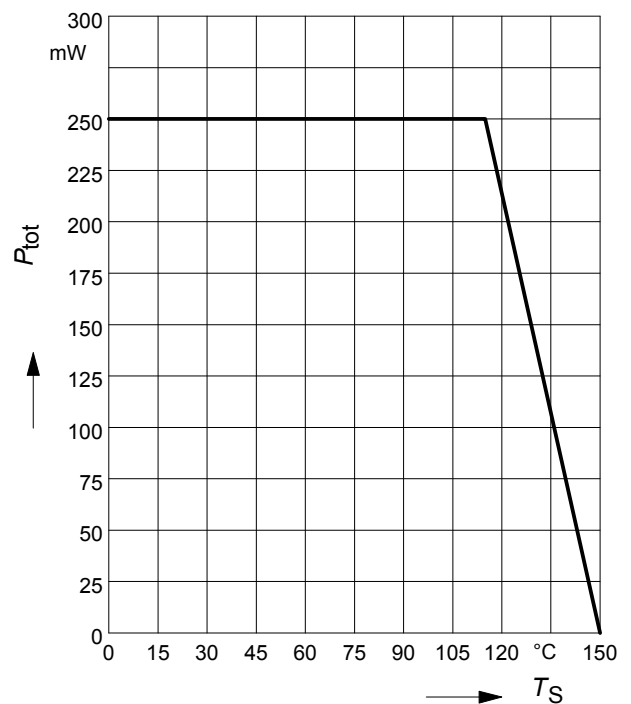
Total power dissipation $P_{tot} = f(T_S)$

BCR116L3



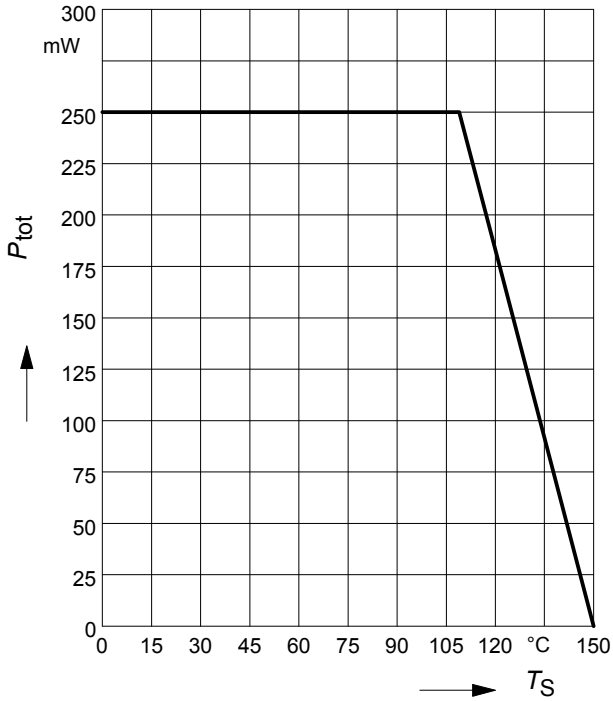
Total power dissipation $P_{tot} = f(T_S)$

BCR116S



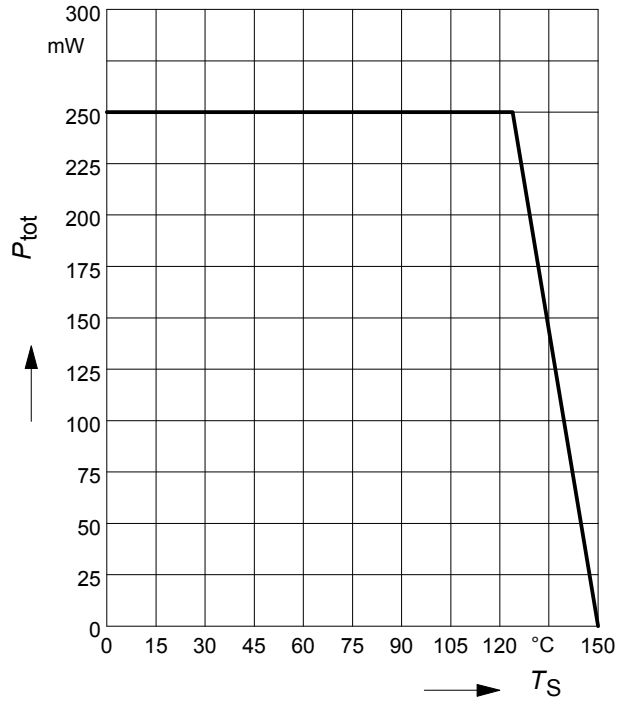
Total power dissipation $P_{tot} = f(T_S)$

BCR116T



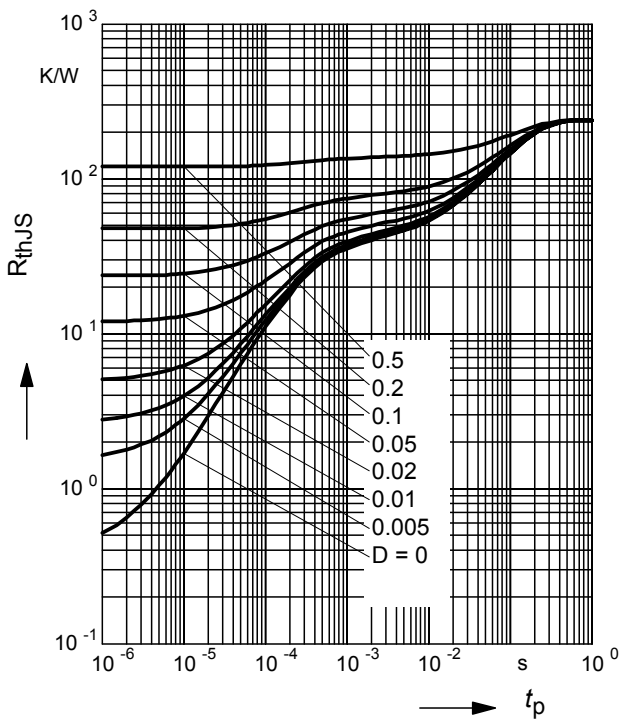
Total power dissipation $P_{tot} = f(T_S)$

BCR116W



Permissible Pulse Load $R_{thJS} = f(t_p)$

BCR116



Permissible Pulse Load

$P_{totmax}/P_{totDC} = f(t_p)$

BCR116



Permissible Puls Load $R_{thJS} = f(t_p)$

BCR116F



Permissible Pulse Load

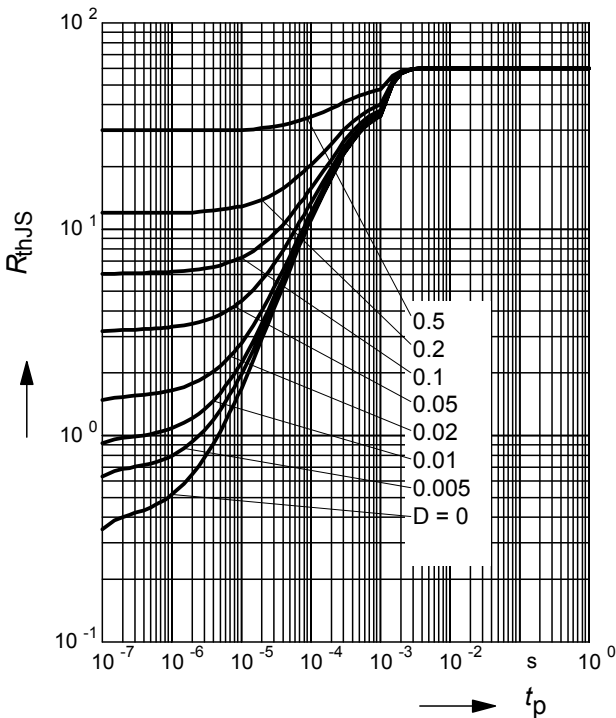
$P_{totmax}/P_{totDC} = f(t_p)$

BCR116F



Permissible Puls Load $R_{thJS} = f(t_p)$

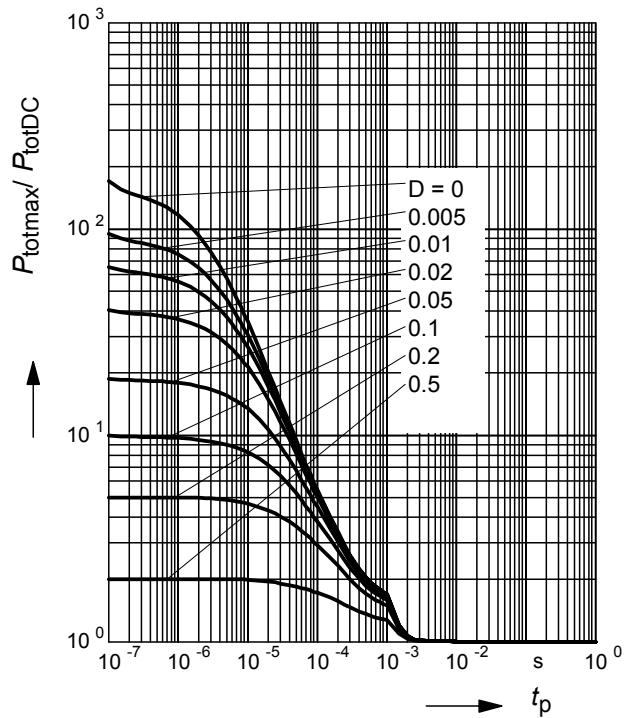
BCR116L3



Permissible Pulse Load

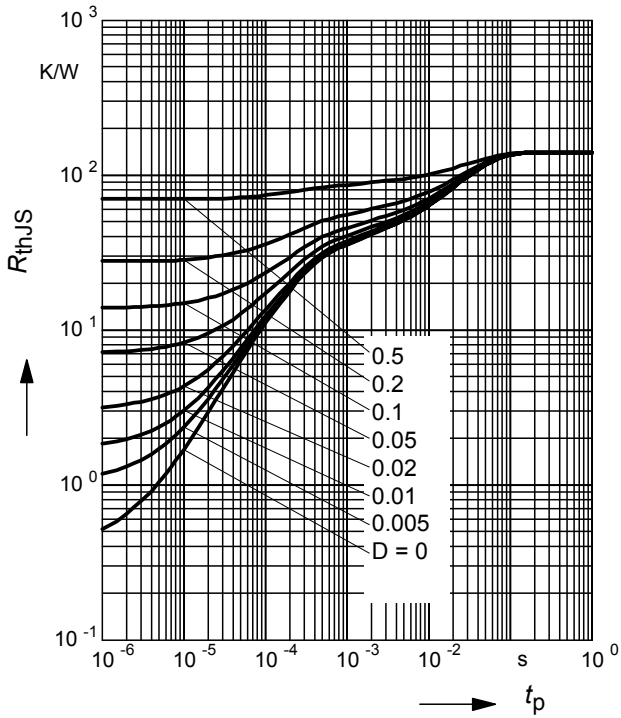
$P_{totmax}/P_{totDC} = f(t_p)$

BCR116L3



Permissible Puls Load $R_{thJS} = f(t_p)$

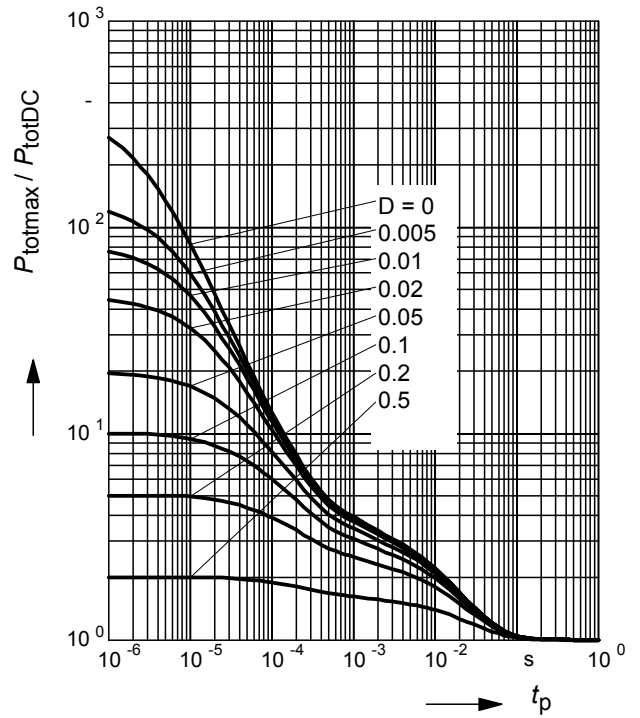
BCR116S



Permissible Pulse Load

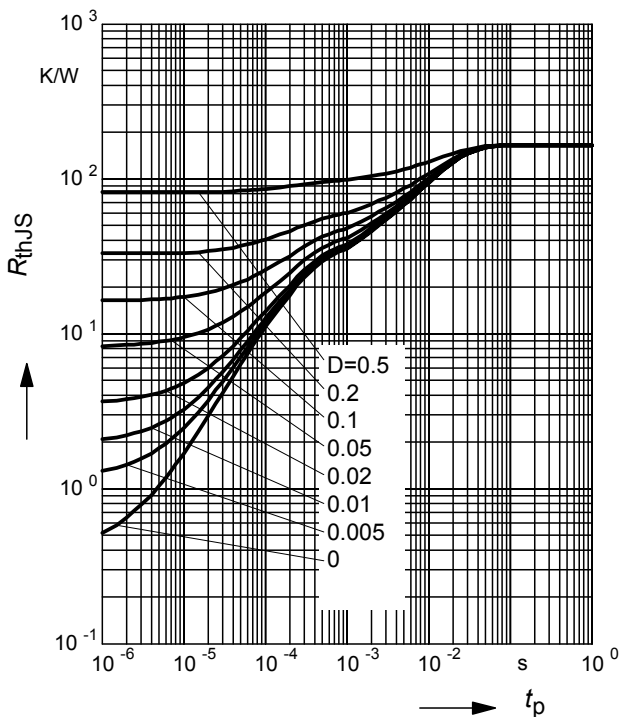
$P_{totmax}/P_{totDC} = f(t_p)$

BCR116S



Permissible Puls Load $R_{thJS} = f(t_p)$

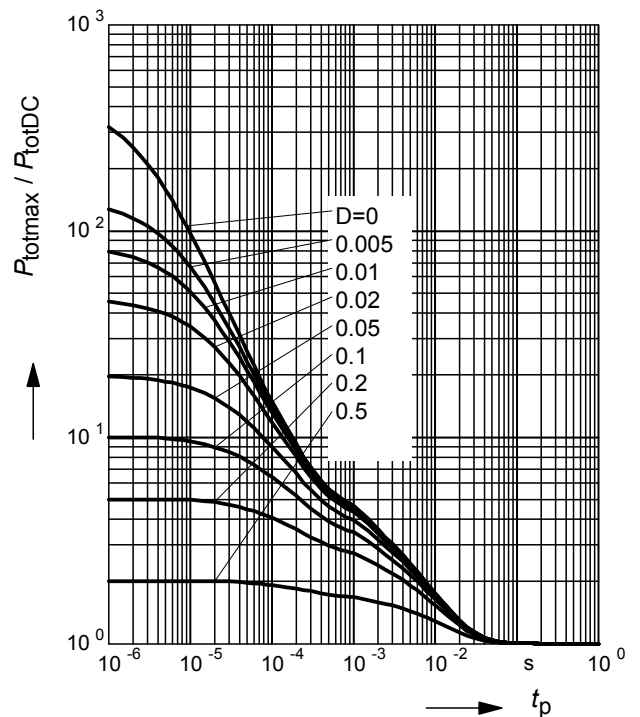
BCR116T



Permissible Pulse Load

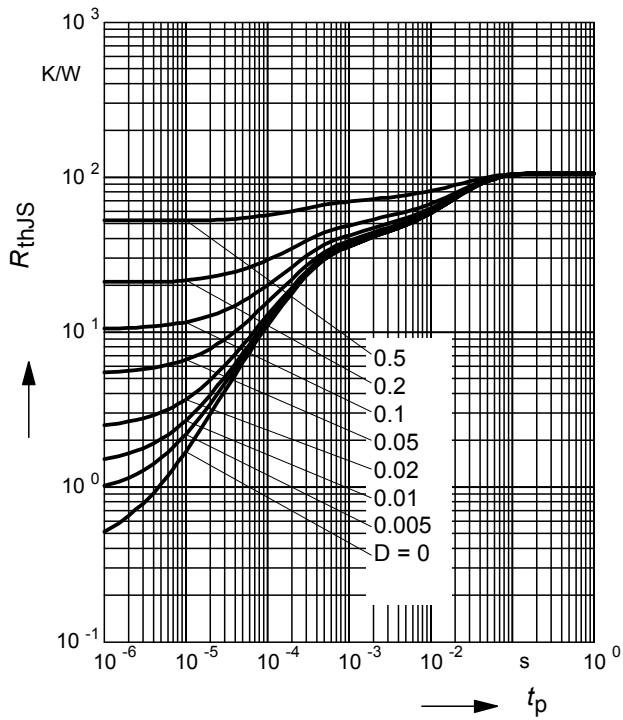
$P_{totmax}/P_{totDC} = f(t_p)$

BCR116T



Permissible Puls Load $R_{thJS} = f(t_p)$

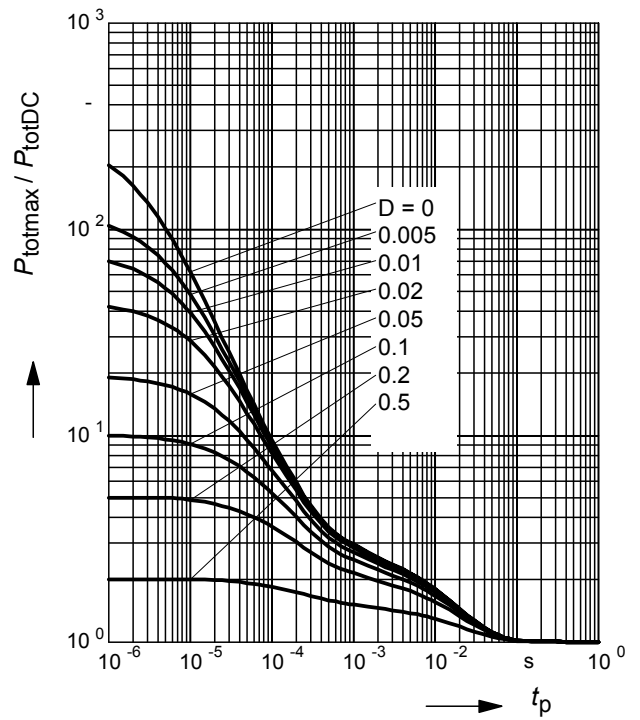
BCR116W



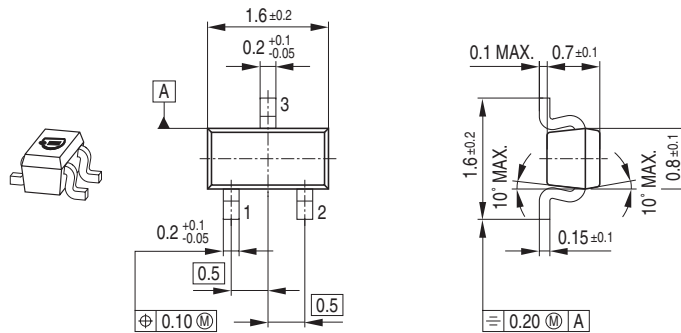
Permissible Pulse Load

$P_{totmax}/P_{totDC} = f(t_p)$

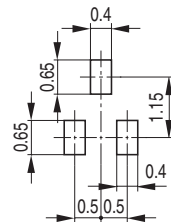
BCR116W



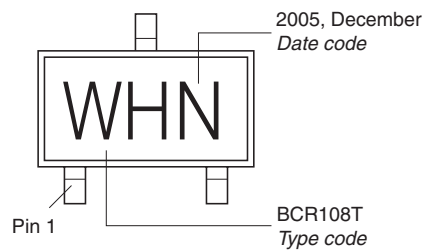
Package Outline



Foot Print

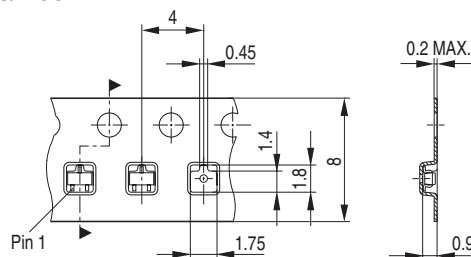


Marking Layout (Example)



Standard Packing

Reel $\varnothing 180 \text{ mm} = 3.000 \text{ Pieces/Reel}$
 Reel $\varnothing 330 \text{ mm} = 10.000 \text{ Pieces/Reel}$

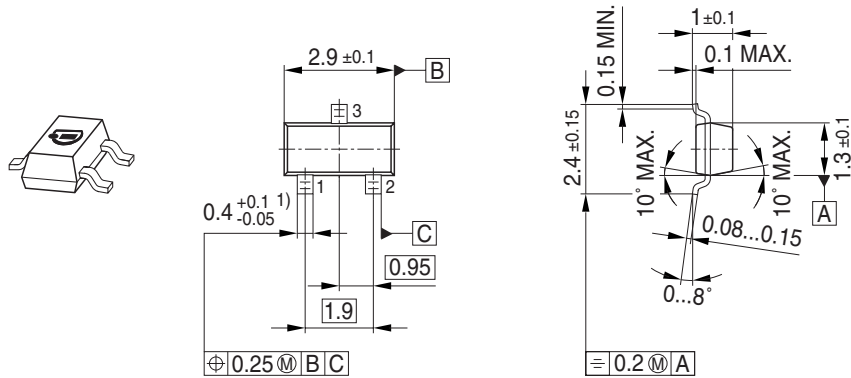


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75¹⁾) CES-Code

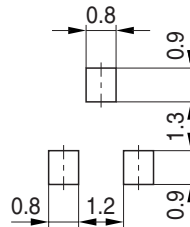
Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

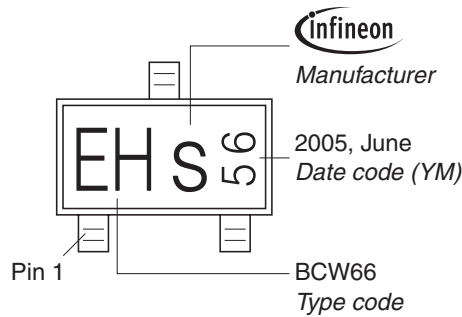
Package Outline



Foot Print

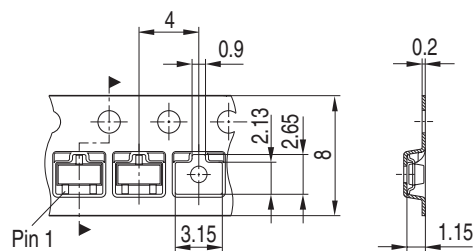


Marking Layout (Example)

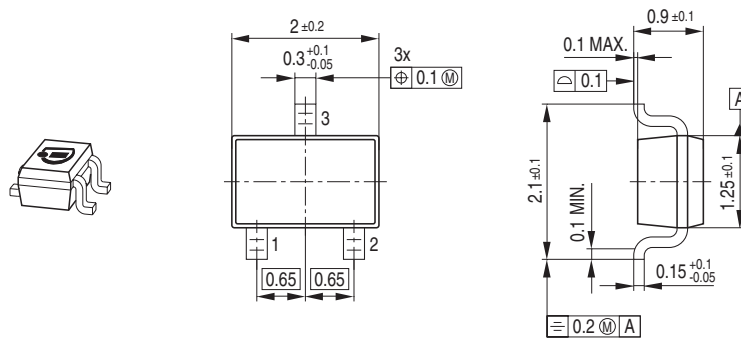


Standard Packing

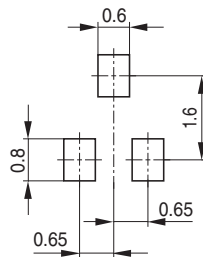
Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



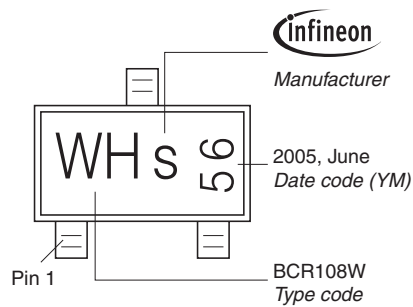
Package Outline



Foot Print

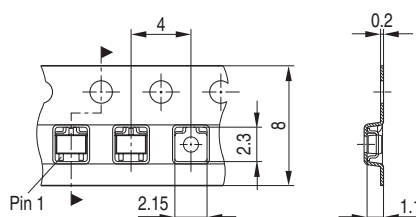


Marking Layout (Example)

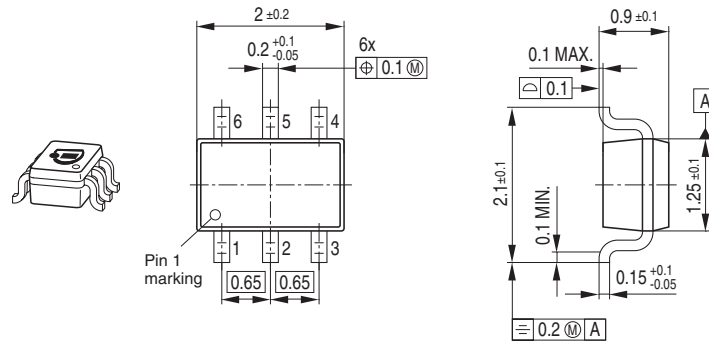


Standard Packing

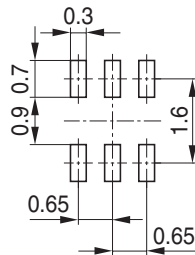
Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



Package Outline

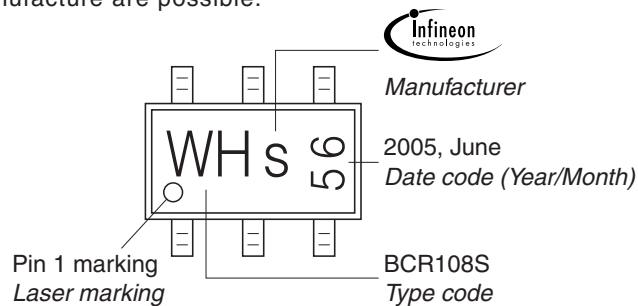


Foot Print



Marking Layout (Example)

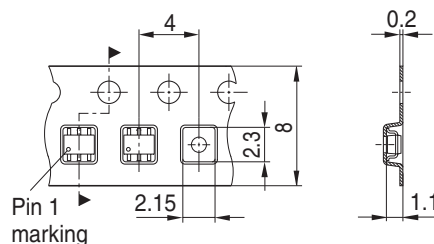
Small variations in positioning of Date code, Type code and Manufacture are possible.



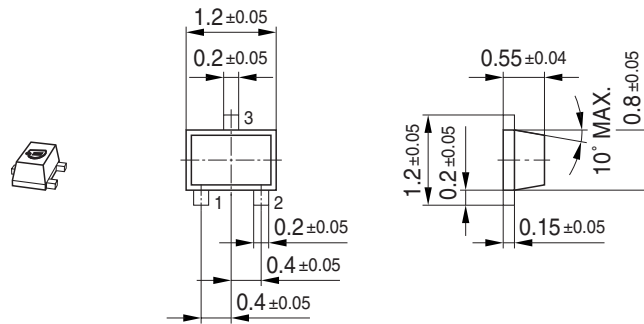
Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel

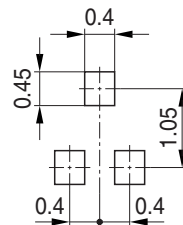
For symmetric types no defined Pin 1 orientation in reel.



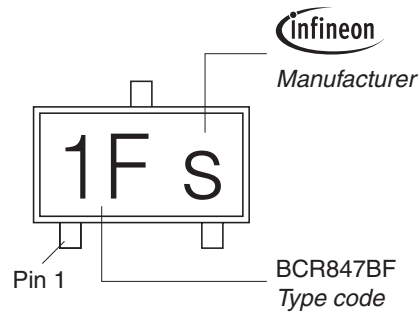
Package Outline



Foot Print

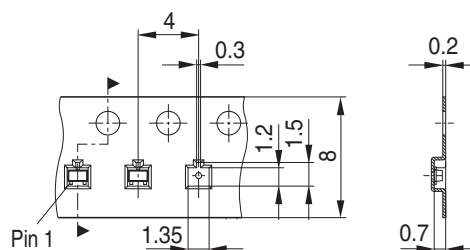


Marking Layout (Example)

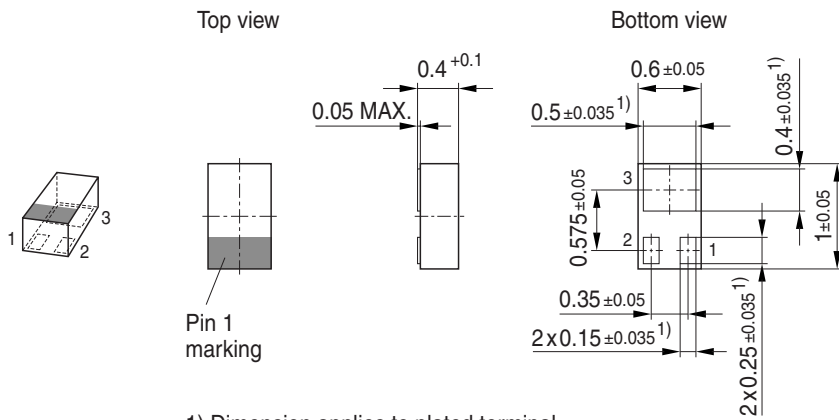


Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



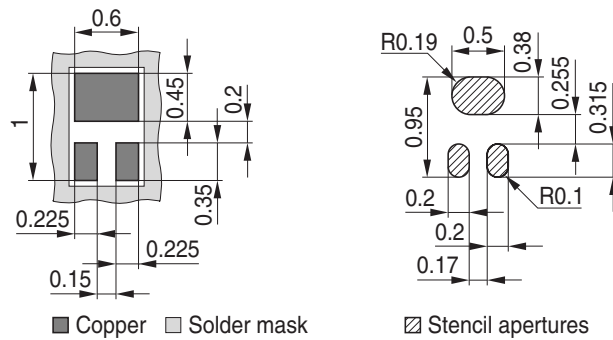
Package Outline



1) Dimension applies to plated terminal

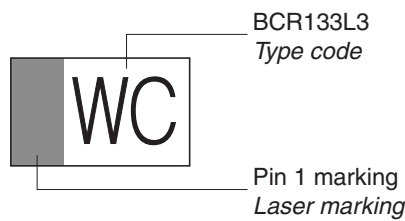
Foot Print

For board assembly information please refer to Infineon website "Packages"



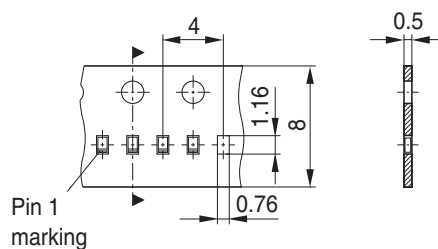
■ Copper □ Solder mask ▨ Stencil apertures

Marking Layout



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



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