Device Overview

The 89HPES16T7 is a member of the IDT PRECISE™ family of PCI Express switching solutions. The PES16T7 is a 16-lane, 7-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high performance applications such as servers, storage and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to six downstream ports and supports switching between downstream ports.

Features

- **High Performance PCI Express Switch**
  - *Sixteen 2.5 Gbps PCI Express lanes*
  - *Seven switch ports*
  - *Upstream port configurable up to x8*
  - *Two downstream ports configurable up to x4, four downstream ports are x1*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Sizes up to 2048 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Automatic per port link width negotiation to x8, x4, x2 or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- **Legacy Support**
  - *PCI compatible INTx emulation*
  - *Bus locking*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates sixteen 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Supports ECRC and Advanced Error Reporting*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC and server motherboards*
- **Power Management**
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.1)*
    - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
  - *Unused SerDes are disabled*

Block Diagram

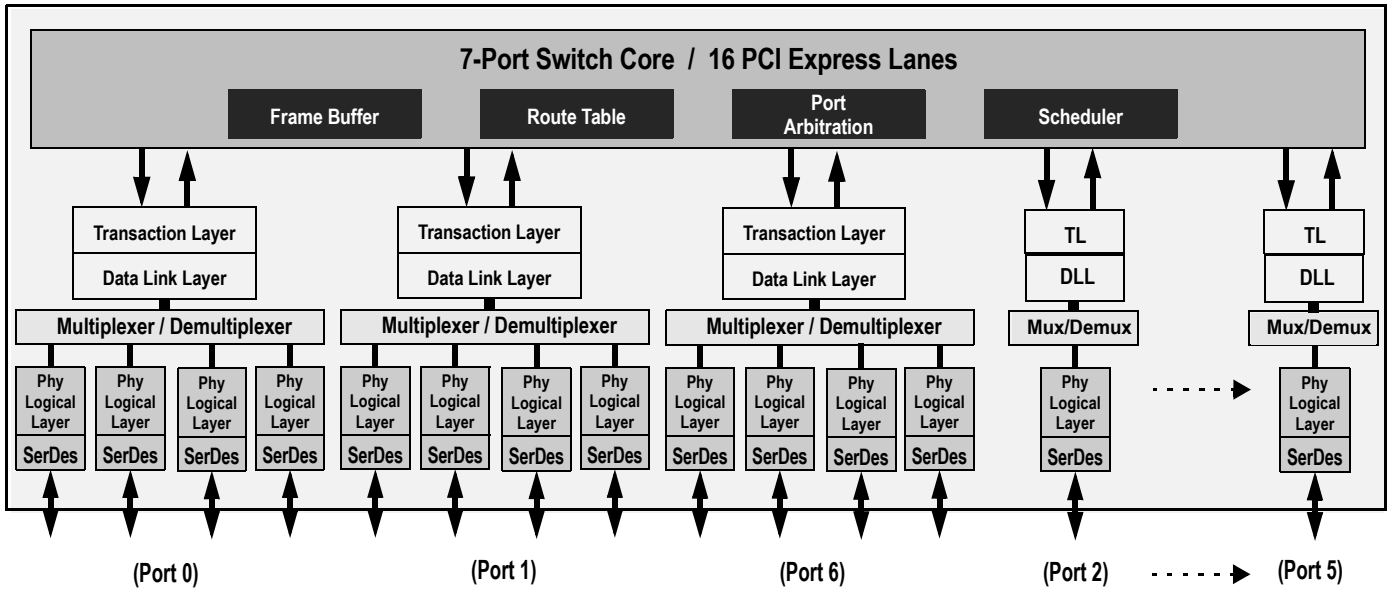


Figure 1 Internal Block Diagram

- **Testability and Debug Features**
  - *Ability to read and write any internal register via the SMBus*
- **Twelve General Purpose Input/Output pins**
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- **Packaged in a 25mm x 25mm 320-ball BGA with 1 mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES16T7 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 7 ports across 16 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification revision 1.1.

The PES16T7 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers. The PES16T7 can operate either as a store and forward switch or a cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to allow efficient switching for applications requiring additional narrow port connectivity and also some high-end connectivity.

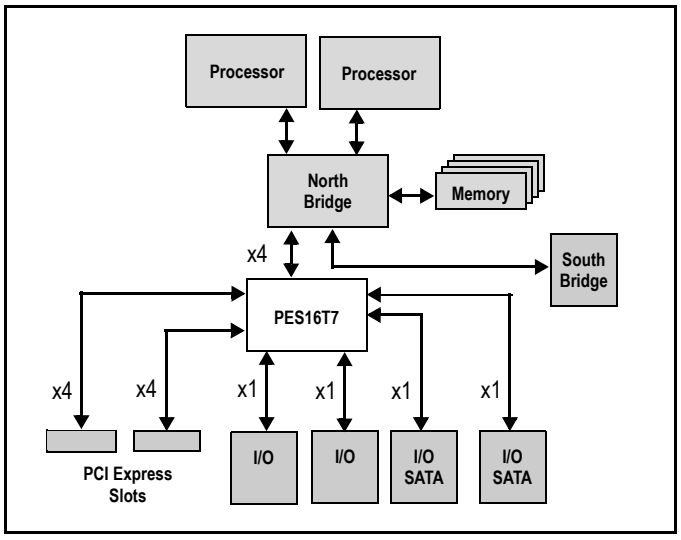


Figure 2 I/O Expansion Application

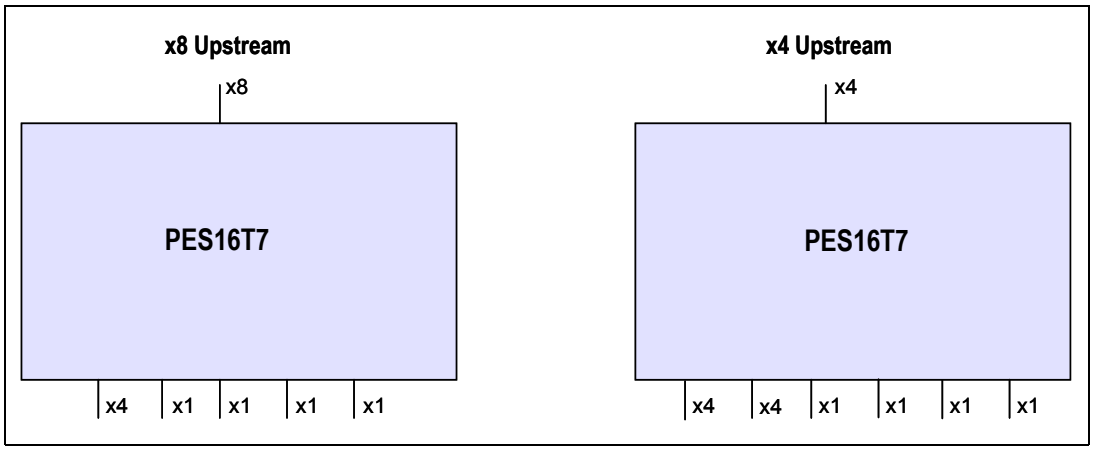


Figure 3 Configuration Options

SMBus Interface

The PES16T7 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES16T7, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES16T7 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 4, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 4(a), the master and slave SMBuses are tied together and the PES16T7 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES16T7 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES16T7 may be configured to operate in a split configuration as shown in Figure 4(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES16T7 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

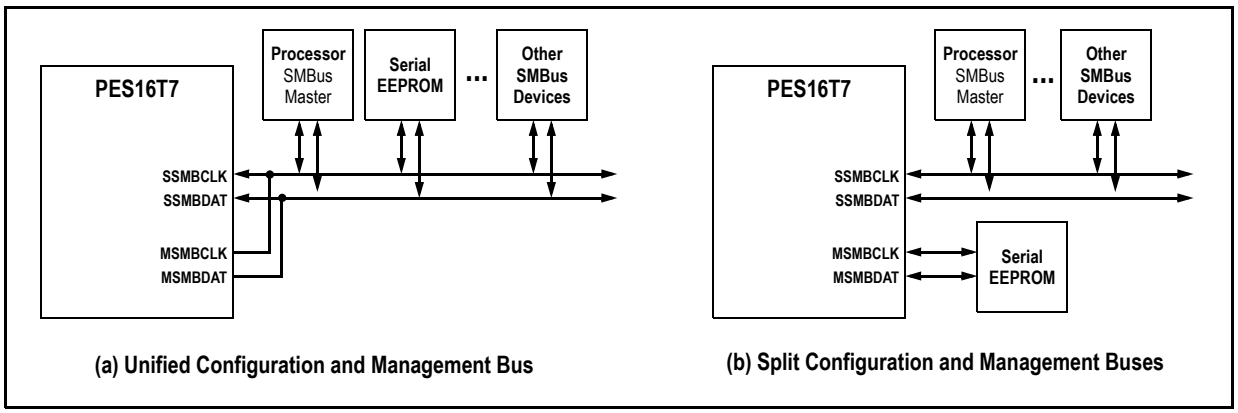


Figure 4 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES16T7 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES16T7 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES16T7 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES16T7. In response to an I/O expander interrupt, the PES16T7 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES16T7 provides 12 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES16T7. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE1RP[3:0] PE1RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1.
PE1TP[3:0] PE1TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1.
PE2RP[0] PE2RN[0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[0] PE2TN[0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE3RP[0] PE3RN[0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pair for port 3.
PE4RP[0] PE4RN[0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pair for port 4.
PE4TP[0] PE4TN[0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pair for port 4.
PE5RP[0] PE5RN[0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pair for port 5.
PE5TP[0] PE5TN[0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pair for port 5.
PE6RP[3:0] PE6RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pair for port 6.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE6TP[3:0] PE6TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pair for port 6.
PEREFCLKP[2:1] PEREFCLKN[2:1]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input

Table 4 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: I/O Expander interrupt 1 input
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: I/O Expander interrupt 3 input
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P6RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 6

Table 4 General Purpose I/O Pins (Part 2 of 2)

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. This value may not be overridden.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside PES16T7 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES16T7 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES16T7 switch operating mode. These pins should be static and not change after the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved

Table 5 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.

Table 6 Test Pins (Part 1 of 2)

Signal	Type	Name/Description
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}IO	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	**Ground.**

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES16T7 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	CML	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE1RN[3:0]	I				
	PE1RP[3:0]	I				
	PE1TN[3:0]	O				
	PE1TP[3:0]	O				
	PE2RN[0]	I				
	PE2RP[0]	I				
	PE2TN[0]	O				
	PE2TP[0]	O				
	PE3RN[0]	I				
	PE3RP[0]	I				
	PE3TN[0]	O				
	PE3TP[0]	O				
	PE4RN[0]	I				
	PE4RP[0]	I				
	PE4TN[0]	O				
	PE4TP[0]	O				
	PE5RN[0]	I				
	PE5RP[0]	I				
	PE5TN[0]	O				
	PE5TP[0]	O				
	PE6RN[3:0]	I				
	PE6RP[3:0]	I				
	PE6TN[3:0]	O				
	PE6TP[3:0]	O				
	PEREFCLKN[2:1]	I	LVPECL/ CML	Diff Clock Input		Refer to Table 9
	PEREFCLKP[2:1]	I				
	REFCLKM	I	LVTTL	Input	pull-down	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[2]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[11:0]	I/O	LVTTL	High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[2:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 54K Ω for pull-up and 251K Ω for pull-down.
2. Schmitt Trigger Input (STI).

Logic Diagram — PES16T7

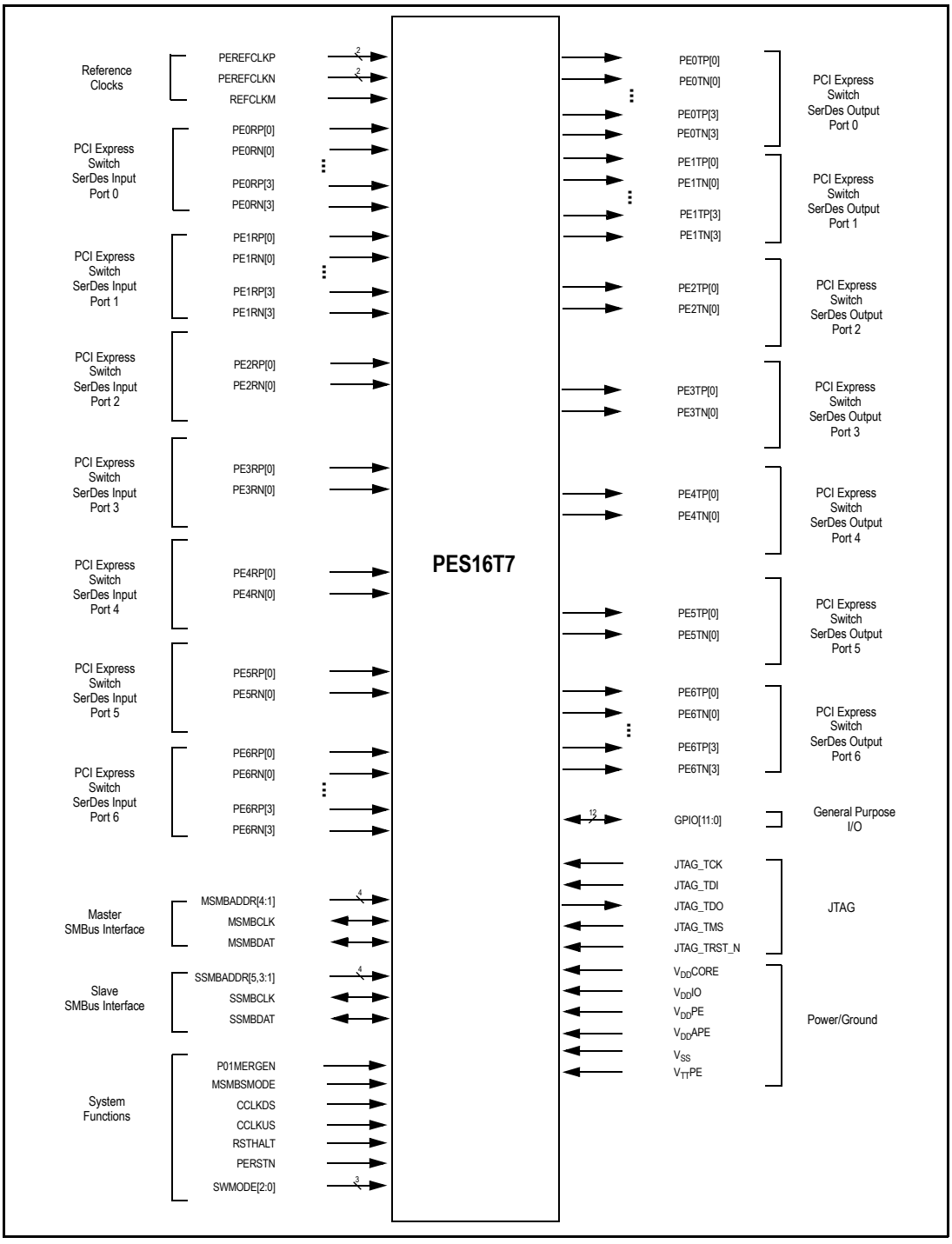


Figure 5 PES16T7 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[11:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 6.

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

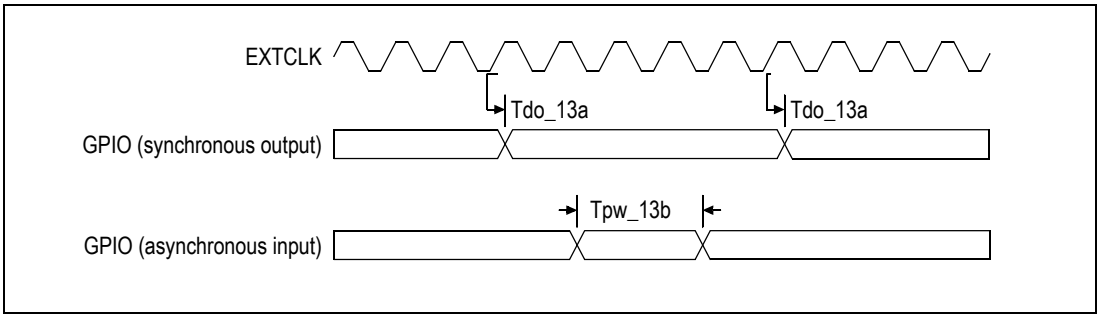


Figure 6 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 7.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

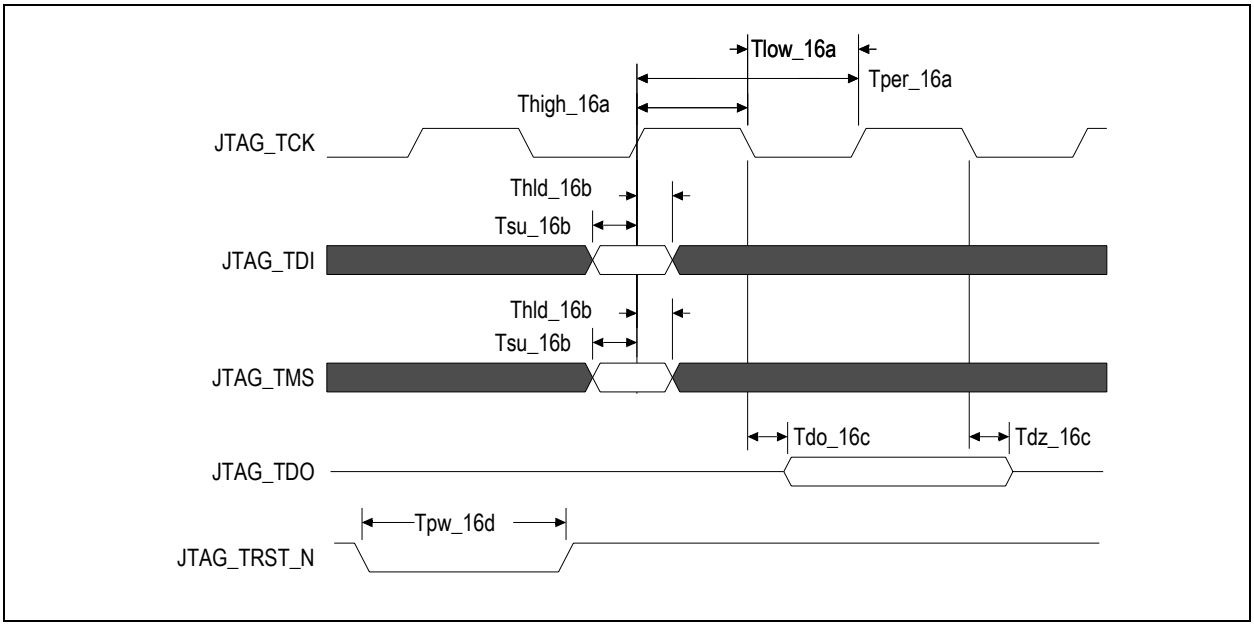


Figure 7 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES16T7 Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES16T7, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 14 PES16T7 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
8/4/1/1/1/1	mA	793	1013	974	1123	486	522	369	419	1	1	2.8W	3.6W
	Watts	0.79	1.11	0.97	1.24	0.49	0.57	0.55	0.66	0.003	0.004		

Table 15 PES16T7 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES16T7 (25mm^2 BXG320 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES16T7 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	12.8	°C/W	Zero air flow
		10.1	°C/W	1 m/S air flow
		9.1	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	7.5	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.7	°C/W	
P	Power Dissipation of the Device	3.6	Watts	Maximum

Table 16 Thermal Specifications for PES16T7, 25x25 mm BXG320 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

Heat Sink

Table 17 lists heat sink requirements for the PES16T7 under two common usage scenarios. As shown in this table, a heat sink is not required in most cases.

Air Flow	Board Size	Board Layers	Heat Sink Requirement
Zero	3.9"x6.2" (ExpressModule form factor) or larger	10 or more	No heat sink required
1 m/S or more	Any	Any	No heat sink required

Table 17 Heat Sink Requirements Based on Air Flow and Board Characteristics

Thermal Usage Examples

The junction-to-ambient thermal resistance is a measure of a device's ability to dissipate heat from the die to its surroundings in the absence of a heat sink. The general formula to determine θ_{JA} is:

$$\theta_{JA} = (T_J - T_A)/P$$

Thermal reliability of a device is generally assured when the actual value of T_J in the specific system environment being considered is less than the maximum T_J specified for the device. Using an ambient temperature of 70°C and assuming a system with 1m/S airflow, the actual value of T_J is:

$$T_{J(actual)} = T_A + P * \theta_{JA(eff)} = 70^oC + 3.6W * 10.1W/^oC = 106^oC$$

The actual T_J of 106°C is well below the maximum T_J of 125°C specified for the device (shown in Table 16). Therefore, no heat sink is needed in this scenario. The formula is also useful from a system design perspective. It can be used to determine if a heat sink should be added to the device based on some desired value of T_J. For example, if for reliability purposes the desired T_J is 100°C, then the maximum allowable T_A is:

$$T_{A(allowed)} = T_{J(desired)} - (P * \theta_{JA(effective)})$$
$$T_{A(allowed)} = 100^oC - (3.6W * 10.1W/^oC) = 100^oC - 36^oC = 64^oC$$

An appropriate level of increased air flow and/or a heat sink can be added to achieve this lower ambient temperature. Please contact ssdhelp@idt.com for further assistance.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	$V_{DD}I/O$ (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

Package Pinout — 320-BGA Signal Pinout for PES16T7

The following table lists the pin numbers and signal names for the PES16T7 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B11	V_{SS}		C21	V_{DD}CORE		E23	V_{DD}PE	
A2	V_{SS}		B12	PE6TP02		C22	V_{SS}		E24	V_{DD}CORE	
A3	V_{DD}CORE		B13	V_{SS}		C23	V_{SS}		F1	V_{SS}	
A4	V_{DD}CORE		B14	PE6TN03		C24	V_{DD}CORE		F2	V_{DD}APE	
A5	V_{SS}		B15	V_{SS}		D1	V_{DD}CORE		F3	V_{DD}IO	
A6	V_{DD}CORE		B16	V_{DD}APE		D2	V_{SS}		F4	V_{SS}	
A7	V_{SS}		B17	V_{DD}APE		D3	V_{DD}CORE		F21	V_{DD}APE	
A8	PE6TP00		B18	MSMBSMODE		D4	V_{DD}PE		F22	V_{DD}APE	
A9	V_{DD}CORE		B19	V_{DD}IO		D5	V_{DD}PE		F23	V_{DD}PE	
A10	PE6TN01		B20	V_{DD}CORE		D6	V_{SS}		F24	V_{SS}	
A11	V_{SS}		B21	V_{SS}		D7	PE6RP00		G1	V_{DD}CORE	
A12	PE6TN02		B22	V_{DD}CORE		D8	V_{SS}		G2	V_{DD}APE	
A13	V_{SS}		B23	V_{DD}CORE		D9	V_{TT}PE		G3	V_{DD}PE	
A14	PE6TP03		B24	V_{SS}		D10	V_{SS}		G4	P01MERGEN	
A15	V_{SS}		C1	V_{SS}		D11	PE6RN01		G21	GPIO_11	1
A16	V_{DD}CORE		C2	V_{DD}CORE		D12	V_{DD}APE		G22	GPIO_10	1
A17	V_{SS}		C3	V_{SS}		D13	PE6RP02		G23	V_{DD}PE	
A18	V_{DD}CORE		C4	V_{DD}APE		D14	V_{TT}PE		G24	V_{DD}CORE	
A19	V_{DD}CORE		C5	V_{DD}PE		D15	PE6RP03		H1	V_{SS}	
A20	V_{SS}		C6	V_{SS}		D16	V_{SS}		H2	V_{DD}APE	
A21	V_{DD}CORE		C7	PE6RN00		D17	V_{TT}PE		H3	V_{DD}APE	
A22	V_{SS}		C8	V_{SS}		D18	V_{DD}PE		H4	V_{TT}PE	
A23	V_{DD}CORE		C9	V_{SS}		D19	V_{DD}APE		H21	GPIO_09	1
A24	V_{SS}		C10	V_{DD}PE		D20	V_{DD}CORE		H22	GPIO_08	1
B1	V_{DD}CORE		C11	PE6RP01		D21	V_{SS}		H23	V_{DD}APE	
B2	V_{DD}CORE		C12	V_{DD}APE		D22	V_{DD}CORE		H24	V_{SS}	
B3	V_{DD}CORE		C13	PE6RN02		D23	V_{DD}CORE		J1	PEREFCLKN1	
B4	V_{DD}APE		C14	V_{SS}		D24	V_{SS}		J2	V_{SS}	
B5	V_{DD}CORE		C15	PE6RN03		E1	V_{SS}		J3	V_{SS}	
B6	V_{DD}IO		C16	V_{DD}PE		E2	V_{DD}APE		J4	V_{SS}	
B7	V_{SS}		C17	V_{DD}PE		E3	V_{DD}IO		J21	V_{DD}APE	
B8	PE6TN00		C18	REFCLKM		E4	V_{DD}CORE		J22	V_{DD}APE	
B9	V_{SS}		C19	V_{DD}PE		E21	V_{DD}IO		J23	V_{DD}APE	
B10	PE6TP01		C20	V_{DD}APE		E22	V_{DD}IO		J24	PEREFCLKP2	

Table 19 PES16T7 320-pin Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
K1	PEREFCLKP1		P22	PE5RN00		W3	SSMBADDR_3		AA24	V_{DD}IO	
K2	V_{DD}PE		P23	V_{SS}		W4	SSMBADDR_5		AB1	V_{DD}CORE	
K3	V_{DD}PE		P24	V_{SS}		W21	PERSTN		AB2	V_{DD}IO	
K4	V_{DD}PE		R1	V_{SS}		W22	SWMODE1		AB3	V_{DD}PE	
K21	V_{SS}		R2	V_{SS}		W23	SWMODE_0		AB4	PE1RN03	
K22	V_{SS}		R3	PE2RP00		W24	RSTHALT		AB5	V_{SS}	
K23	V_{SS}		R4	PE2RN00		Y1	SSMBDAT		AB6	PE1RN02	
K24	PEREFCKN2		R21	V_{TT}PE		Y2	V_{DD}IO		AB7	V_{DD}APE	
L1	V_{SS}		R22	V_{DD}PE		Y3	V_{DD}PE		AB8	PE1RP01	
L2	V_{SS}		R23	PE5TN00		Y4	CCLKUS		AB9	V_{SS}	
L3	V_{DD}APE		R24	PE5TP00		Y21	V_{SS}		AB10	V_{SS}	
L4	V_{DD}APE		T1	JTAG_TMS		Y22	V_{DD}APE		AB11	V_{SS}	
L21	V_{SS}		T2	JTAG_TCK		Y23	V_{DD}IO		AB12	PE1RN00	
L22	V_{DD}PE		T3	JTAG_TDI		Y24	CCLKDS		AB13	V_{DD}APE	
L23	V_{DD}PE		T4	JTAG_TDO		AA1	V_{DD}CORE		AB14	PE0RN03	
L24	V_{SS}		T21	GPIO_07	1	AA2	V_{DD}IO		AB15	V_{SS}	
M1	PE3TN00		T22	V_{DD}APE		AA3	V_{SS}		AB16	V_{DD}PE	
M2	PE3TP00		T23	V_{DD}PE		AA4	PE1RP03		AB17	PE0RN02	
M3	V_{TT}PE		T24	GPIO_06		AA5	V_{TT}PE		AB18	V_{DD}PE	
M4	V_{DD}PE		U1	MSMBADDR_3		AA6	PE1RP02		AB19	PE0RN01	
M21	PE4RP00		U2	JTAG_TRST_N		AA7	V_{SS}		AB20	V_{SS}	
M22	PE4RN00		U3	MSMBADDR_1		AA8	PE1RN01		AB21	PE0RN00	
M23	V_{SS}		U4	MSMBADDR_2		AA9	V_{DD}APE		AB22	V_{DD}APE	
M24	V_{SS}		U21	GPIO_04	1	AA10	V_{SS}		AB23	V_{DD}APE	
N1	V_{SS}		U22	GPIO_05	1	AA11	V_{TT}PE		AB24	V_{DD}CORE	
N2	V_{SS}		U23	GPIO_03	1	AA12	PE1RP00		AC1	V_{SS}	
N3	PE3RP00		U24	GPIO_02	1	AA13	V_{SS}		AC2	V_{DD}IO	
N4	PE3RN00		V1	SSMBADDR_1		AA14	PE0RP03		AC3	V_{DD}APE	
N21	V_{TT}PE		V2	MSMBADDR_4		AA15	V_{TT}PE		AC4	V_{SS}	
N22	V_{SS}		V3	MSMBCLK		AA16	V_{SS}		AC5	PE1TN03	
N23	PE4TN00		V4	MSMBDAT		AA17	PE0RP02		AC6	V_{SS}	
N24	PE4TP00		V21	GPIO_00	1	AA18	V_{DD}APE		AC7	PE1TP02	
P1	PE2TN00		V22	GPIO_01	1	AA19	PE0RP01		AC8	V_{SS}	
P2	PE2TP00		V23	V_{SS}		AA20	V_{TT}PE		AC9	PE1TP01	
P3	V_{DD}PE		V24	SWMODE_2		AA21	PE0RP00		AC10	V_{SS}	
P4	V_{DD}PE		W1	SSMBCLK		AA22	V_{DD}PE		AC11	PE1TN00	
P21	PE5RP00		W2	SSMBADDR_2		AA23	V_{DD}PE		AC12	V_{SS}	

Table 19 PES16T7 320-pin Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AC13	PE0TP03		AC22	V_{DD}PE		AD7	PE1TN02		AD16	PE0TN02	
AC14	V_{SS}		AC23	V_{DD}PE		AD8	V_{SS}		AD17	V_{SS}	
AC15	V_{SS}		AC24	V_{DD}CORE		AD9	PE1TN01		AD18	PE0TN01	
AC16	PE0TP02		AD1	V_{SS}		AD10	V_{SS}		AD19	V_{SS}	
AC17	V_{SS}		AD2	V_{DD}CORE		AD11	PE1TP00		AD20	PE0TP00	
AC18	PE0TP01		AD3	V_{DD}CORE		AD12	V_{SS}		AD21	V_{SS}	
AC19	V_{SS}		AD4	V_{SS}		AD13	PE0TN03		AD22	V_{DD}CORE	
AC20	PE0TN00		AD5	PE1TP03		AD14	V_{SS}		AD23	V_{SS}	
AC21	V_{SS}		AD6	V_{SS}		AD15	V_{DD}CORE		AD24	V_{SS}	

Table 19 PES16T7 320-pin Signal Pin-Out (Part 3 of 3)

Alternate Signal Functions

Pin	GPIO	Alternate
V21	GPIO_00	P2RSTN
V22	GPIO_01	P4RSTN
U24	GPIO_02	IOEXPINTN0
U23	GPIO_03	IOEXPINTN1
U21	GPIO_04	IOEXPINTN2
U22	GPIO_05	IOEXPINTN3
T21	GPIO_07	GPEN
H22	GPIO_08	P1RSTN
H21	GPIO_09	P3RSTN
G22	GPIO_10	P5RSTN
G21	GPIO_11	P6RSTN

Table 20 PES16T7 Alternate Signal Functions

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
A3	AB24	B6	C5	B4	D9
A4	AC24	B19	C10	B16	D14
A6	AD2	E3	C16	B17	D17
A9	AD3	E21	C17	C4	H4
A16	AD15	E22	C19	C12	M3
A18	AD22	F3	D4	C20	N21
A19		Y2	D5	D12	R21
A21		Y23	D18	D19	AA5
A23		AA2	E23	E2	AA11
B1		AA24	F23	F2	AA15
B2		AB2	G3	F21	AA20
B3		AC2	G23	F22	
B5			K2	G2	
B20			K3	H2	
B22			K4	H3	
B23			L22	H23	
C2			L23	J21	
C21			M4	J22	
C24			P3	J23	
D1			P4	L3	
D3			R22	L4	
D20			T23	T22	
D22			Y3	Y22	
D23			AA22	AA9	
E4			AA23	AA18	
E24			AB3	AB7	
G1			AB16	AB13	
G24			AB18	AB22	
AA1			AC22	AB23	
AB1			AC23	AC3	

Table 21 PES16T7 Power Pins

Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	C3	H24	R2	AC12
A2	C6	J2	V23	AC14
A5	C8	J3	Y21	AC15
A7	C9	J4	AA3	AC17
A11	C14	K21	AA7	AC19
A13	C22	K22	AA10	AC21
A15	C23	K23	AA13	AD1
A17	D2	L1	AA16	AD4
A20	D6	L2	AB5	AD6
A22	D8	L21	AB9	AD8
A24	D10	L24	AB10	AD10
B7	D16	M23	AB11	AD12
B9	D21	M24	AB15	AD14
B11	D24	N1	AB20	AD17
B13	E1	N2	AC1	AD19
B15	F1	N22	AC4	AD21
B21	F4	P23	AC6	AD23
B24	F24	P24	AC8	AD24
C1	H1	R1	AC10	

Table 22 PES16T7 Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	Y24	System
CCLKUS	I	Y4	
GPIO_00	I/O	V21	General Purpose Input/Output
GPIO_01	I/O	V22	
GPIO_02	I/O	U24	
GPIO_03	I/O	U23	
GPIO_04	I/O	U21	
GPIO_05	I/O	U22	
GPIO_06	I/O	T24	
GPIO_07	I/O	T21	
GPIO_08	I/O	H22	
GPIO_09	I/O	H21	
GPIO_10	I/O	G22	
GPIO_11	I/O	G21	
JTAG_TCK	I	T2	JTAG
JTAG_TDI	I	T3	
JTAG_TDO	O	T4	
JTAG_TMS	I	T1	
JTAG_TRST_N	I	U2	
MSMBADDR_1	I	U3	SMBus
MSMBADDR_2	I	U4	
MSMBADDR_3	I	U1	
MSMBADDR_4	I	V2	
MSMBCLK	I/O	V3	
MSMBDAT	I/O	V4	
MSMBSMODE	I	B18	System
P01MERGEN	I	G4	
PE0RN00	I	AB21	PCI Express
PEORN01	I	AB19	
PE0RN02	I	AB17	
PE0RN03	I	AB14	
PE0RP00	I	AA21	
PE0RP01	I	AA19	
PE0RP02	I	AA17	

Table 23 89PES16T7 Alphabetical Signal List (Part 1 of 4)

Signal Name	I/O Type	Location	Signal Category
PE0RP03	I	AA14	PCI Express (cont.)
PE0TN00	O	AC20	
PE0TN01	O	AD18	
PE0TN02	O	AD16	
PE0TN03	O	AD13	
PE0TP00	O	AD20	
PE0TP01	O	AC18	
PE0TP02	O	AC16	
PE0TP03	O	AC13	
PE1RN00	I	AB12	
PE1RN01	I	AA8	
PE1RN02	I	AB6	
PE1RN03	I	AB4	
PE1RP00	I	AA12	
PE1RP01	I	AB8	
PE1RP02	I	AA6	
PE1RP03	I	AA4	
PE1TN00	O	AC11	
PE1TN01	O	AD9	
PE1TN02	O	AD7	
PE1TN03	O	AC5	
PE1TP00	O	AD11	
PE1TP01	O	AC9	
PE1TP02	O	AC7	
PE1TP03	O	AD5	
PE2RN00	I	R4	
PE2RP00	I	R3	
PE2TN00	I	P1	
PE2TP00	I	P2	
PE3RN00	I	N4	
PE3RP00	I	N3	
PE3TN00	O	M1	
PE3TP00	O	M2	
PE4RN00	O	M22	
PE4RP00	O	M21	
PE4TN00	O	N23	

Table 23 89PES16T7 Alphabetical Signal List (Part 2 of 4)

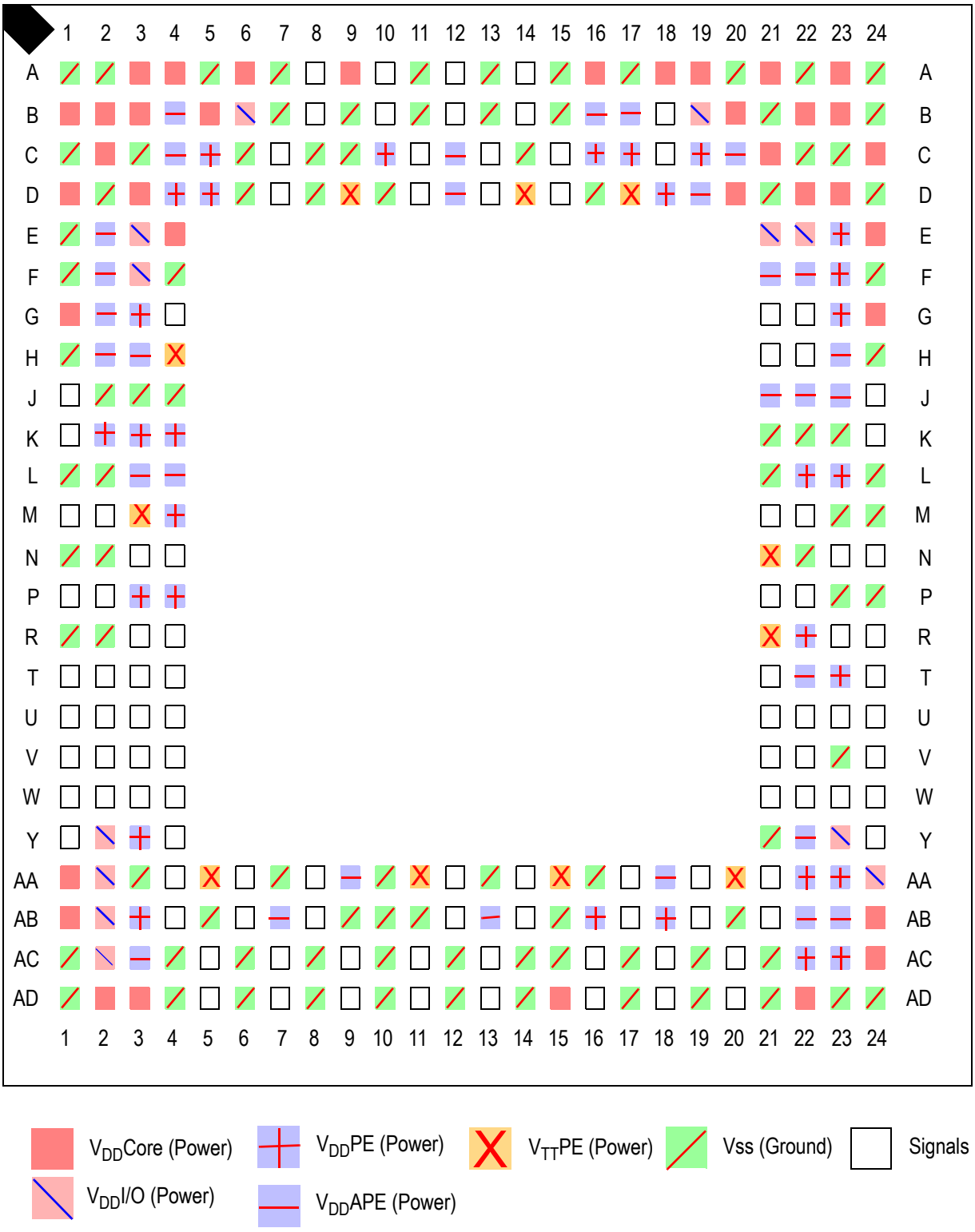
Signal Name	I/O Type	Location	Signal Category
PE4TP00	O	N24	PCI Express (cont.)
PE5RN00	I	P22	
PE5RP00	I	P21	
PE5TN00	I	R23	
PE5TP00	I	R24	
PE6RN00	I	C7	
PE6RN01	I	D11	
PE6RN02	I	C13	
PE6RN03	I	C15	
PE6RP00	I	D7	
PE6RP01	I	C11	
PE6RP02	I	D13	
PE6RP03	I	D15	
PE6TN00	O	B8	
PE6TN01	O	A10	
PE6TN02	O	A12	
PE6TN03	O	B14	
PE6TP00	O	A8	
PE6TP01	O	B10	
PE6TP02	O	B12	
PE6TP03	O	A14	
PEREFCLKN1	I	J1	
PEREFCLKN2	I	K24	
PEREFCLKP1	I	K1	
PEREFCLKP2	I	J24	
PERSTN	I	W21	System
REFCLKM	I	C18	PCI Express
RSTHALT	I	W24	System
SSMBADDR_1	I	V1	SMBus Interface
SSMBADDR_2	I	W2	
SSMBADDR_3	I	W3	
SSMBADDR_5	I	W4	
SSMBCLK	I/O	W1	
SSMBDAT	I/O	Y1	

Table 23 89PES16T7 Alphabetical Signal List (Part 3 of 4)

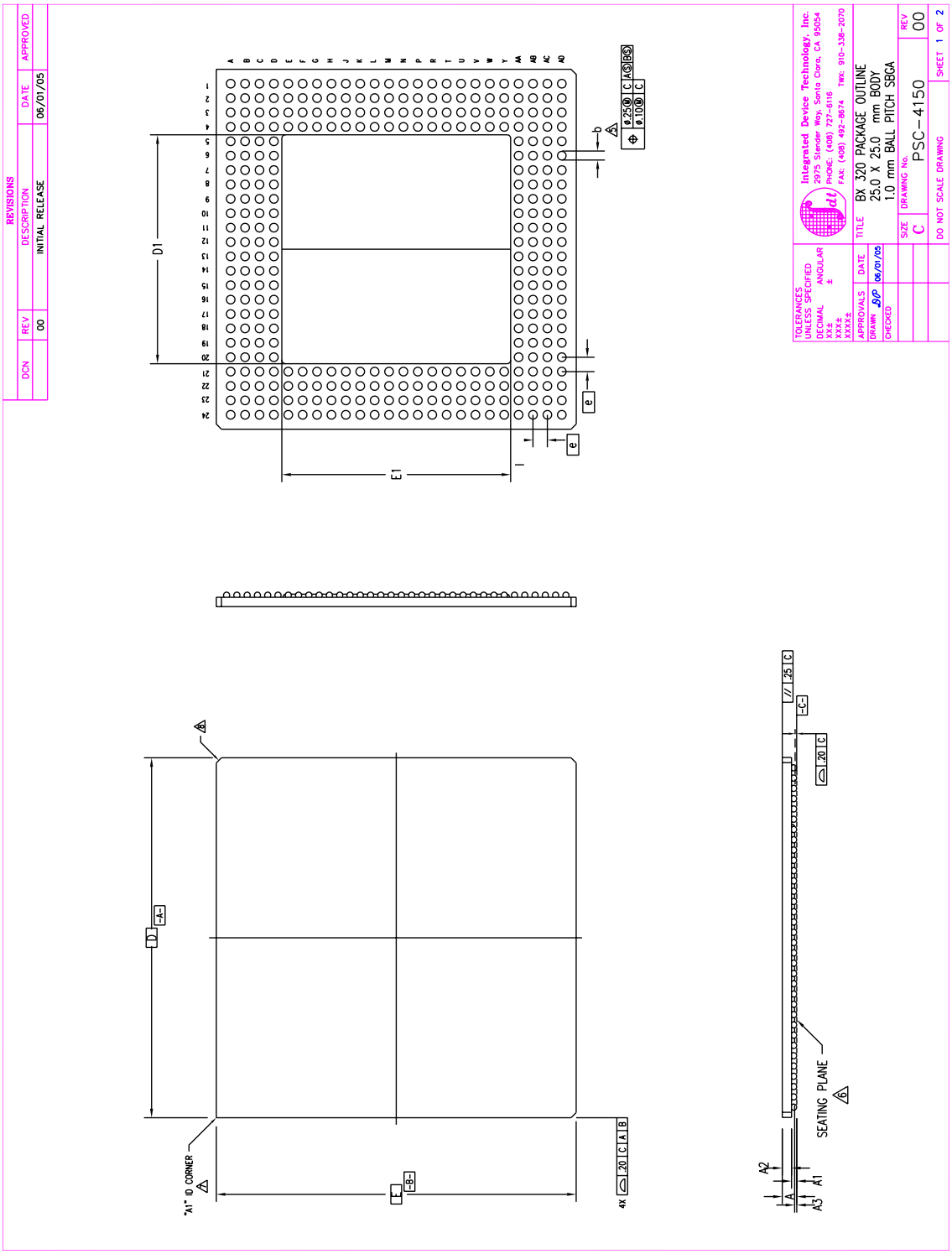
Signal Name	I/O Type	Location	Signal Category
SWMODE_0	I	W23	System
SWMODE_1	I	W22	
SWMODE_2	I	V24	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 21 for a listing of power pins.		
V_{SS}	See Table 22 for a listing of ground pins.		

Table 23 89PES16T7 Alphabetical Signal List (Part 4 of 4)

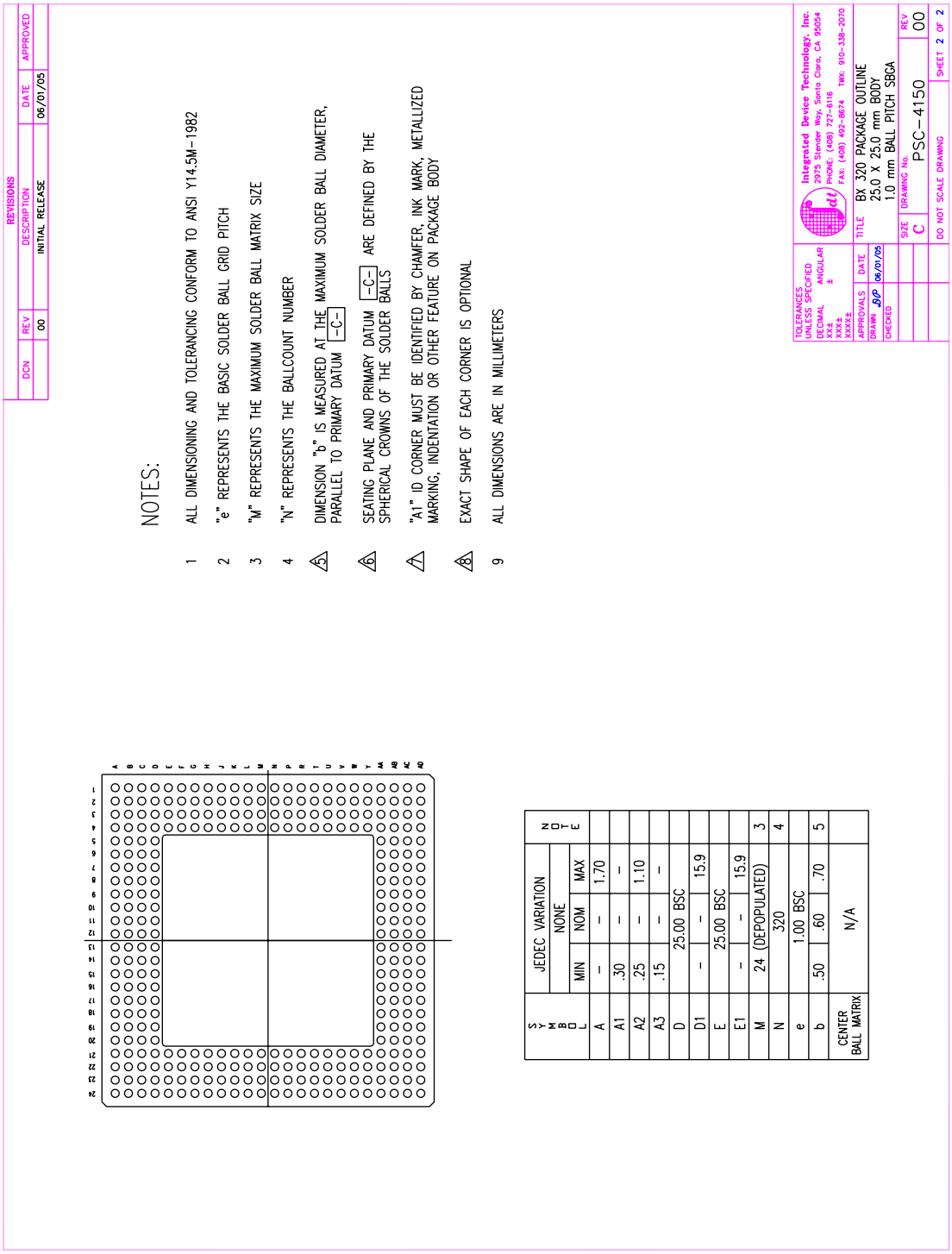
PES16T7 Pinout — Top View



PES16T7 Package Drawing — 320-Pin BX320/BXG320



PES32T8 Package Drawing — Page Two



Revision History

February 8, 2007: Initial publication.

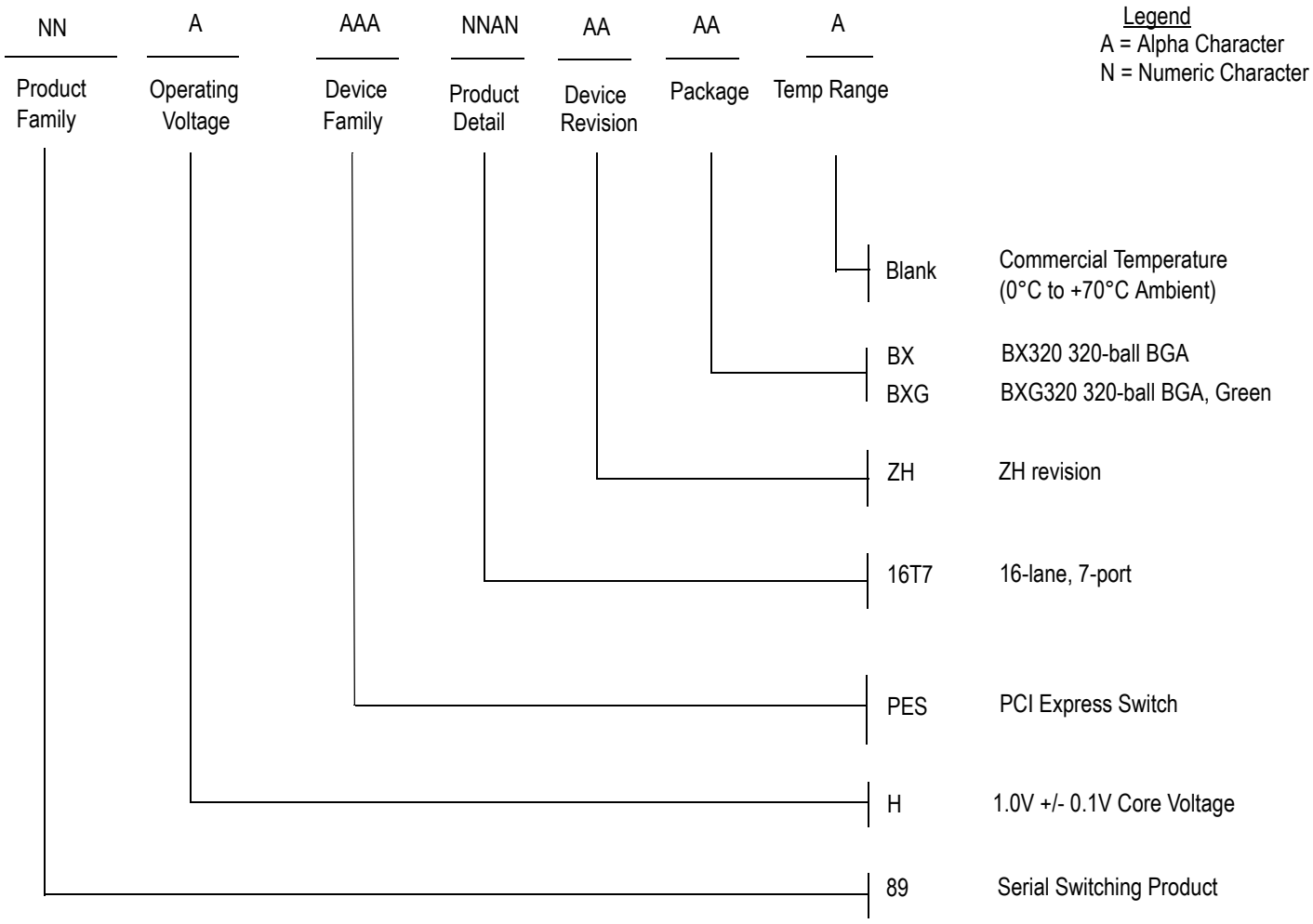
April 4, 2007: In Table 3, revised description for MSMBCLK signal.

May 30, 2007: Changed device revision in Ordering Information from ZD to ZH.

November 14, 2007: Added new parameter, Termination Resistor, to Table 9, Input Clock Requirements.

March 25, 2008: Added θ_{JB} and θ_{JC} parameters to Table 16, Thermal Specifications.

Ordering Information



Valid Combinations

89HPES16T7ZHBX	320-pin BX320 package, Commercial Temperature
89HPES16T7ZHBXG	320-pin Green BX320 package, Commercial Temperature

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(Rev.1.0 Mar 2020)

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