

### General Description

The [XR76203-Q](#), [XR76205-Q](#) and [XR76208-Q](#) are synchronous step-down regulators combining the controller, drivers, bootstrap diode and MOSFETs in a single package for point-of-load supplies well suited for automotive applications. Qualified per AEC-Q100, the XR76203-Q, XR76205-Q and XR76208-Q have load current ratings of 3A, 5A and 8A respectively. A wide 5.5V to 40V input voltage range allows for single supply operation from 12V battery systems required to withstand load dump, industry standard 24V  $\pm 10\%$ , 18V-36V, and rectified 18VAC and 24VAC rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR76203-Q, XR76205-Q and XR76208-Q provide extremely fast line and load transient response using ceramic output capacitors. They require no loop compensation, simplifying circuit implementation and reducing overall component count. The control loop also provides 0.07% load and 0.15% line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in discontinuous conduction mode (DCM) at light current loads, thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit, and UVLO helps achieve safe operation under abnormal operating conditions.

The XR76203-Q, XR76205-Q and XR76208-Q are available in a RoHS-compliant, green / halogen-free, space-saving QFN 5x5mm package.

### FEATURES

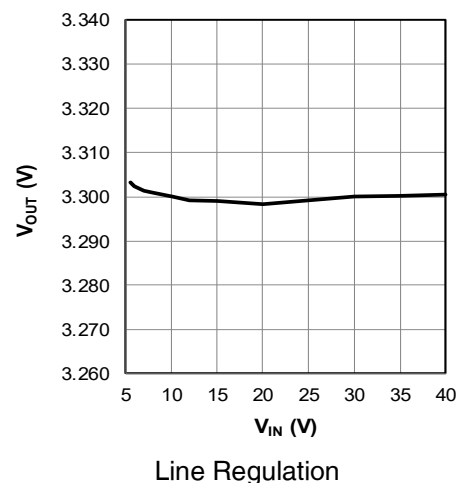
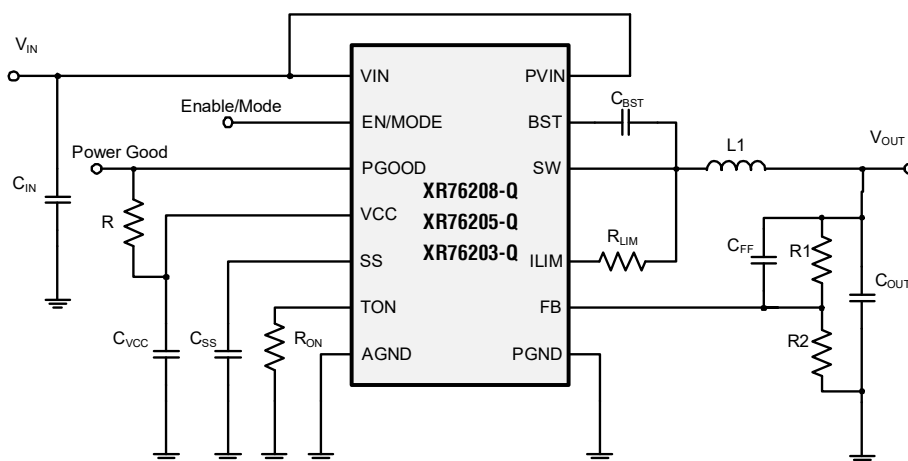
- Automotive AEC-Q100 qualified
  - Temperature Grade 1: -40°C to 125°C
  - HBM ESD Class Level 2
  - CDM ESD Class Level C4B
- Controller, drivers, bootstrap diode and MOSFETs integrated in one package
- 3A, 5A and 8A step down regulators
  - Wide 5.5V to 40V input voltage range
  - $\geq 0.6V$  adjustable output voltage
- Proprietary Constant On-Time control
  - No loop compensation required
  - Stable ceramic output capacitor operation
  - Programmable 200ns to 2 $\mu$ s on-time
  - Constant 100kHz to 800kHz frequency
- Selectable CCM or CCM / DCM
  - CCM / DCM for high efficiency at light-load
  - CCM for constant frequency at light-load
- Programmable hiccup current limit with thermal compensation
- Precision enable and Power Good flag
- Programmable soft-start
- 30-pin 5x5mm QFN package with wettable flanks

### APPLICATIONS

- Automotive systems
- Distributed power architecture
- Point-of-Load converters
- Power supply modules
- FPGA, DSP, and processor supplies
- Industrial and military

### Typical Application

Ordering Information - [Back Page](#)



**Absolute Maximum Ratings**

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PV<sub>IN</sub>, V<sub>IN</sub>.....-0.3V to 43V  
 V<sub>CC</sub>.....-0.3V to 6.0V  
 BST.....-0.3V to 48V<sup>(1)</sup>  
 BST-SW.....-0.3V to 6V  
 SW, ILIM.....-1V to 43V<sup>(1, 2)</sup>  
 ALL other pins.....-0.3V to V<sub>CC</sub>+0.3V  
 Storage temperature.....-65°C to +150°C  
 Junction temperature.....150°C  
 Power dissipation.....Internally Limited  
 Lead temperature (Soldering, 10 sec).....300°C  
 ESD rating (HBM - Human Body Model).....±2kV  
 ESD rating (Charged Device Model (CDM) per AEC Q100-011, Non-corner pins).....±500V  
 ESD Rating (Charged Device Model (CDM) per AEC Q100-011, Corner pins 1, 7, 8, 14, 15, 22, 23, 30).....±750V

**Operating Conditions**

PV<sub>IN</sub>.....5V to 40V  
 V<sub>IN</sub>.....5.5V to 40V  
 SW, ILIM.....-1V to 40V<sup>(1)</sup>  
 PGOOD, V<sub>CC</sub>, T<sub>ON</sub>, SS, EN, FB.....-0.3V to 5.5V  
 Switching frequency.....100kHz to 800kHz<sup>(3)</sup>  
 Junction temperature range.....-40°C to +125°C  
 XR76203-Q package thermal resistance, θ<sub>JA</sub>.....28°C/W  
 XR76205-Q package thermal resistance, θ<sub>JA</sub>.....26°C/W  
 XR76208-Q package thermal resistance, θ<sub>JA</sub>.....25°C/W  
 XR76203-Q package power dissipation at 25°C.....3.6W  
 XR76205-Q package power dissipation at 25°C.....3.8W  
 XR76208-Q package power dissipation at 25°C.....4.0W

Note 1: No external voltage applied.

Note 2: SW pin's minimum DC range is -1V, transient is -5V for less than 50ns.

Note 3: Recommended frequency.

**Electrical Characteristics**

Unless otherwise noted: T<sub>J</sub> = 25°C, V<sub>IN</sub> = 24V, BST = V<sub>CC</sub>, SW = AGND = PGND = 0V, C<sub>VCC</sub> = 4.7µF. Limits applying over the full operating temperature range are denoted by a “•”

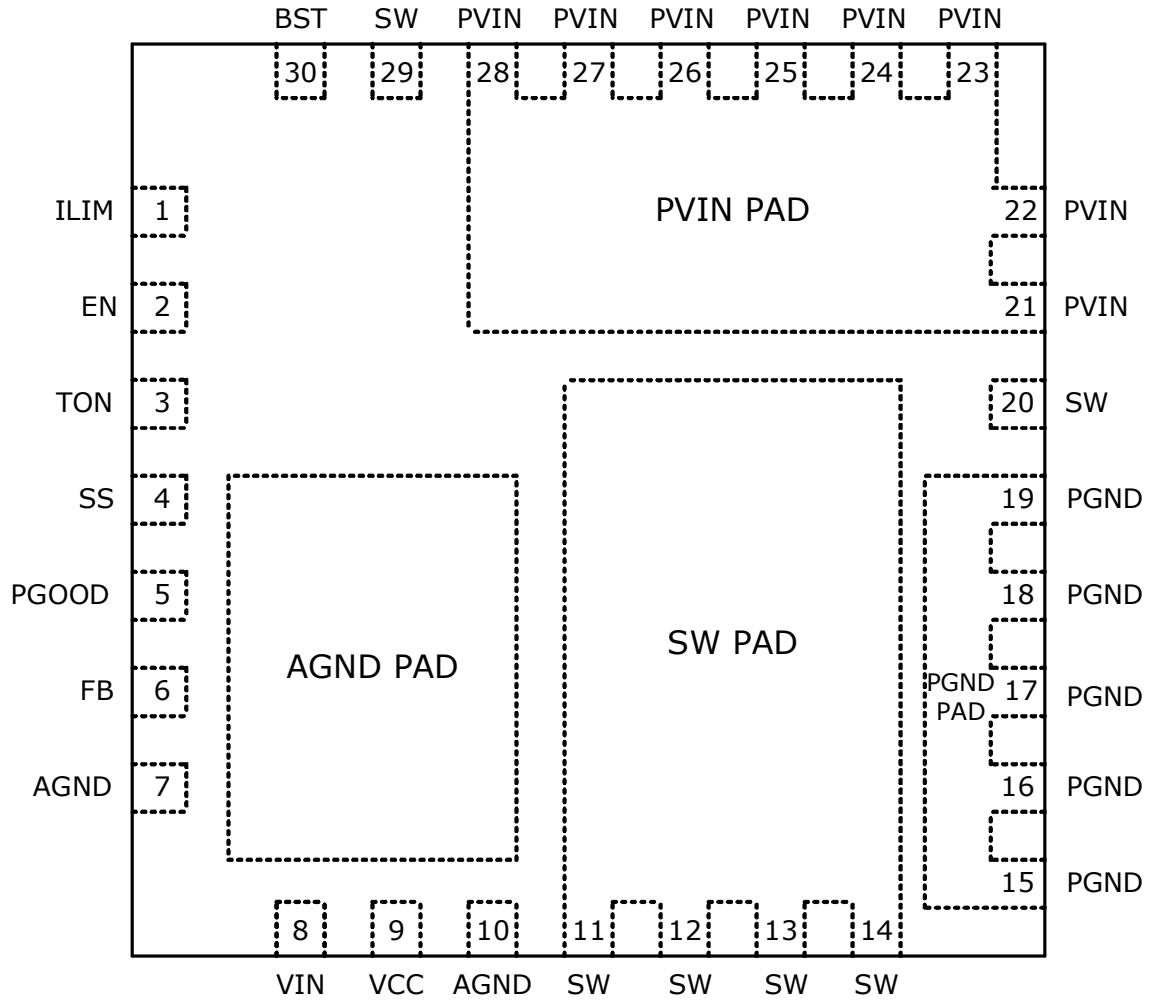
Symbol	Parameter	Conditions		Min	Typ	Max	Units
<b>Power Supply Characteristics</b>							
V <sub>IN</sub>	Input voltage range	V <sub>CC</sub> regulating	•	5.5		40	V
I <sub>VIN</sub>	VIN input supply current	Not switching, V <sub>IN</sub> = 24V, V <sub>FB</sub> = 0.7V	•		0.7	2	mA
I <sub>VIN</sub>	VIN input supply current (XR76203-Q)	f = 300kHz, R <sub>ON</sub> = 215kΩ, V <sub>FB</sub> = 0.58V			12		mA
I <sub>VIN</sub>	VIN input supply current (XR76205-Q)	f = 300kHz, R <sub>ON</sub> = 215kΩ, V <sub>FB</sub> = 0.58V			15		mA
I <sub>VIN</sub>	VIN input supply current (XR76208-Q)	f = 300kHz, R <sub>ON</sub> = 215kΩ, V <sub>FB</sub> = 0.58V			19		mA
I <sub>OFF</sub>	Shutdown current	Enable = 0V, V <sub>IN</sub> = 12V			1		µA
<b>Enable and Under-Voltage Lock-Out UVLO</b>							
V <sub>IH_EN_1</sub>	EN pin rising threshold		•	1.8	1.9	2.0	V
V <sub>EN_H_1</sub>	EN pin hysteresis				70		mV
V <sub>IH_EN_2</sub>	EN pin rising threshold for DCM / CCM operation		•	2.8	3.0	3.1	V
V <sub>EN_H_2</sub>	EN pin hysteresis				100		mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	VCC UVLO start threshold, rising edge		•	4.00	4.25	4.40	V
	VCC UVLO hysteresis				230		mV
<b>Reference Voltage</b>							
V <sub>REF</sub>	Reference voltage	V <sub>IN</sub> = 5.5V to 40V, VCC regulating		0.596	0.600	0.604	V
		V <sub>IN</sub> = 5.5V to 40V, VCC regulating	•	0.594	0.600	0.606	V
	DC line regulation	CCM, closed loop, V <sub>IN</sub> =5.5V-40V, applies to any C <sub>OUT</sub>			±0.33		%
	DC load regulation	CCM, closed loop, applies to any C <sub>OUT</sub>			±0.39		%
<b>Programmable Constant On-Time</b>							
T <sub>ON1</sub>	On-time 1	R <sub>ON</sub> = 237kΩ, V <sub>IN</sub> = 40V	•	1570	1840	2120	ns
	f corresponding to on-time 1	V <sub>OUT</sub> = 24V, V <sub>IN</sub> = 40V, R <sub>ON</sub> = 237kΩ	•	283	326	382	kHz
T <sub>ON(MIN)</sub>	Minimum programmable on-time	R <sub>ON</sub> = 14kΩ, V <sub>IN</sub> = 40V			120		ns
T <sub>ON2</sub>	On-time 2	R <sub>ON</sub> = 14kΩ, V <sub>IN</sub> = 24V	•	174	205	236	ns
T <sub>ON3</sub>	On-time 3	R <sub>ON</sub> = 35.7kΩ, V <sub>IN</sub> = 24V	•	407	479	550	ns
	f corresponding to on-time 3	V <sub>OUT</sub> = 3.3V, V <sub>IN</sub> = 24V, R <sub>ON</sub> = 35.7kΩ	•	250	287	338	kHz
	f corresponding to on-time 3	V <sub>OUT</sub> = 5.0V, V <sub>IN</sub> = 24V, R <sub>ON</sub> = 35.7kΩ	•	379	435	512	kHz
	Minimum off-time		•		250	350	ns
<b>Diode Emulation Mode</b>							
	Zero crossing threshold	DC value measured during test			-2		mV
<b>Soft-start</b>							
	SS charge current		•	-14	-10	-6	μA
	SS discharge current	Fault present	•	1			mA
<b>VCC Linear Regulator</b>							
	VCC output voltage	V <sub>IN</sub> = 6V to 40V, I <sub>LOAD</sub> = 0 to 30mA	•	4.8	5.0	5.2	V
		V <sub>IN</sub> = 5V, I <sub>LOAD</sub> = 0 to 20mA	•	4.51	4.7		V
<b>Power Good Output</b>							
	Power Good threshold			-10	-6.9	-5	%
	Power Good hysteresis				1.6	4	%
	Power Good sink current			1			mA
<b>Protection: OCP, OTP, Short-Circuit</b>							
	Hiccup timeout				110		ms
	ILIM pin source current			45	50	55	μA
	ILIM current temperature coefficient				0.4		%/°C
	OCP comparator offset		•	-8	0	+8	mV
	Current limit blanking	GL rising > 1V			100		ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	Thermal shutdown threshold <sup>(1)</sup>	Rising temperature			150		°C
	Thermal hysteresis <sup>(1)</sup>				15		°C
	VSCTH feedback pin short-circuit threshold	Percent of $V_{REF}$ , short circuit is active after PGOOD is asserted	•	50	60	70	%
<b>XRP76203 Output Power Stage</b>							
$R_{DSON}$	High-side MOSFET $R_{DSON}$	$I_{DS} = 1A$			115	160	mΩ
	Low-side MOSFET $R_{DSON}$				40	59	mΩ
$I_{OUT}$	Maximum output current		•	3			A
<b>XRP76205 Output Power Stage</b>							
$R_{DSON}$	High-side MOSFET $R_{DSON}$	$I_{DS} = 2A$			42	59	mΩ
	Low-side MOSFET $R_{DSON}$				40	59	mΩ
$I_{OUT}$	Maximum output current		•	5			A
<b>XRP76208 Output Power Stage</b>							
$R_{DSON}$	High-side MOSFET $R_{DSON}$	$I_{DS} = 2A$			42	59	mΩ
	Low-side MOSFET $R_{DSON}$				16.2	21.5	mΩ
$I_{OUT}$	Maximum output current		•	8			A

Note 1: Guaranteed by design.

Pin Configuration, Top View

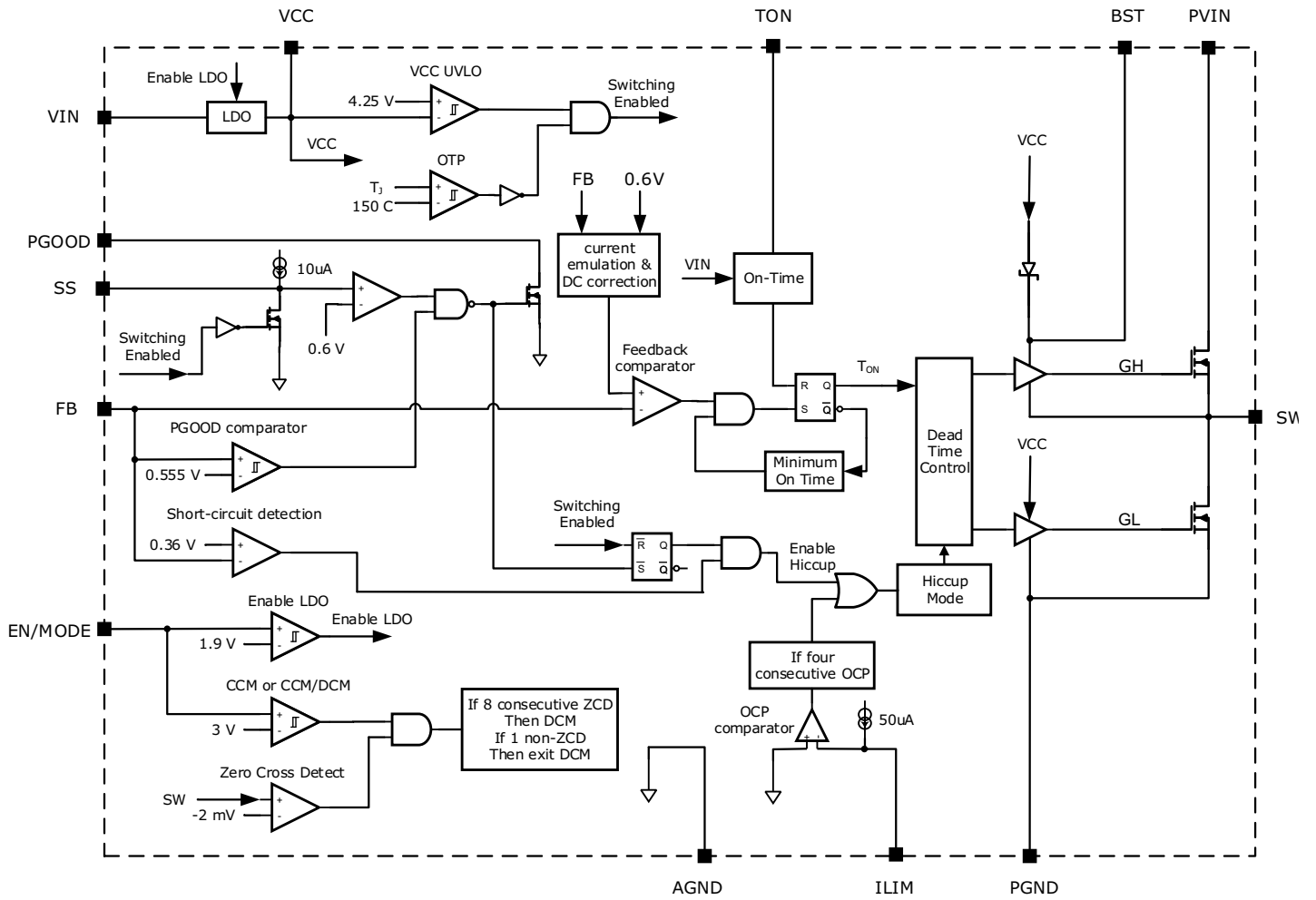


## Pin Assignments

Pin No.	Pin Name	Type	Description
1	ILIM	A	Over-current protection programming. Connect with a resistor to SW.
2	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the regulator on and it will operate in CCM. If the voltage is raised above 3.0V, then the regulator will operate in DCM / CCM depending on load.
3	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
4	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10 $\mu$ A internal source current.
5	PGOOD	O, OD	Power-Good output. This open-drain output is pulled low when V <sub>OUT</sub> is outside the regulation.
6	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to V <sub>OUT</sub> and AGND in order to program V <sub>OUT</sub> .
7, 10, AGND Pad	AGND	A	Signal ground for control circuitry. Connect AGND Pad with a short trace to pins 7 and 10.
8	VIN	A	Supply input for the regulator's LDO. Normally it is connected to PVIN.
9	VCC	A	The output of regulator's LDO. For operation using a 5V rail, VCC should be shorted to VIN.
11-14, 20, 29, SW Pad	SW	PWR	Switch node. The drain of the low-side N-channel MOSFET. The source of the high-side MOSFET is wire-bonded to the SW Pad. Pins 20 and 29 are internally connected to the SW pad.
15-19, PGND Pad	PGND	PWR	Ground of the power stage. Should be connected to the system's power ground plane. The source of the low-side MOSFET is wire-bonded to PGND Pad.
21-28, PVIN Pad	PVIN	PWR	Input voltage for power stage. The drain of the high-side N-channel MOSFET.
30	BST	A	High-side driver supply pin. Connect a bootstrap capacitor between BST and pin 29.

Type: A = Analog, I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram



### Typical Performance Characteristics

Unless otherwise noted:  $V_{IN} = 24V$ ,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 8A$ ,  $f = 400kHz$ ,  $T_A = 25^\circ C$ . Schematic from the application information section.

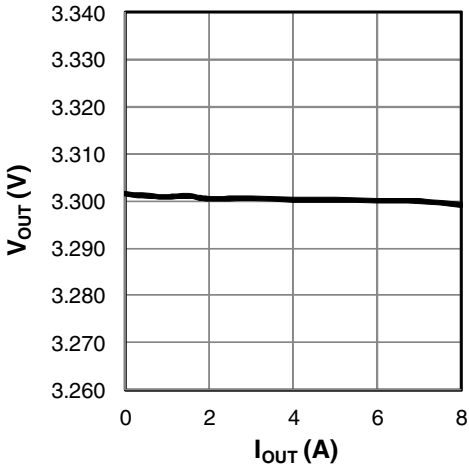


Figure 1: Load Regulation

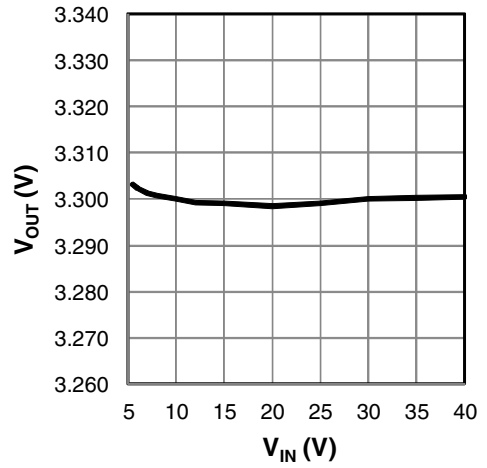


Figure 2: Line Regulation

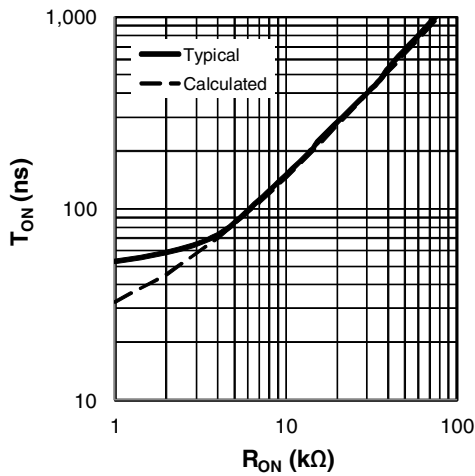


Figure 3:  $T_{ON}$  versus  $R_{ON}$

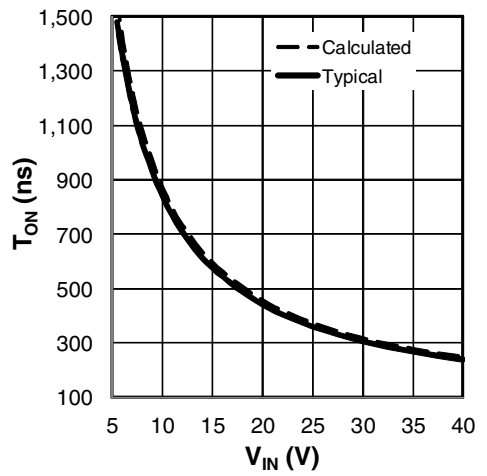


Figure 4:  $T_{ON}$  versus  $V_{IN}$ ,  $R_{ON} = 27.4k\Omega$

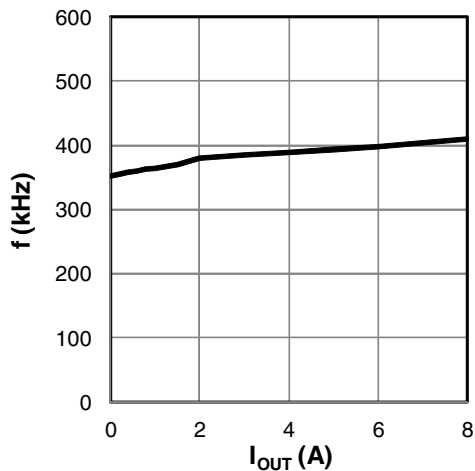


Figure 5: Frequency versus  $I_{OUT}$

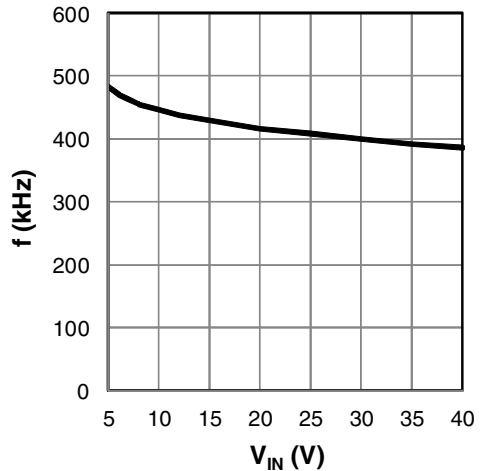


Figure 6: Frequency versus  $V_{IN}$



Typical Performance Characteristics

Unless otherwise noted:  $V_{IN} = 24V$ ,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 8A$ ,  $f = 400kHz$ ,  $T_A = 25^\circ C$ . Schematic from the application information section.

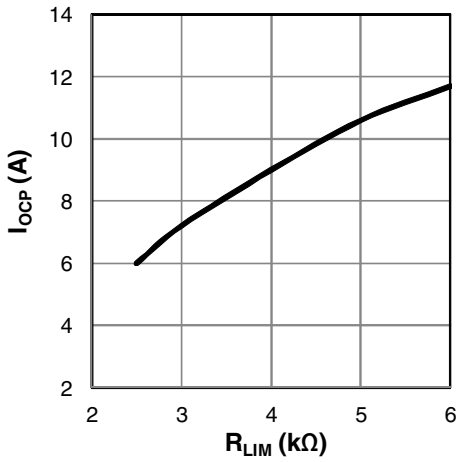


Figure 7: XR76208-Q  $I_{OCP}$  versus  $R_{LIM}$

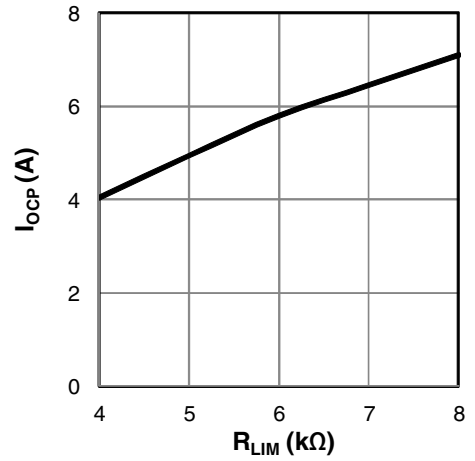


Figure 8: XR76205-Q  $I_{OCP}$  versus  $R_{LIM}$

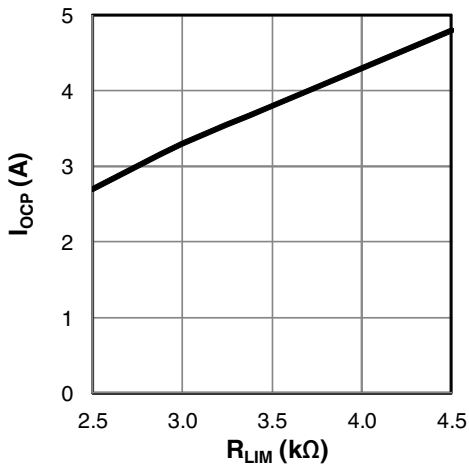


Figure 9: XR76203-Q  $I_{OCP}$  versus  $R_{LIM}$

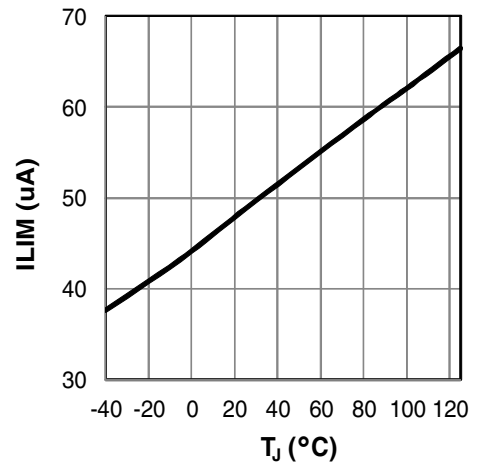


Figure 10:  $I_{LIM}$  versus Temperature

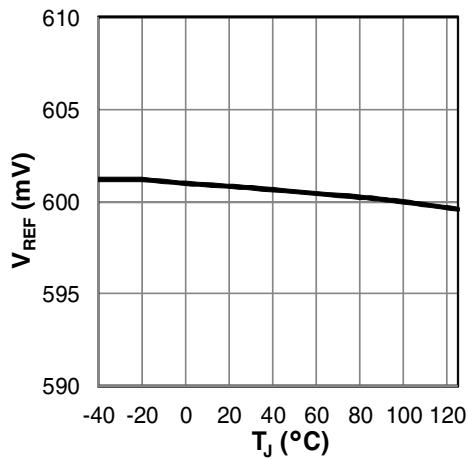


Figure 11:  $V_{REF}$  versus Temperature

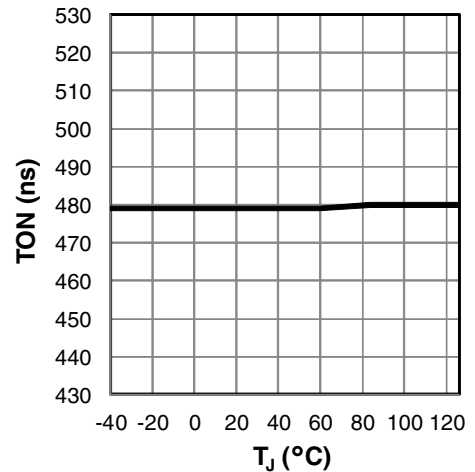


Figure 12:  $T_{ON}$  versus Temperature,  $R_{ON} = 35.7k\Omega$

### Typical Performance Characteristics

Unless otherwise noted:  $V_{IN} = 24V$ ,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 8A$ ,  $f = 400kHz$ ,  $T_A = 25^\circ C$ . Schematic from the application information section.

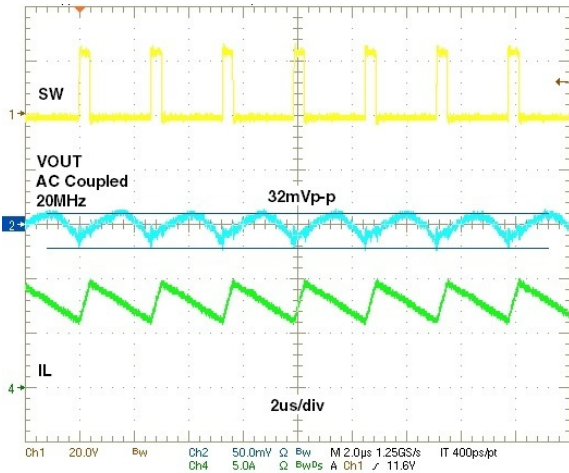


Figure 13: Steady State,  $I_{OUT}=8A$

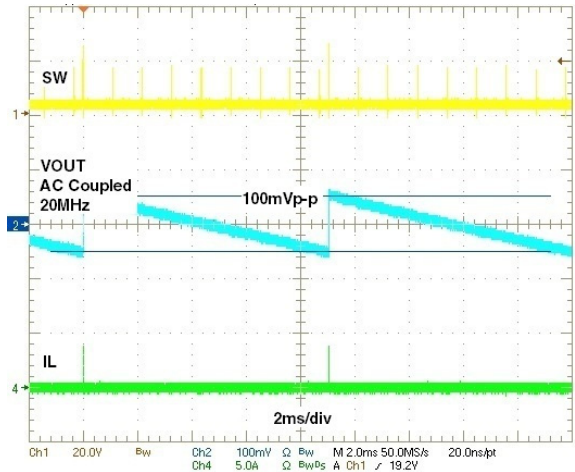


Figure 14: Steady State, DCM,  $I_{OUT}=0A$

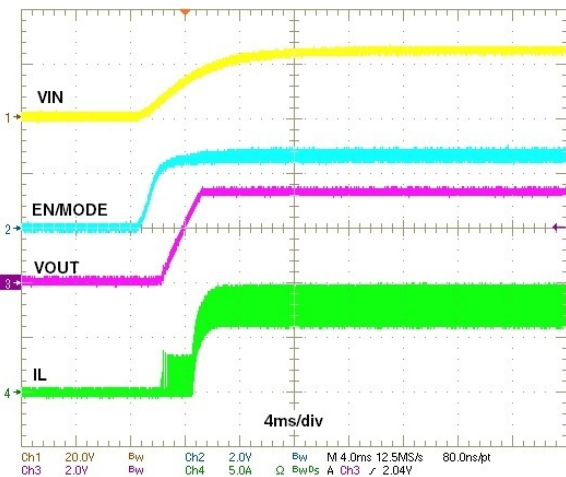


Figure 15: Power-up, Forced CCM

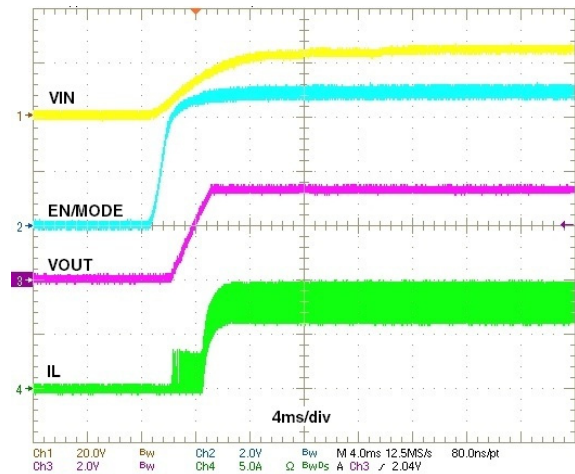


Figure 16: Power-up, DCM / CCM

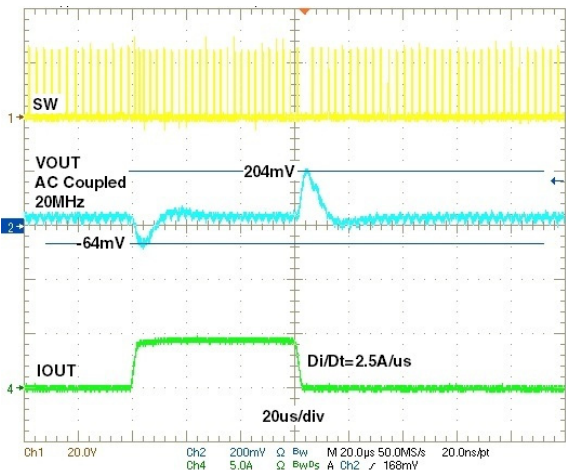


Figure 17: Load Step, Forced CCM, 0A - 4A - 0A

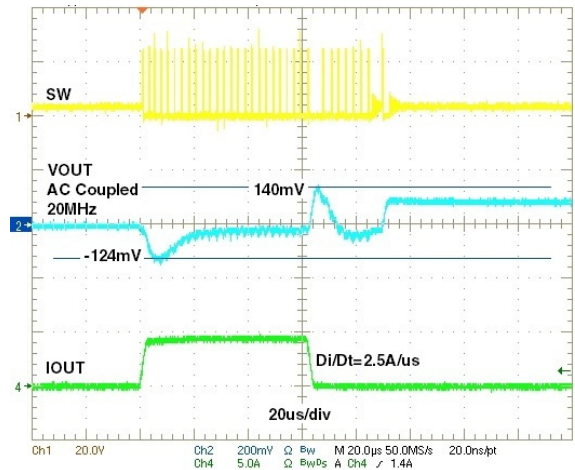


Figure 18: Load Step, DCM / CCM, 0A - 4A - 0A

## Efficiency

Unless otherwise noted:  $T_{AMBIENT} = 25^{\circ}C$ , no air flow,  $f = 400kHz$ , inductor losses are included, the schematic is from the Application Information section.

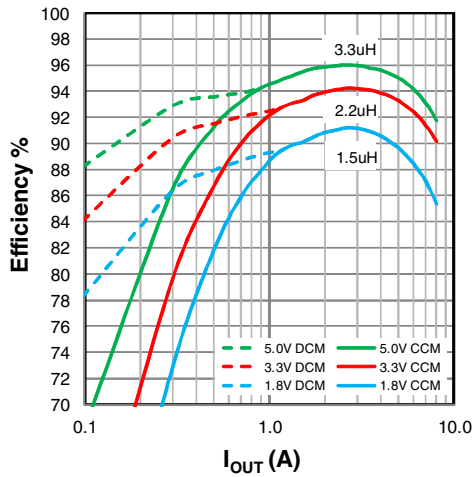


Figure 19: XR76208-Q Efficiency,  $V_{IN} = 12V$

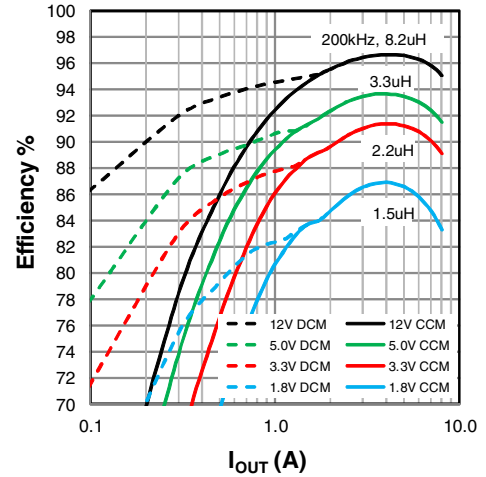


Figure 20: XR76208-Q Efficiency,  $V_{IN} = 24V$

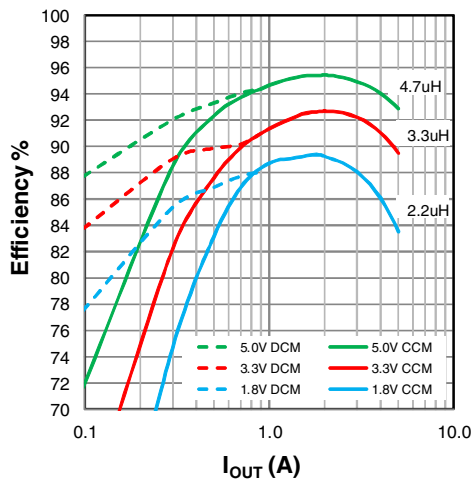


Figure 21: XR76205-Q Efficiency,  $V_{IN} = 12V$

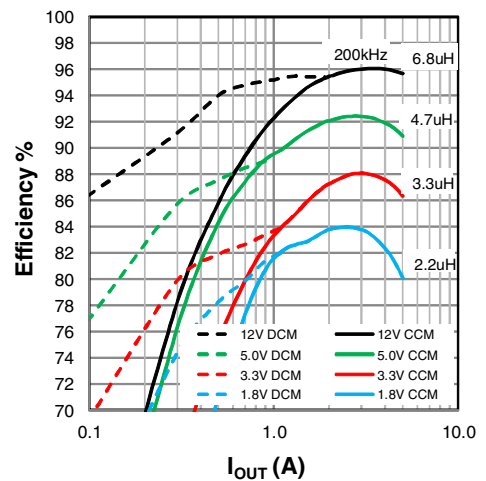


Figure 22: XR76205-Q Efficiency,  $V_{IN} = 24V$

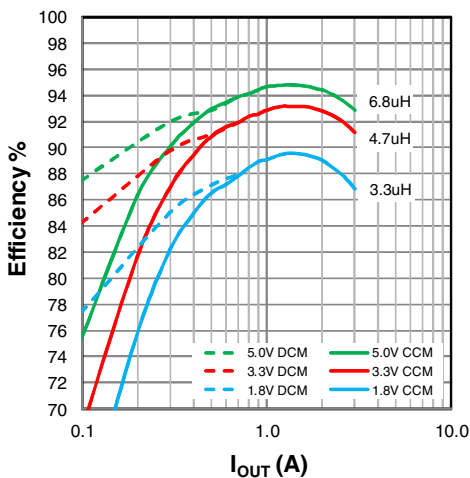


Figure 23: XR76203-Q Efficiency,  $V_{IN} = 12V$

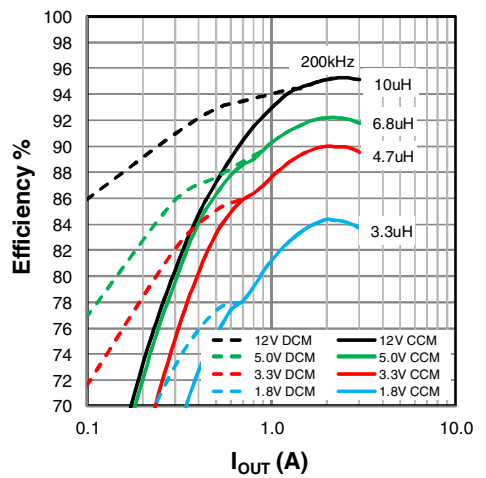


Figure 24: XR76203-Q Efficiency,  $V_{IN} = 24V$

## Thermal Derating

Unless otherwise noted: no air flow,  $f = 400\text{kHz}$ , the schematic is from the Application Information section.

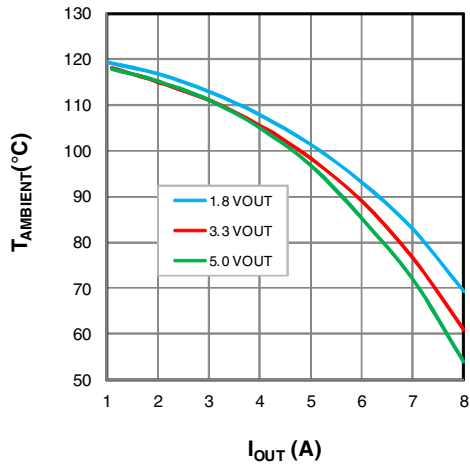


Figure 25: XR76208-Q,  $V_{IN} = 12\text{V}$

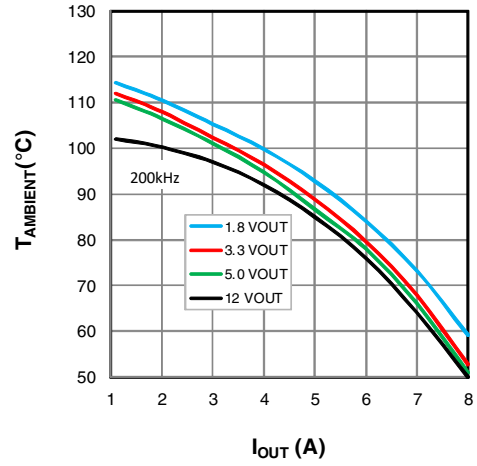


Figure 26: XR76208-Q,  $V_{IN} = 24\text{V}$

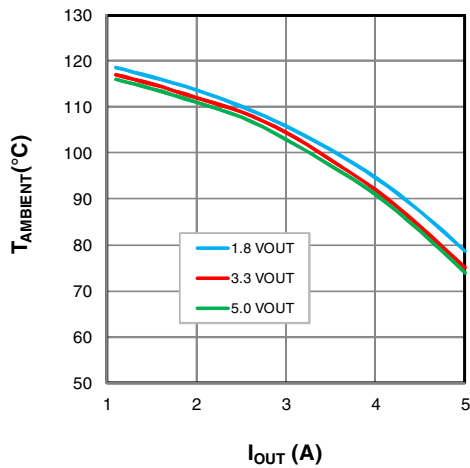


Figure 27: XR76205-Q,  $V_{IN} = 12\text{V}$

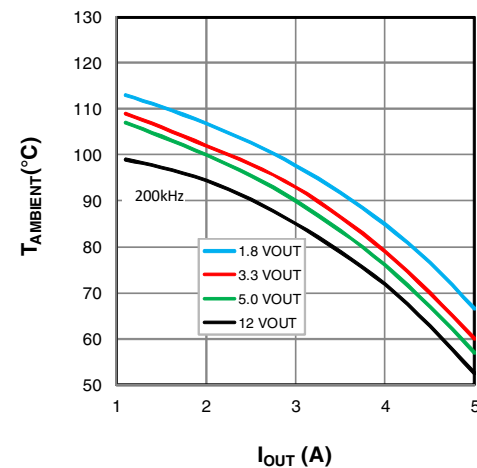


Figure 28: XR76205-Q,  $V_{IN} = 24\text{V}$

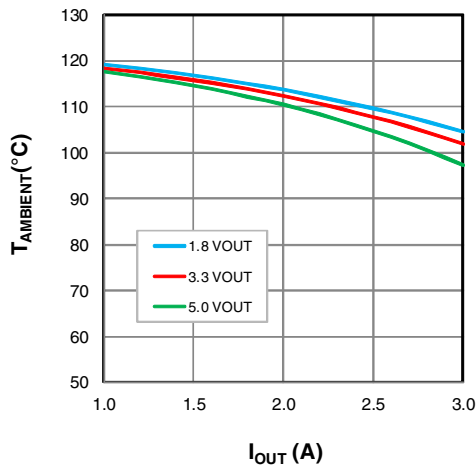


Figure 29: XR76203-Q,  $V_{IN} = 12\text{V}$

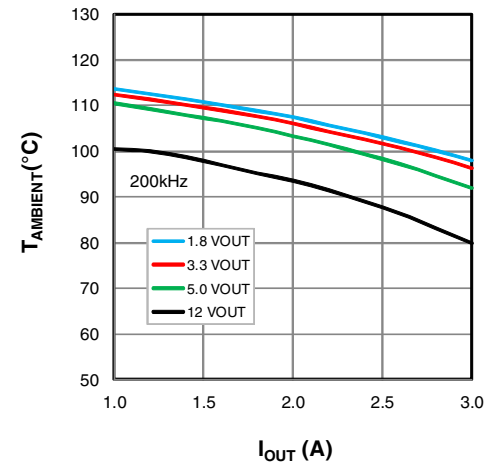


Figure 30: XR76203-Q,  $V_{IN} = 24\text{V}$

## Functional Description

XR76203-Q, XR76205-Q and XR76208-Q are synchronous step-down, proprietary emulated current-mode Constant On-Time (COT) regulators. The on-time, which is programmed via  $R_{ON}$ , is inversely proportional to  $V_{IN}$  and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with GH signal turning on the high-side (control) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When  $V_{FB}$  drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

### Enable / Mode Input (EN/MODE)

The EN/MODE pin accepts a tri-level signal that is used to control turn on / off. It also selects between two modes of operation: 'Forced CCM' and 'DCM / CCM'. If EN/MODE is pulled below 1.8V, the regulator shuts down. A voltage between 2.0V and 2.8V selects the Forced CCM mode, which will run the regulator in continuous conduction at all times. A voltage higher than 3.1V selects the DCM / CCM mode, which will run the regulator in discontinuous conduction at light loads.

### Selecting the Forced CCM Mode

In order to set the regulator to operate in Forced CCM, a voltage between 2.0V and 2.8V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from  $V_{IN}$ . If  $V_{IN}$  is well regulated, use a resistor divider and set the voltage to 2.5V. If  $V_{IN}$  varies over a wide range, the circuit shown in Figure 31 can be used to generate the required voltage. Note that at  $V_{IN}$  of 5.5V and 40V, the nominal Zener voltage is 4.0V and 5.0V respectively. Therefore for  $V_{IN}$  in the range of 5.5V to 40V, the circuit shown in Figure 31 will generate  $V_{EN}$  required for Forced CCM.

### Selecting the DCM / CCM Mode

In order to set the regulator operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to EN/MODE pin. If an external control signal is available, it can

be directly connected to EN/MODE. In applications where an external control is not available, EN/MODE input can be derived from  $V_{IN}$ . If  $V_{IN}$  is well regulated, use a resistor divider and set the voltage to 4V. If  $V_{IN}$  varies over a wide range, the circuit shown in Figure 32 can be used to generate the required voltage.

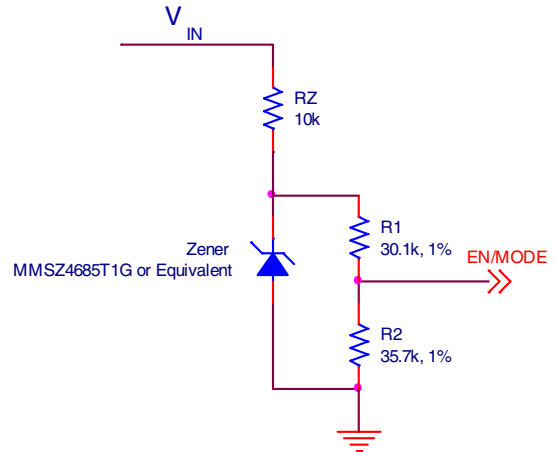


Figure 31: Selecting Forced CCM by Deriving EN/MODE from  $V_{IN}$

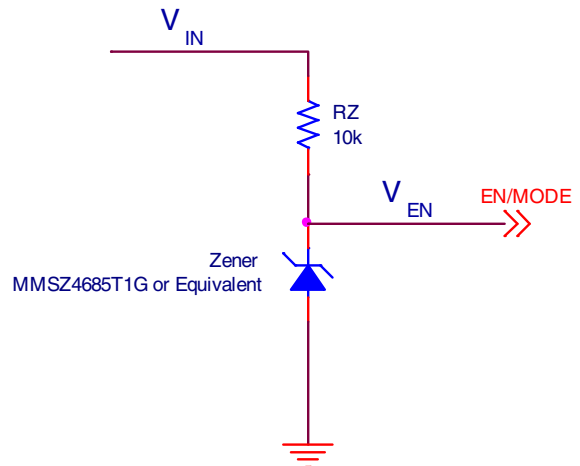


Figure 32: Selecting DCM/CCM by Deriving EN/MODE from  $V_{IN}$

**Programming the On-Time**

The on-time  $T_{ON}$  is programmed via resistor  $R_{ON}$  according to following equation:

$$R_{ON} = \frac{V_{IN} \times [T_{ON} - (25 \times 10^{-9})]}{3.05 \times 10^{-10}}$$

where  $T_{ON}$  is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f \times Eff}$$

where:

$f$  is the desired switching frequency at nominal  $I_{OUT}$

$Eff$  is the regulator efficiency corresponding to nominal  $I_{OUT}$  shown in Figures 19 - 24

Substituting for  $T_{ON}$  in the first equation, we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{f \times Eff}\right) - [(25 \times 10^{-9}) \times V_{IN}]}{3.05 \times 10^{-10}}$$

**Over-Current Protection (OCP)**

If load current exceeds the programmed over-current  $I_{OCP}$ , for four consecutive switching cycles, the regulator enters the hiccup mode of operation. In the hiccup mode, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, the hiccup timeout will repeat. The regulator will remain in hiccup mode until load current is reduced below the programmed  $I_{OCP}$ . In order to program the over-current protection, use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

$RLIM$  is resistor value for programming  $I_{OCP}$

$I_{OCP}$  is the over-current threshold to be programmed

$RDS$  is the MOSFET rated On Resistance; XR76208-Q = 21.5mΩ, XR76205-Q = 59mΩ, XR76203-Q = 59mΩ

8mV is the OCP comparator maximum offset

$ILIM$  is the internal current that generates the necessary OCP comparator threshold (use 45μA)

Note that  $ILIM$  has a positive temperature coefficient of 0.4%/°C (Figure 10). This is meant to roughly match and compensate for the positive temperature coefficient of the synchronous FET. A graph of typical  $I_{OCP}$  versus  $RLIM$  is shown in Figures 7-9. The maximum allowable  $RLIM$  for XR76205-Q is 8.06kΩ.

**Short-Circuit Protection (SCP)**

If the output voltage drops below 60% of its programmed value, the regulator will enter hiccup mode. The hiccup will persist until the short-circuit is removed. The SCP circuit becomes active after  $PGOOD$  asserts high.

**Over-Temperature (OTP)**

OTP triggers at a nominal die temperature of 150°C. The gate of the switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

**Programming the Output Voltage**

Use an external voltage divider as shown in the Application Circuit to program the output voltage  $V_{OUT}$ .

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1\right)$$

where  $R2$  has a nominal value of 2kΩ.

**Programming the Soft-Start**

Place a capacitor  $C_{SS}$  between the  $SS$  and  $AGND$  pins to program the soft-start. In order to program a soft-start time of  $t_{SS}$ , calculate the required capacitance  $C_{SS}$  from the following equation:

$$C_{SS} = t_{SS} \times \left(\frac{10\mu A}{0.6V}\right)$$

### Feed-Forward Capacitor ( $C_{FF}$ )

A feed-forward capacitor ( $C_{FF}$ ) may be necessary, depending on the Equivalent Series Resistance (ESR) of  $C_{OUT}$ . If only ceramic output capacitors are used for  $C_{OUT}$ , then a  $C_{FF}$  is necessary. Calculate  $C_{FF}$  from:

$$C_{FF} = \frac{1}{2 \times \pi \times R1 \times 7 \times f_{LC}}$$

where:

$R1$  is the resistor that  $C_{FF}$  is placed in parallel with

$f_{LC}$  is the frequency of output filter double-pole

$f_{LC}$  frequency must be less than 11kHz when using ceramic  $C_{OUT}$ . If necessary, increase L and / or  $C_{OUT}$  in order to meet this constraint.

When using capacitors with higher ESR such as PANASONIC TPE series, a  $C_{FF}$  is not required, provided the following conditions are met:

1. The frequency of output filter LC double-pole  $f_{LC}$  should be less than 11kHz.
2. The frequency of ESR Zero  $f_{Zero,ESR}$  should be at least five times larger than  $f_{LC}$ .

Note that if  $f_{Zero,ESR}$  is less than  $5f_{LC}$ , then it is recommended to set the  $f_{LC}$  at less than 2kHz.  $C_{FF}$  is still not required.

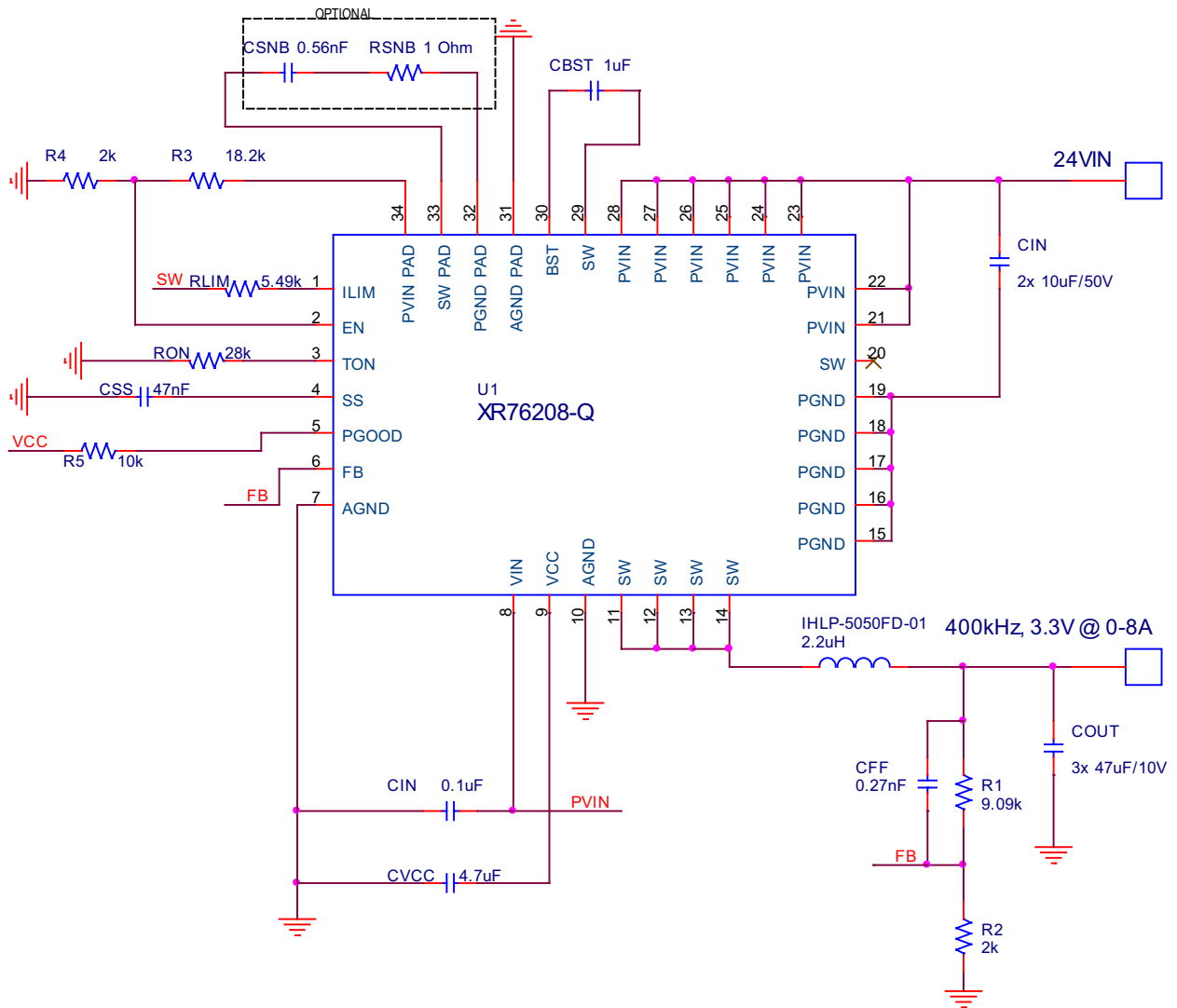
### Maximum Allowable Voltage Ripple at FB pin

Note that the steady-state voltage ripple at feedback pin FB ( $V_{FB,RIPPLE}$ ) must not exceed 50mV in order for the regulator to function correctly. If  $V_{FB,RIPPLE}$  is larger than 50mV, then  $C_{OUT}$  should be increased as necessary in order to keep the  $V_{FB,RIPPLE}$  below 50mV.

### Feed-Forward Resistor ( $R_{FF}$ )

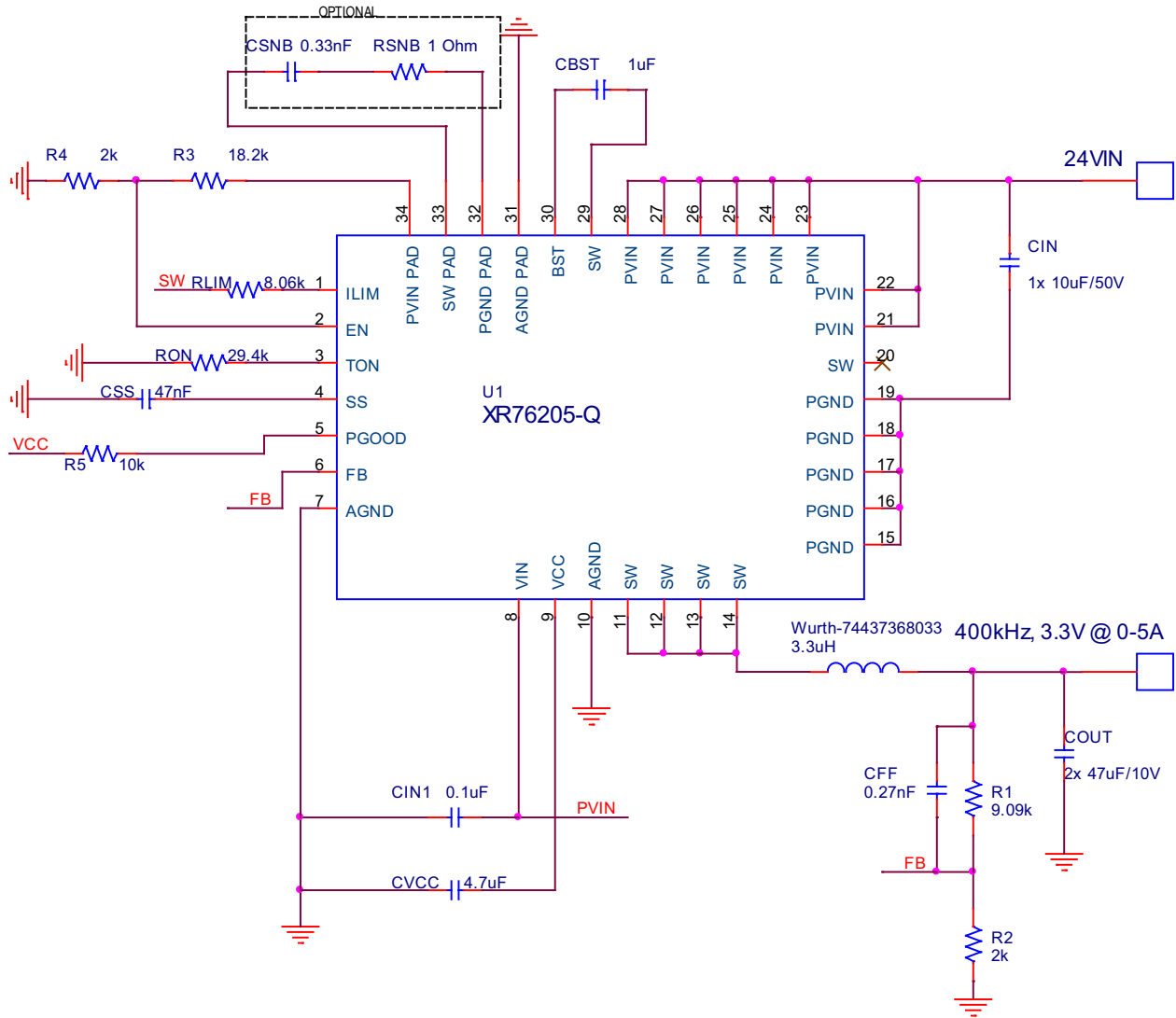
Poor PCB layout can cause FET switching noise at the output and may couple to the FB pin via  $C_{FF}$ . Excessive noise at FB will cause poor load regulation. To solve this problem place a resistor  $R_{FF}$  in series with  $C_{FF}$ . An  $R_{FF}$  value up to 2% of  $R1$  is acceptable.

Application Circuit, XR76208-Q

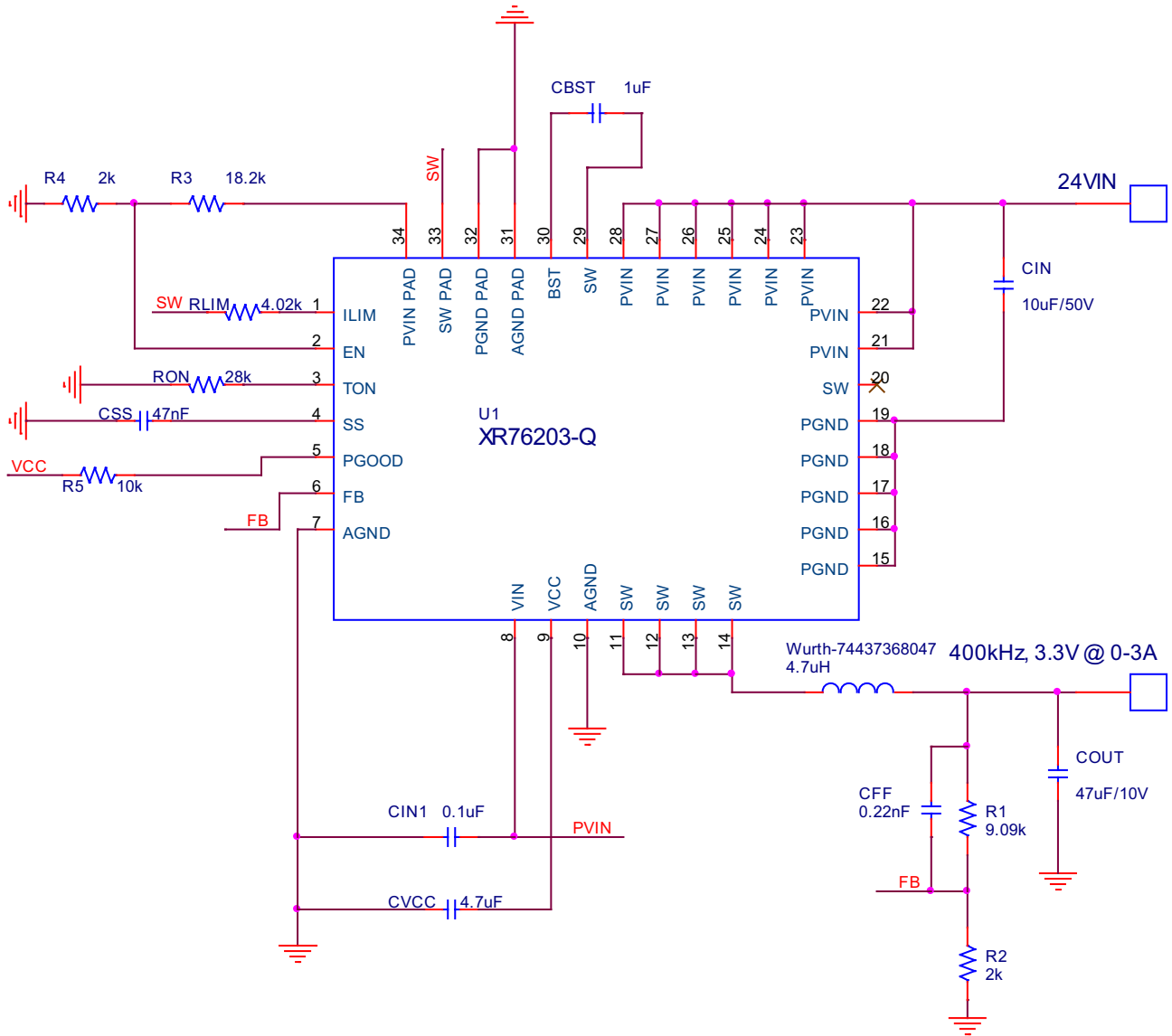




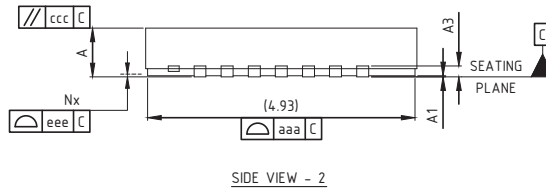
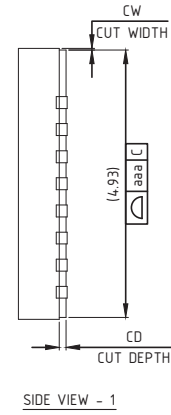
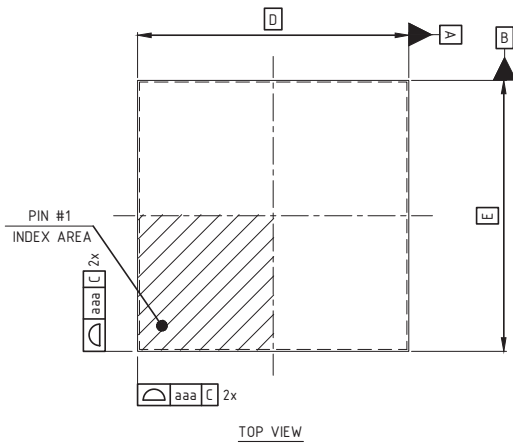
Application Circuit, XR76205-Q



Application Circuit, XR76203-Q

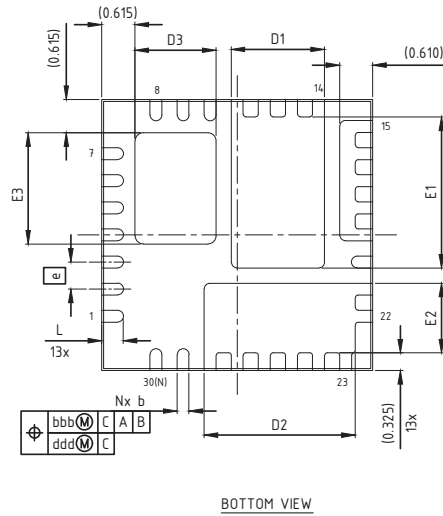


Mechanical Dimensions



Dimension Table			
Thickness Symbol	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20 Ref.	---
b	0.18	0.25	0.30
CD	0.13	0.15	0.17
CW	0.010	0.035	0.060
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
D1	1.570	1.720	1.820
E1	2.635	2.785	2.885
D2	2.635	2.785	2.885
E2	1.135	1.285	1.385
D3	1.345	1.495	1.595
E3	1.903	2.053	2.153
L	0.30	0.40	0.50
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	30		

TERMINAL DETAIL

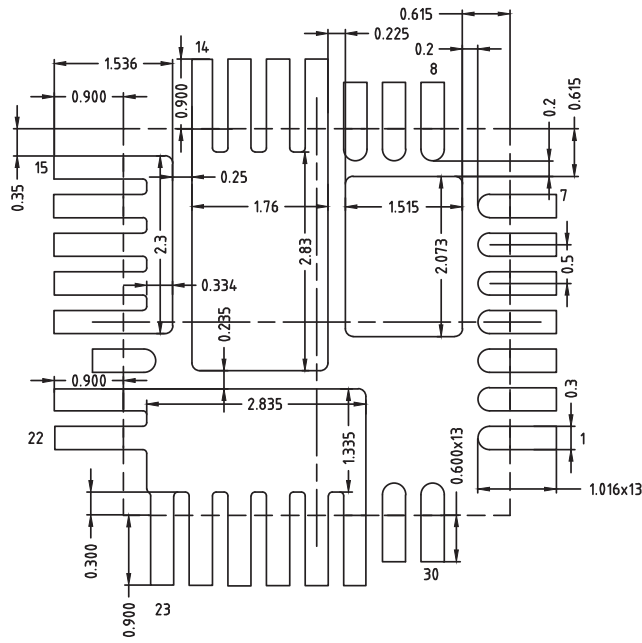


NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

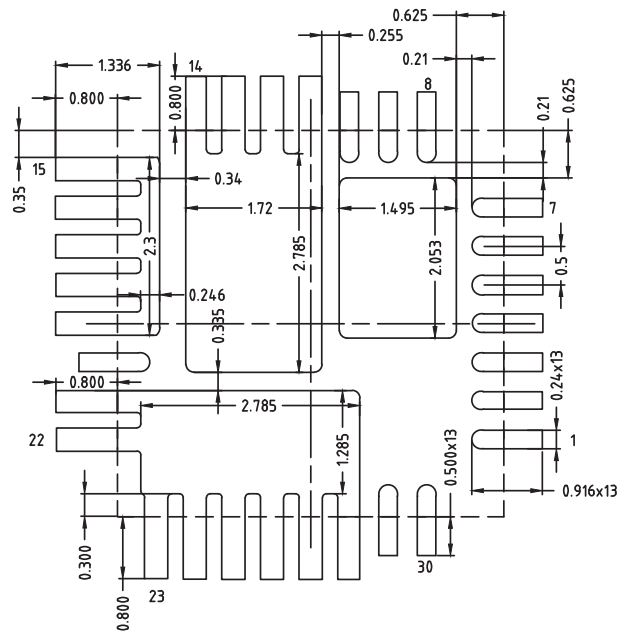
Drawing No.: POD-0000093

Revision: B

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000093

Revision: B

## Ordering Information<sup>(1)</sup>

Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free <sup>(2)</sup>
XR76208-Q				
XR76208EL-Q	-40°C ≤ T <sub>J</sub> ≤ 125°C	5x5mm QFN	Tray	Yes
XR76208ELTR-Q	-40°C ≤ T <sub>J</sub> ≤ 125°C	5x5mm QFN	Tape and Reel	Yes
XR76208EVB-Q	XR76208-Q Evaluation Board			
XR76205-Q				
XR76205EL-Q	-40°C ≤ T <sub>J</sub> ≤ 125°C	5x5mm QFN	Tray	Yes
XR76205ELTR-Q	-40°C ≤ T <sub>J</sub> ≤ 125°C	5x5mm QFN	Tape and Reel	Yes
XR76205EVB-Q	XR76205-Q Evaluation Board			
XR76203-Q				
XR76203EL-Q	-40°C ≤ T <sub>J</sub> ≤ 125°C	5x5mm QFN	Tray	Yes
XR76203ELTR-Q	-40°C ≤ T <sub>J</sub> ≤ 125°C	5x5mm QFN	Tape and Reel	Yes
XR76203EVB-Q	XR76203-Q Evaluation Board			

Notes:

1. Refer to [www.maxlinear.com/XR76203-Q](http://www.maxlinear.com/XR76203-Q), [www.maxlinear.com/XR76205-Q](http://www.maxlinear.com/XR76205-Q), and [www.maxlinear.com/XR76208-Q](http://www.maxlinear.com/XR76208-Q) for most up-to-date Ordering Information.
2. Visit [www.maxlinear.com](http://www.maxlinear.com) for additional information on Environmental Rating.

## Revision History

Revision	Date	Description
1A	January 2017	Initial Release
1B	March 2017	Removed preliminary from XR76203-Q
1C	March 2017	Removed preliminary from XR76208-Q
1D	June 2018	Updated to MaxLinear logo. Updated format and Ordering Information table. Added recommended land pattern and stencil.
1E	October 2019	Correct block diagram by changing the input gate into the Hiccup Mode from an AND gate to an OR gate. Updated Ordering Information.



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