

ORCA ORT8850 Evaluation Board

8 x 850Mbps/s SERDES Plus up to 899K FPGA Gates on One Chip!

Making the Right Choice

Choosing the right backplane transceiver solution is an important investment decision, but evaluating your options shouldn't be complicated. Lattice has created the ORCA® ORT8850 Evaluation Board so you can efficiently test the performance of a completed PCB design based on the ORT8850 Field Programmable System Chip (FPSC) architecture.

Examine Features Such as:

- FPSC flexibility
- ORT8850 performance and features
- Programmable I/O capabilities
- Output strength and clarity

Working on an ORT8850 Application?

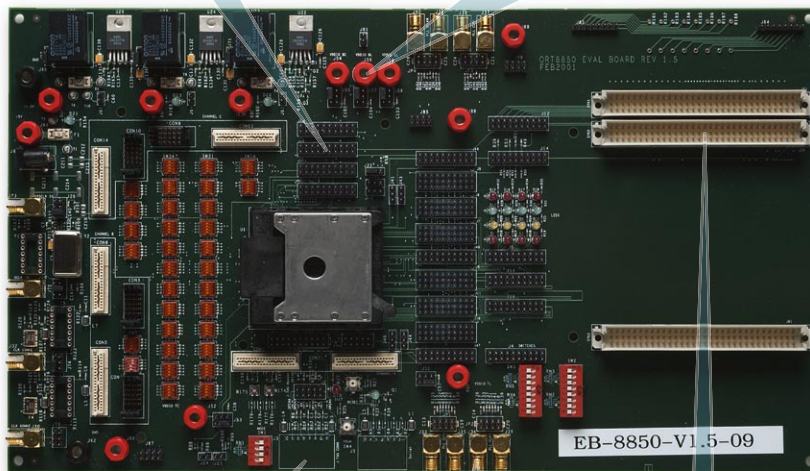
Use the ORT8850 Evaluation Board to help develop your customized ORT8850 solution in an established and flexible environment. Download your design to the ORT8850 for instant feedback.

FPSC I/O Access

Connect to the ORT8850's programmable I/O through standard PCB headers. Check Tx/Rx data through microstrip connectors.

VDD I/O Control

Controls six I/O banks at 3.3V, 2.5V or 1.8V. The ORT8850 supports 12 I/O standards.



Programming and JTAG

Download your design to the ORT8850. Or, use board-specific evaluation bit streams available from Lattice.

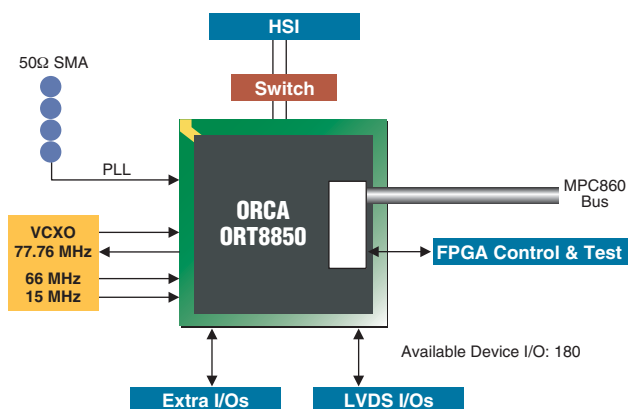
PLL Clock Inputs

Send differential clock signals straight to the ORT8850's four PLLs. Or, use the on-board 77.76MHz VCXO and 66MHz and 15MHz oscillators.

Microprocessor Interfaces

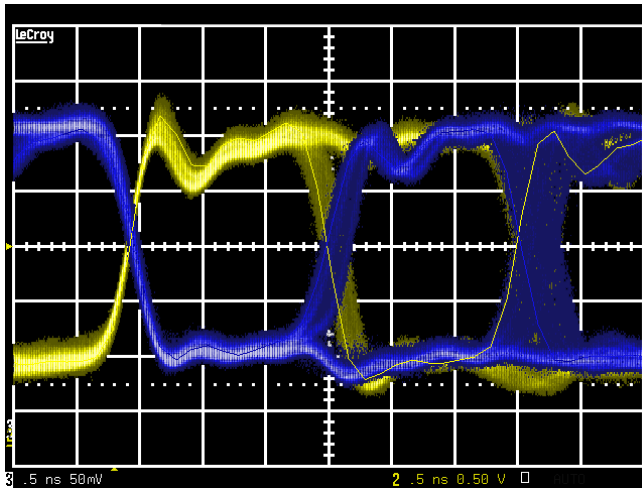
Connect to Power-PC and third-party development daughter cards via MC860 connectors.

ORT8850 Evaluation Board Block Diagram



Full Feature Set

- 180 of the ORT8850H's I/Os are accessible on the board. These include 32 HSI (LVDS) I/Os and other I/Os directly from up to 899K FPGA system gates.
- Includes a regulated power supply for easy set-up.
- Downloadable programming bit streams are available from www.latticesemi.com for testing specific functions of the ORT8850.



About the ORCA ORT8850...

Lattice's ORT8850 is a Field Programmable System Chip based on the ORCA Series 4 Architecture. The ORT8850 integrates eight 850Mbits/s backplane transceiver channels with a flexible FPGA logic core. Features of the ORT8850 include:

- Up to 899K of usable FPGA system gates and 147Kb Embedded RAM (ORT8850H)
- Internal performance of >250MHz
- LVDS I/Os compliant with EIA-644
- Multi-channel alignment FIFOs available
- SONET scrambler/descrambler
- Four programmable PLLs
- 297 programmable user I/O (ORT8850H)

See www.latticesemi.com for complete specifications of the ORT8850

ispLEVER™ Development Tools

ispLEVER is an integrated software system for the development of all Lattice programmable logic devices, including the ORT8850. The ispLEVER software incorporates ASIC design techniques and FPGA development methodologies that meet today's high-speed design demands.

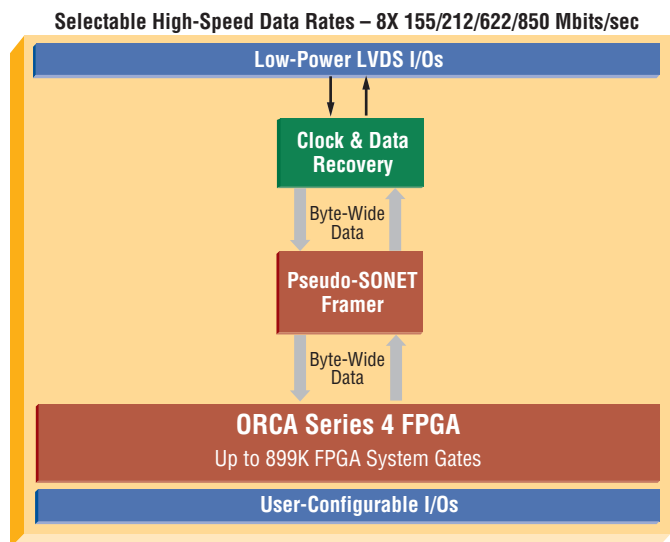


Sharpen Your Focus With the Eye of the ORT8850

Clean data transmission has always been important, but with data wavelengths getting shorter than your backplane, it's crucial! We've focused our engineering efforts on the ORT8850 I/O structure to provide high-quality data transmission exceeding today's tight standards.

With the ORT8850 Evaluation board, you can measure the I/O performance of the ORT8850 in an environment you control. The signal to the left is an actual data-eye of a PRBS pattern generated by the ORT8850's LVDS I/Os at 880Mbits/sec.

ORCA ORT8850 Block Diagram



- Included with the ORT8850 Evaluation Board:
 - ORT8850H-BM680 device
 - ORCA Download Cable
 - Power supply
 - Board schematic and bill of materials

- Available on www.latticesemi.com:
 - ORT8850 Eval Board User Manual and Tutorial
 - IBIS and HSPICE Models, and BSDL files
 - Schematic and Gerber files
 - Evaluation bit streams

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August 2002
 Order #: I0145