

The MPC9446 is a 2.5 V and 3.3 V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3 V, 2.5 V and dual supply voltages are supported for mixed-voltage applications. The MPC9446 offers 10 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9446 is specified for the extended temperature range of -40°C to 85°C .

Features

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3 V/2.5 V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Maximum output skew of 200 ps (150 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32-lead LQFP package, Pb-free
- Ambient operating temperature range of -40 to 85°C
- **For drop in replacement part use 87946AYI-147**

Functional Description

The MPC9446 is a full static fanout buffer design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks. Two independent LVCMOS compatible clock inputs are available. This feature supports redundant clock sources or the addition of a test clock into the system design. Each of the three output banks can be individually supplied by 2.5 V or 3.3 V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9446 can be reset and the outputs are disabled by deasserting the MR/ $\overline{\text{OE}}$ pin (logic high state). Asserting MR/ $\overline{\text{OE}}$ will enable the outputs.

All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated $50\ \Omega$ transmission lines. Please consult the MPC9456 specification for a 1:10 mixed voltage buffer with LVPECL compatible inputs. For series terminated transmission lines, each of the MPC9446 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a $7\times 7\ \text{mm}^2$ 32-lead LQFP package.

MPC9446

**LOW VOLTAGE SINGLE OR
DUAL SUPPLY 2.5 V AND 3.3 V
LVCMOS CLOCK
DISTRIBUTION BUFFER**



**AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04**

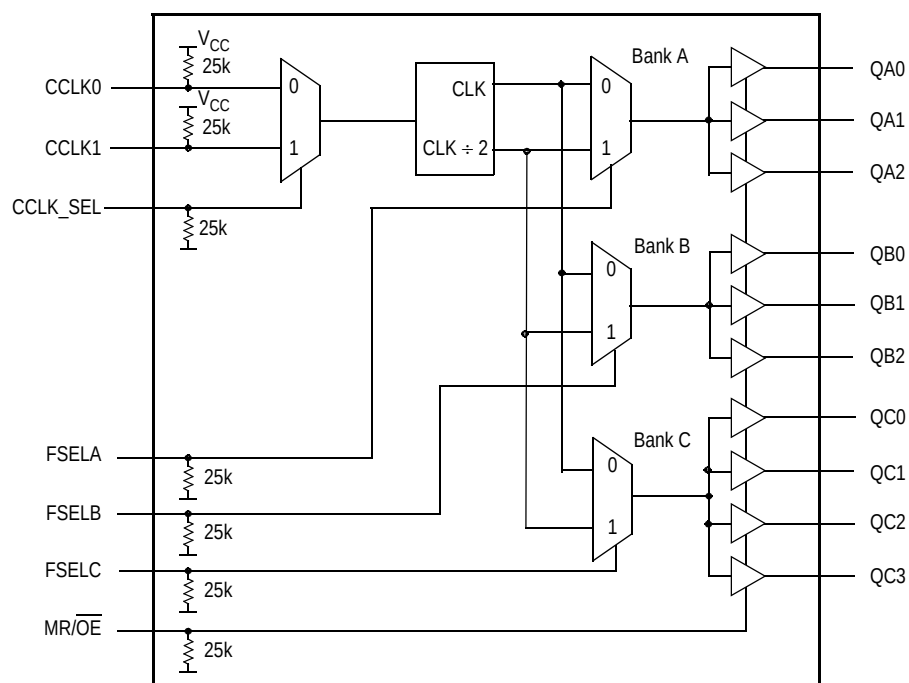


Figure 1. MPC9446 Logic Diagram

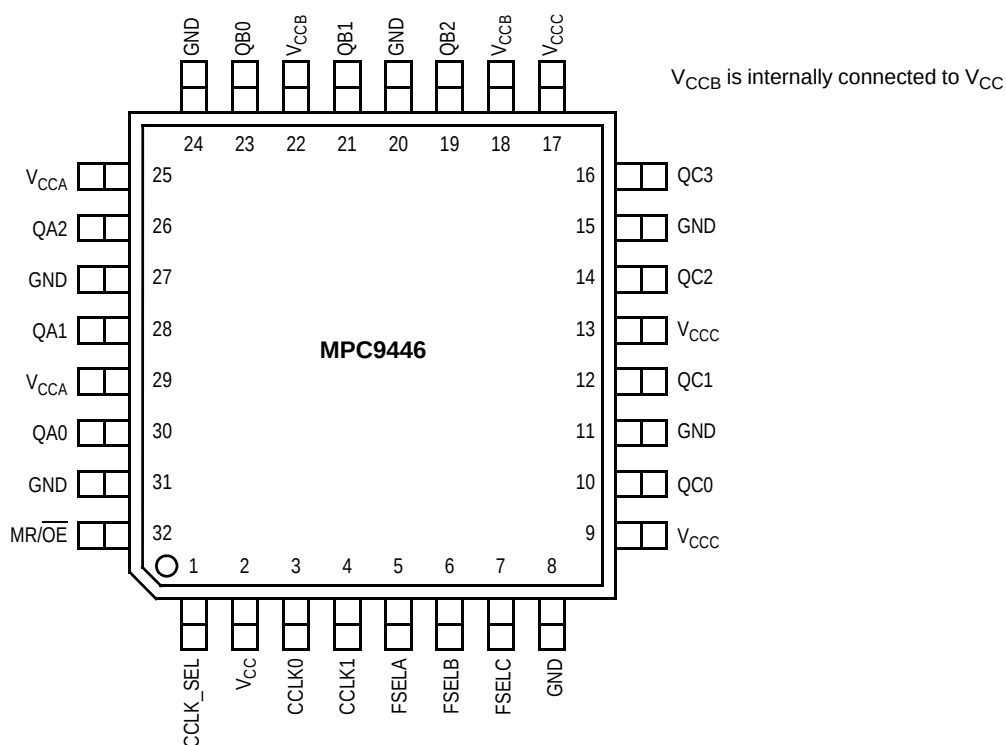


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK0,1	Input	LVC MOS	LVC MOS clock inputs
FSELA, FSELB, FSELC	Input	LVC MOS	Output bank divide select input
MR/ $\overline{\text{OE}}$	Input	LVC MOS	Internal reset and output (high impedance) control
GND		Supply	Negative voltage supply (GND)
$V_{\text{CCA}}, V_{\text{CCB}}^{(1)}, V_{\text{CCC}}$		Supply	Positive voltage supply for output banks
V_{CC}		Supply	Positive voltage supply for core (VCC)
QA0 – QA2	Output	LVC MOS	Bank A outputs
QB0 – QB2	Output	LVC MOS	Bank B outputs
QC0 – QC3	Output	LVC MOS	Bank C outputs

1. V_{CCB} is internally connected to V_{CC} .

Table 2. Supported Single and Dual Supply Configurations

Supply Voltage Configuration	$V_{\text{CC}}^{(1)}$	$V_{\text{CCA}}^{(2)}$	$V_{\text{CCB}}^{(3)}$	$V_{\text{CCC}}^{(4)}$	GND
3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	0 V
Mixed Voltage Supply	3.3 V	3.3 V or 2.5 V	3.3 V	3.3 V or 2.5 V	0 V
2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	0 V

- V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels.
- V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels.
- V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels. V_{CCB} is internally connected to V_{CC} .
- V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels.

Table 3. Function Table (Controls)

Control	Default	0	1
CCLK_SEL	0	CCLK0	CCLK1
FSELA	0	$f_{\text{QA0:2}} = f_{\text{REF}}$	$f_{\text{QA0:2}} = f_{\text{REF}} \div 2$
FSELB	0	$f_{\text{QB0:2}} = f_{\text{REF}}$	$f_{\text{QB0:2}} = f_{\text{REF}} \div 2$
FSELC	0	$f_{\text{QC0:3}} = f_{\text{REF}}$	$f_{\text{QC0:3}} = f_{\text{REF}} \div 2$
MR/ $\overline{\text{OE}}$	0	Outputs enabled	Internal reset outputs disabled (tristate)

Table 4. Absolute Maximum Ratings⁽¹⁾

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	−0.3	3.6	V	
V_{IN}	DC Input Voltage	−0.3	$V_{\text{CC}}+0.3$	V	
V_{OUT}	DC Output Voltage	−0.3	$V_{\text{CC}}+0.3$	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_{S}	Storage Temperature	−65	125	°C	

- Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	

Table 6. DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3 \text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.8	V	LVC MOS
I_{IN}	Input Current ⁽¹⁾			200	μA	$V_{IN} = \text{GND}$ or $V_{IN} = V_{CC}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^{(2)}$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}^{(2)}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output Impedance		14 – 17		Ω	
$I_{CCQ}^{(3)}$	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

1. Input pull-up / pull-down resistors influence input current.
2. The MPC9446 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
3. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 7. AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3 \text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)⁽¹⁾

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		250 ⁽²⁾	MHz	
f_{MAX}	Maximum Output Frequency	0 0		250 ⁽²⁾ 125	MHz MHz	FSELx = 0 FSELx = 1
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ⁽³⁾	ns	0.8 to 2.0 V
t_{PLH} t_{PHL}	Propagation Delay CCLK0,1 to any Q CCLK0,1 to any Q	2.2 2.2	2.8 2.8	4.45 4.2	ns ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{sk(O)}$	Output-to-Output Skew Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew			2.25	ns	
$t_{sk(P)}$	Output Pulse Skew ⁽⁴⁾			200	ps	
DC _Q	Output Duty Cycle	47 45	50 50	53 55	% %	DC _{REF} = 50% DC _{REF} = 25%–75%
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT} .
2. The MPC9446 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
3. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
4. Output pulse skew $t_{sk(P)}$ is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$. Output duty cycle is frequency dependent: $DC_Q = (0.5 \pm t_{sk(P)} \cdot f_{OUT})$. For example at $f_{OUT} = 125 \text{ MHz}$ the output duty cycle limit is $50\% \pm 2.5\%$.

Table 8. DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5 \text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.7	V	LVC MOS
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15 \text{ mA}^{(1)}$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15 \text{ mA}$
Z_{OUT}	Output Impedance		17 – 20 ⁽²⁾		Ω	
I_{IN}	Input Current ⁽²⁾			± 200	μA	$V_{IN} = \text{GND}$ or $V_{IN} = V_{CC}$
$I_{CCQ}^{(3)}$	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

1. The MPC9446 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.
2. Input pull-up / pull-down resistors influence input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 9. AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5 \text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)⁽¹⁾

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		250 ⁽²⁾	MHz	
f_{MAX}	Maximum Output Frequency	$\div 1$ output $\div 2$ output	0 0	250 ⁽²⁾ 125	MHz MHz	FSELx = 0 FSELx = 1
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ⁽³⁾	ns	0.7 to 1.7 V
t_{PLH} t_{PHL}	Propagation Delay CCLK0,1 to any Q CCLK0,1 to any Q	2.6 2.6		5.6 5.5	ns ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{sk(O)}$	Output-to-Output Skew Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew			3.0	ns	
$t_{sk(P)}$	Output Pulse Skew ⁽⁴⁾			200	ps	
DC_Q	Output Duty Cycle	$\div 1$ or $\div 2$ output	50	55	%	$DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT} .
2. The MPC9446 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
3. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
4. Output pulse skew $t_{sk(P)}$ is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$. Output duty cycle is frequency dependent: $DC_Q = (0.5 \pm t_{sk(P)} \cdot f_{OUT})$. For example at $f_{OUT} = 125 \text{ MHz}$ the output duty cycle limit is $50\% \pm 2.5\%$.

Table 10. AC Characteristics ($V_{CC} = 3.3 \text{ V} + 5\%$, $V_{CCA}, V_{CCB}, V_{CCC} = 2.5 \text{ V} + 5\%$ or $3.3 \text{ V} + 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)^{(1) (2)}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$t_{sk(O)}$	Output-to-Output Skew Within one bank Any output bank, same output divider Any output, Any output divider			150 250 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew			2.5	ns	
$t_{PLH, HL}$	Propagation Delay CCLK0,1 to any Q	See 3.3 V Table				
$t_{sk(P)}$	Output Pulse Skew ⁽³⁾			250	ps	
DC_Q	Output Duty Cycle	$\div 1$ or $\div 2$ output	50	55	%	$DC_{REF} = 50\%$

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT} .
2. For all other AC specifications, refer to 2.5 V or 3.3 V tables according to the supply voltage of the output bank.
3. Output pulse skew $t_{sk(P)}$ is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$. Output duty cycle is frequency dependent: $DC_Q = (0.5 \pm t_{sk(P)} \cdot f_{OUT})$.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9446 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω , the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current, and thus, only a single terminated line can be driven by each output of the MPC9446 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9446 clock driver is effectively doubled due to its capability to drive multiple lines.

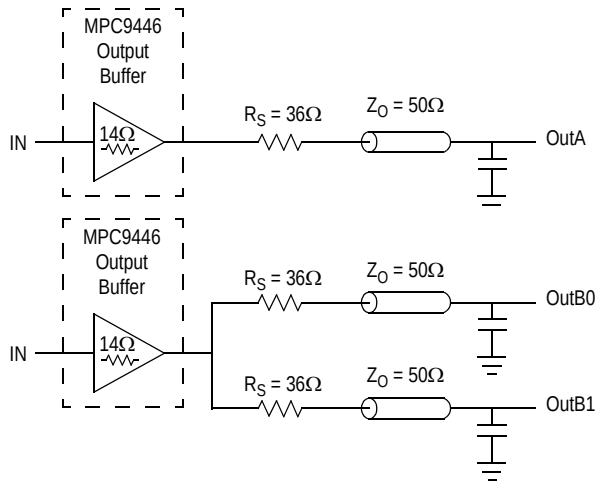


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9446 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9446. The output waveform in Figure 4 shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of

the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50 \Omega \parallel 50 \Omega \\ R_S &= 36 \Omega \parallel 36 \Omega \\ R_0 &= 14 \Omega \\ V_L &= 3.0 (25 \div (18 + 14 + 25)) \\ &= 1.31 \text{ V} \end{aligned}$$

At the load end, the voltage will double, due to the near unity reflection coefficient, to 2.5 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

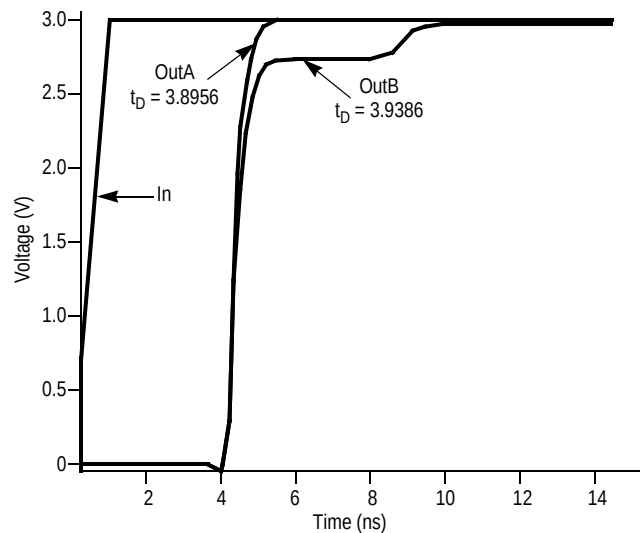


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 5 should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.

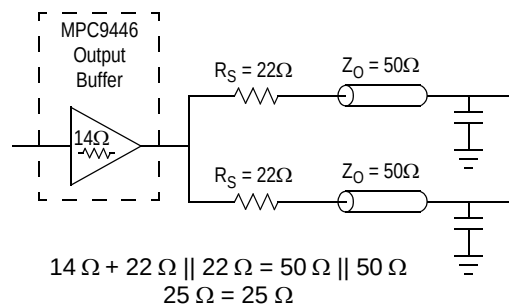


Figure 5. Optimized Dual Line Termination

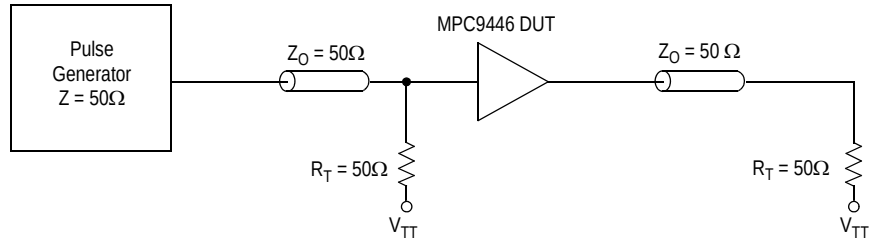


Figure 6. CCLK0, 1 MPC9446 AC Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$

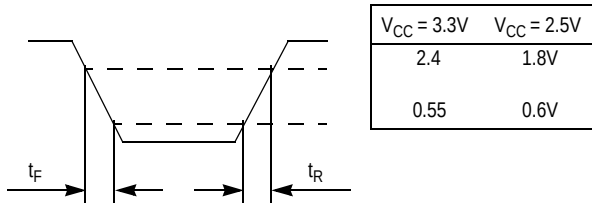


Figure 7. Output Transition Time Test Reference

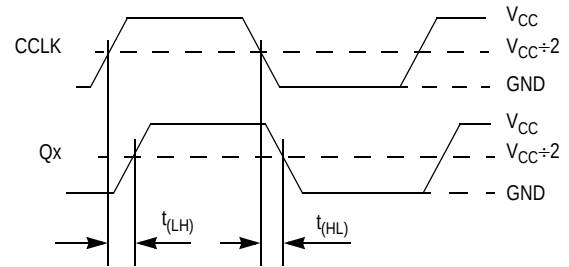
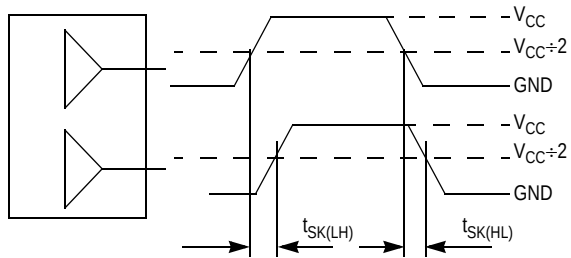
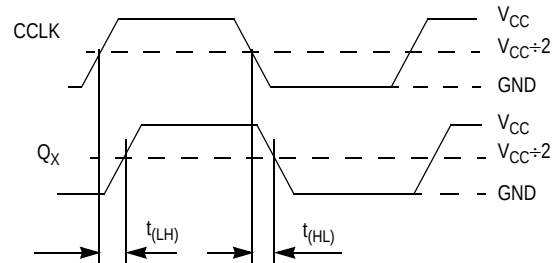


Figure 8. Propagation Delay (t_{PD}) Test Reference



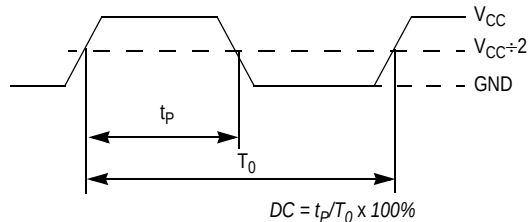
The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device.

Figure 9. Output-to-Output Skew $t_{SK(LH, HL)}$



$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Figure 10. Output Pulse Skew ($t_{SK(P)}$) Test Reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 11. Output Duty Cycle (DC)

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

PAGE 3 OF 3

**CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE**

Revision History Sheet

Rev	Table	Page	Description of Change	Date
5		1	NRND – Not Recommend for New Designs	12/21/12
5		1	Removed NRND - Not Recommended For New Designs Updated Data Sheet format	2/13/15
5		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02	3/14/16

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.