Description

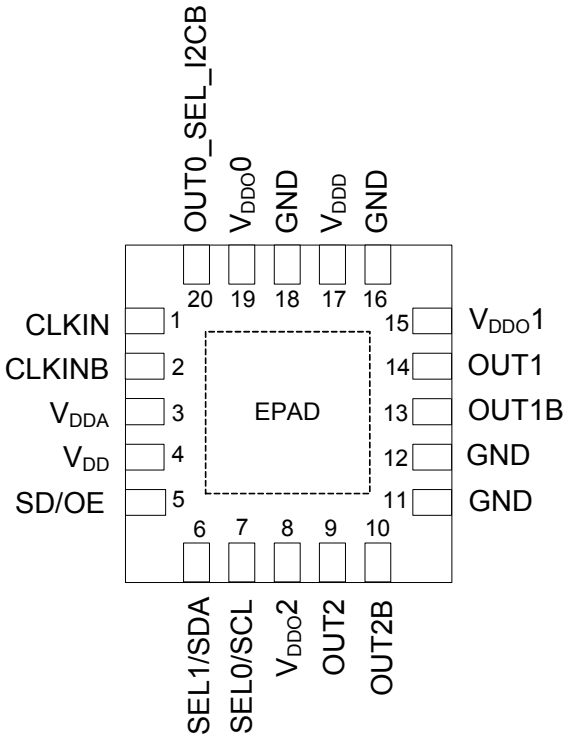
The 5P49V5943 is a programmable clock generator intended for high performance consumer, networking, industrial, computing, and data-communications applications. Configurations may be stored in on-chip One-Time Programmable (OTP) memory or changed using I^2C interface. This is IDTs fifth generation of programmable clock technology (VersaClock® 5).

The frequencies are generated from a single input reference clock.

Two select pins allow up to 4 different configurations to be programmed and accessible using processor GPIOs or bootstrapping. The different selections may be used for different operating modes (full function, partial function, partial power-down), regional standards (US, Japan, Europe) or system production margin testing.

The device may be configured to use one of two I^2C addresses to allow multiple devices to be used in a system.

Pin Assignment



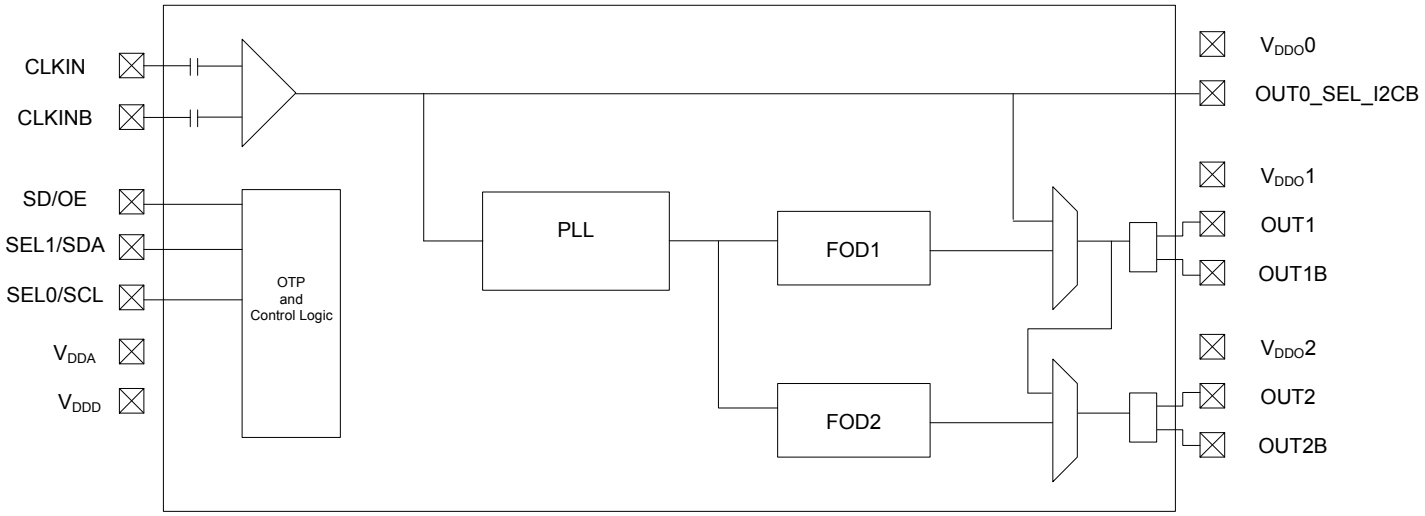
20-pin VFQFPN

Features

- Generates up to two independent output frequencies
- High performance, low phase noise PLL, <0.7 ps RMS typical phase jitter on outputs:
  - PCIe Gen1, 2, 3 compliant clock capability
  - USB 3.0 compliant clock capability
  - 1 GbE and 10 GbE
- Two fractional output dividers (FODs)
- Independent Spread Spectrum capability on each output pair
- Four banks of internal non-volatile in-system programmable or factory programmable OTP memory
- I^2C serial programming interface
- One reference LVCMOS output clock
- Two universal output pairs:
  - Each configurable as one differential output pair or two LVCMOS outputs
- I/O Standards:
  - Single-ended I/Os: 1.8V to 3.3V LVCMOS
  - Differential I/Os - LVPECL, LVDS and HCSL
- Input frequency ranges:
  - LVDS, LVPECL, HCSL Differential Clock Input (CLKIN, CLKINB) – 1MHz to 350MHz
- Output frequency ranges:
  - LVCMOS Clock Outputs – 1MHz to 200MHz
  - LVDS, LVPECL, HCSL Differential Clock Outputs – 1MHz to 350MHz
- Individually selectable output voltage (1.8V, 2.5V, 3.3V) for each output pair
- Programmable loop bandwidth
- Programmable output to output skew
- Programmable slew rate control
- Individual output enable/disable
- Power-down mode
- 1.8V, 2.5V or 3.3V core V_{DDD}, V_{DDA}
- Available in 20-pin VFQFPN 3mm x 3mm package
- -40° to +85°C industrial temperature operation

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Functional Block Diagram



Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

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Table 1: Pin Descriptions

Number	Name	Type		Description
1	CLKIN	Input	Pull-down	Differential clock input. Weak 100kohms internal pull-down.
2	CLKINB	Input	Pull-down	Complementary differential clock input. Weak 100kohms internal pull-down.
3	VDDA	Power		Analog functions power supply pin. Connect to 1.8V to 3.3V. VDDA and VDDD should have the same voltage applied.
4	VDD	Power		Power supply pin. Connect to 1.8 to 3.3V.
5	SD/OE	Input	Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD). The SH bit controls the configuration of the SD/OE pin. The SH bit needs to be high for SD/OE pin to be configured as SD. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW only when pin is configured as OE (Default is active LOW.) Weak internal pull down resistor. When configured as SD, device is shut down, differential outputs are driven high/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs can be selected to be tri-stated or driven high/low, depending on the programming bits as shown in the SD/OE Pin Function Truth table.
6	SEL1/SDA	Input	Pull-down	Configuration select pin, or I2C SDA input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
7	SEL0/SCL	Input	Pull-down	Configuration select pin, or I2C SCL input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
8	VDDO2	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT2/OUT2B.
9	OUT2	Output		Output Clock 2. Please refer to the Output Drivers section for more details.
10	OUT2B	Output		Complementary Output Clock 2. Please refer to the Output Drivers section for more details.
11	GND	Power		Connect to ground.
12	GND	Power		Connect to ground.
13	OUT1B	Output		Complementary Output Clock 1. Please refer to the Output Drivers section for more details.
14	OUT1	Output		Output Clock 1. Please refer to the Output Drivers section for more details.
15	VDDO1	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1/OUT1B.
16	GND	Power		Connect to ground.
17	VDDD	Power		Digital functions power supply pin. Connect to 1.8 to 3.3V. VDDA and VDDB should have the same voltage applied.
18	GND	Power		Connect to ground.
19	VDDO0	Power		Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
20	OUT0_SELB_I2C	Input/Output	Pull-down	Latched input/LVCMOS Output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 8 and 9. If a weak pull up (10Kohms) is placed on OUT0_SEL_I2CB, pins 8 and 9 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 8 and 9 will act as the SDA and SCL pins of an I2C interface. After power up, the pin acts as a LVCMOS reference output.
ePAD		Power		Connect to ground pad.

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PLL Features and Descriptions

Spread Spectrum

To help reduce electromagnetic interference (EMI), the 5P49V5943 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The 5P49V5943 implements spread spectrum using the Fractional-N output divide, to achieve controllable modulation rate and spreading magnitude. The Spread spectrum can be applied to any output clock, any clock frequency, and any spread amount from ±0.25% to ±2.5% center spread and -0.5% to -5% down spread.

Table 2: Loop Filter

PLL loop bandwidth range depends on the input reference frequency (Fref) and can be set between the loop bandwidth range as shown in the table below.

Input Reference Frequency–Fref (MHz)	Loop Bandwidth Min (kHz)	Loop Bandwidth Max (kHz)
1	40	126
350	300	1000

Table 3: Configuration Table

This table shows the SEL1, SEL0 settings to select the configuration stored in OTP. Four configurations can be stored in OTP. These can be factory programmed or user programmed.

OUT0_SEL_I2CB @ POR	SEL1	SEL0	I^2C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	X	X	Yes	1	I2C defaults
0	X	X	Yes	0	0

At power up time, the SEL0 and SEL1 pins must be tied to either the VDDD/VDDA power supply so that they ramp with that supply or are tied low (this is the same as floating the pins). This will cause the register configuration to be loaded that is selected according to Table 3 above. Providing that OUT0_SEL_I2CB was 1 at POR and OTP register 0:7=0, after the first 10mS of operation the levels of the SELx pins can be changed, either to low or to the same level as VDDD/VDDA. The SELx pins must be driven with a digital signal of < 300ns Rise/Fall time and only a single pin can be changed at a time.

After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

If OUT0_SEL_I2CB was 0 at POR, alternate configurations can only be loaded via the I2C interface.

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Reference Clock Input Pins

The 5P49V5943 supports one reference clock input. The clock input (CLKIN, CLKINB) is a fully differential input that only accepts a reference clock. The differential input accepts differential clocks from all the differential logic types and can also be driven from a single ended clock on one of the input pins.

OTP Interface

The 5P49V5943 can also store its configuration in an internal OTP. The contents of the device's internal programming registers can be saved to the OTP by setting burn_start (W114[3]) to high and can be loaded back to the internal programming registers by setting usr_rd_start(W114[0]) to high.

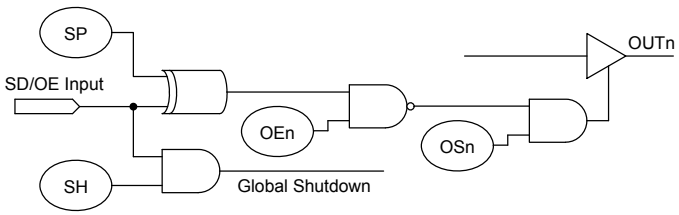
To initiate a save or restore using I^2C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the 5P49V5943 will not generate Acknowledge bits. The 5P49V5943 will acknowledge the instructions after it has completed execution of them. During that time, the I^2C bus should be interpreted as busy by all other users of the bus.

On power-up of the 5P49V5943, an automatic restore is performed to load the OTP contents into the internal programming registers. The 5P49V5943 will be ready to accept a programming instruction once it acknowledges its 7-bit I^2C address.

Availability of Primary and Secondary I^2C addresses to allow programming for multiple devices in a system. The I^2C slave address can be changed from the default 0xD4 to 0xD0 by programming the I2C_ADDR bit D0. *VersaClock 5 Programming Guide* provides detailed I^2C programming guidelines and register map.

SD/OE Pin Function

The polarity of the SD/OE signal pin can be programmed to be either active HIGH or LOW with the SP bit (W16[1]). When SP is “0” (default), the pin becomes active LOW and when SP is “1”, the pin becomes active HIGH. The SD/OE pin can be configured as either to shutdown the PLL or to enable/disable the outputs. The SH bit controls the configuration of the SD/OE pin The SH bit needs to be high for SD/OE pin to be configured as SD.



When configured as SD, device is shut down, differential outputs are driven High/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs are driven high/low.

Table 4: SD/OE Pin Function Truth Table

SH bit	SP bit	OSn bit	OEn bit	SD/OE	OUTn
0	0	0	x	x	Tri-state[2]
0	0	1	0	x	Output active
0	0	1	1	0	Output active
0	0	1	1	1	Output driven High Low
0	1	0	x	x	Tri-state[2]
0	1	1	0	x	Output active
0	1	1	1	0	Output driven High Low
0	1	1	1	1	Output active
1	0	0	x	0	Tri-state[2]
1	0	1	0	0	Output active
1	0	1	1	0	Output active
1	1	0	x	0	Tri-state[2]
1	1	1	0	0	Output active
1	1	1	1	0	Output driven High Low
1	x	x	x	1	Output driven High Low [1]

Note 1 : Global Shutdown
Note 2 : Tri-state regardless of OEn bits

Output Alignment

Each output divider block has a synchronizing POR pulse to provide startup alignment between outputs. This allows alignment of outputs for low skew performance. The phase alignment works both for integer output divider values and for fractional output divider values.

Besides the POR at power up, the same synchronization reset is also triggered when switching between configurations with the SEL0/1 pins. This ensures that the outputs remain aligned in every configuration. This reset causes the outputs to suspend for a few hundred microseconds so the switchover is not glitch-less. The reset can be disabled for applications where glitch-less switch over is required and alignment is not critical.

When using I^2C to reprogram an output divider during operation, alignment can be lost. Alignment can be restored by manually triggering the reset through I^2C.

When alignment is required for outputs with different frequencies, the outputs are actually aligned on the falling edges of each output by default. Rising edge alignment can also be achieved by utilizing the programmable skew feature to delay the faster clock by 180 degrees. The programmable skew feature also allows for fine tuning of the alignment.

For details of register programming, please see VersaClock 5 Family Register Descriptions and Programming Guide for details.

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Output Divides

Each of the four output divides are comprised of a 12-bit integer counter, and a 24-bit fractional counter. The output divide can operate in integer divide only mode for improved performance, or utilize the fractional counters to generate any frequency with a synthesis accuracy better than 50ppb.

The Output Divide also has the capability to apply a spread modulation to the output frequency. Independent of output frequency, a triangle wave modulation between 30 and 63kHz may be generated.

Output Skew

For outputs that share a common output divide value, there will be the ability to skew outputs by quadrature values to minimize interaction on the PCB. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. So, for 100 MHz output and a 2800 MHz VCO, you can select how many 11.161pS units you want added to your skew (resulting in units of 0.402 degrees). For example, 0, 0.402, 0.804, 1.206, 1.408, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

Output Drivers

The OUT1 to OUT2 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels

The operating voltage ranges of each output is determined by its independent output power pin (V_{DDO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential HCSL, LVPECL operation, and 1. 8V, 2.5V, or 3.3V are supported for LVCMOS and differential LVDS operation.

Each output may be enabled or disabled by register bits. When disabled an output will be in a logic 0 state as determined by the programming bit table shown on page 6.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the OUTx and OUTxB outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to both the OUTx and OUTxB pins. The OUTx and OUTxB outputs can be selected to be phase-aligned with each other or inverted relative to one another by register programming bits. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Device Hardware Configuration

The 5P49V5943 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with up to 4 complete device configuration.

These configurations can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The 5P49V5943 has an internal power-up reset (POR) circuit. The POR circuit will remain active for a maximum of 10ms after device power-up.

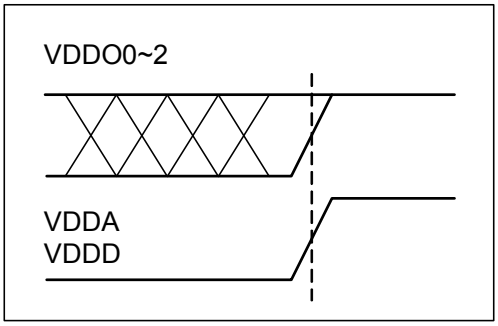
Upon internal POR circuit expiring, the device will exit reset and begin self-configuration.

The device will load internal registers according to Table 3.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the selected source and begin operation.

Power Up Ramp Sequence

VDDA and VDDD must ramp up together. VDDO0~2 must ramp up before, or concurrently with, VDDA and VDDD. All power supply pins must be connected to a power rail even if the output is unused. All power supplies must ramp in a linear fashion and ramp monotonically.

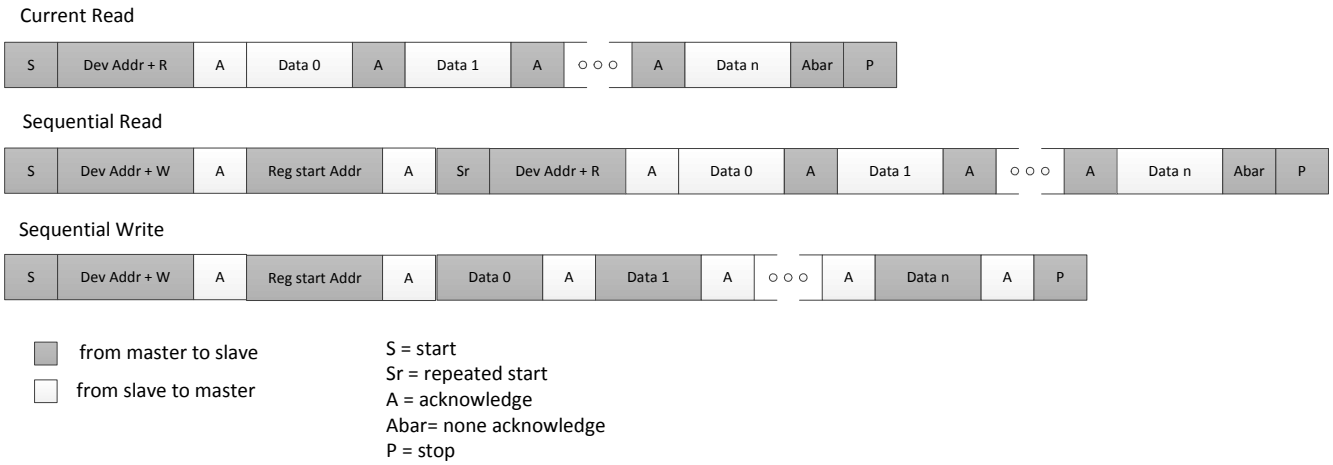


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I²C Mode Operation

The device acts as a slave device on the I²C bus using one of the two I²C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.



I²C Slave Read and Write Cycle Sequencing

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Table 5: I²C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	Input HIGH Level	For SEL1/SDA pin and SEL0/SCL pin.	0.7xVDDD		5.5 [2]	V
VIL	Input LOW Level	For SEL1/SDA pin and SEL0/SCL pin.	GND-0.3		0.3xVDDD	V
VHYS	Hysteresis of Inputs		0.05xVDDD			V
IIN	Input Leakage Current		-1		30	µA
VOL	Output LOW Voltage	IOL = 3 mA			0.4	V

Table 6: I²C Bus AC Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
FSCLK	Serial Clock Frequency (SCL)		10		400	kHz
tBUF	Bus free time between STOP and START		1.3			µs
tSU:START	Setup Time, START		0.6			µs
tHD:START	Hold Time, START		0.6			µs
tSU:DATA	Setup Time, data input (SDA)		0.1			µs
tHD:DATA	Hold Time, data input (SDA) 1		0			µs
tOVD	Output data valid from clock				0.9	µs
CB	Capacitive Load for Each Bus Line				400	pF
tR	Rise Time, data and clock (SDA, SCL)		20 + 0.1xCB		300	ns
tF	Fall Time, data and clock (SDA, SCL)		20 + 0.1xCB		300	ns
tHIGH	HIGH Time, clock (SCL)		0.6			µs
tLOW	LOW Time, clock (SCL)		1.3			µs
tSU:STOP	Setup Time, STOP		0.6			µs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 2: I2C inputs are 5V tolerant.

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Table 7: Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P49V5943. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.465V
Inputs CLKIN, CLKINB Other inputs	 0V to 1.2V voltage swing single-ended -0.5V to V_{DDD}
Outputs, V_{DDO} (LVCMOS)	-0.5V to V_{DDO}+ 0.5V
Outputs, I_O (SDA)	10mA
Package Thermal Impedance, θ_{JA}	42°C/W (0 mps)
Package Thermal Impedance, θ_{JC}	41.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C

Table 8: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDOX}	Power supply voltage for supporting 1.8V outputs	1.71	1.8	1.89	V
V_{DDOX}	Power supply voltage for supporting 2.5V outputs	2.375	2.5	2.625	V
V_{DDOX}	Power supply voltage for supporting 3.3V outputs	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply.	1.71		3.465	V
T_A	Operating temperature, ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVCMOS only)			15	pF
F_{IN}	External reference clock CLKIN, CLKINB	5		350	MHz
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Note: $V_{DDO}1$, $V_{DDO}2$, $V_{DDO}3$, and $V_{DDO}4$ must be powered on either before or simultaneously with V_{DDD}, V_{DDA} and $V_{DDO}0$.

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Table 9: Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance (T_A = +25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
CIN	Input Capacitance (CLKIN, CLKINB, SD/OE, SEL1/SDA, SEL0/SCL)		3	7	pF
Pull-down Resistor	SD/OE, SEL1/SDA, SEL0/SCL, CLKIN, CLKINB, OUT0_SEL_I2CB	100		300	kΩ
ROUT	LVCMOS Output Driver Impedance (VDDO = 1.8V, 2.5V, 3.3V)		17		Ω

Table 10: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Iddcore[3]	Core Supply Current	100 MHz on all outputs, 25 MHz REFCLK		30	34	mA
Iddox	Output Buffer Supply Current	LVPECL, 350 MHz, 3.3V VDDOx		42	47	mA
		LVPECL, 350 MHz, 2.5V VDDOx		37	42	mA
		LVDS, 350 MHz, 3.3V VDDOx		18	21	mA
		LVDS, 350 MHz, 2.5V VDDOx		17	20	mA
		LVDS, 350 MHz, 1.8V VDDOx		16	19	mA
		HCSL, 250 MHz, 3.3V VDDOx, 2 pF load		29	33	mA
		HCSL, 250 MHz, 2.5V VDDOx, 2 pF load		28	33	mA
		LVCMOS, 50 MHz, 3.3V, VDDOx [1,2]		16	18	mA
		LVCMOS, 50 MHz, 2.5V, VDDOx [1,2]		14	16	mA
		LVCMOS, 50 MHz, 1.8V, VDDOx [1,2]		12	14	mA
		LVCMOS, 200 MHz, 3.3V VDDOx[1]		36	42	mA
		LVCMOS, 200 MHz, 2.5V VDDOx[1,2]		27	32	mA
		LVCMOS, 200 MHz, 1.8V VDDOx[1,2]		16	19	mA
Iddpd	Power Down Current	SD asserted, I2C Programming		10	14	mA

1. Single CMOS driver active.
2. Measured into a 5” 50 Ohm trace with 2 pF load.
3. Iddcore = IddA+ IddD, no loads.

Table 11: Electrical Characteristics – Differential Clock Input Parameters [1,2] (Supply Voltage V_{DDA}, V_{DDD}, V_{DDO}0 = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VIH	Input High Voltage - CLKIN, CLKINB	Single-ended input	0.55		1.7	V
VIL	Input Low Voltage - CLKIN, CLKINB	Single-ended input	GND - 0.3		0.4	V
VSWING	Input Amplitude - CLKIN, CLKINB	Peak to Peak value, single-ended	200		1200	mV
dv/dt	Input Slew Rate - CLKIN, CLKINB	Measured differentially	0.4		8	V/ns
IIL	Input Leakage Low Current	VIN = GND	-5		5	µA
IIH	Input Leakage High Current	VIN = 1.7V			20	µA
dTIN	Input Duty Cycle	Measurement from differential waveform	45		55	%

1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through ±75mV window centered around differential zero.

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Table 12: DC Electrical Characteristics for 3.3V LVCMOS (V_{DDO} = 3.3V±5%, TA = -40°C to +85°C)[1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = -15mA	2.4		VDDO	V
VOL	Output LOW Voltage	IOL = 15mA			0.4	V
IOZDD	Output Leakage Current (OUT1~4)	Tri-state outputs, VDDO = 3.465V			5	µA
IOZDD	Output Leakage Current (OUT0)	Tri-state outputs, VDDO = 3.465V			30	µA
VIH	Input HIGH Voltage	Single-ended inputs - SD/OE	0.7xVDDD		VDDD + 0.3	V
VIL	Input LOW Voltage	Single-ended inputs - SD/OE	GND - 0.3		0.3xVDDD	V
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	2		VDDO0 + 0.3	V
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	SD/OE, SEL1/SDA, SEL0/SCL			300	ns

1. See “Recommended Operating Conditions” table.

Table 13: DC Electrical Characteristics for 2.5V LVCMOS (V_{DDO} = 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = -12mA	0.7xVDDO			V
VOL	Output LOW Voltage	IOL = 12mA			0.4	V
IOZDD	Output Leakage Current (OUT1~4)	Tri-state outputs, VDDO = 2.625V			5	µA
IOZDD	Output Leakage Current (OUT0)	Tri-state outputs, VDDO = 2.625V			30	µA
VIH	Input HIGH Voltage	Single-ended inputs - SD/OE	0.7xVDDD		VDDD + 0.3	V
VIL	Input LOW Voltage	Single-ended inputs - SD/OE	GND - 0.3		0.3xVDDD	V
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	1.7		VDDO0 + 0.3	V
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	SD/OE, SEL1/SDA, SEL0/SCL			300	ns

Table 14: DC Electrical Characteristics for 1.8V LVCMOS (V_{DDO} = 1.8V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = -8mA	0.7 xVDDO		VDDO	V
VOL	Output LOW Voltage	IOL = 8mA			0.25 x VDDO	V
IOZDD	Output Leakage Current (OUT1~4)	Tri-state outputs, VDDO = 3.465V			5	µA
IOZDD	Output Leakage Current (OUT0)	Tri-state outputs, VDDO = 3.465V			30	µA
VIH	Input HIGH Voltage	Single-ended inputs - SD/OE	0.7 * VDDD		VDDD + 0.3	V
VIL	Input LOW Voltage	Single-ended inputs - SD/OE	GND - 0.3		0.3 * VDDD	V
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	0.65 * VDDO0		VDDO0 + 0.3	V
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	SD/OE, SEL1/SDA, SEL0/SCL			300	ns

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Table 15: DC Electrical Characteristics for LVDS (V_{DDO} = 3.3V±5% or 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\triangle V_{OT}$	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	1.125	1.25	1.375	V
$\triangle V_{OS}$	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -		6	12	mA

Table 16: DC Electrical Characteristics for LVDS (V_{DDO} = 1.8V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\triangle V_{OT}$	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	0.8	0.875	0.95	V
$\triangle V_{OS}$	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -		6	12	mA

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Table 17: DC Electrical Characteristics for LVPECL (V_{DDO} = 3.3V±5% or 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output Voltage HIGH, terminated through 50Ω tied to V_{DD} - 2 V	V_{DDO} - 1.19		V_{DDO} - 0.69	V
V_{OL}	Output Voltage LOW, terminated through 50Ω tied to V_{DD} - 2 V	V_{DDO} - 1.94		V_{DDO} - 1.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	0.55		0.993	V

Table 18: Electrical Characteristics – DIF 0.7V Low Power HCSL Differential Outputs

(V_{DDO} = 3.3V±5%, 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
dV/dt	Slew Rate	Scope averaging on	1		4	V/ns	1,2,3
ΔdV/dt	Slew Rate	Scope averaging on			20	%	1,2,3
VHIGH	Voltage High	Statistical measurement on single-ended signal using oscilloscope math function (Scope averaging ON)	660		850	mV	1,6,7
VLOW	Voltage Low		-150		150	mV	1,6
VMAX	Maximum Voltage	Measurement on single-ended signal using absolute value (Scope averaging off)			1150	mV	1
VMIN	Minimum Voltage		-300			mV	1
VSWING	Voltage Swing	Scope averaging off	300			mV	1,2,6
VCROSS	Crossing Voltage Value	Scope averaging off	250		550	mV	1,4,6
ΔVCROSS	Crossing Voltage variation	Scope averaging off			140	mV	1,5

1. Guaranteed by design and characterization. Not 100% tested in production
2. Measured from differential waveform.
3. Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
4. V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
5. The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS} min/max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.
6. Measured from single-ended waveform.
7. Measured with scope averaging off, using statistics function. Variation is difference between min. and max.

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Table 19: AC Timing Electrical Characteristics

(V_{DDO} = 3.3V+5% or 2.5V+5% or 1.8V ±5%, TA = -40°C to +85°C)

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
fIN [1]	Input Frequency	Input frequency limit (CLKIN, CLKINB)	1		350	MHz
fOUT	Output Frequency	Single ended clock output limit (LVCMOS)	1		200	MHz
		Differential cock output limit (LVPECL/ LVDS/HCSL)	1		350	
fVCO	VCO Frequency	VCO operating frequency range	2600		2900	MHz
fPFD	PFD Frequency	PFD operating frequency range	1 [1]		150	MHz
fBW	Loop Bandwidth	Input frequency = 25MHz	0.06		0.9	MHz
t2	Input Duty Cycle	Duty Cycle	45	50	55	%
t3 [5]	Output Duty Cycle	Measured at VDD/2, all outputs except Reference output OUT0, VDDOX= 2.5V or 3.3V	45	50	55	%
		Measured at VDD/2, all outputs except Reference output OUT0, VDDOX=1.8V	40	50	60	%
		Measured at VDD/2, Reference output OUT0 (5MHz - 120MHz) with 50% duty cycle input	40	50	60	%
		Measured at VDD/2, Reference output OUT0 (150.1MHz - 200MHz) with 50% duty cycle input	30	50	70	%
t4 [2]	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDDOX=3.3V	1.0	2.2		V/ns
	Slew Rate, SLEW[1:0] = 01		1.2	2.3		
	Slew Rate, SLEW[1:0] = 10		1.3	2.4		
	Slew Rate, SLEW[1:0] = 11		1.7	2.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 2.5V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDDOX=2.5V	0.6	1.3		
	Slew Rate, SLEW[1:0] = 01		0.7	1.4		
	Slew Rate, SLEW[1:0] = 10		0.6	1.4		
	Slew Rate, SLEW[1:0] = 11		1.0	1.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 1.8V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDDOX=1.8V	0.3	0.7		
	Slew Rate, SLEW[1:0] = 01		0.4	0.8		
	Slew Rate, SLEW[1:0] = 10		0.4	0.9		
	Slew Rate, SLEW[1:0] = 11		0.7	1.2		
t5	Rise Times	LVDS, 20% to 80%		300		ps
	Fall Times	LVDS, 80% to 20%		300		
	Rise Times	LVPECL, 20% to 80%		400		
	Fall Times	LVPECL, 80% to 20%		400		

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t6	Clock Jitter	Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, differential outputs (1.8V to 3.3V nominal output voltage) OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		46		ps
		Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, LVCMOS outputs (1.8 to 3.3V nominal output voltage) OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		74		ps
		RMS Phase Jitter (12kHz to 5MHz integration range) reference clock (OUT0), 25 MHz LVCMOS outputs (1.8 to 3.3V nominal output voltage). OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		0.5		ps
		RMS Phase Jitter (12kHz to 20MHz integration range) differential output, VDDO = 3.465V, 25MHz input, 156.25MHz output frequency OUT0=25MHz OUT1=100MHz OUT2=125MHz OUT3=156.25MHz		0.75	1.5	ps
t7	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0 ns.		75		ps
t8 [3]	Startup Time	PLL lock time from power-up, measured after all VDD's have raised above 90% of their target value.			10	ms
t9 [4]	Startup Time	PLL lock time from shutdown mode		3	4	ms

1. Practical lower frequency is determined by loop filter settings.
2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
3. Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.
4. Actual PLL lock time depends on the loop configuration.
5. Duty Cycle is only guaranteed at max slew rate settings.

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Table 20: PCI Express Jitter Specifications (V_{DDO} = 3.3V±5% or 2.5V±5%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	PCIe Industry Specification	Units	Notes
t_J (PCIe Gen1)	Phase Jitter Peak-to-Peak	f = 100MHz, 25MHz Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		30		86	ps	1,4
$t_{REFCLK_HF_RMS}$ (PCIe Gen2)	Phase Jitter RMS	f = 100MHz, 25MHz Input High Band: 1.5MHz - Nyquist (clock frequency/2)		2.56		3.10	ps	2,4
$t_{REFCLK_LF_RMS}$ (PCIe Gen2)	Phase Jitter RMS	f = 100MHz, 25MHz Input Low Band: 10kHz - 1.5MHz		0.27		3.0	ps	2,4
t_{REFCLK_RMS} (PCIe Gen3)	Phase Jitter RMS	f = 100MHz, 25MHz Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.8		1.0	ps	3,4

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

1. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1.
2. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band).
3. RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI_Express_Base_r3.0 10 Nov, 2010 specification, and is subject to change pending the final release version of the specification.
4. This parameter is guaranteed by characterization. Not tested in production.

Table 21: Jitter Specifications [1,2,3]

(VDDx = 3.3V+5% or 2.5V+5%, TA = -40°C to +85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OC-12 Random Jitter (12 kHz–5 MHz)	J_{OC12}	CLKIN = 19.44 MHz, All CLKn at 155.52 MHz[5]	-	0.69	0.95	ps
PCI Express 1.1 Common Clocked		Total Jitter[6]	-	9.1	12	ps
PCI Express 2.1 Common Clocked		RMS Jitter[6], 10 kHz to 1.5MHz	-	0.1	0.3	ps
		RMS Jitter[6], 1.5MHz to 50MHz	-	0.9	1.1	ps
PCI Express 3.0 Common Clocked		RMS Jitter[6]	-	0.2	0.4	ps

Notes:

[1] All measurements with Spread Spectrum Off.

[2] For best jitter performance, keep the single ended clock input slew rates at more than 1.0 V/ns and the differential clock input slew rates more than 0.3 V/ns.

[3] All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 3 ps rms, contact IDT for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.

[4] DJ for PCI and GbE is < 5 ps pp.

[5] Output FOD in Integer mode.

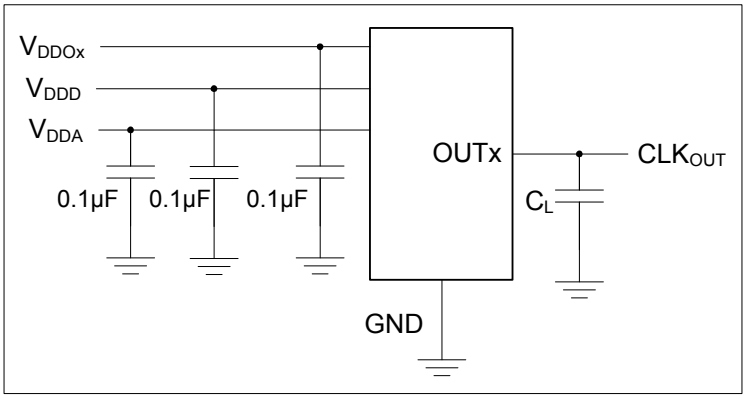
[6] All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. Jitter is measured with the Intel Clock Jitter Tool, Ver. 1.6.6.

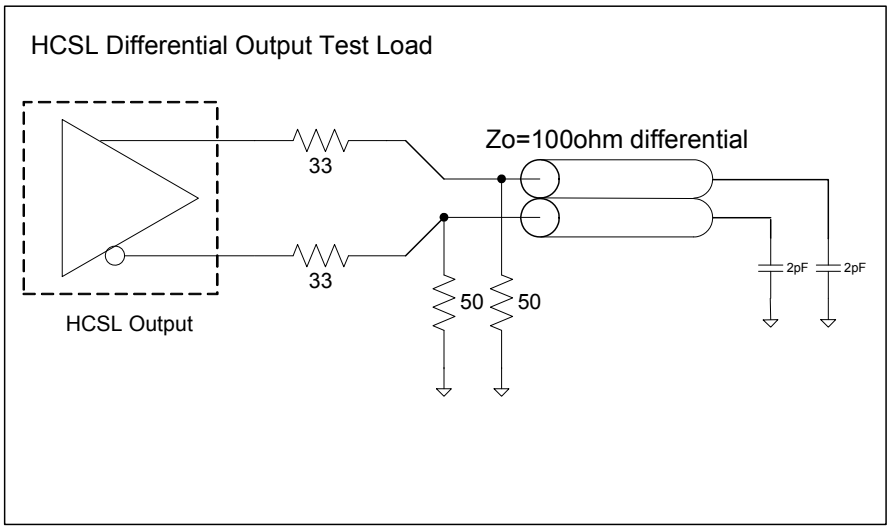
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Table 22: Spread Spectrum Generation Specifications

Symbol	Parameter	Description	Min	Typ	Max	Unit
f_{OUT}	Output Frequency	Output Frequency Range	5		300	MHz
f_{MOD}	Mod Frequency	Modulation Frequency	30 to 63			kHz
f_{SPREAD}	Spread Value	Amount of Spread Value (programmable) - Center Spread	±0.25% to ±2.5%			$\%f_{OUT}$
		Amount of Spread Value (programmable) - Down Spread	-0.5% to -5%			

Test Circuits and Loads

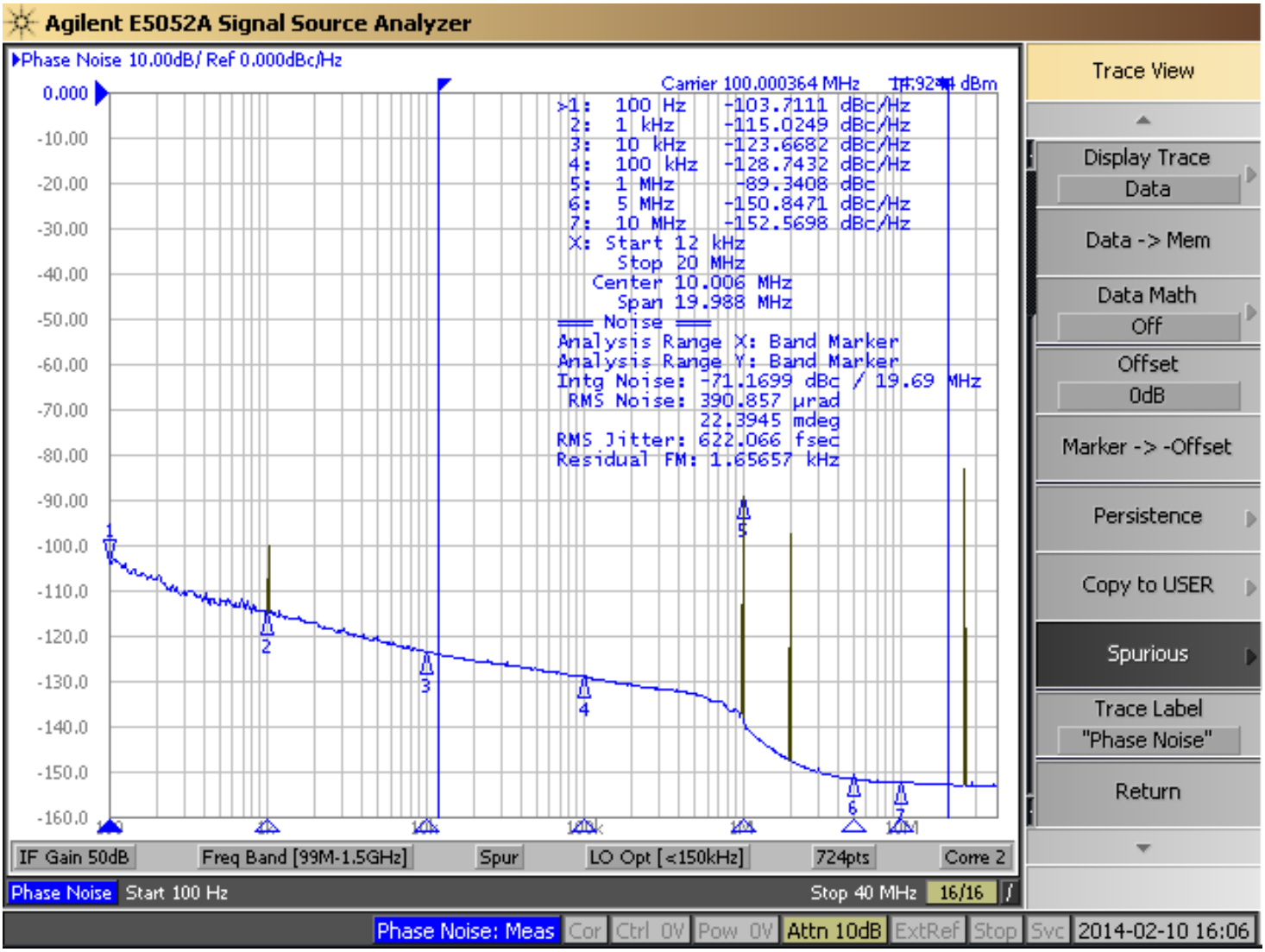




Test Circuits and Loads for Outputs

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Typical Phase Noise at 100MHz (3.3V, 25°C)



NOTE: All outputs operational at 100MHz, Phase Noise Plot with Spurs On.

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5P49V5943 Application Schematic

The following figure shows an example of 5P49V5943 application schematic. Input and output terminations shown are intended as examples only and may not represent the exact user configuration. In this example, the device is operated at V_{DDD}, V_{DDA} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. 5P49V5943 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

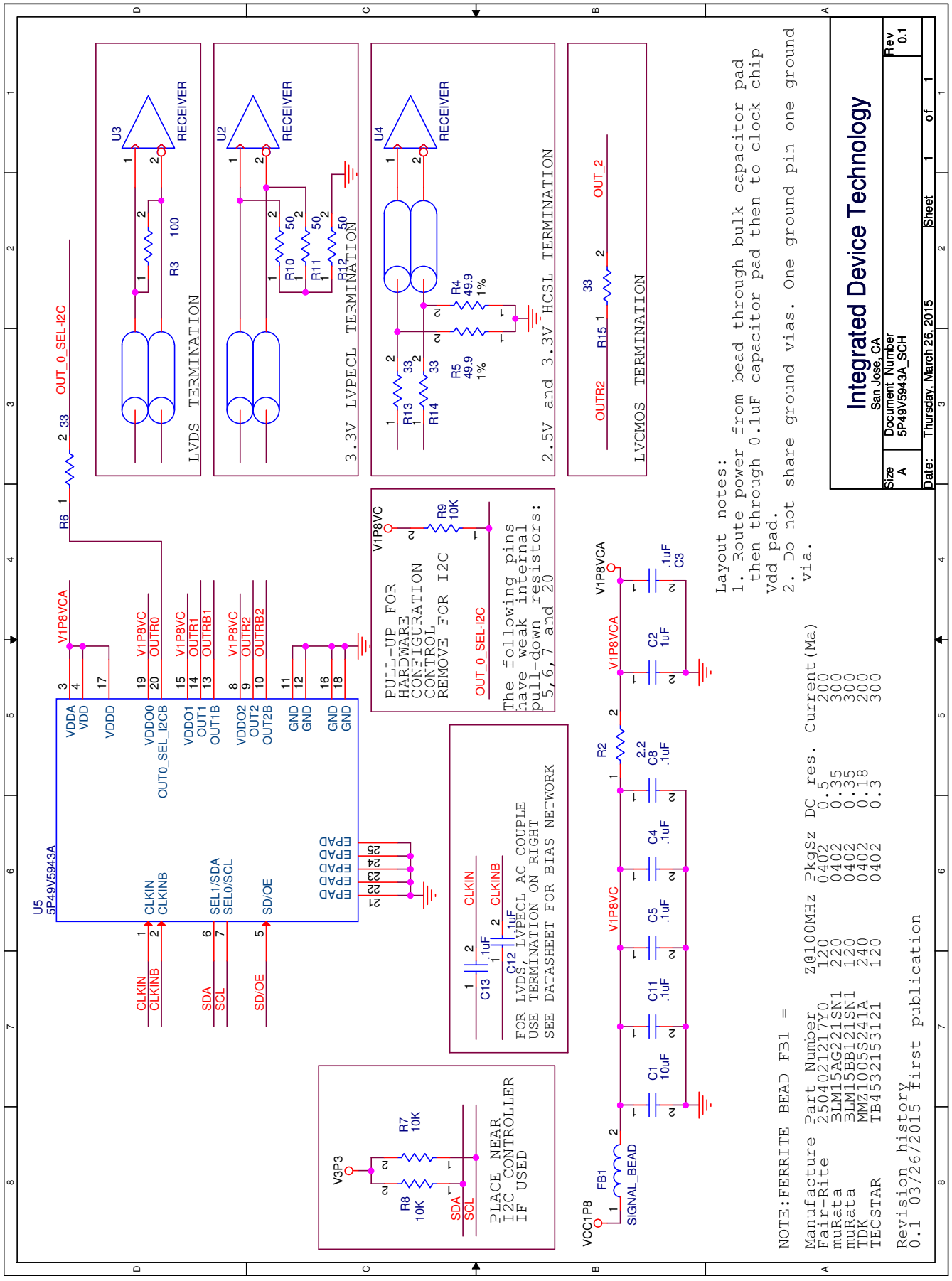
In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

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5P49V5943 Reference Schematic

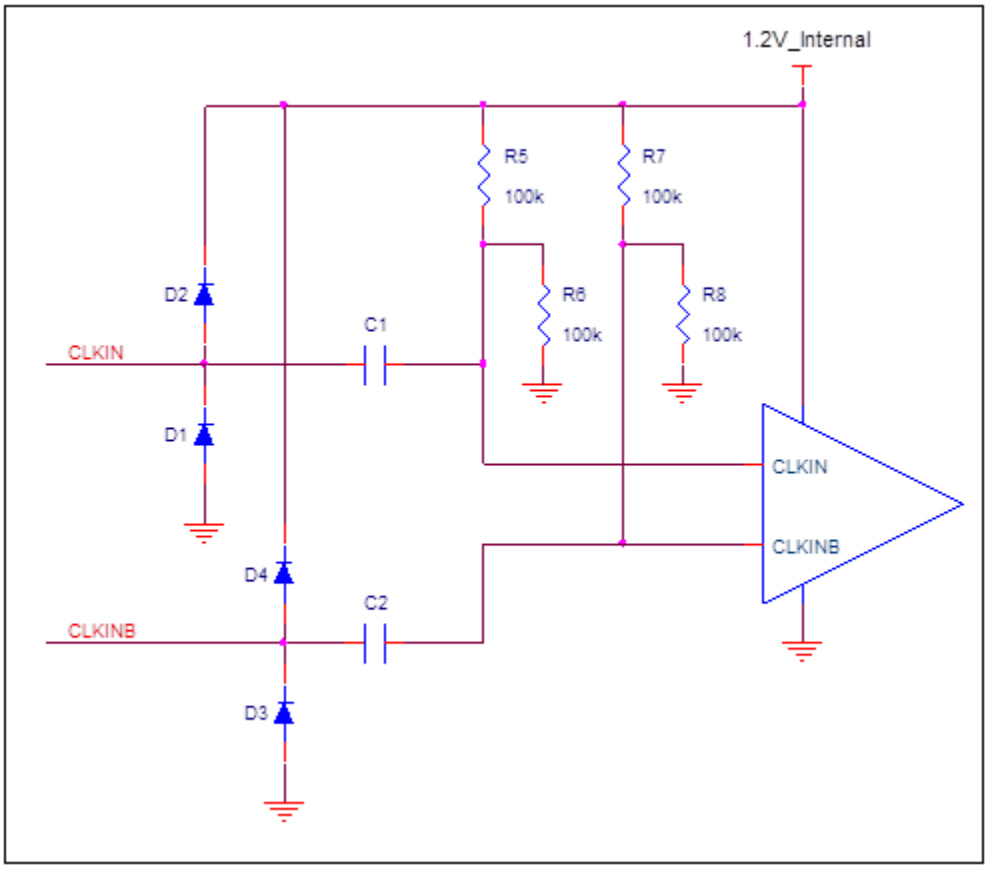


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CLKIN Equivalent Schematic

Figure *CLKIN Equivalent Schematic* below shows the basis of the requirements on VIH max, VIL min and the 1200 mV p-p single ended Vswing maximum.

- The CLKIN and CLKINB Vih max spec comes from the cathode voltage on the input ESD diodes D2 and D4, which are referenced to the internal 1.2V supply. CLKIN or CLKINB voltages greater than 1.2V + 0.5V =1.7V will be clamped by these diodes. CLKIN and CLKINB input voltages less than -0.3V will be clamped by diodes D1 and D3.
- The 1.2V p-p maximum Vswing input requirement is determined by the internally regulated 1.2V supply for the actual clock receiver. This is the basis of the Vswing spec in Table 13.

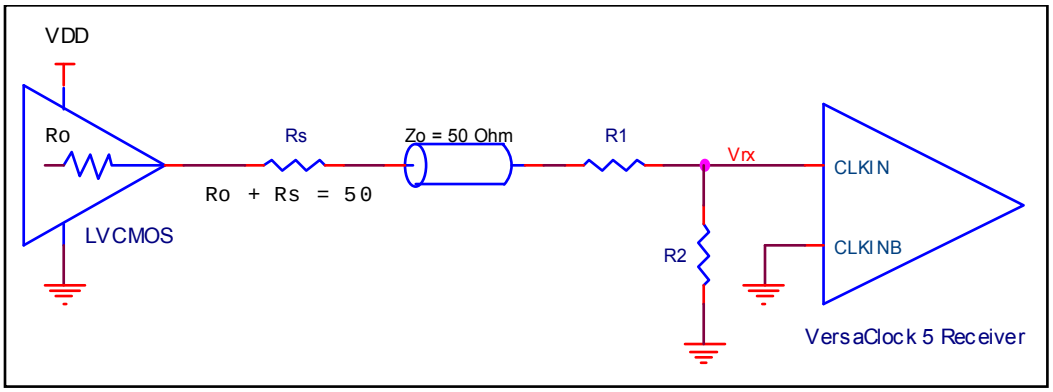


CLKIN Equivalent Schematic

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Wiring the Differential Input to Accept Single-Ended Levels

Figure *Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels* shows how a differential input can be wired to accept single ended levels. This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that Vrx p-p at CLKIN is less than the maximum value of 1.2V.



Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Table 23 *Nominal Voltage Divider Values vs Driver VDD* shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver VDD, the VersaClock Vddo_0 and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the impedance of the R1-R2 divider. To assist this assessment, the total load on the driver is included in the table.

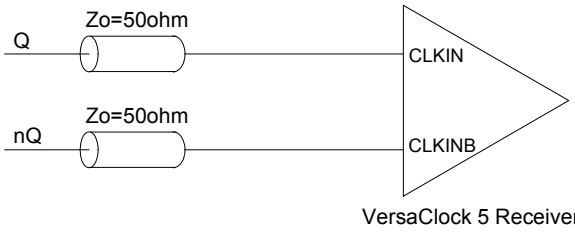
Table 23: Nominal Voltage Divider Values vs Driver VDD

LVCMOS Driver VDD	Ro+Rs	R1	R2	Vrx (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

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HCSL Differential Clock Input Interface

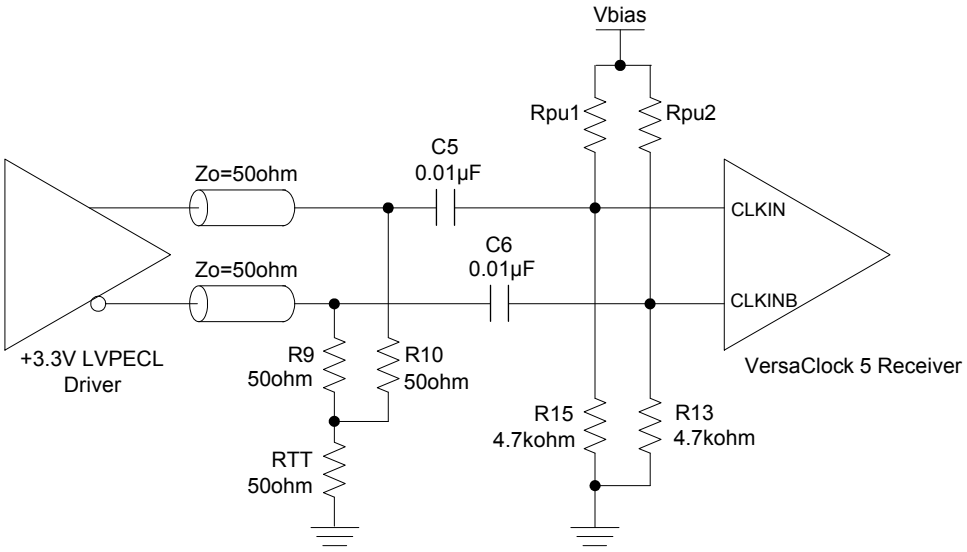
CLKIN/CLKINB will accept DC coupled HCSL signals.



CLKIN, CLKINB Input Driven by an HCSL Driver

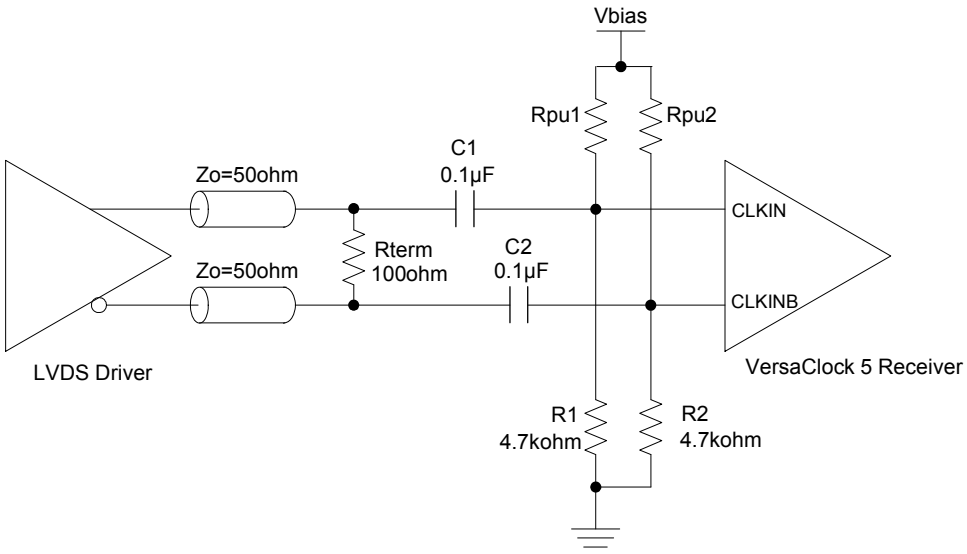
3.3V Differential LVPECL Clock Input Interface

The logic levels of 3.3V LVPECL and LVDS can exceed VIH max for the CLKIN/B pins. Therefore the LVPECL levels must be AC coupled to the VersaClock differential input and the DC bias restored with external voltage dividers. A single table of bias resistor values is provided below for both for 3.3V LVPECL and LVDS. Vbias can be VDDD, V_{DDOX} or any other available voltage at the VersaClock receiver that is most conveniently accessible in layout.



CLKIN, CLKINB Input Driven by a 3.3V LVPECL Driver

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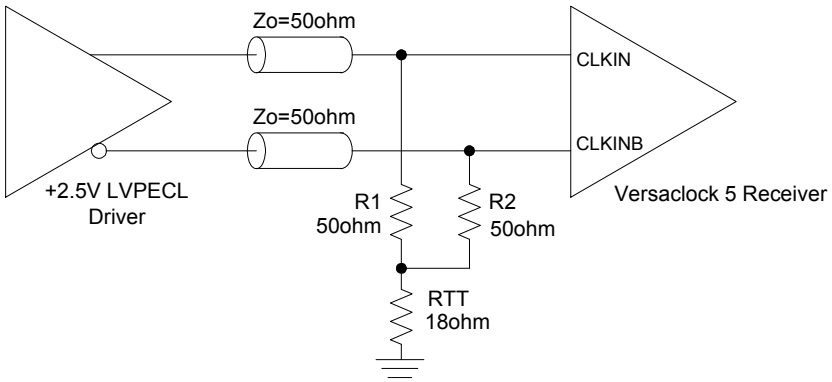
CLKIN, CLKINB Input Driven by an LVDS Driver

Table 24: Bias Resistors for 3.3V LVPECL and LVDS Drive to CLKIN/B

Vbias (V)	Rpu1/2 (kohm)	CLKIN/B Bias Voltage (V)
3.3	22	0.58
2.5	15	0.60
1.8	10	0.58

2.5V Differential LVPECL Clock Input Interface

The maximum DC 2.5V LVPECL voltage meets the VIH max CLKIN requirement. Therefore 2.5V LVPECL can be connected directly to the CLKIN terminals without AC coupling

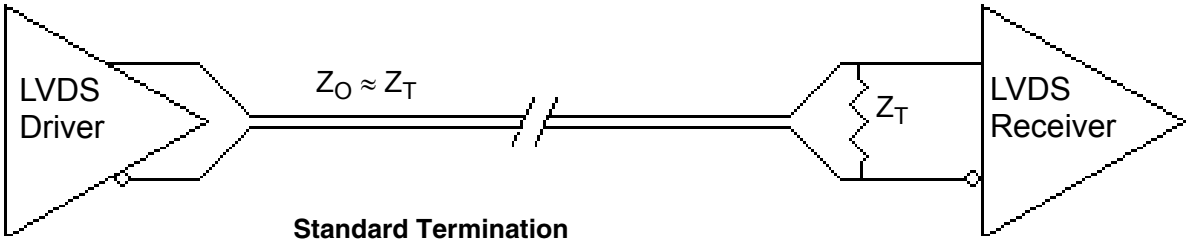


CLKIN, CLKINB Input Driven by a 2.5V LVPECL Driver

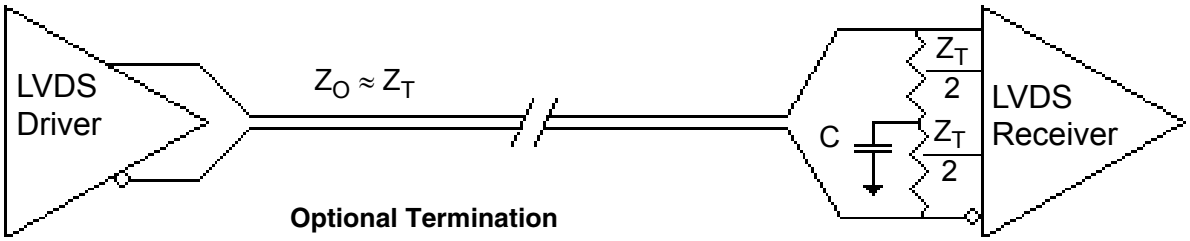
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LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω. and 132Ω. The actual value should be selected to match the differential impedance (Zo) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω. differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure *Standard Termination* or the termination of figure *Optional Termination* can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the IDT LVDS output. If using a non-standard termination, it is recommended to contact IDT and confirm that the termination will function as intended. For example, the LVDS outputs cannot be AC coupled by placing capacitors between the LVDS outputs and the 100 ohm shunt load. If AC coupling is required, the coupling caps must be placed between the 100 ohm shunt termination and the receiver. In this manner the termination of the LVDS output remains DC coupled.



Standard Termination



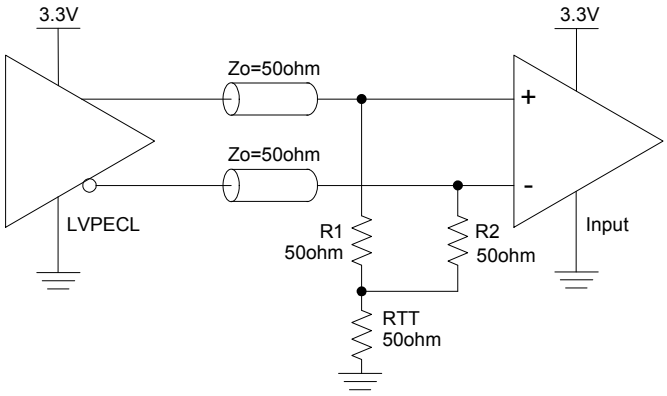
Optional Termination

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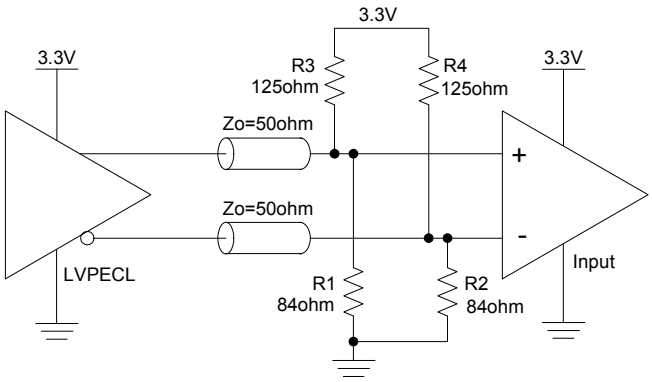
Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. The figure below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



3.3V LVPECL Output Termination (1)

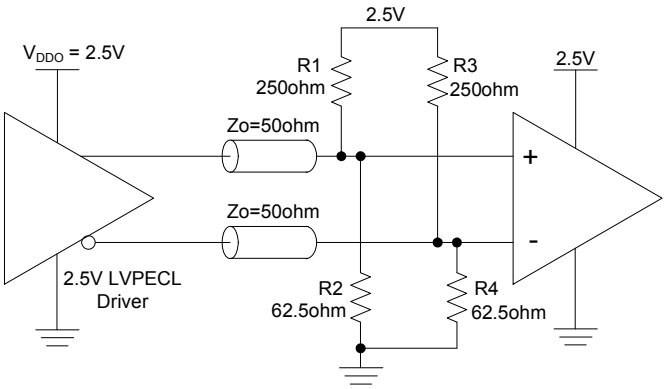


3.3V LVPECL Output Termination (2)

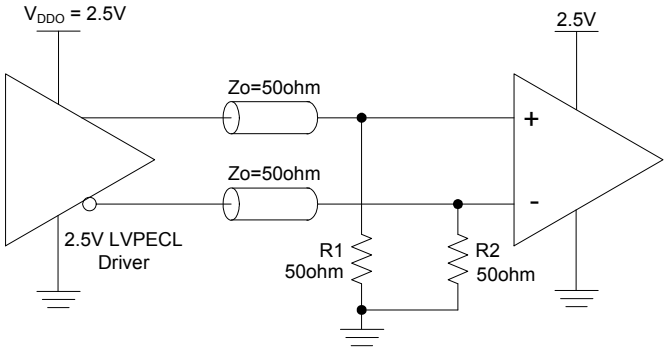
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Termination for 2.5V LVPECL Outputs

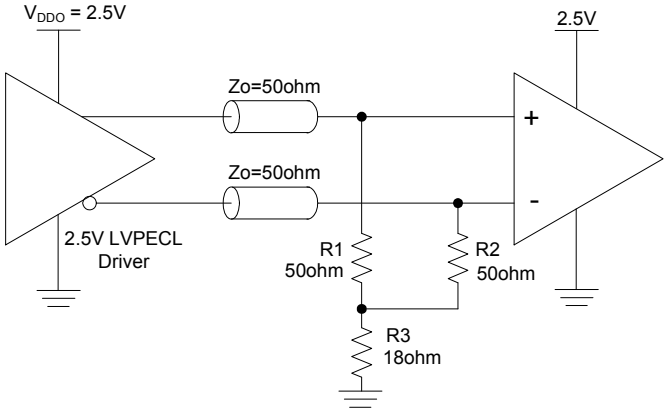
Figures *2.5V LVPECL Driver Termination Example (1) and (2)* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DDO} – 2V. For V_{DDO} = 2.5V, the V_{DDO} – 2V is very close to ground level. The R3 in Figure *2.5V LVPECL Driver Termination Example (3)* can be eliminated and the termination is shown in example (2).



2.5V LVPECL Driver Termination Example (1)



2.5V LVPECL Driver Termination Example (2)



2.5V LVPECL Driver Termination Example (3)

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PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used Common Clock Architecture in which a copy of the reference clock is provided to both ends of the PCI Express Link.

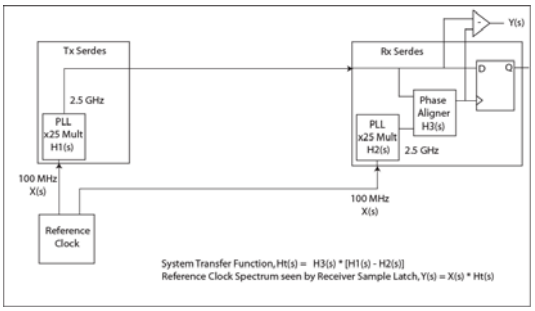
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

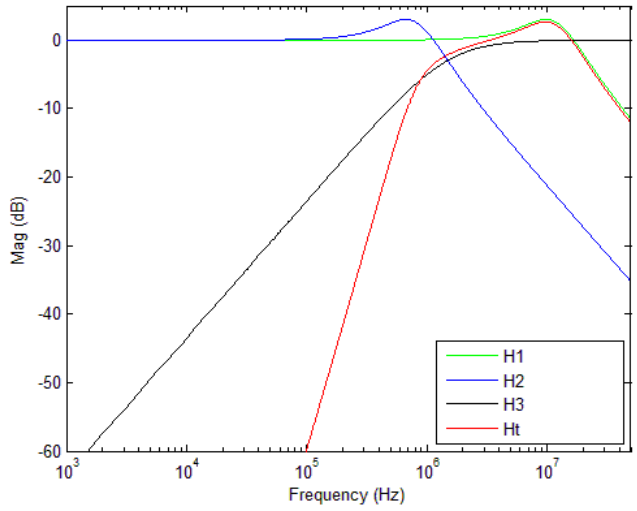
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



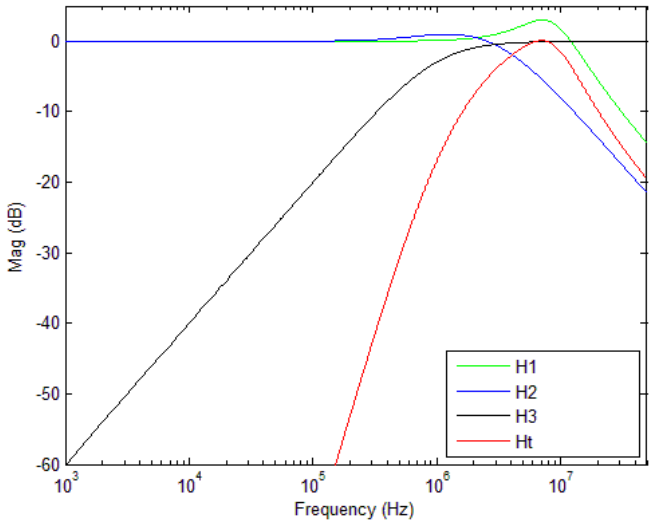
PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

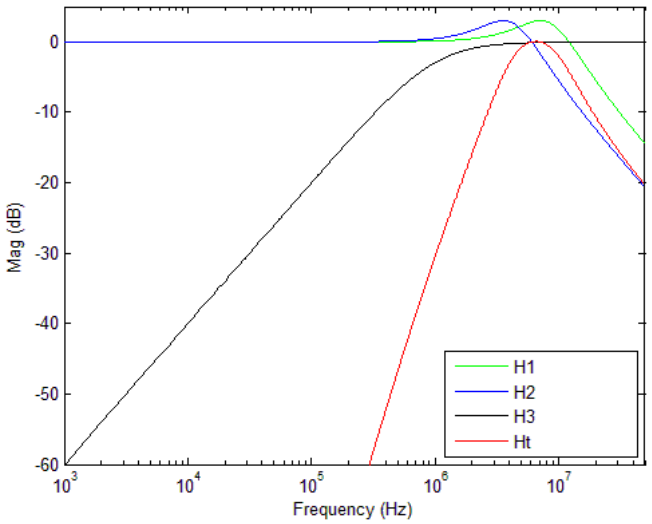


PCIe Gen1 Magnitude of Transfer Function

For PCI Express Gen2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



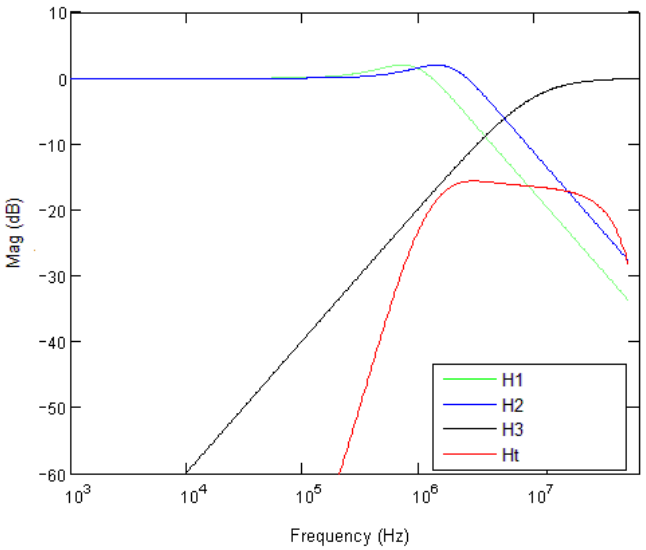
PCIe Gen2A Magnitude of Transfer Function



PCIe Gen2B Magnitude of Transfer Function

For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.

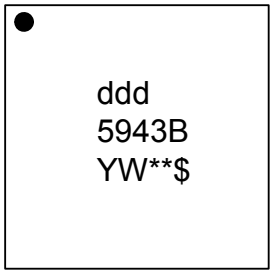
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PCIe Gen3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note PCI Express Reference Clock Requirements.

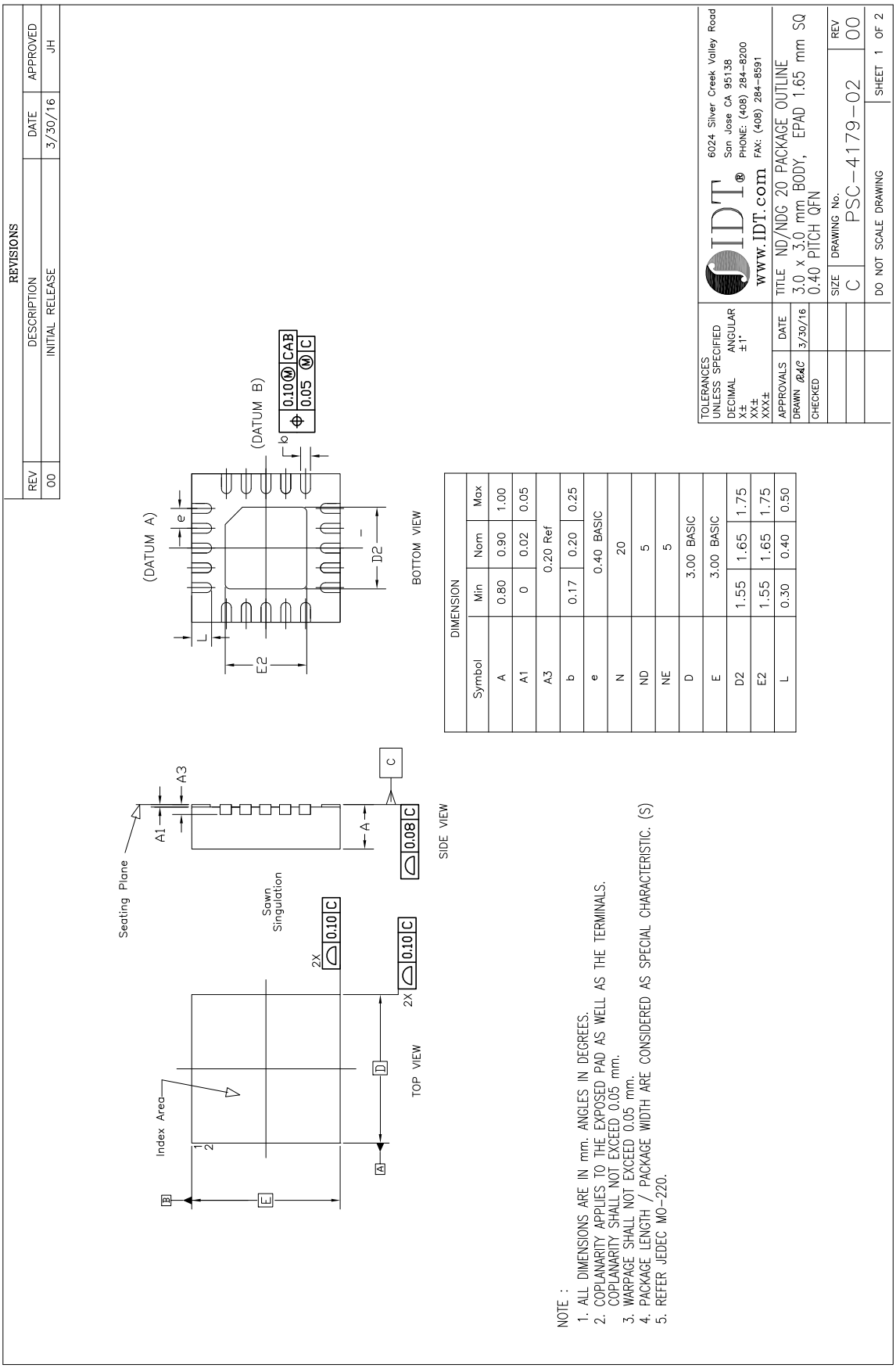
Marking Diagram



1. “ddd” denotes dash code.
2. Line 2: truncated part number
3. “YW” is the last digit of the year and week that the part was assembled.
4. “**” denotes sequential lot number.
5. “$” denotes mark code.

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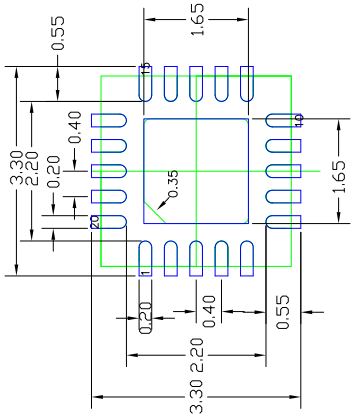
Package Outline and Dimensions (20-pin 3 x 3 mm VFQFPN)



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Package Outline and Dimensions (20-pin 3 x 3 mm VFQFPN), cont.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	3/30/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
X±	±1°
XX±	
XXX±	

APPROVALS	DATE
DRAWN	3/30/16
CHECKED	

IDT® 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com

TITLE ND/NDG 20 PACKAGE OUTLINE 3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ 0.40 PITCH QFN

SIZE	DRAWING No.	REV
C	PSC-4179-02	00

DO NOT SCALE DRAWING | SHEET 2 OF 2

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Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P49V5943BdddNDGI	see page 29	Trays	20-pin VFQFPN	-40° to +85°C
5P49V5943BdddNDGI8		Tape and Reel	20-pin VFQFPN	-40° to +85°C

Note: “ddd” denotes the dash code.
“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Date	Description of Change
March 3, 2017	Updated PODs and legal disclaimer
February 24, 2017	1. Added “Output Alignment” section. 2. Update “Output Divides” section.

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(Rev.1.0 Mar 2020)

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