SUPERLITE™ SY55851A

2.5V/3.3V, 3.0GHz CML AnyGate® Any Logic with 50Ω Outputs

Features

- Guaranteed AC Parameters Over Temperature:
  - fMAX > 3.0GHz
  - t_r / t_f < 100ps
  - Propagation delay < 280ps
- Guaranteed Operation Over -40° to +85°C Temperature Range
- Wide Supply Voltage Range: 2.3V to 3.6V
- Single IC Provides 8 Logic Functions
- 2:1 MUX Capability
- Fully Differential I/O
- Source Terminated CML Outputs for Fast edge Rates (50Ω Load)
- Guaranteed Matched Propagation Delays:
  - Select (S)-to-out: < 280ps
  - Input (A and B)-to-out: < 280ps
- Accepts LVPECL and CML Input Signals
- Functions as LVPECL-to-CML Translator
- Available in a 10-pin (3mm x 3mm) MSOP Package

Applications

- Port bypass
- Data communication systems
- Wireless communication systems
- Telecom systems

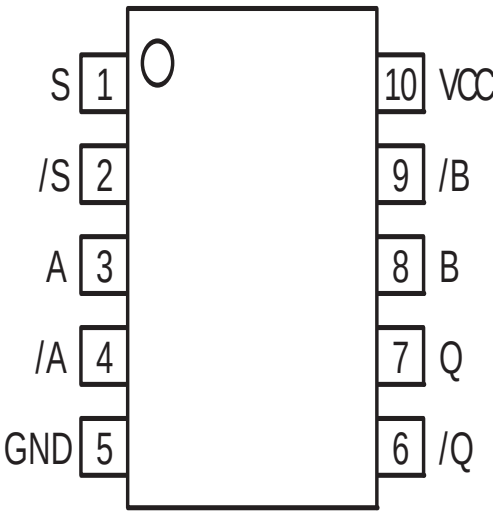
General Description

The SY55851A is a highly flexible, universal logic gate capable of up to 3.0GHz operation. This AnyGate differential logic device will produce all possible logic functions of two Boolean variables. It can be configured as any of the following gates: AND, NAND, OR, NOR, XOR, XNOR, DELAY, NEGATION (NOT). The SY55851A can also function as a 2-input multiplexer.

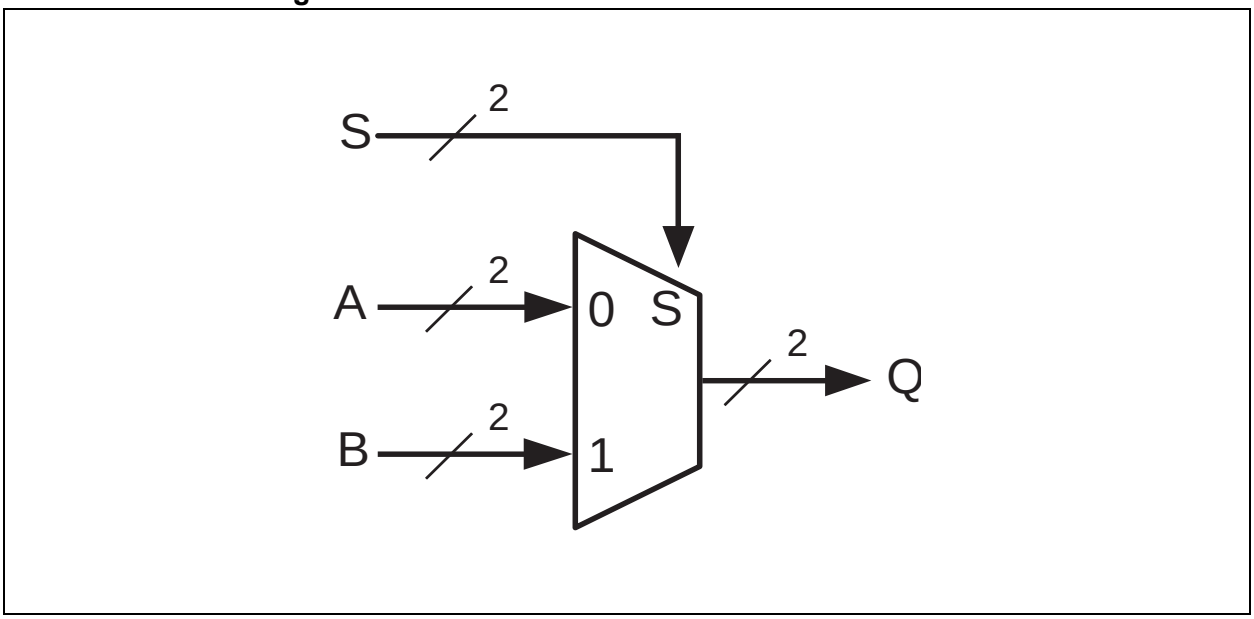
The SY55851A has an output stage optimized for 50Ω loads.

Package Type

SY55851A
10-Pin
MSOP
(K10-1)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage, V_{CC} ..... –0.5V to +6.0V
Input Voltage, V_{IN} ..... –0.5V to V_{CC} +0.5V
CML Output Voltage, V_{OUT} ..... V_{CC} -1.0 to V_{CC}+0.5V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

Electrical Characteristics: V_{CC}= 2.3V to 3.6V; GND = 0V; T_A = –40°C to +85°C unless otherwise stated (Note 1)						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply Voltage	V_{CC}	2.3	—	3.6	V	
Power Supply Current	I_{CC}	—	46	60	mA	No Load
Output High Voltage	V_{OH}	V_{CC}-0.040	V_{CC}-0.010	V_{CC}	V	No Load
Output Low Voltage	V_{OL}	V_{CC}-1.000	V_{CC}-0.800	V_{CC}-0.650	V	No Load
Output Voltage Swing (Note 2)	V_{OUT}	—	0.400	—	V	
Output Source Impedance	R_{OUT}	40	50	60	Ω	
Input High Voltage	V_{IH}	1.6	—	V_{CC}	V	
Input Low Voltage	V_{IL}	1.5	—	V_{CC}-0.1	V	
Differential Input Voltage	V_{ID}	100	—	—	mV	

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

2: Outputs are terminated through a 100Ω resistor across Q and /Q. See Figure 6-1.

TABLE 1-2: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.3V to 3.6V; GND = 0V; TA = -40°C to 85°C, unless otherwise stated (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
Maximum Operating Frequency	f_{MAX}	3.0	—	—	GHz	
Propagation Delay (A,B,S to Q)	t_{PD}	130	—	280	ps	
Output Rise/Fall Time Q (20% to 80%)	t_r, t_f	—	65	100	ps	

Note 1: Specification for packaged product only.

2: Outputs are terminated through a 100Ω resistor across Q and /Q. See Figure 6-1.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	+85	°C	
Storage Temperature Range	T_S	–65	—	+150	°C	
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20s
Thermal Resistances						
Junction-to-Ambient	θ_{JA}	—	113	—	°C/W	Still Air
		—	96	—	°C/W	500lfpm
Junction-to-Case	θ_{JC}	—	42	—	°C/W	

2.0 FUNCTIONAL DESCRIPTION

2.1 Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased to $V_{CC}/2$ through an internal voltage divider consisting of two 75kΩ resistors. Since some logic functions necessitate an output to be connected to two inputs, SY55851A inputs have no internal terminations. For typical terminations see Section 5.0, Input Interface Applications.

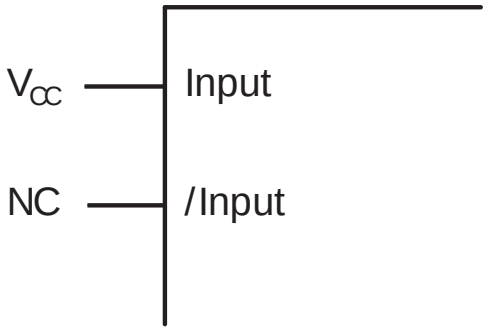
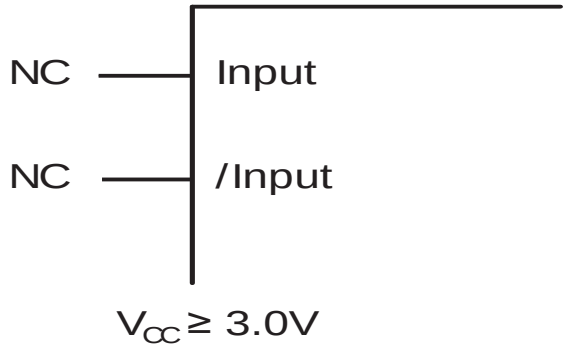


FIGURE 2-1: *Hard Wiring a Logic "1" (1)*

Note 1: Input is either A, B, S input, and /Input is either /A, /B, /S input.

To keep an input at static logic zero at $V_{CC} \geq 3.0V$, leave both inputs unconnected or tie the complement input to V_{CC}. For $V_{CC} < 3.0V$ applications, connect the complement input to V_{CC} and leave the true input unconnected. These are the only safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (No Connect) pins should be unconnected.



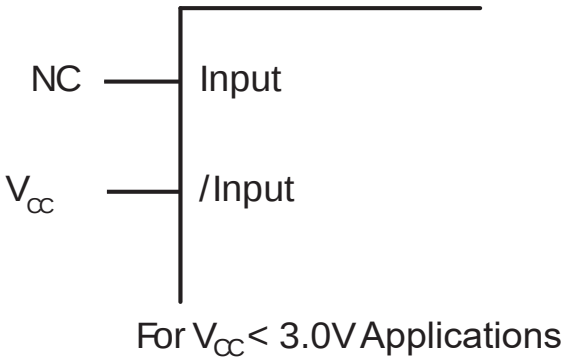
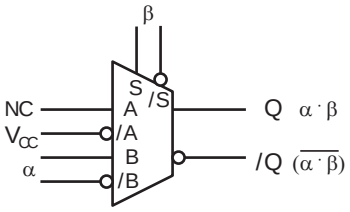


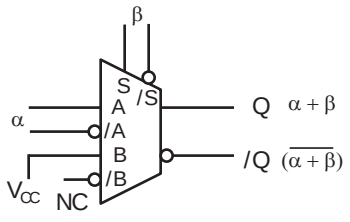
FIGURE 2-2: *Hard Wiring a Logic "0" (1)*

3.0 TRUTH TABLES



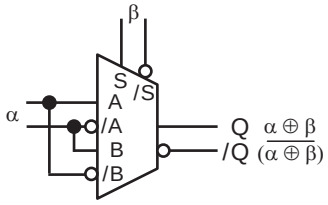
AND/NAND

A	B	S	Q	/Q
	α	β	α·β	$(\overline{\alpha \cdot \beta})$
L	L	L	L	H
L	H	L	L	H
L	L	H	L	H
L	H	H	H	L



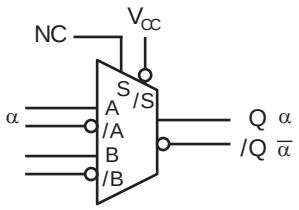
OR/NOR

A	B	S	Q	/Q
α		β	α + β	$\overline{\alpha + \beta}$
L	H	L	L	H
H	H	L	H	L
L	H	H	H	L
H	H	H	H	L



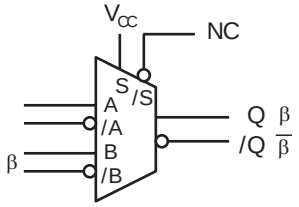
XOR/XNOR

A	B	S	Q	/Q
α		β	α ⊕ β	$\overline{\alpha \oplus \beta}$
L	H	L	L	H
L	H	H	H	L
H	L	L	H	L
H	L	H	L	H

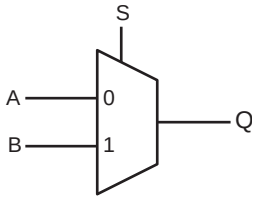


DELAY/NEGATION

A	B	S	Q	/Q
α			α	$\overline{\alpha}$
L	X	L	L	H
H	X	L	H	L



A	B	S	Q	/Q
	β		β	$\overline{\beta}$
X	L	H	L	H
X	H	H	H	L



2:1 MUX

S	Q	/Q
H	B	/B
L	A	/A

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1, 2	S, /S	CML, LVPECL, LVTTL Input Selector: This is one of the differential inputs to the logic block. It represents either one Boolean input for a 2-variable logic function, or the select input for a 2-input MUX. See Section 5.0, Input Interface Applications.
3, 4	A, /A	CML, LVPECL Input: This is one of the differential inputs to the logic block. For a 2-variable logic function, it is either a constant value or a Boolean input. For a 2-input MUX, this signal represents the output when S is set to logic zero. See Section 5.0, Input Interface Applications.
5	GND	Negative Supply Voltage
6, 7	/Q, Q	Differential CML Output: This is the differential CML output for the logic block. See Section 6.0, CML Output Termination.
8, 9	B, /B	CML, LVPECL Input: This is one of the differential inputs to the logic block. For a 2-variable logic function, it is either a constant value or a Boolean input. For a 2-input MUX, this signal represents the output when S is set to logic one. See Section 5.0, Input Interface Applications.
10	VCC	Positive Supply Voltage

5.0 INPUT INTERFACE APPLICATIONS

All inputs to the SY55851A must be externally terminated. All inputs accept the output from any other member of this family.

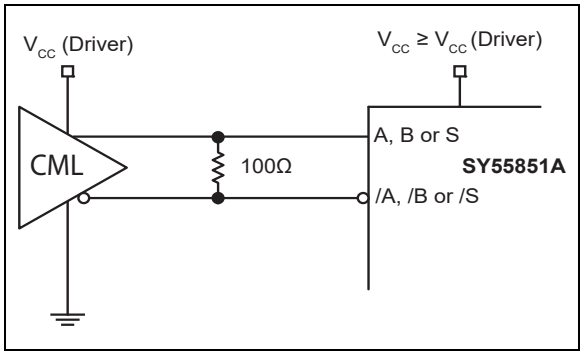


FIGURE 5-1: *CML-DC Coupled.*

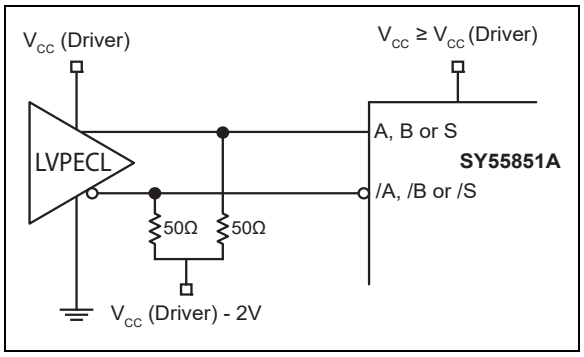


FIGURE 5-2: *LVPECL-DC Coupled* (1)

Note 1: V_{CC} (Driver) and $V_{CC} \geq 3V$

6.0 CML OUTPUT TERMINATION

All outputs are source terminated 50Ω CML differential drivers as shown in Figure 6-1 below.

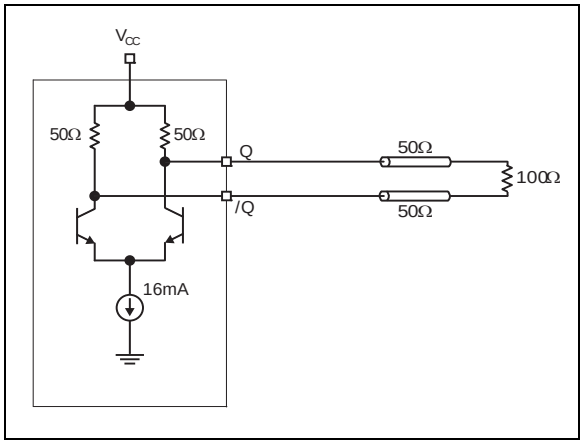


FIGURE 6-1: *Differentially Terminated (50Ω Load CML Output).*

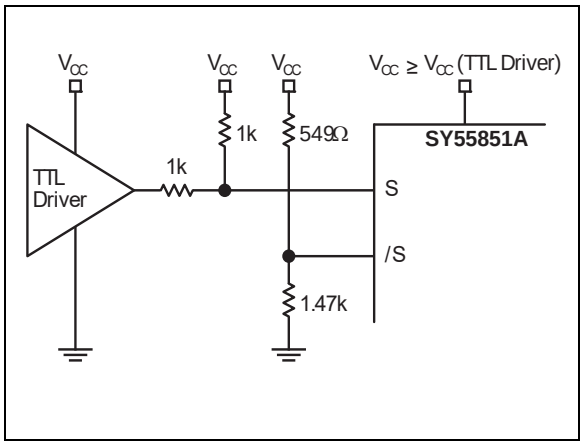
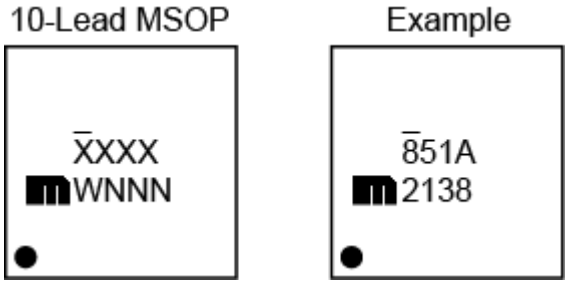


FIGURE 6-2: *Interfacing TTL-to-CML Select Inputs.*

7.0 PACKAGING INFORMATION

7.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

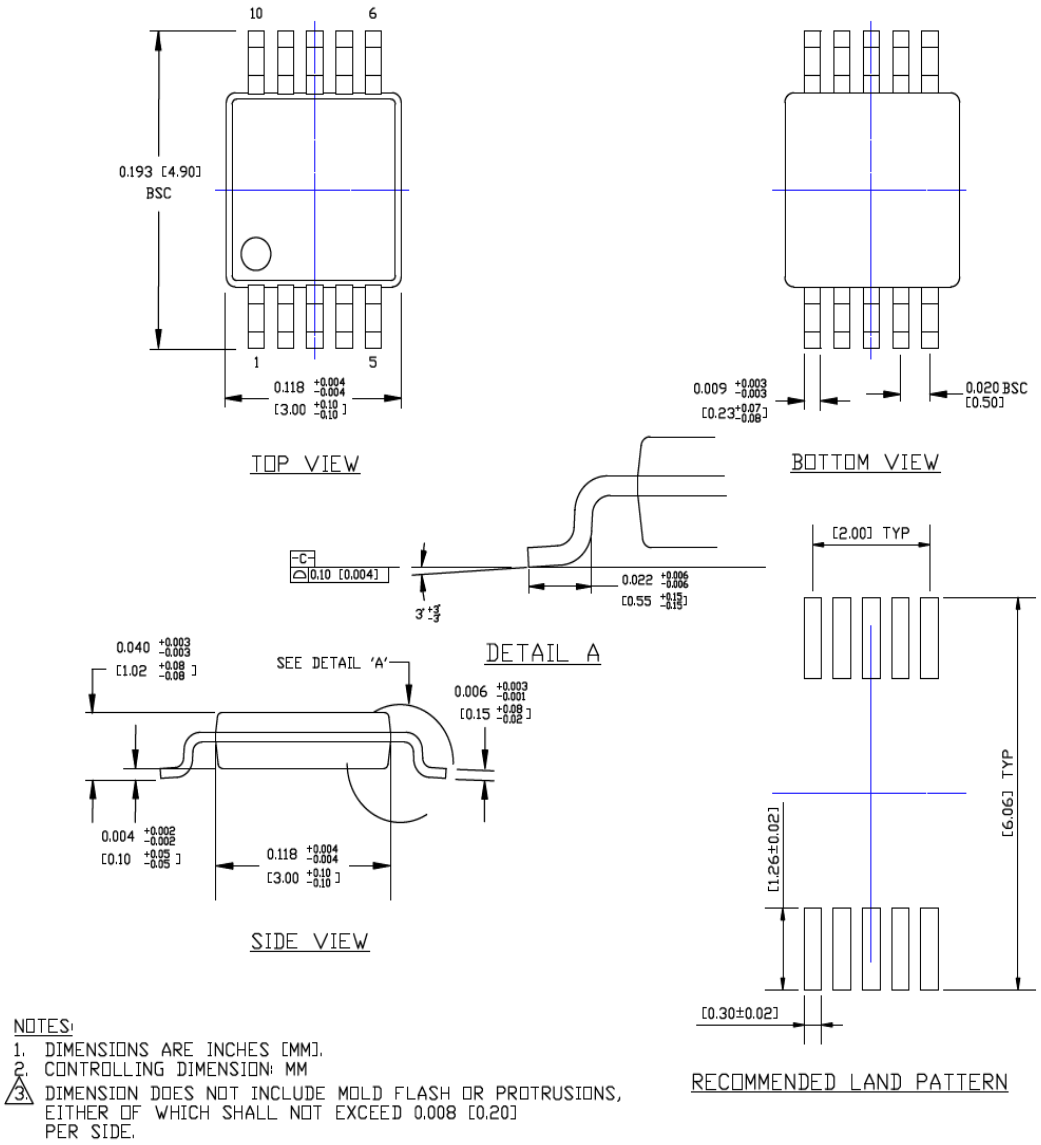
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

10-Lead MSOP Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

DRAWING #	MSOP-10LD-PL-1	UNIT	INCH [MM]



NOTES:
1. DIMENSIONS ARE INCHES [MM].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.20] PER SIDE.

APPENDIX A: REVISION HISTORY

Revision A (February 2019)

- Converted Micrel document M999-072909 to Microchip data sheet template DS20006135A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X	XX
Device	Feature	Supply Voltage Range	Package	Junction Temperature Range	Special Processing

Device:	SY55851:		2.5V/3.3V, 3.0 GHz CML AnyGate® Any Logic with 50Ω Outputs
Feature:	A	=	Optimized for 50Ω Loads
Supply Voltage Range:	U	=	2.5V/3.3V
Package:	K	=	10-Lead MSOP
Temperature Range:	G	=	–40°C to +85°C (NiPdAu Lead Free)
Special Processing:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) SY55851AUKG:
SY55851, Optimized for 50Ω Loads, 2.5V/3.3V Output Voltage, 10-Lead MSOP, –40°C to +85°C Junction Temperature Range, 100/Tube

b) SY55851AUKGTR:
SY55851, Optimized for 50Ω Loads, 2.5V/3.3V Output Voltage, 10-Lead MSOP, –40°C to +85°C Junction Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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ISBN: 978-1-5224-4128-1

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Norway - Trondheim
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Poland - Warsaw
Tel: 48-22-3325737

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