THCV233 and THCV234

V-by-One®HS High-speed video data transmitter and receiver

1. General Description

THCV233 and THCV234 are V-by-One® HS High-speed digital data transmitter/receiver.

It has one high-speed data lane and, effective maximum serial data rate is 3.36Gbps/lane.

2. Features

- LVDS Input internal termination
- CORE 1.8V, LVDS 3.3V
- Package: 48 pin QFN
- EU RoHS Compliant
- Data width selectable: 24/32 bit
- Single/Dual Link selectable
- AC coupling
- Wide frequency range
- CDR requires no external freq. reference
- Supports Spread Spectrum Clocking:
- Up to 30kHz/±0.5%(center spread)

Si/So:Single-in/Single-out, Si/Do:Single-in/Dual-out
Si/DDo:Single-in/Distributed Dual-out
Di/So:Dual-in/Single-out, Di/SSo:Dual-in/Selected Single-out

Table 1

Product	TMP	VDL	Width	Mode	LVDS Clock Freq.
THCV233	0ºC - 70 ºC	1.62V – 1.98V	24bit	Si/So	9MHz – 100MHz
				Si/DDo	20MHz – 100MHz
				Si/Do	40MHz – 100MHz
			32bit	Si/So	9MHz – 85MHz
				Si/DDo	20MHz – 85MHz
				Si/Do	40MHz – 85MHz
		1.71V – 1.89V	32bit	Si/So	9MHz – 105MHz
				Si/DDo	20MHz – 105MHz
				Si/Do	40MHz – 105MHz
	-40ºC - 105 ºC	1.62V – 1.98V	24bit	Si/So	9MHz – 100MHz
				Si/DDo	20MHz – 100MHz
				Si/Do	40MHz – 100MHz
			32bit	Si/So	9MHz – 75MHz
				Si/DDo	20MHz – 75MHz
				Si/Do	40MHz – 75MHz
		1.7V – 1.98V	24bit	Si/So	9MHz – 100MHz
				Si/DDo	20MHz – 100MHz
				Si/Do	40MHz – 100MHz
			32bit	Si/So	9MHz – 81MHz
				Si/DDo	20MHz – 81MHz
				Si/Do	40MHz – 81MHz
THCV234	0ºC - 70 ºC	1.62V – 1.98V	24bit	Si/So	9MHz – 100MHz
				Si/DDo	20MHz – 100MHz
				Si/Do	40MHz – 100MHz
			32bit	Si/So	9MHz – 85MHz
				Si/DDo	20MHz – 85MHz
				Si/Do	40MHz – 85MHz
		1.71V – 1.89V	32bit	Si/So	9MHz – 105MHz
				Si/DDo	20MHz – 105MHz
				Si/Do	40MHz – 105MHz
	-40ºC - 105 ºC	1.71V – 1.98V	24bit	Si/So	9MHz –95MHz
				Si/DDo	20MHz – 95MHz
				Si/Do	40MHz – 95MHz
			32bit	Si/So	9MHz – 71.25MHz
				Si/DDo	20MHz – 71.25MHz
				Si/Do	40MHz – 71.25MHz

3.Block Diagram

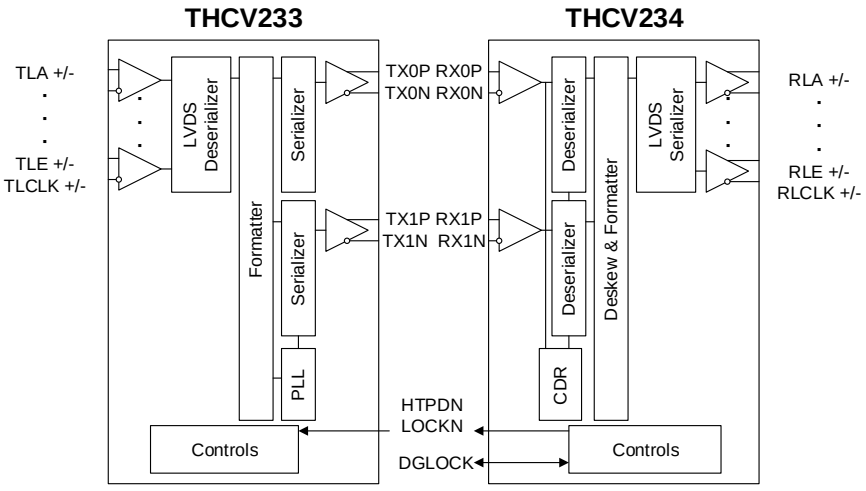

Figure 1

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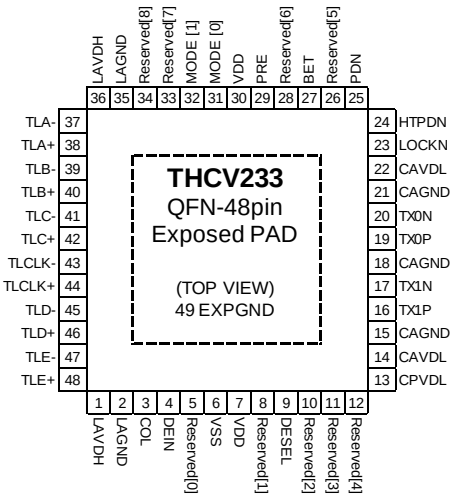
4. Pin Configuration

THCV233



THCV234

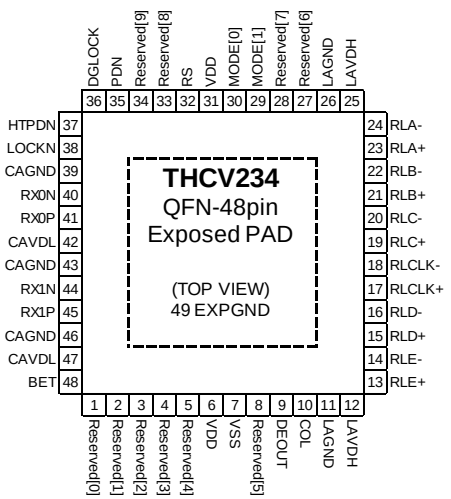


Figure 2

5. Pin Description

Table 2 THCV233 Pin Description

Pin Name	Pin #	Type*	Description
TLA -/+	37,38	LI	LVDS signal input.
TLB -/+	39,40	LI	
TLC -/+	41,42	LI	
TLCLK -/+	43,44	LI	
TLD -/+	45,46	LI	
TLE -/+	47,48	LI	
TX0N/P	20,19	CO	High-speed CML signal output.
TX1N/P	17,16	CO	
LOCKN	23	I	Lock detect input(LOCKN). It must be connected to Rx LOCKN with a Tx side 10kΩ pull-up resistor. LOCKN is input only.
HTPDN	24	I	Hot plug detect input (HTPDN). It must be connected to Rx HTPDN with a Tx side 10kΩ pull-up resistor. HTPDN is input only.
Reserved [3,2,0]	11,10,5	-	It must be open.
Reserved [1]	8	-	It must be connected with a pull-up resistor to 3.3V.
DEIN	4	I	DE input for LVDS data sets (DEIN). DEIN is external DE input pin. When input LVDS does not contain DE signal, DE can be provided as external input. Activation of DEIN function follow the following settings. DESEL=L : DE input from DEIN is used for processing. DESEL=H : DE input from LVDS is used for processing.
DESEL	9	I	DE input selector. H : DE input from LVDS is used for processing L : DE input from DEIN is used for processing
Reserved [4,5,6,7,8]	12,26,28 33,34	I	It must be connected to GND.
MODE [1:0]	32,31	I	Operation mode select input. MODE[1:0] =LL : Single-in/Distribution dual-out =LH : Single-in/Single-out =HL : Single-in/Dual-out =HH : Reserved (Forbidden)
PDN	25	I	Power down Schmitt input. H: Normal operation, L: Power down
PRE	29	I	Pre-Emphasis level select input for High Speed CML signal output. H : 100%, L : 0%
COL	3	I	Data width setting for High speed CML signal output. H : 24bit, L : 32bit
BET	27	I	Field-BET entry. H : Field BET Operation, L : Normal Operation
LAVDH	1,36	P33	LVDS power supply (3.3V)
LAGND	2,35	GND	LVDS GND
CAVDL	22,14	P18	High-speed signal analog power supply (1.8V)
CAGND	21,18,15	GND	High-speed signal analog GND
CPVDL	13	P18	High-speed signal PLL power supply (1.8V)
VDD	7,30	P18	Logic power supply (1.8V)
VSS	6	GND	Logic GND
EXPGND	49	GND	Exposed PAD GND

*Type symbol
I=3.3V CMOS input
LI=LVDS output, CO=CML output
P33=Power 3.3V, P18=Power 1.8V, GND=GND

Table 3 THCV234 Pin Description

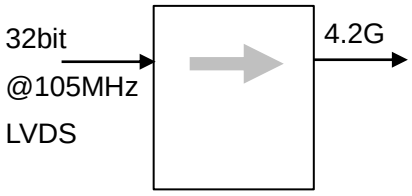
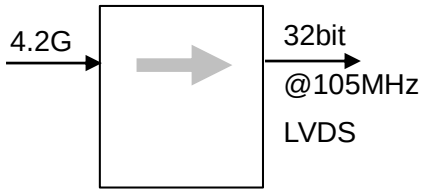
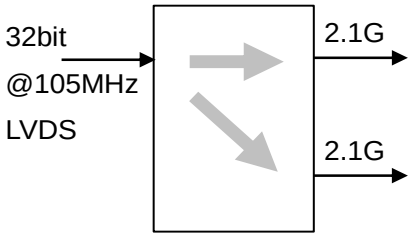
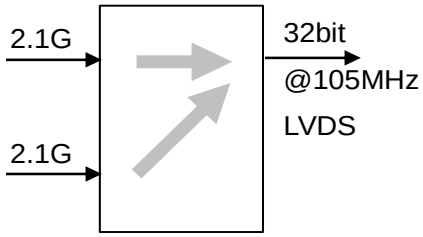
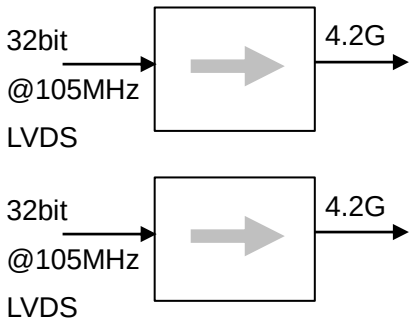
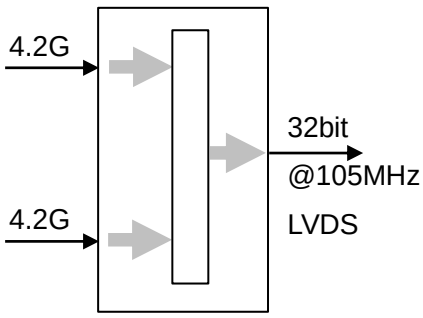
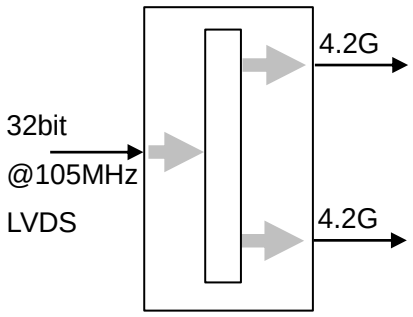
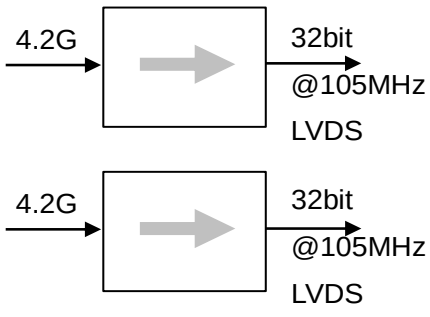
Pin Name	Pin #	Type*	Description
RLA -/+	24,23	LO	LVDS signal output.
RLB -/+	22,21	LO	
RLC -/+	20,19	LO	
RLCLK -/+	18,17	LO	
RLD -/+	16,15	LO	
RLE -/+	14,13	LO	
RX0N/P	40,41	CI	High-speed CML signal input.
RX1N/P	44,45	CI	
LOCKN	38	OD	Lock detect output (LOCKN). It must be connected to Tx LOCKN with a Tx side10kΩ pull-up resistor. LOCKN is output only.
HTPDN	37	OD	Hot plug detect output (HTPDN). It must be connected to Tx HTPDN with a Tx side 10kΩ pull-up resistor. HTPDN is output only.
Reserved [1,2]	2,3	-	It must be open.
Reserved [5]	8	-	It must be connected with a pull-up resistor to 3.3V.
DEOUT	9	O	DE signal output (DEOUT) for LVDS data sets. When used as DEOUT, no external component is required. It is push pull output. DEOUT output DE timing depending upon data stream state. DEOUT is output only. Bit Error Test (BET) result output under Field-BET operation H : No error, L : Bit error occurred
DGLOCK	36	BPU	Multiple-chip configuration total Rx side LOCKN indicator (DGLOCK). When used as DGLOCK, it is internally connected with a pull-up resistor to 3.3V. No external component is required. LOCKN arrange among Rx Multiple-chip configuration is achieved by connecting all DGLOCK pins.
Reserved [0,3,4,6,7,8,9]	1,4,5,27, 28,33,34	-	It must be connected to GND.
MODE [1:0]	29,30	I	Operation mode select input. MODE [1:0] =LL : Dual-in/Selected single-out (Lane0) =LH : Dual-in/Single-out =HL : Dual-in/Selected single-out (Lane1) =HH : Single-in/Single-out
PDN	35	I	Power down Schmitt input. H: Normal operation, L: Power down
RS	32	I	LVDS output swing range select input. H : Normal swing (350mv@typ.), L : Reduced swing (200mv@typ.) Latch select input under Field-BET operation H : Latched result, L : NOT Latched result
COL	10	I	Data width setting for High Speed CML signal output. H : 24bit, L : 32bit
BET	48	I	Field-BET entry. H : Field BET Operation, L : Normal Operation
LAVDH	12,25	P33	LVDS power supply (3.3V)
LAGND	11,26	GND	LVDS GND
CAVDL	42,47	P18	High-speed signal analog power supply (1.8V)
CAGND	39,43,46	GND	High-speed signal analog GND
VDD	6,31	P18	Logic power supply (1.8V)
VSS	7	GND	Logic GND
EXPGND	49	GND	Exposed PAD GND

*Type symbol
I=3.3V CMOS input, O=3.3V CMOS output, OD= OpenDrain output
BPU =CMOS Bi-directional buffer with an on-chip pullup resistor
LO=LVDS output, CI=CML input
P33=Power 3.3V, P18=Power 1.8V, GND=GND

6. Operation Mode

Table 4 Operation Mode

(0°C≤TMP≤70°C)

THCV233	THCV234
Single-In/Single-Out  MODE[1:0]=LH	Single-In/Single-Out  MODE[1:0]=HH
Single-In/Dual-Out  MODE[1:0]=HL	Dual-In/Single-Out  MODE[1:0]=LH
Single-In/Single-Out * 2  MODE[1:0]=LH	Dual-In/Selected Single-Out  MODE[1:0]=LL / HL
Single-In/Distributed Dual-Out  MODE[1:0]=LL	Single-In/Single-Out * 2  MODE[1:0]=HH

7. Function Description

Functional Overview

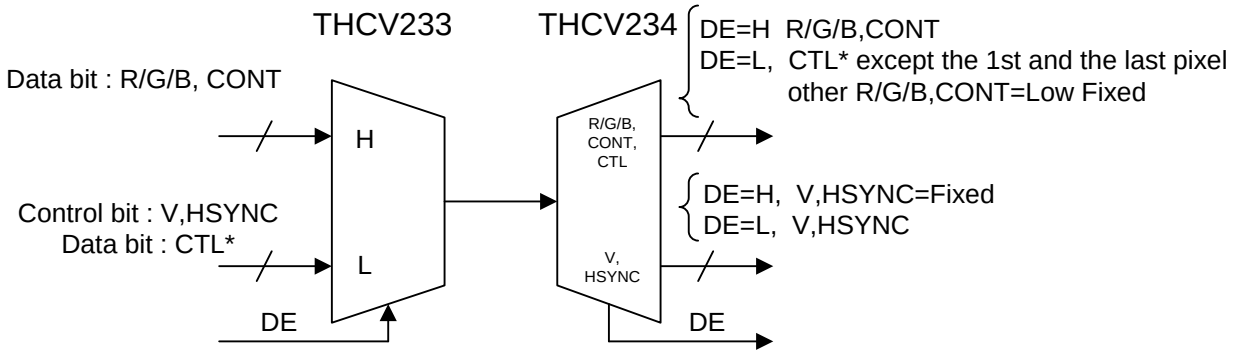
With High Speed CML SerDes, proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV233 and THCV234 enable transmission of 24/32bit video data, 2bit control data and Data Enable (DE) through high speed serial line by single/dual differential pair cable with minimal external components.

THCV233, LVDS data (including video data, control data and DE) and serializes video data and control data separately, depending on polarity of DE. DE is a signal which indicates whether video or control data are active. When DE is high, it serializes video data inputs into CML data streams. And it transmits serialized control data when DE is low. Instead of DE in the LVDS format, THCV233 has DEIN LVCMOS-input pin, which enables to transfer LVDS input data with external DE input via DEIN.

THCV234, automatically extracts clock from the incoming data streams and converts high-speed serial data into video data with DE being high or control data with DE being low, recognizing which type of serial data is being sent by transmitter. And it outputs the recovered data in the form of LVDS data. THCV234 has DEOUT output pin which transmits DE signal in LVCMOS. THCV234 can seamlessly operate for a wide range of a serial bit rate from 270Mbps to 4.2Gbps/lane.

DE signal (TLC[6] / DEIN) Input Requirement

There are some requirements for DE signal as described in Figure 3, Figure 4 Figure 14 and Table 24.
If DE=Low, control data of same cycle and particular assigned data bit 'CTL' except the first and the last pixel are transmitted. Otherwise video data are transmitted during DE=High.
Control data from receiver in DE=High period are previous data of DE transition. See Figure 4.
The length of DE being low and high is at least 2 clock cycles long, as described in Figure 14 and Table 24.
Data Enable must be toggled like High -> Low -> High at regular interval.



*CTL are particular assigned bit among R/G/B, CONT that can carry arbitrary data during DE=Low period.

Figure 3 Conceptual diagram of the basic operation of the chipset

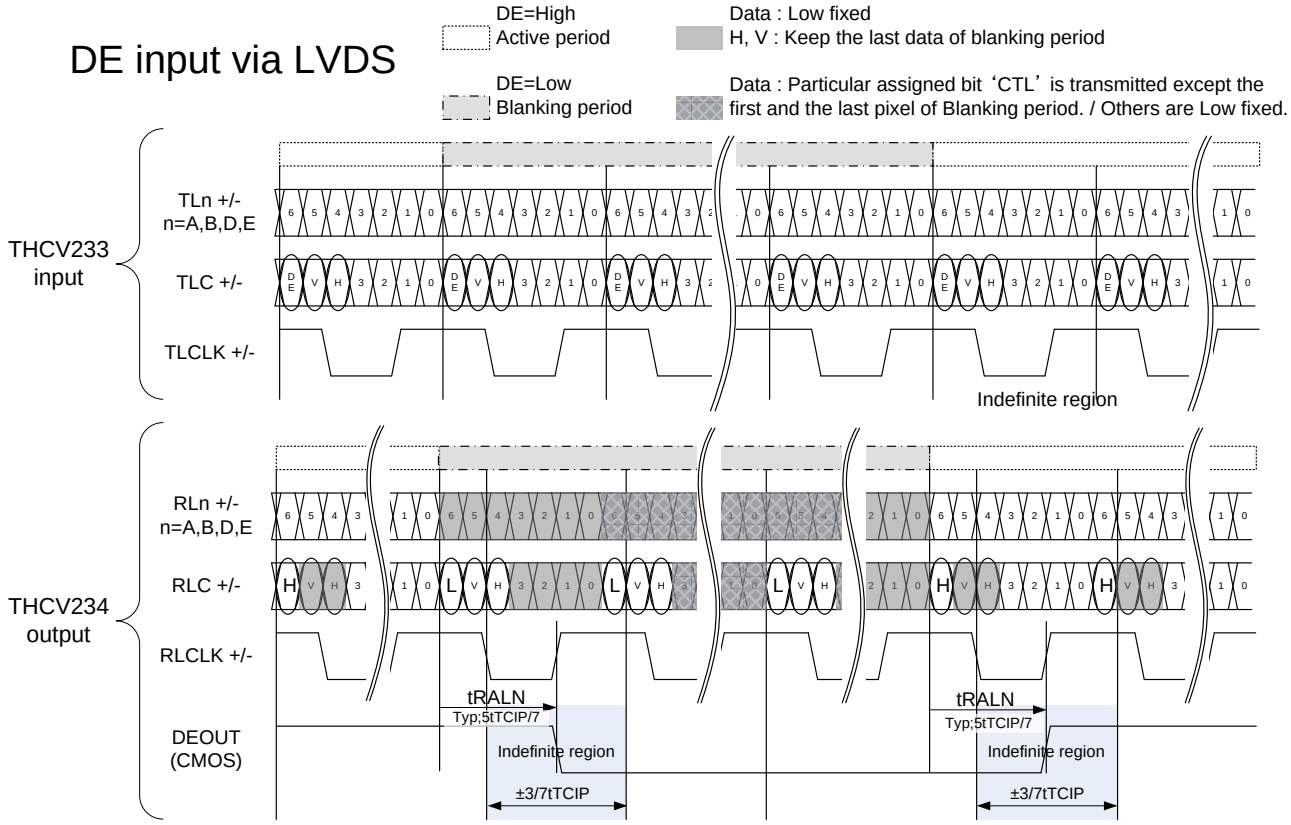


Figure 4 Data bit and control bit transmission when DE is from LVDS (default)

Data Enable input of THCV233 (DEIN)

DEIN is external DE input. When input LVDS does not contain DE signal, DE can be provided via DEIN. Activation setting of DEIN function is described in the following “Data Enable Select of THCV233”.

Data Enable output of THCV234 (DEOUT)

DEOUT output DE timing depending upon data stream state.

Data Enable Select of THCV233

Depending on pin setting THCV233 can deal with several DE alternatives.
DESEL pin is "choice of DE input" selector.
H : DE input from LVDS is used for processing, L : DE input from DEIN is used for processing
Figure 5 indicate DEIN operation. User must take care of data indefinite region and had better ignore them.

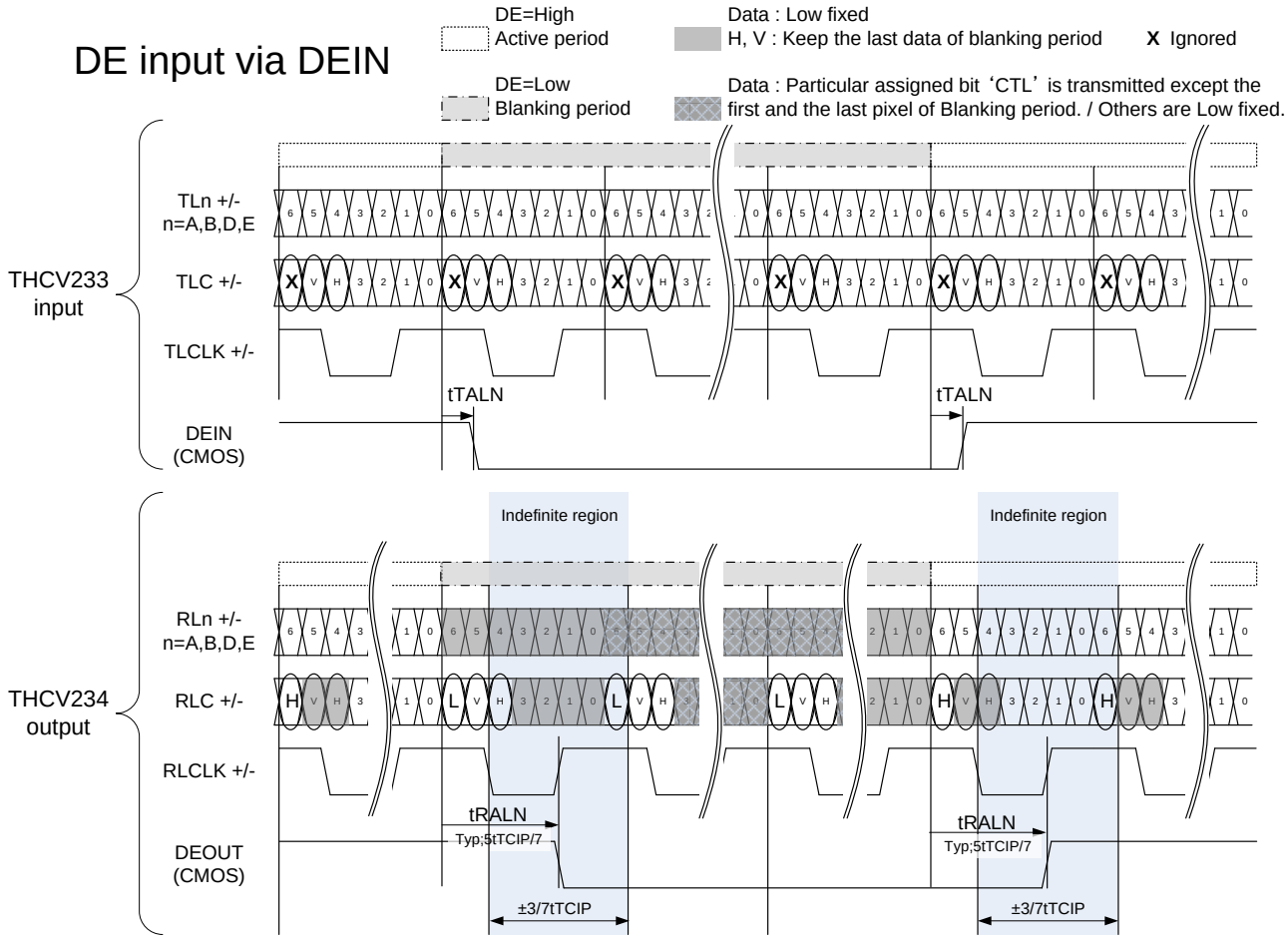


Figure 5 Data bit and control bit transmission when DE is from DEIN

Color depth or data width setting function (COL)

COL pin enables to select data width. E-ch. (TLE-/+ and RLE-/+) is disable with COL=H.

Table 5 Data Width Setting Function

COL	Mode Function
L	32bit-Data width
H	24bit-Data width

Operation mode function of THCV233 (MODE[1:0])

MODE[1:0] pins select data transfer mode of THCV233 as Table 2.

Table 6 Operation Mode Setting Function for THCV233

MODE[1:0]	Operation mode
LL	Single-in / Distribution Dual-out
LH	Single-in / Single-out
HL	Single-in / Dual-out
HH	Reserved (forbidden)

Operation mode function of THCV234 (MODE[1:0])

MODE[1:0] pins select data transfer mode of THCV234 as Table 2.

Table 7 Operation Mode Setting Function for THCV234

MODE[1:0]	Operation mode
LL	Dual-in / Selected single-out (Lane 0)
LH	Dual-in / Single-out
HL	Dual-in / Selected single-out (Lane 1)
HH	Single-in /Single-out

Multiple-chip configuration total Rx side LOCKN indicator (DGLOCK)

In order to reduce the number of cables needed for HTPDN and LOCKN in multiple-Rx chip configuration, THCV234 is equipped with the DGLOCK pin. When all the DGLOCK pins are connected as in Figure 6, the connected Rx chips can share the CDR lock status, making all the Rx chips in the same operation status.

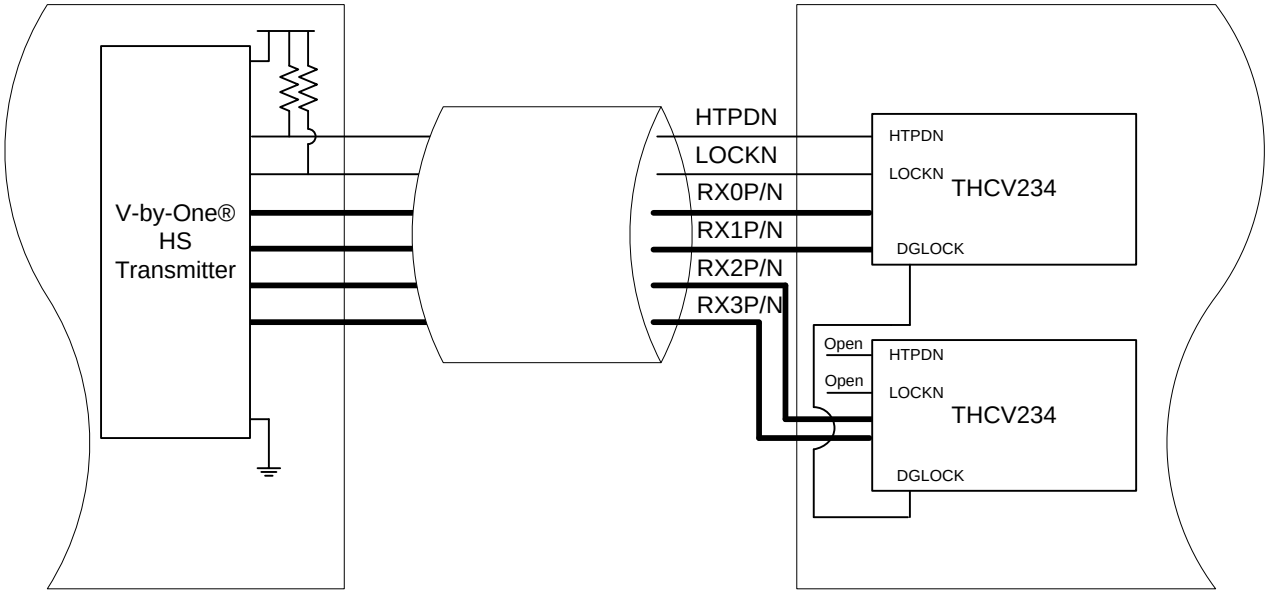


Figure 6 Usage of DGLOCK in multiple-Rx configuration

LVDS Mapping

LVDS data (video data, control data, DE) are mapped as Figure 7. TLC[6] is special bit for DE(data enable), and TLC[5:4] are for control data bits and the other bits are for video data. Among video data there are special assigned bit 'CTL' are defined for the data transmission under DE=low condition.

The number of LVDS channel depends on color depth mode(COL).

TLD[6] is not available in 24bit Data-width mode.

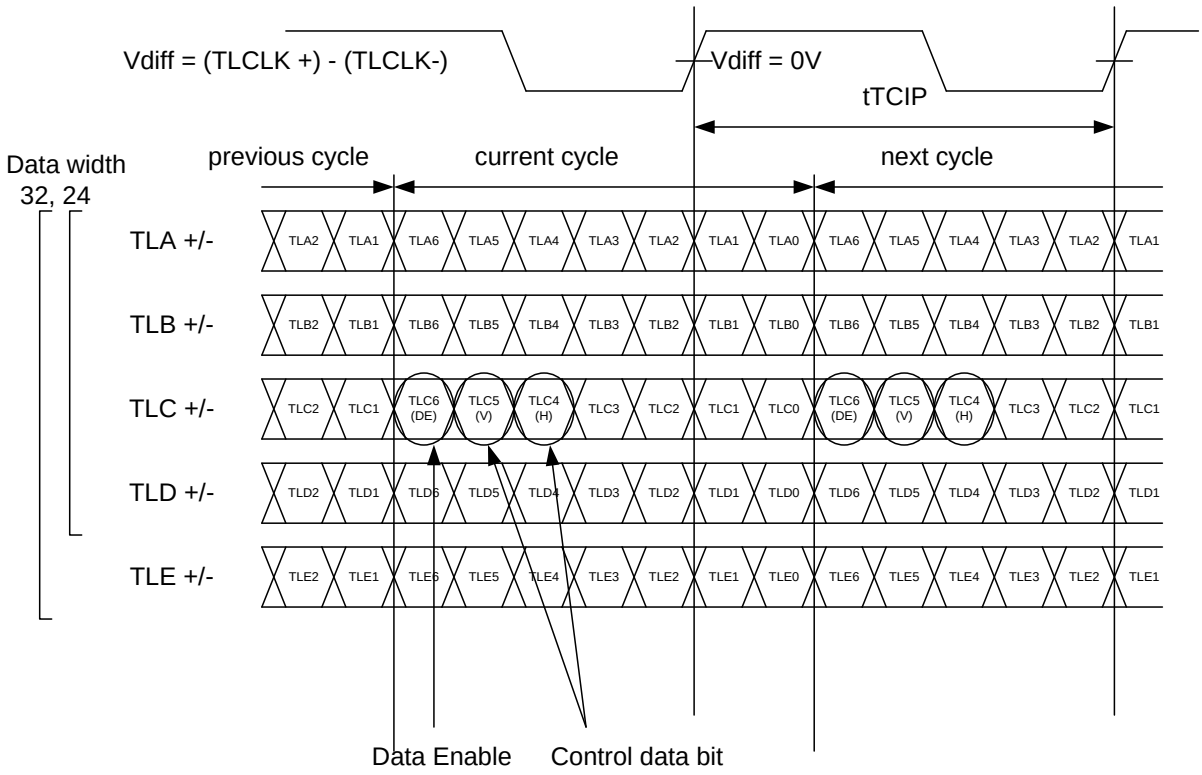


Figure 7 LVDS Data mapping timing diagram

Table 8 LVDS Color Data Mapping Table

THCV233 Input	THCV234 Output	COL		Symbol defined by V-by-One@ HS
		H (8bit)	L (10bit)	
TLA[0]	RLA[0]	R[2]	R[4]	D2
TLA[1]	RLA[1]	R[3]	R[5]	D3
TLA[2]	RLA[2]	R[4]	R[6]	D4
TLA[3]	RLA[3]	R[5]	R[7]	D5
TLA[4]	RLA[4]	R[6]	R[8]	D6
TLA[5]	RLA[5]	R[7]	R[9]	D7
TLA[6]	RLA[6]	G[2]	G[4]	D10
TLB[0]	RLB[0]	G[3]	G[5]	D11
TLB[1]	RLB[1]	G[4]	G[6]	D12
TLB[2]	RLB[2]	G[5]	G[7]	D13
TLB[3]	RLB[3]	G[6]	G[8]	D14
TLB[4]	RLB[4]	G[7]	G[9]	D15
TLB[5]	RLB[5]	B[2]*2	B[4]*2	D18
TLB[6]	RLB[6]	B[3]*2	B[5]*2	D19
TLC[0]	RLC[0]	B[4]*2	B[6]*2	D20
TLC[1]	RLC[1]	B[5]*2	B[7]*2	D21
TLC[2]	RLC[2]	B[6]*2	B[8]*2	D22
TLC[3]	RLC[3]	B[7]*2	B[9]*2	D23
TLC[4]	RLC[4]	HSYNC	HSYNC	Hsync
TLC[5]	RLC[5]	VSYNC	VSYNC	Vsync
TLC[6]	RLC[6]	DE	DE	DE
TLD[0]	RLD[0]	R[0]	R[2]	D0
TLD[1]	RLD[1]	R[1]	R[3]	D1
TLD[2]	RLD[2]	G[0]	G[2]	D8
TLD[3]	RLD[3]	G[1]	G[3]	D9
TLD[4]	RLD[4]	B[0]*2	B[2]*2	D16
TLD[5]	RLD[5]	B[1]*2	B[3]*2	D17
TLD[6]	RLD[6]	N/A*1	CONT[1]*2*3	D25*3
TLE[0]	RLE[0]	Channel Power Down	R[0]*2	D30
TLE[1]	RLE[1]		R[1]*2	D31
TLE[2]	RLE[2]		G[0]*2	D28
TLE[3]	RLE[3]		G[1]*2	D29
TLE[4]	RLE[4]		B[0]*2	D26
TLE[5]	RLE[5]		B[1]*2	D27
TLE[6]	RLE[6]		CONT[2]*2*3	D24*3

*1 N/A: Not available, THCV234 output RLDn[6]=Low.
*2 CTL bits, which are carried during DE=Low except the 1st and the last pixel
*3 3D flags defined in the V-by-One® HS Standard are assigned to the following bit.
V-by-One® HS Standard Packer/Unpacker D[24](3DLR) <=> LVDS T/RLE[6]
V-by-One® HS Standard Packer/Unpacker D[25](3DEN) <=> LVDS T/RLD[6]

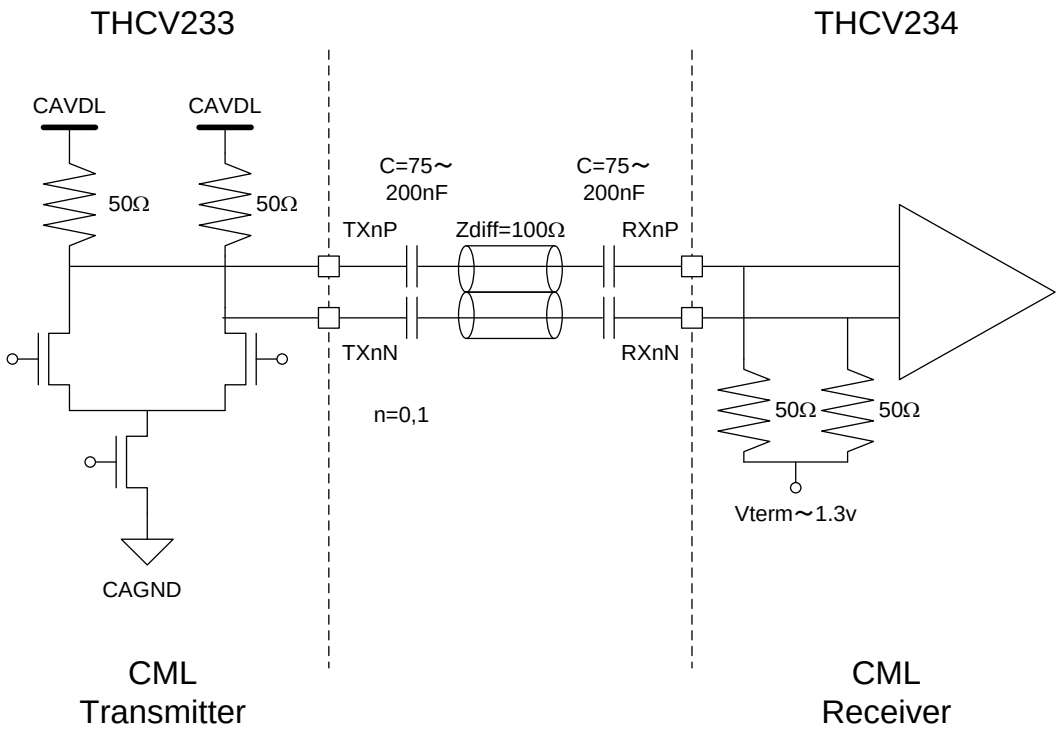
THCV234 LVDS Reduced swing output function (RS)

RS controls THCV234 LVDS output swing level.

Table 9 LVDS output swing level

RS	Output swing
L	Reduced swing (200mV typical)
H	Normal swing (350mV typical)

CML Buffer



Capacitor on transmitter side is mandatory, while receiver side is optional and recommended.

Figure 8 High-Speed CML Buffer Scheme

Lock detect and Hot-plug function

LOCKN and HTPDN are both open drain outputs from THCV234. Pull-up resistors are needed at THCV233 side to 3.3V. See Figure 9.

If THCV234 is not active (power down mode (PDN=L) or powered off), HTPDN is open. Otherwise, HTPDN is pulled down by THCV234.

HTPDN of THCV233 side is high when THCV234 is not active or the receiver board is not connected. Then THCV233 enters into the power down mode. When HTPDN transits from High to Low, THCV233 starts up and transmits training pattern for link training.

LOCKN indicates whether THCV234 is in the lock state or not. If THCV234 is in the unlock state, LOCKN is open. Otherwise (in the lock state), it's pulled down by THCV234.

THCV233 keeps transmitting training pattern until LOCKN transits to Low. After training done, THCV234 sinks current and LOCKN is Low. Then THCV233 starts transmitting normal data pattern.

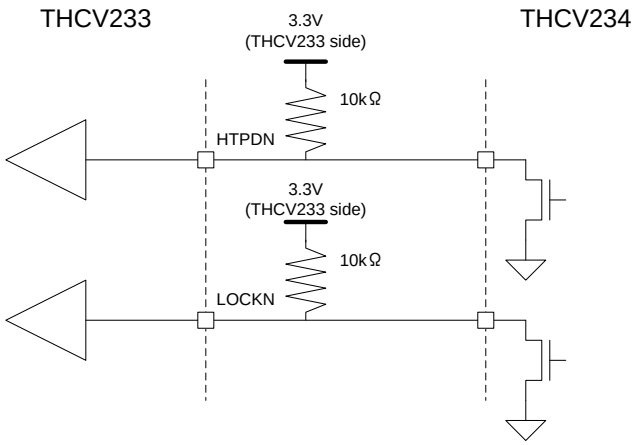


Figure 9 Hot-plug and Lock Detect Scheme

No HTPDN connection option

HTPDN connection between THCV233 and THCV234 can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken as Low. See Figure 10.

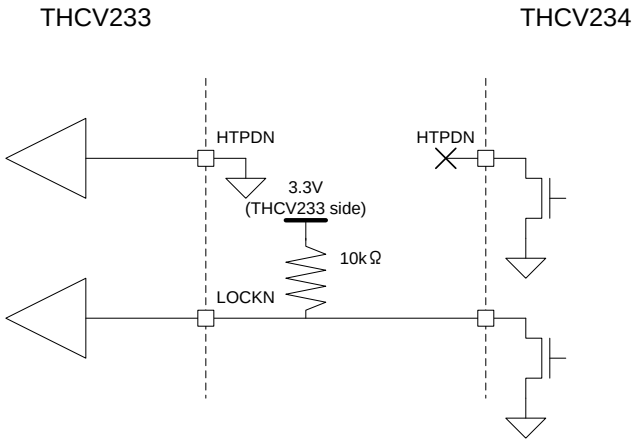


Figure 10 HTPDN is not Connected Scheme

THCV233 Pre-emphasis function (PRE)

Pre-emphasis can equalize severe signal degradation caused by long distance or high-speed transmission. PRE, select the strength of pre-emphasis.

Table 10 Pre-emphasis function table

PRE	Description
L	without Pre-emphasis
H	with 100% Pre-emphasis

Field BET Operation

In order to help users to check validity of high speed serial lines, THCV233/THCV234 has an operation mode in which they act as a bit error tester (BET). In this mode, THCV233 internally generates test pattern which is then serialized onto the high speed serial line. THCV234 receives the data stream and checks bit errors.

This "Field BET" mode is activated by setting BET= H both on THCV233 and THCV234. Pattern Generator CLK is from LVDS-CLK and the pattern is then 8b/10b encoded, scrambled, and serialized onto the high speed serial lines. As for THCV234, the internal test pattern check circuit gets enabled and reports result on DEOUT pin. The DEOUT pin goes LOW whenever bit errors occur, or it stays HIGH when there is no bit error. Refer to Figure 11. User can select 2 kinds of check result, “Latched-result” or “NOT latched result”. The latch is reset by setting RS=L.

Table 11 THCV233-234 Field BET operation pin settings

THCV233	THCV234		Conditions	
BET	BET	RS	Operation	Output Latch select
L	L	-	Normal Operation	-
H	H	L	FieldBET Operation	NOT latched result
H	H	H		Latched result

Table 12 THCV234 Field BET result

DEOUT	Output
L	Bit error occurred
H	No error

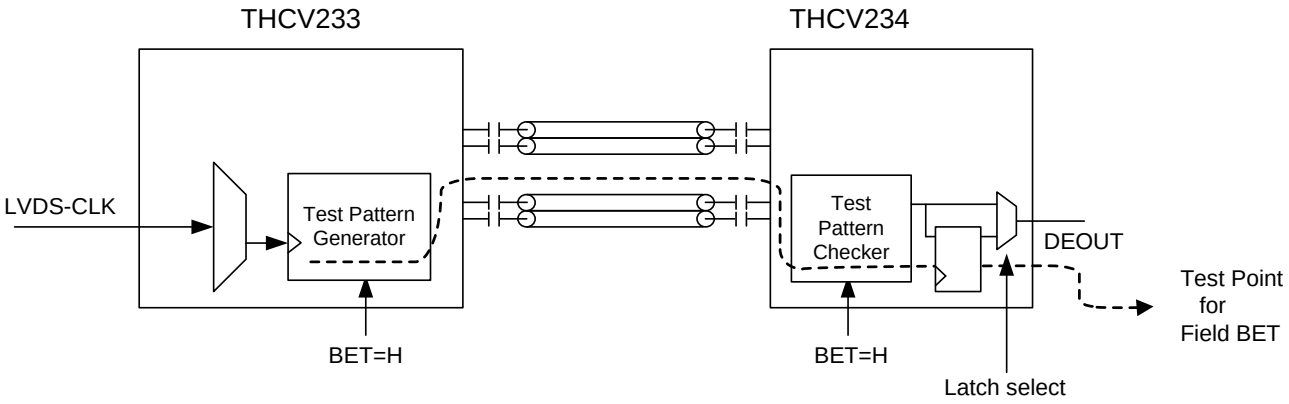


Figure 11 Field BET Configuration

8. Absolute Maximum Ratings*

Table 13 THCV233 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Units
1.8v Supply Voltage（CAVDL,CPVDL,VDD）	VDL	-0.3	-	+2.1	V
3.3v Supply Voltage(LAVDH)	VDH	-0.3	-	+4.0	V
CMOS Input Voltage	-	-0.3	-	VDH+0.3	V
LVDS Receiver Input Voltage	-	-0.3	-	VDH+0.3	V
CML Transmitter Output Voltage	-	-0.3	-	VDL+0.3	V
Output Current	-	-50	-	50	mA
Storage Temperature	-	-55	-	+125	°C
Junction Temperature	-	-	-	+125	°C
Reflow Peak Temperature/Time	-	-	-	+260/10sec	°C
Maximum Power Dissipation @＋25° C	-	-	-	3.2	W

Table 14 THCV234 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Units
1.8v Supply Voltage（CAVDL,CPVDL,VDD）	VDL	-0.3	-	+2.1	V
3.3v Supply Voltage(LAVDH)	VDH	-0.3	-	+4.0	V
CMOS Input Voltage	-	-0.3	-	VDH+0.3	V
CML Receiver Input Voltage	-	-0.3	-	VDL+0.3	V
LVDS Transmitter Output Voltage	-	-0.3	-	VDH+0.3	V
Output Current	-	-30	-	30	mA
Storage Temperature	-	-55	-	+125	°C
Junction Temperature	-	-	-	+125	°C
Reflow Peak Temperature/Time	-	-	-	+260/10sec	°C
Maximum Power Dissipation @＋25°C	-	-	-	3.2	W

* “Absolute Maximum Ratings” are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

9. Operating Conditions

There are two types of operating temperature ranges as shown below.

1. From 0°C to 70°C
2. From -40°C to 105°C

Details are shown in the table below.

Table 15 THCV233 Operating Conditions (0°C≤TMP≤70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
1.8v Supply Voltage（CAVDL,CPVDL,VDD）	VDL	1.62 or 1.71(1)	1.80	1.98 or 1.89(1)	V
3.3v Supply Voltage(LAVDH)	VDH	3.00	3.30	3.60	V
Operating Ambient Temperature	TMP	0	-	70	°C

Table 16 THCV233 Operating Conditions (-40°C≤TMP≤105°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
1.8v Supply Voltage（CAVDL,CPVDL,VDD）	VDL	1.62 or 1.70(1)	1.80	1.98	V
3.3v Supply Voltage(LAVDH)	VDH	3.00	3.30	3.60	V
Operating Ambient Temperature	TMP	-40	-	105	°C

Table 17 THCV234 Operating Conditions (0°C≤TMP≤70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
1.8v Supply Voltage（CAVDL,CPVDL,VDD）	VDL	1.62 or 1.71(1)	1.80	1.98 or 1.89(1)	V
3.3v Supply Voltage(LAVDH)	VDH	3.00	3.30	3.60	V
Operating Ambient Temperature	TMP	0	-	70	°C

Table 18 THCV234 Operating Conditions (-40°C≤TMP≤105°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
1.8v Supply Voltage（CAVDL,CPVDL,VDD）	VDL	1.70	1.80	1.98	V
3.3v Supply Voltage(LAVDH)	VDH	3.00	3.30	3.60	V
Operating Ambient Temperature	TMP	-40	-	105	°C

(1) Maximum value of LVDS CLK Frequency depends on minimum value of VDL. Refer to Table 1.

10. Electrical Specifications

DC Specifications

Table 19 THCV233 and THCV234 3.3V CMOS DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIH	High Level Input Voltage	I,BPU	2.1	-	VDH	V
VIL	Low Level Input Voltage	I,BPU	0	-	0.7	V
VOH	High Level Output Voltage	O IOH=-8mA	2.4	-	VDH	V
VOL	Low Level Output Voltage	O IOL=8mA	-	-	0.4	V
		O,BPU IOL=4mA	-	-	0.4	V
IIH	Input Leak Current High	VIN=VDH	-10	-	+10	uA
IIL	Input Leak Current Low	VIN=GND	-10	-	+10	uA

Table 20 THCV233 LVDS, CML DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VTTH	LVDS Differential Input High Threshold	-	-	-	100	mV
VTTL	LVDS Differential Input Low Threshold	-	-100	-	-	mV
ITIH	LVDS Input Leak Current High	TLx+/-=VDH, PDN=L x=A~E,CLK	-	-	±10	uA
ITIL	LVDS Input Leak Current Low	TLx+/-=GND, PDN=L x=A~E,CLK	-	-	±10	uA
RTIN	LVDS Differential Input Resistance	PDN=L	80	100	120	Ω
VTOD	CML Differential Mode Output Voltage	-	200	300	400	mV
PRE	CML Pre-emphasis Level	PRE=L	-	0	-	%
		PRE=H	80	100	120	%
VTOC	CML Common Mode Output Voltage	PRE=L	VDL-VTOD			mV
		PRE=H	VDL-2×VTOD			mV
ITOH	CML Output Leak Current High	PDN=L	-	-	±10	uA
ITOS	CML Output Short Circuit Current	VDL=1.8V	-90	-	-	mA

Table 21 THCV234 LVDS, CML DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input Low Threshold	-	-50	-	-	mV
IRIH	CML Input Leak Current High	PDN=L, RXnP/N=VDL n=0,1	-	-	±10	uA
IRIL	CML Input Leak Current Low	PDN=L, RXnP/N=GND n=0,1	-	-	±10	uA
IRRIH	CML Input Current High	RXnP/N=VDL, n=0,1	-	-	2	mA
IRRIL	CML Input Current Low	RXnP/N=GND, n=0,1	-6	-	-	mA
RRIN	CML Differential Input Resistance	-	80	100	120	Ω
VROD	LVDS Differential Mode Output Voltage (Normal Swing)	RL=100Ω, RS=H	250	350	450	mV
	LVDS Differential Mode Output Voltage (Reduced Swing)35	RL=100Ω, RS=L	100	200	300	mV
ΔVROD	Change in VROD bet1.375ween Complementary Output States	RL=100Ω	-	-	35	mV
VROC	LVDS Common Mode Output Voltage	RL=100Ω	1.125	1.25	1.375	V
ΔVROC	Change in VROC between Complementary Output States	RL=100Ω	-	-	35	mV
IROS	LVDS Output Short Circuit Current	RLx+/-=GND	-30	-	-	mA
IROZ	LVDS Output TRI-STATE Current	PDN=L, RLx+/-=GND, VDH x=A~E,CLK	-	-	±10	uA

Supply Currents

Table 22 THCV233 Supply Currents

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ITCCW_M	Transmitter Supply Current for VDL (Worst Case Pattern as shown in Figure 12)	SiSo 10bit 85MHz PRE=H, PDN=H	-	-	150	mA
		SiDo 10bit 85MHz PRE=H, PDN=H	-	-	185	mA
		SiDDo 10bit 85MHz PRE=H PDN=H	-	-	225	mA
		SiSo 10bit 105MHz PRE=H, PDN=H VDL=1.89V	-	-	161	mA
		SiDo 10bit 105MHz PRE=H, PDN=H VDL=1.89V	-	-	188	mA
		SiDDo 10bit 105MHz PRE=H, PDN=H VDL=1.89V	-	-	234	mA
ITCCW33_M	Transmitter Supply Current for VDH (Worst Case Pattern as shown in Figure 12)	SiSo 10bit, PRE=H PDN=H	-	-	12	mA
		SiDo 10bit, PRE=H PDN=H	-	-	12	mA
		SiDDo 10bit, PRE=H PDN=H	-	-	12	mA
ITCCS	Transmitter Power Down Supply Current	PDN=L All Inputs =Fixed LorH	-	-	170	uA

Table 23 THCV234 Supply Currents

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IRCCW_M	Receiver Supply Current for VDL (Worst Case Pattern as shown in Figure 12)	SiSo 10bit 85MHz PDN=H	-	-	90	mA
		DiSo 10bit 85MHz PDN=H	-	-	90	mA
		DiSSo 10bit 85MHz PDN=H	-	-	90	mA
		SiSo 10bit 105MHz PDN=H, VDL=1.89V	-	-	117	mA
		DiSo 10bit 105MHz PDN=H, VDL=1.89V	-	-	107	mA
		DiSSo 10bit 105MHz PDN=H, VDL=1.89V	-	-	107	mA
IRCCW33_M	Receiver Supply Current for VDH (Worst Case Pattern as shown in Figure 12)	SiSo 10bit 85MHz PDN=H	-	-	90	mA
		DiSo 10bit 85MHz PDN=H	-	-	90	mA
		DiSSo 10bit 85MHz PDN=H	-	-	90	mA
		SiSo 10bit 105MHz PDN=H	-	-	101	mA
		DiSo 10bit 105MHz PDN=H	-	-	101	mA
		DiSSo 10bit 105MHz PDN=H	-	-	101	mA
IRCCS	Receiver Power Down Supply Current	PDN=L All Inputs =Fixed LorH	-	-	150	uA

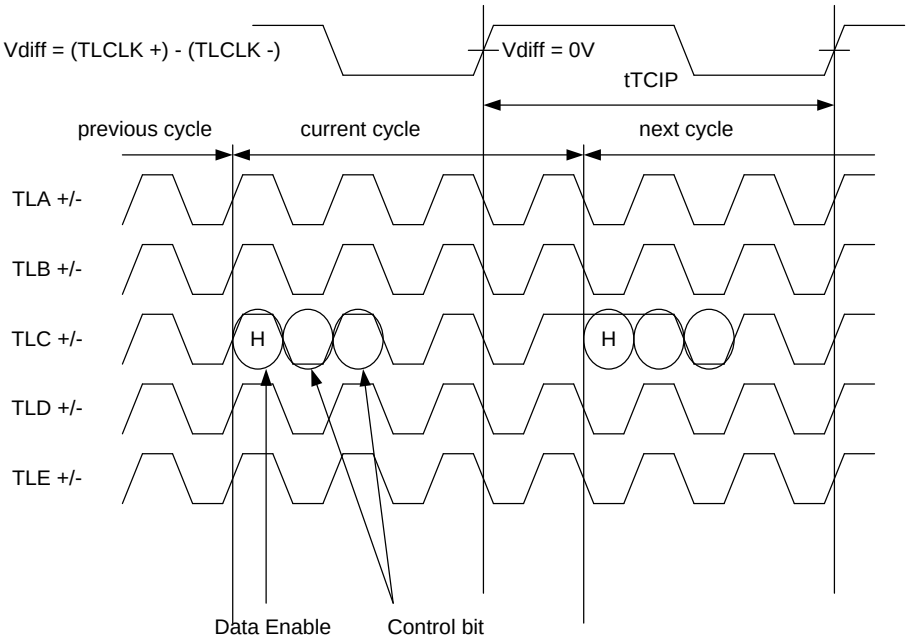


Figure 12 Worst Case Pattern

Switching Characteristics

Table 24 DE signal (TLC[6] / DEIN) Input Requirement

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tDEH	DE=High Duration	-	2×tTCIP			sec
tDEL	DE=Low Duration	SiSo, SiDDo	2×tTCIP			sec
		SiDo	4×tTCIP			sec

Table 25 THCV233 Switching Characteristics (0°C≤TMP≤70°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tTBIT	Unit Interval	COL=H	333	tTCIP/30	3704	ps
		COL=L	294	tTCIP/40	2778	ps
		COL=L VDL=1.71V~1.89V	238	tTCIP/40	2778	ps
tTCIP	TLCLK Period	COL=H, Si/So	10	-	111	ns
		COL=H, Si/DDo	10	-	50	ns
		COL=H, Si/Do	10	-	25	ns
		COL=L, Si/So	11.76	-	111	ns
		COL=L, Si/DDo	11.76	-	50	ns
		COL=L, Si/Do	11.76	-	25	ns
		COL=L, Si/So VDL=1.71V~1.89V	9.52	-	111	ns
		COL=L, Si/DDo VDL=1.71V~1.89V	9.52	-	50	ns
		COL=L, Si/Do VDL=1.71V~1.89V	9.52	-	25	ns
tTCIH	LVDS Differential Clock High Time	-	2×tTCIP/7	4×tTCIP/7	5×tTCIP/7	ns
tTCIL	LVDS Differential Clock Low Time	-	2×tTCIP/7	4×tTCIP/7	5×tTCIP/7	ns
tSK	LVDS Receiver Skew Margin	tTCIP=75MHz	-440	-	440	ps
		tTCIP=85MHz	-390	-	390	ps
		tTCIP=95MHz	-340	-	340	ps
		tTCIP=100MHz	-330	-	330	ps
		tTCIP=105MHz	-310	-	310	ps
tTIP1	LVDS Input Data Position1	-	-tSK	0	+tSK	ns
tTIP0	LVDS Input Data Position0	-	tTCIP/7-tSK	tTCIP/7	tTCIP/7+tSK	ns
tTIP6	LVDS Input Data Position6	-	2xtTCIP/7-tSK	2xtTCIP/7	2xtTCIP/7+tSK	ns
tTIP5	LVDS Input Data Position5	-	3xtTCIP/7-tSK	3xtTCIP/7	3xtTCIP/7+tSK	ns
tTIP4	LVDS Input Data Position4	-	4xtTCIP/7-tSK	4xtTCIP/7	4xtTCIP/7+tSK	ns
tTIP3	LVDS Input Data Position3	-	5xtTCIP/7-tSK	5xtTCIP/7	5xtTCIP/7+tSK	ns
tTIP2	LVDS Input Data Position2	-	6xtTCIP/7-tSK	6xtTCIP/7	6xtTCIP/7+tSK	ns
tTALN	LVDS-ALNIN timing tolerance	-	0	-	3×tTCIP/7	ns
tTRF	CML Output Rise and Fall Time(20%-80%)	-	50	-	150	ps
tTOSK	CML Lane0/1 Output Inter Pair Skew	-	-2	-	2	UI
tTCD	Input Clock to Output Data Delay	SiDDo 10bit 85MHz	143.4	-	150.2	ns
tTLH	VDL On to VDH On Delay	-	0	-	-	ns
tTPD	Power On to PDN High Delay	-	0	-	-	ns
tTPDL	PDN Low Pulse Width	-	1	-	-	ms
tTPLL0	PDN High to CML Output Delay	-	-	-	10	ms
tTPLL1	PDN Low to CML Output High Fix Delay	-	-	-	20	ns
tTNP0	LOCKN High to Training Pattern Output Delay	-	-	-	10	ms
tTNP1	LOCKN Low to Data Pattern Output Delay	-	-	-	10	ms

Table 26 THCV233 Switching Characteristics (-40°C≤TMP≤105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tTBIT	Unit Interval	COL=H	333	tTCIP/30	3704	ps
		COL=L	333	tTCIP/40	2778	ps
		COL=H VDL=1.70V~1.98V	333	tTCIP/30	3704	ps
		COL=L VDL=1.70V~1.98V	309	tTCIP/40	2778	ps
tTCIP	TLCLK Period	COL=H, Si/So	10	-	111	ns
		COL=H, Si/DDo	10	-	50	ns
		COL=H, Si/Do	10	-	25	ns
		COL=L, Si/So VDL=1.62V~1.98V	13.3	-	111	ns
		COL=L, Si/DDo VDL=1.62V~1.98V	13.3	-	50	ns
		COL=L, Si/Do VDL=1.62V~1.98V	13.3	-	25	ns
		COL=L, Si/So VDL=1.7V~1.98V	12.35	-	111	ns
		COL=L, Si/DDo VDL=1.7V~1.98V	12.35	-	50	ns
		COL=L, Si/Do VDL=1.7V~1.98V	12.35	-	25	ns
tTCIH	LVDS Differential Clock High Time	-	2×tTCIP/7	4×tTCIP/7	5×tTCIP/7	ns
tTCIL	LVDS Differential Clock Low Time	-	2×tTCIP/7	4×tTCIP/7	5×tTCIP/7	ns
tSK	LVDS Receiver Skew Margin	tTCIP=75MHz	-440	-	440	ps
		tTCIP=85MHz	-390	-	390	ps
		tTCIP=100MHz	-330	-	330	ps
tTIP1	LVDS Input Data Position1	-	-tSK	0	+tSK	ns
tTIP0	LVDS Input Data Position0	-	tTCIP/7-tSK	tTCIP/7	tTCIP/7+tSK	ns
tTIP6	LVDS Input Data Position6	-	2xtTCIP/7-tSK	2xtTCIP/7	2xtTCIP/7+tSK	ns
tTIP5	LVDS Input Data Position5	-	3xtTCIP/7-tSK	3xtTCIP/7	3xtTCIP/7+tSK	ns
tTIP4	LVDS Input Data Position4	-	4xtTCIP/7-tSK	4xtTCIP/7	4xtTCIP/7+tSK	ns
tTIP3	LVDS Input Data Position3	-	5xtTCIP/7-tSK	5xtTCIP/7	5xtTCIP/7+tSK	ns
tTIP2	LVDS Input Data Position2	-	6xtTCIP/7-tSK	6xtTCIP/7	6xtTCIP/7+tSK	ns
tTALN	LVDS-ALNIN timing tolerance	-	0	-	3×tTCIP/7	ns
tTRF	CML Output Rise and Fall Time(20%-80%)	-	50	-	150	ps
tTOSK	CML Lane0/1 Output Inter Pair Skew	-	-2	-	2	UI
tTCD	Input Clock to Output Data Delay	SiDDo 10bit 85MHz	143.4	-	150.2	ns
tTLH	VDL On to VDH On Delay	-	0	-	-	ns
tTPD	Power On to PDN High Delay	-	0	-	-	ns
tTPDL	PDN Low Pulse Width	-	1	-	-	ms
tTPLL0	PDN High to CML Output Delay	-	-	-	10	ms
tTPLL1	PDN Low to CML Output High Fix Delay	-	-	-	20	ns
tTNP0	LOCKN High to Training Pattern Output Delay	-	-	-	10	ms
tTNP1	LOCKN Low to Data Pattern Output Delay	-	-	-	10	ms

Table 27 THCV234 Switching Characteristics (0°C≤TMP≤70°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tRBIT	Unit Interval	COL=H	333	tTCIP/30	3704	ps
		COL=L	294	tTCIP/40	2778	ps
		COL=L VDL=1.71V~1.89V	238	tTCIP/40	2778	ps
tRISK	CML Lane0/1 Input Inter Pair Skew Margin	-	-	-	15	UI
tRLVT	LVDS Differential Output Transition Time	-	-	0.6	1.5	ns
tROP1	LVDS Output Data Position1	SiSo 10bit 105MHz	-0.16	0	0.16	ns
tROP0	LVDS Output Data Position0	SiSo 10bit 105MHz	tTCIP/7-0.16	tTCIP/7	tTCIP/7+0.16	ns
tROP6	LVDS Output Data Position6	SiSo 10bit 105MHz	2xtTCIP/7-0.16	2xtTCIP/7	2xtTCIP/7+0.16	ns
tROP5	LVDS Output Data Position5	SiSo 10bit 105MHz	3xtTCIP/7-0.16	3xtTCIP/7	3xtTCIP/7+0.16	ns
tROP4	LVDS Output Data Position4	SiSo 10bit 105MHz	4xtTCIP/7-0.16	4xtTCIP/7	4xtTCIP/7+0.16	ns
tROP3	LVDS Output Data Position3	SiSo 10bit 105MHz	5xtTCIP/7-0.16	5xtTCIP/7	5xtTCIP/7+0.16	ns
tROP2	LVDS Output Data Position2	SiSo 10bit 105MHz	6xtTCIP/7-0.16	6xtTCIP/7	6xtTCIP/7+0.16	ns
tRALN	LVDS-ALNOUT timing accuracy	-	2×tTCIP/7	5×tTCIP/7	8×tTCIP/7	ns
tRDC	Input Data to Output Clock Delay	SiSo 10bit	808×tRBIT+8	-	808×tRBIT+14.5	ns
tRLH	VDL On to VDH On Delay	-	0	-	-	ns
tRPD	Power On to PDN High Delay	-	0	-	-	ns
tRPDL	PDN Low Pulse Width	-	1.0	-	-	ms
tRHPD0	PDN High to HTPDN Low Delay	-	-	-	1	us
tRHPD1	PDN Low to HTPDN High Delay	-	-	-	1	us
tRPLL0	Training Pattern Input to LOCKN Low Delay	-	-	-	10	ms
tRPLL1	PDN Low to LOCKN High Delay	-	-	-	10	us
tRLCK0	LOCKN Low to LVDS Output Delay	-	-	-	1	ms
tRLCK1	LOCKN High to LVDS HighZ Delay	-	-	-	0	ns

Table 28 THCV234 Switching Characteristics (-40°C≤TMP≤105°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tRBIT	Unit Interval	COL=H	351	tTCIP/30	3704	ps
		COL=L	351	tTCIP/40	2778	ps
tRISK	CML Lane0/1 Input Inter Pair Skew Margin	-	-	-	15	UI
tRLVT	LVDS Differential Output Transition Time	-	-	0.6	1.5	ns
tROP1	LVDS Output Data Position1	SiSo 10bit 71.25MHz	-0.2	0	0.2	ns
tROP0	LVDS Output Data Position0	SiSo 10bit 71.25MHz	tTCIP/7-0.16	tTCIP/7	tTCIP/7+0.16	ns
tROP6	LVDS Output Data Position6	SiSo 10bit 71.25MHz	2xtTCIP/7-0.16	2xtTCIP/7	2xtTCIP/7+0.16	ns
tROP5	LVDS Output Data Position5	SiSo 10bit 71.25MHz	3xtTCIP/7-0.16	3xtTCIP/7	3xtTCIP/7+0.16	ns
tROP4	LVDS Output Data Position4	SiSo 10bit 71.25MHz	4xtTCIP/7-0.16	4xtTCIP/7	4xtTCIP/7+0.16	ns
tROP3	LVDS Output Data Position3	SiSo 10bit 71.25MHz	5xtTCIP/7-0.16	5xtTCIP/7	5xtTCIP/7+0.16	ns
tROP2	LVDS Output Data Position2	SiSo 10bit 71.25MHz	6xtTCIP/7-0.16	6xtTCIP/7	6xtTCIP/7+0.16	ns
tRALN	LVDS-ALNOUT timing accuracy	-	2×tTCIP/7	5×tTCIP/7	8×tTCIP/7	ns
tRDC	Input Data to Output Clock Delay	SiSo 10bit	808×tRBIT+8	-	808×tRBIT+14.5	ns
tRLH	VDL On to VDH On Delay	-	0	-	-	ns
tRPD	Power On to PDN High Delay	-	0	-	-	ns
tRPDL	PDN Low Pulse Width	-	1.0	-	-	ms
tRHPD0	PDN High to HTPDN Low Delay	-	-	-	1	us
tRHPD1	PDN Low to HTPDN High Delay	-	-	-	1	us
tRPLL0	Training Pattern Input to LOCKN Low Delay	-	-	-	10	ms
tRPLL1	PDN Low to LOCKN High Delay	-	-	-	10	us
tRLCK0	LOCKN Low to LVDS Output Delay	-	-	-	1	ms
tRLCK1	LOCKN High to LVDS HighZ Delay	-	-	-	0	ns

11. AC Timing Diagrams and Test Circuits

LVDS Input Switching Characteristics

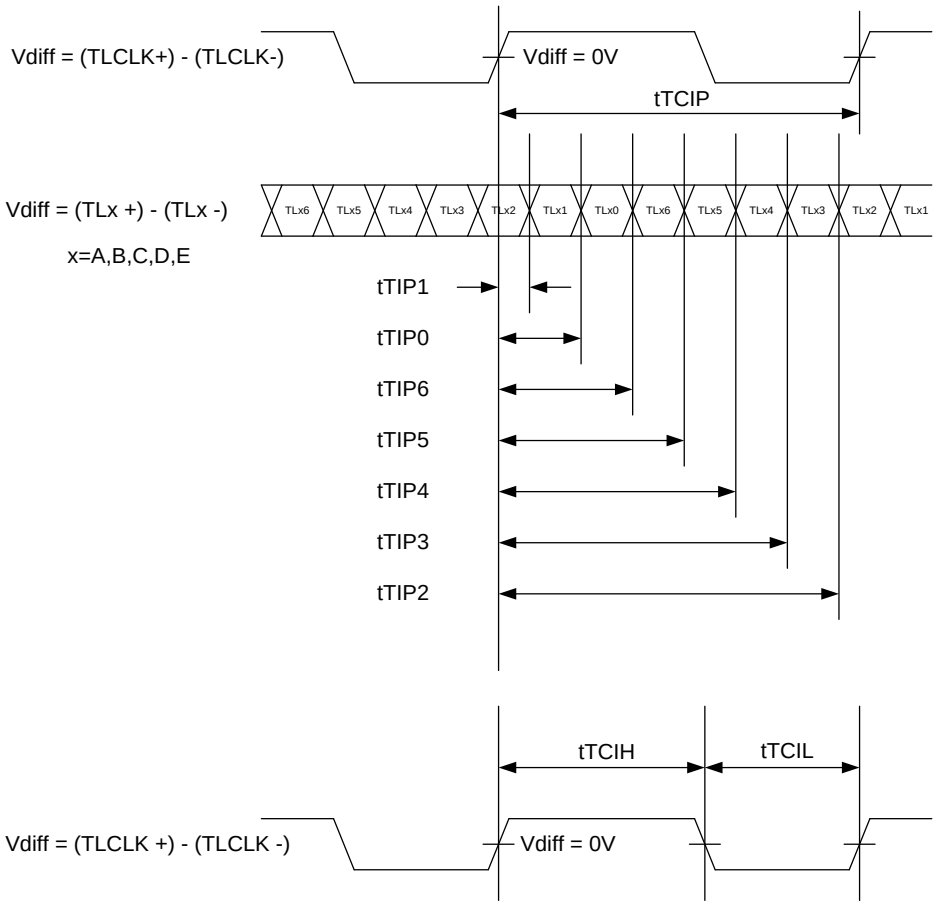


Figure 13 LVDS Input Switching Timing Diagrams

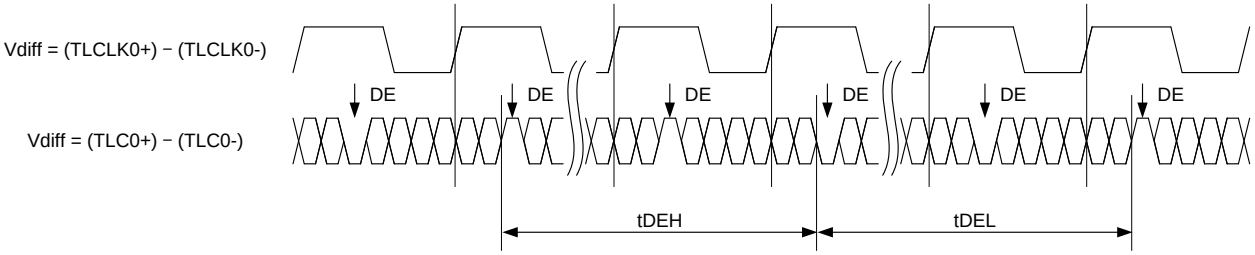


Figure 14 DE period requirement

LVDS Output Switching Characteristics

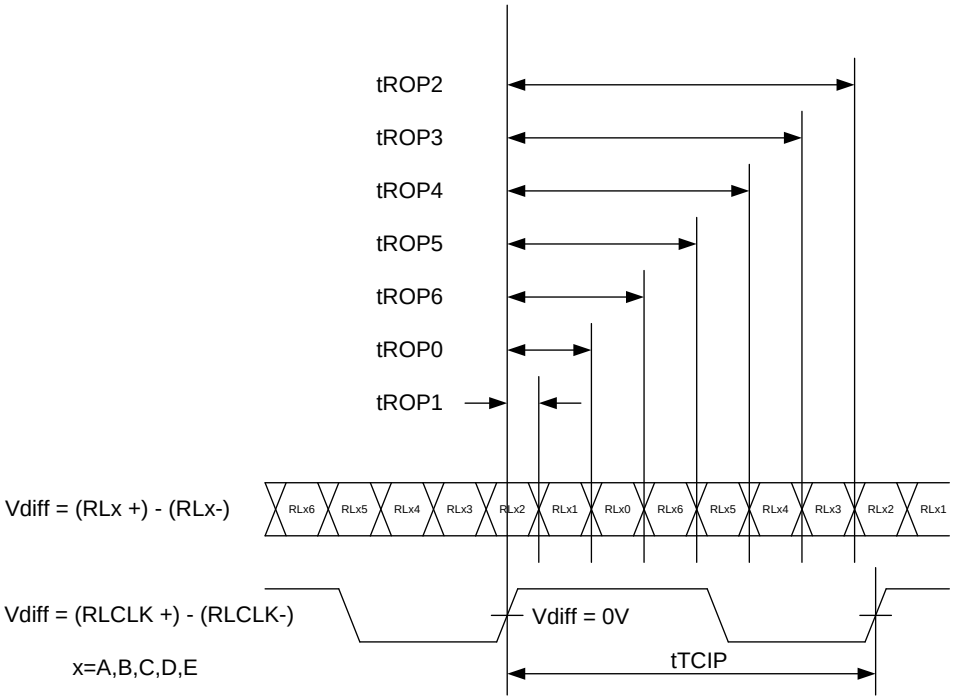


Figure 15 LVDS Output Switching Timing Diagrams

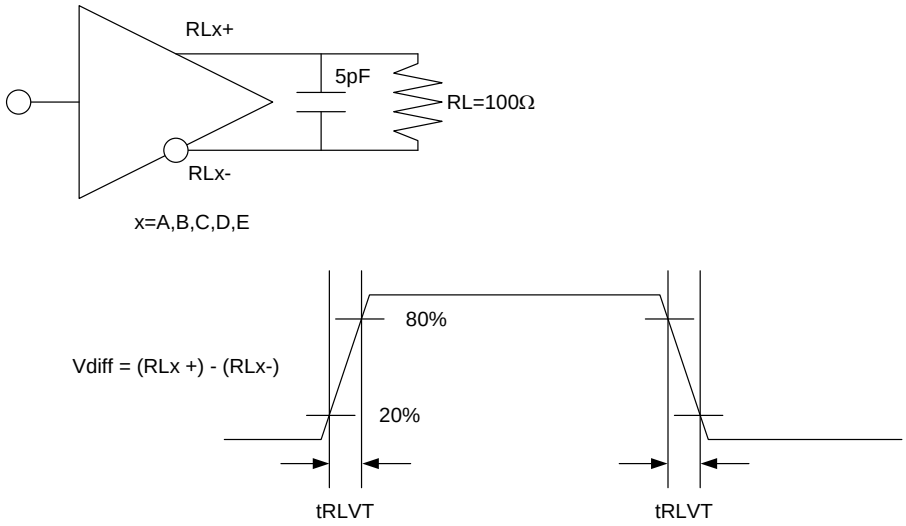


Figure 16 LVDS Output Switching Timing Diagram and Test Circuit.

CML Output Switching Characteristics

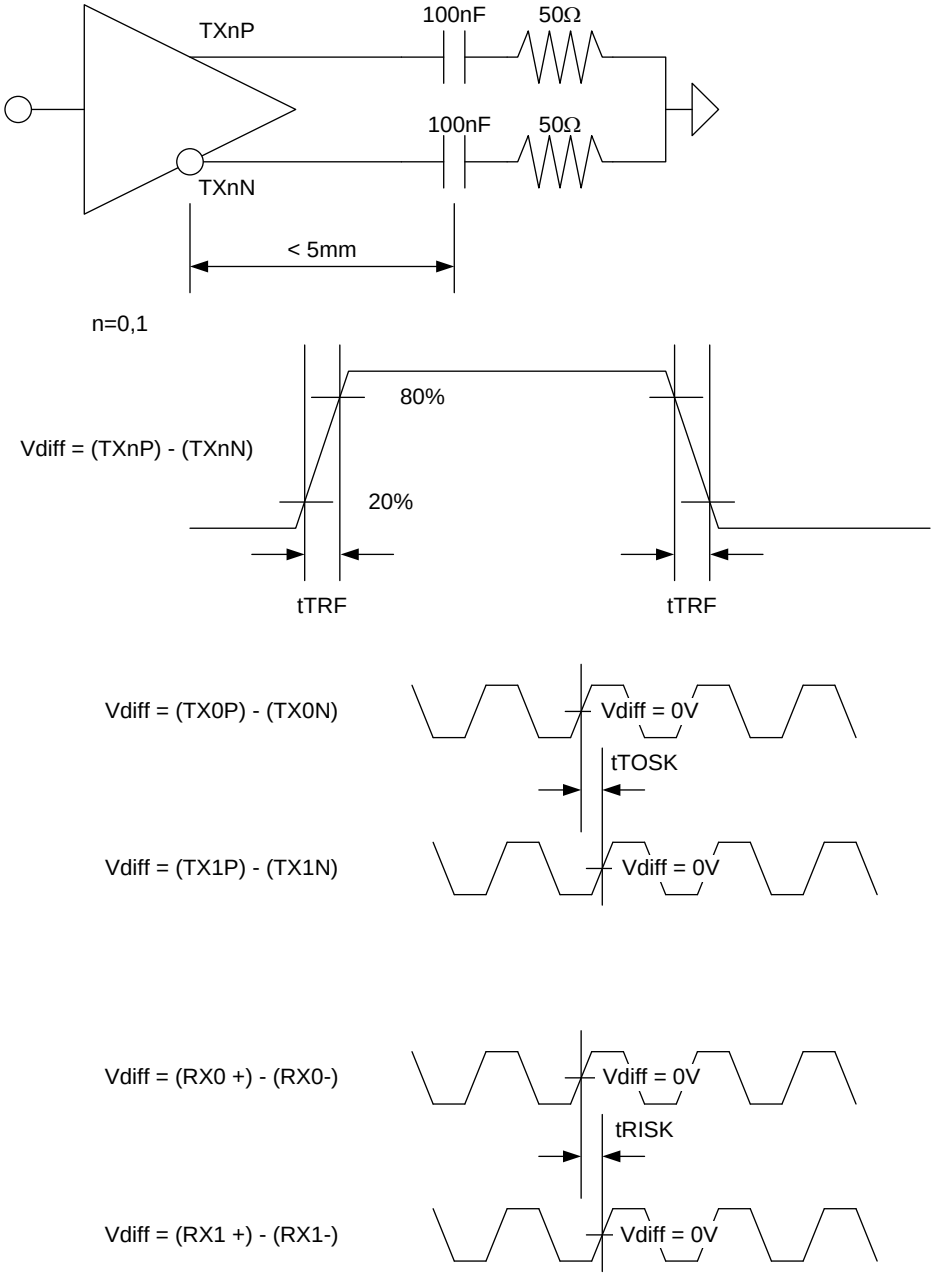


Figure 17 High-Speed CML Output Switching Timing Diagrams and Test Circuit

Latency Characteristics

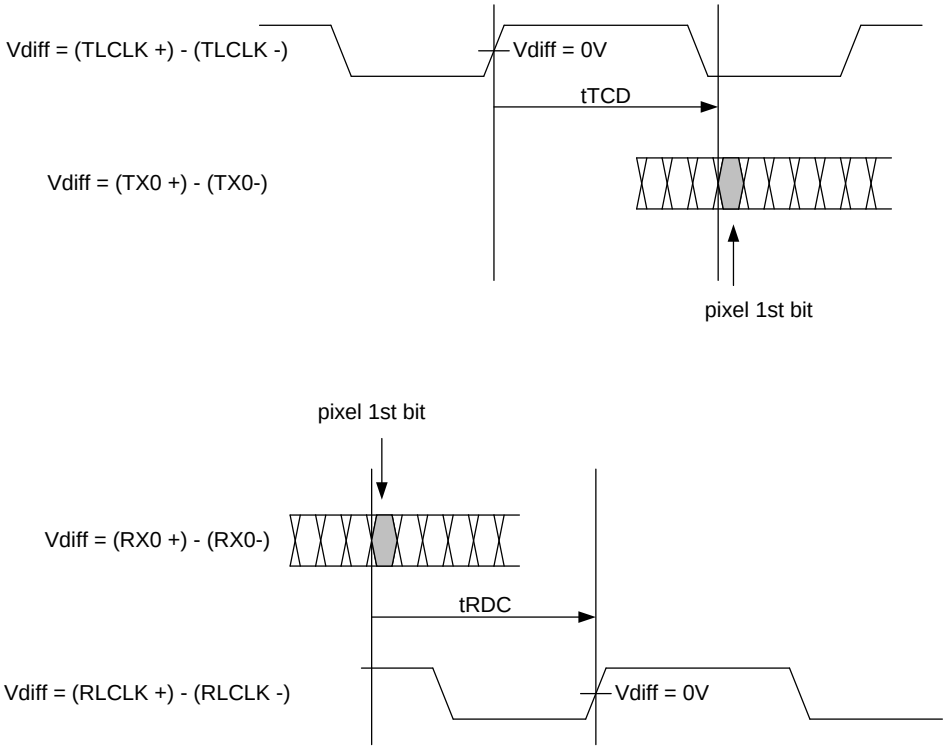


Figure 18 THCV233 and THCV234 Latency

Lock and Unlock Sequence

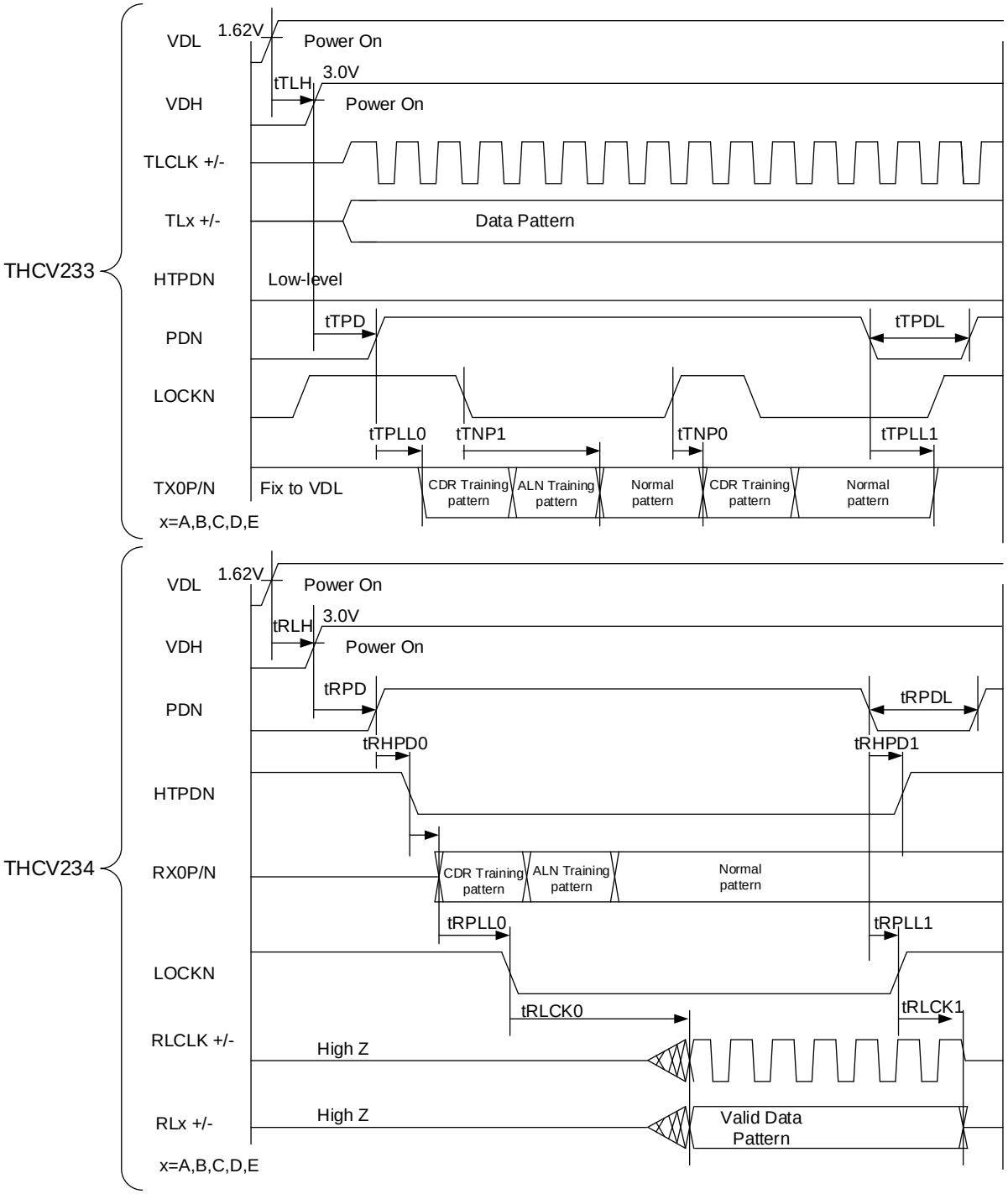


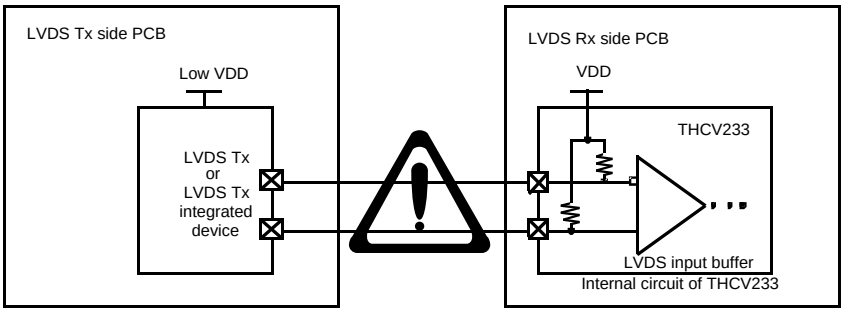
Figure 19 THCV233 and THCV234 Lock/Unlock Sequence

VDH must not precedes VDL, while tTLH and tRLH min. is 0sec; therefore, VDL/H can be at the same time.
tTPD and tRPD minimum is 0sec; therefore, PDN can be applied at the same time as VDL and VDH.
tTPLL0 is the time from “both PDN=High and HTPDN=Low“ moment to Training pattern ignition.
HTPDN could transit from High to Low under PDN=High condition at THCV233, which is different from what Figure 19 indicates but is natural situation.

Note

1)LVDS input pin connection

When LVDS line is not driven from the previous device, the line is pulled up to 3.3V internally in THCV233.This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THCV233. One solution for this problem is PDN=L control during no LVDS input period because pull-up resistors are cut off at power down state.



2)Power On Sequence

Do not apply VDH before VDL. VDL and VDH can be applied at the same time.

3)Data Input Sequence

Don’t input TLCLK+/- before THCV233 is on in order to keep absolute maximum ratings.

4)Cable Connection and Disconnection

Don’t connect and disconnect the LVDS cable, when the power is supplied to the system.

5)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THCV233-234 on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

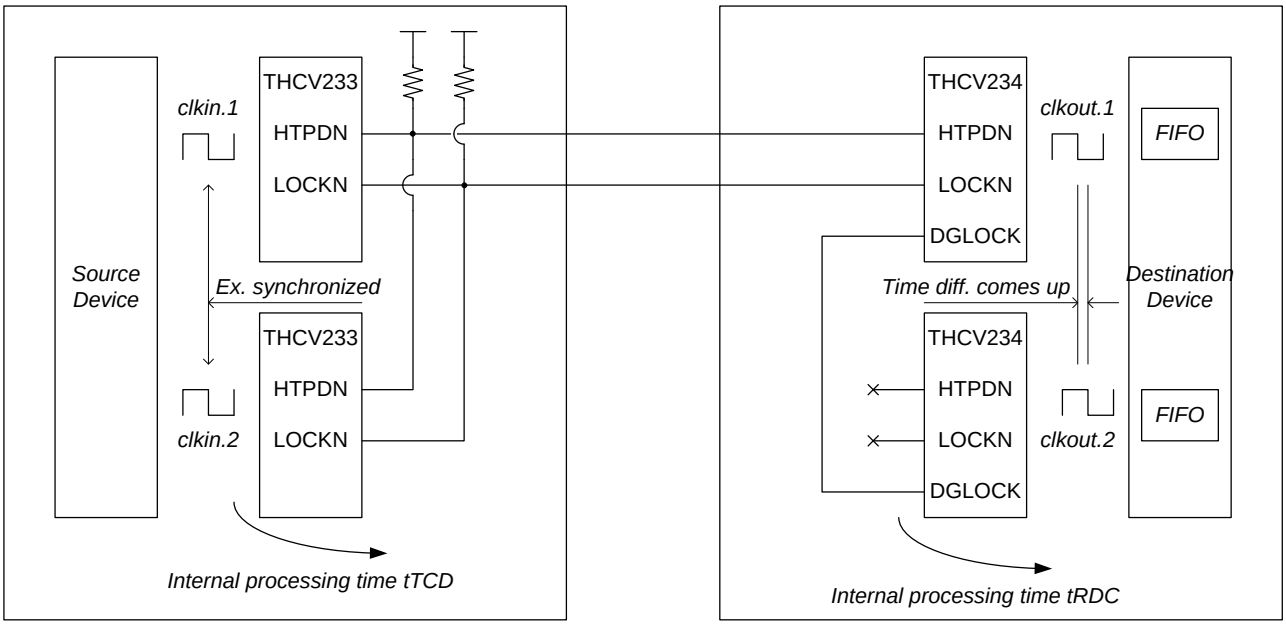
6)Low Input Pulse into PDN Period Requirement

Don’t Input Low Pulse within 1msec into PDN.

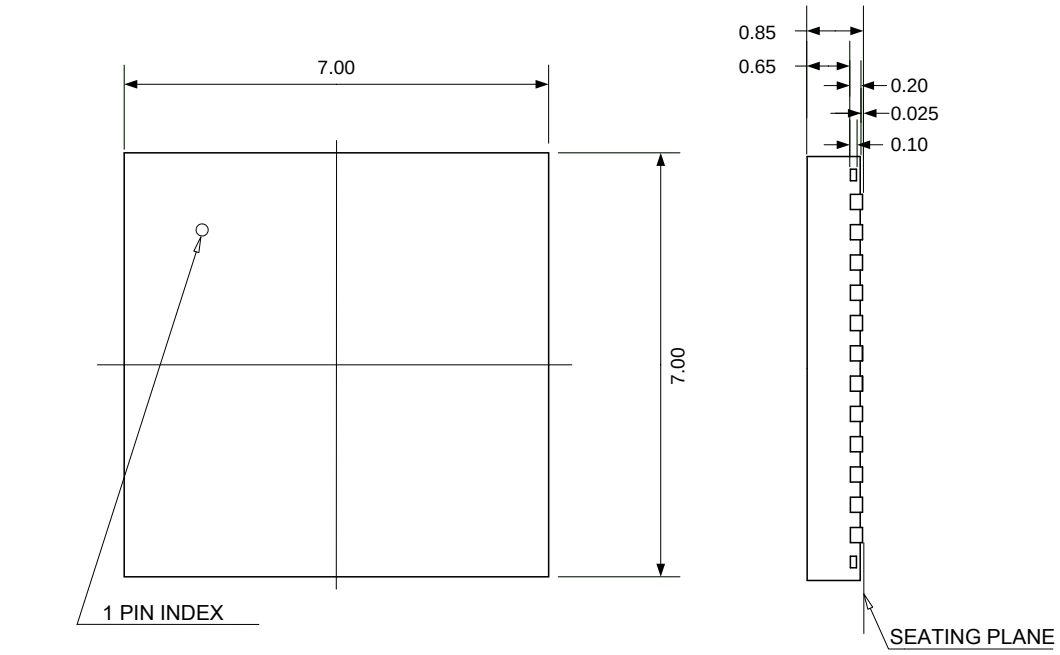
7)Multiple device connection

HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure.
HTPDN should be from just one Rx to multiple Tx because its purpose is only ignition of all Tx.
LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data.
LOCKN of Tx side can be simply split to multiple Tx.
THCV234 DGLOCK connection is appropriate for multiple Rx use.

Also possible time difference of internal processing time (p.23 to 24 THCV233 tTCD and p.25 THCV234 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV234, which may have internal FIFO.

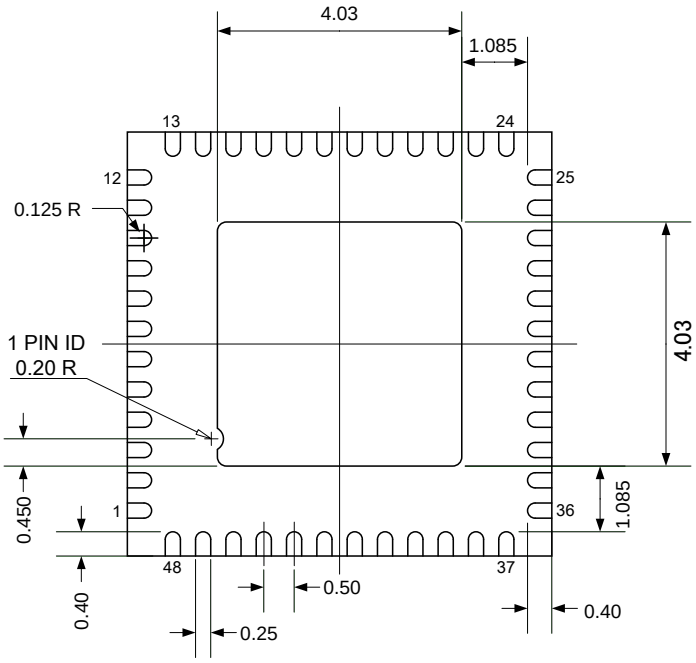


Package



TOP VIEW

SIDE VIEW



BOTTOM VIEW

Unit:mm

Exposed PAD is GND and must be soldered to PCB.

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9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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