OptiMOS™3 Power-Transistor

Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, logic level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications
- Halogen-free according to IEC61249-2-21

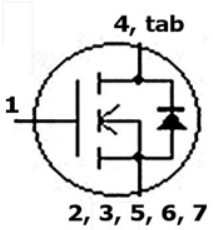
Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	1.6	mΩ
I_D	180	A

RoHS

Halogen-Free

Type	IPB016N06L3 G
Package	PG-TO-263-7
Marking	016N06L



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	180	A
		T_C=100 °C	180	
Pulsed drain current[3]	$I_{D,pulse}$	T_C=25 °C	720	
Avalanche energy, single pulse[4]	E_{AS}	I_D=100 A, R_{GS}=25 Ω	634	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	250	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22
[2] Current is limited by bondwire; with an R_{thJC}=0.6 K/W the chip is able to carry 293 A.
[3] See figure 3 for more detailed information
[4] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.6	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[5)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=196 µA	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	-	0.1	3	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C	-	30	300	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=100 A	-	1.2	1.6	mΩ
		V_{GS}=4.5 V, I_D=50 A	-	1.6	2.7	
Gate resistance	R_G		-	1.3	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=100 A	124	248	-	S

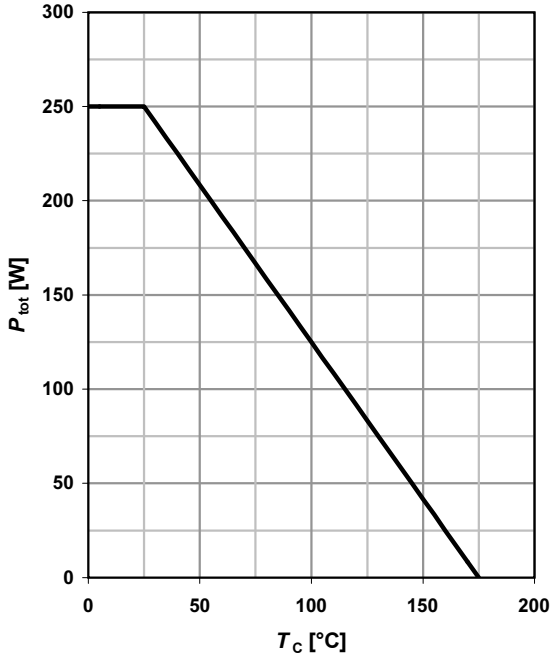
[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	-	21000	28000	pF
Output capacitance	C_{oss}		-	3300	4400	
Reverse transfer capacitance	C_{rss}		-	140	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=100 A, R_G=1.6 Ω	-	35	-	ns
Rise time	t_r		-	79	-	
Turn-off delay time	$t_{d(off)}$		-	131	-	
Fall time	t_f		-	38	-	
Gate Charge Characteristics[6)]						
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 4.5 V	-	65	-	nC
Gate to drain charge	Q_{gd}		-	21	-	
Switching charge	Q_{sw}		-	50	-	
Gate charge total	Q_g		-	125	166	
Gate plateau voltage	$V_{plateau}$		-	3.1	-	V
Output charge	Q_{oss}	V_{DD}=30 V, V_{GS}=0 V	-	165	219	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	180	A
Diode pulse current	$I_{S,pulse}$		-	-	720	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=100A, di_F/dt=100 A/µs	-	71	-	ns
Reverse recovery charge	Q_{rr}		-	87	-	nC

[6)] See figure 16 for gate charge parameter definition

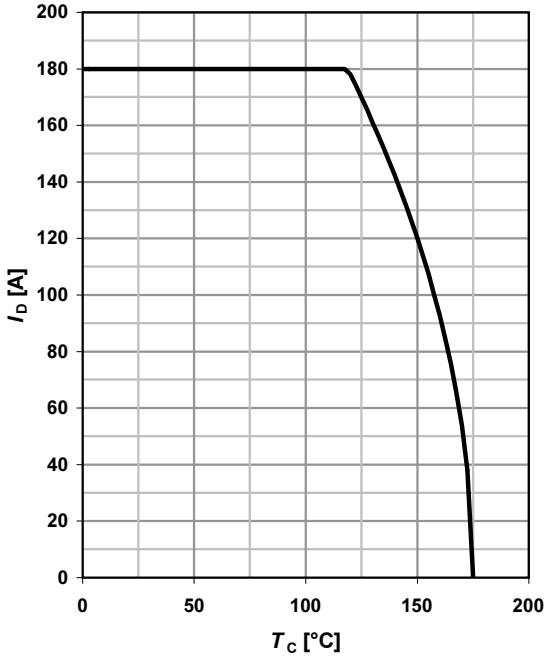
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

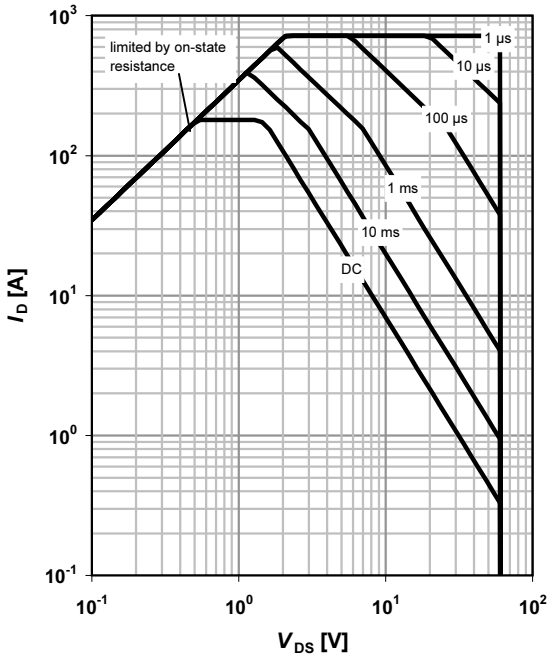
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

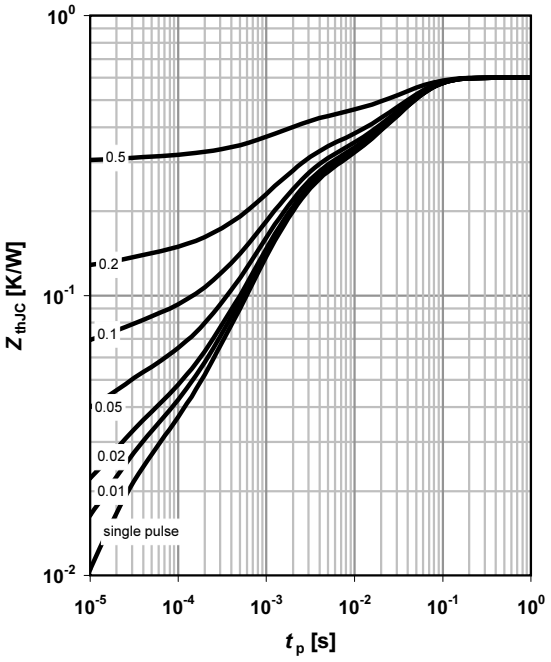
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

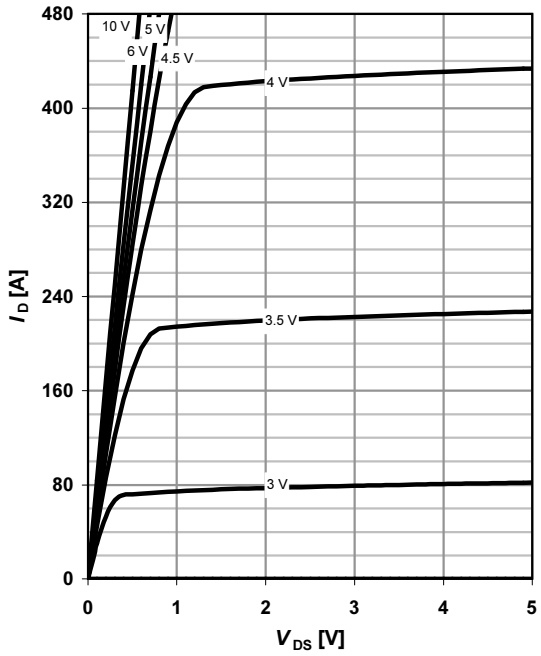
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

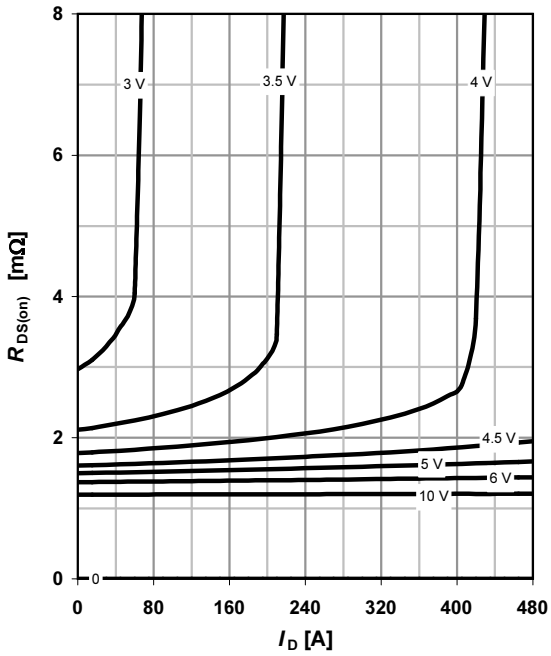
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

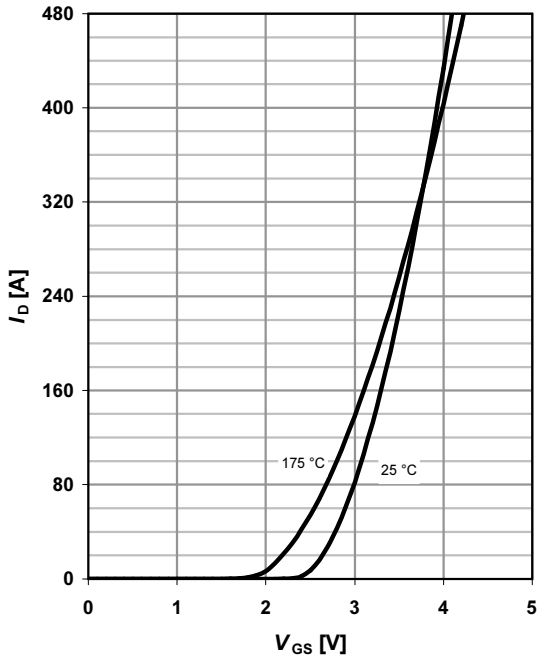
parameter: V_{GS}



7 Typ. transfer characteristics

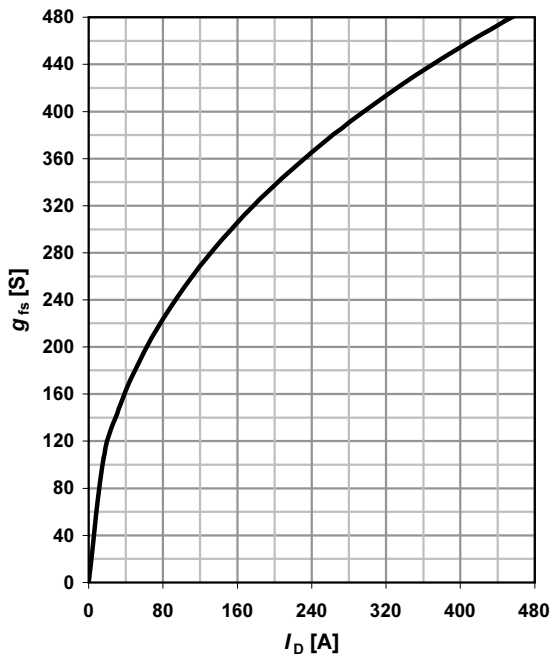
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$

parameter: T_j



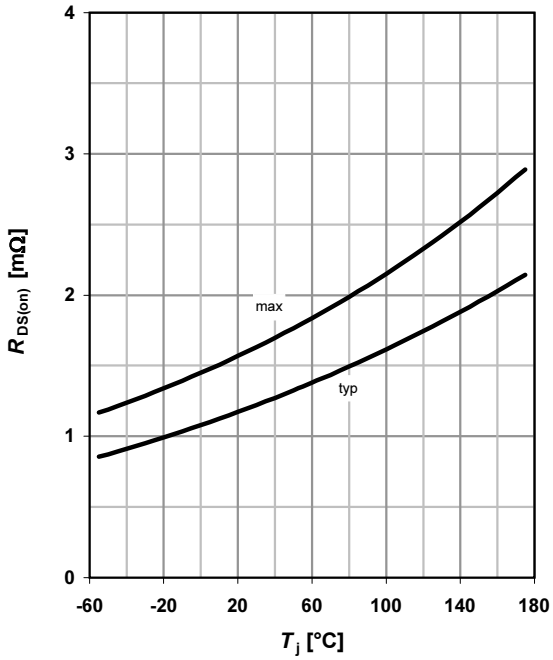
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

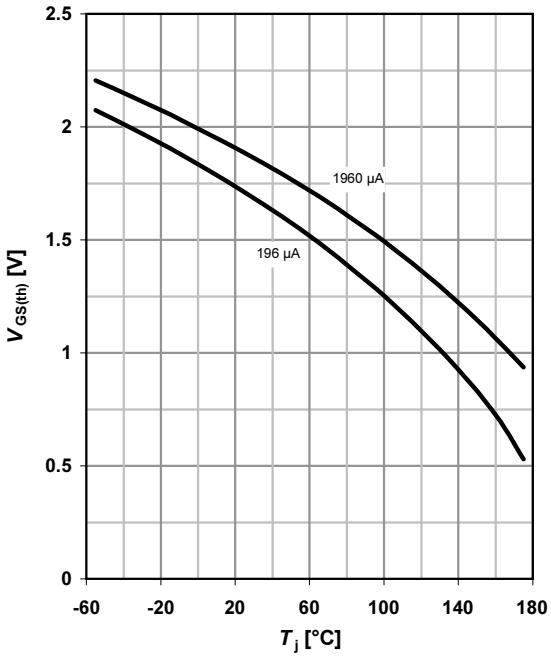
$R_{DS(on)}$=f(T_j); I_D=100 A; V_{GS}=10 V



10 Typ. gate threshold voltage

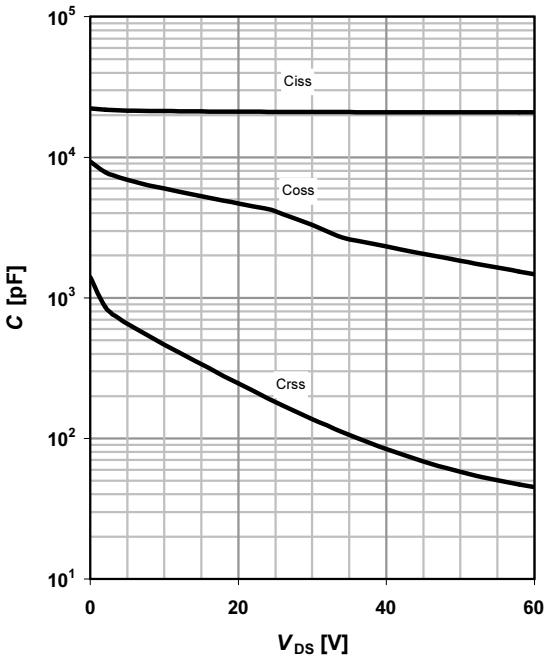
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

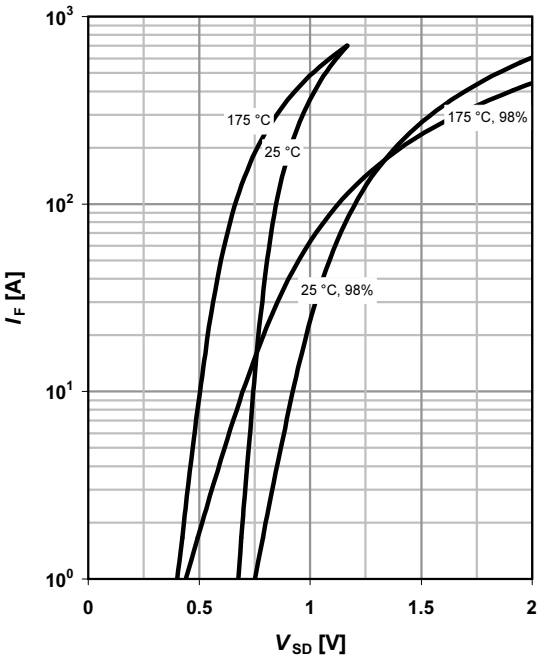
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

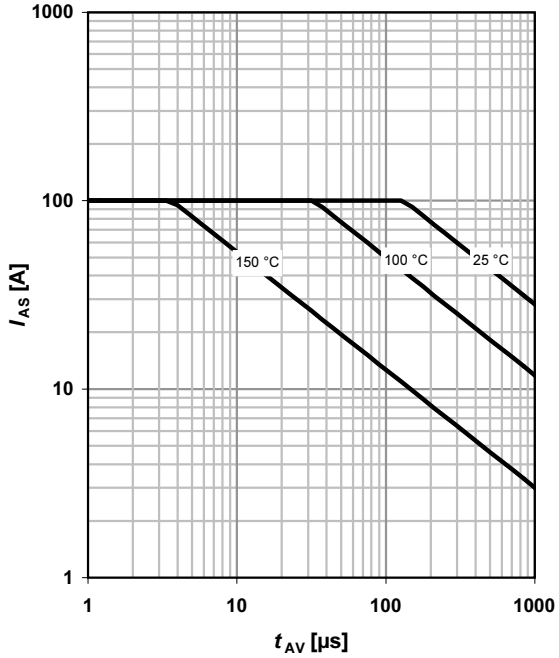
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

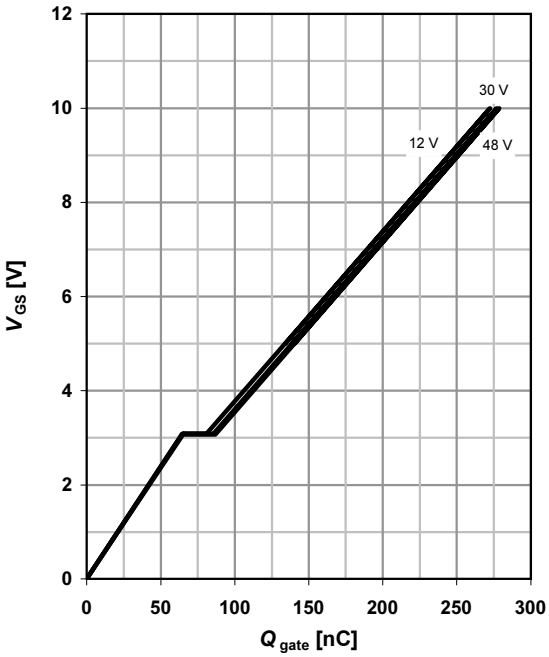
parameter: $T_{j(start)}$



14 Typ. gate charge

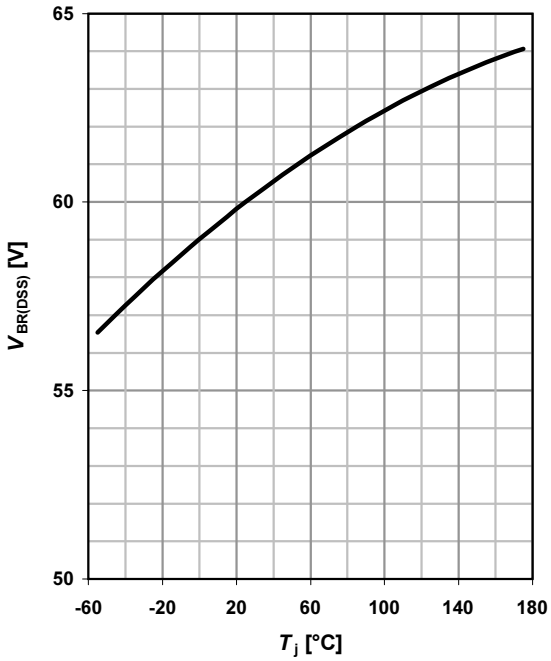
V_{GS}=f(Q_{gate}); I_D=100 A pulsed

parameter: V_{DD}

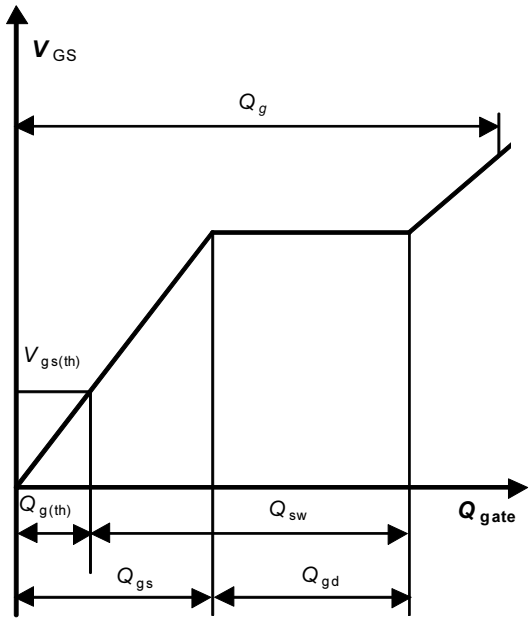


15 Drain-source breakdown voltage

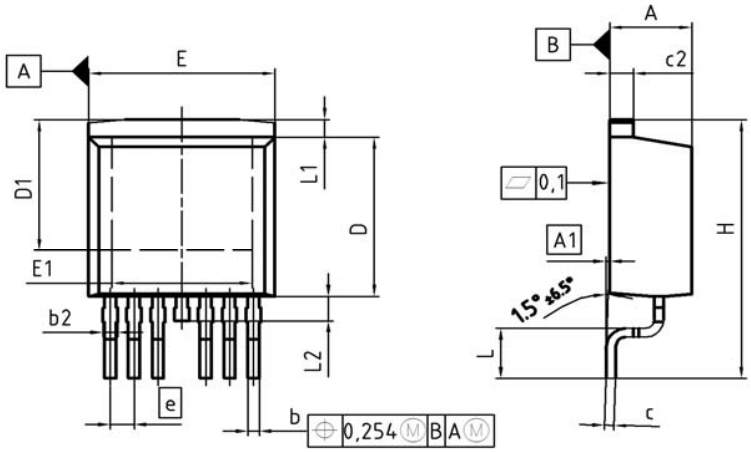
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

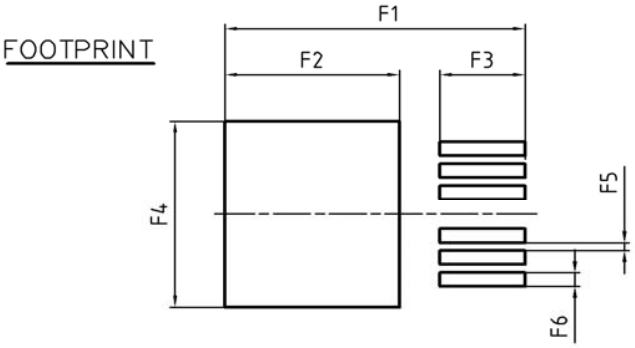


16 Gate charge waveforms



PG-TO-263-7 (D²-Pak 7pin)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.50	0.70	0.020	0.028
b2	0.50	1.00	0.020	0.039
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	6.90	7.90	0.272	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	1.27		0.050	
N	6		6	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	0.37	0.57	0.015	0.022
F6	0.70	0.90	0.028	0.035

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