Low Skew, ÷1/÷2, 3.3V LVPECL/ECL Clock Generator

87322BI

DATA SHEET

General Description

The 87322BI is a low skew, ÷1/÷2 3.3V LVPECL/ECL Clock Generator. Using multiplexed/redundant clock inputs the 87322BI is designed to translate most differential signal levels to LVPECL/ECL levels.

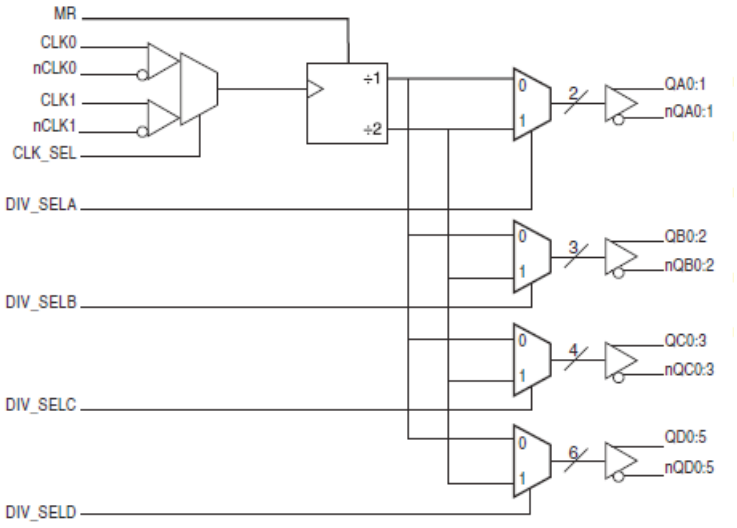
The CLK_SEL input selects between CLK0, nCLK0 and CLK1, nCLK1 as the active input. The divide select inputs, DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input can be used to reset the internal dividers and disable the clock outputs. Disabled outputs QAx, QBx, QCx and QDx will be forced low. Disabled outputs nQAx, nQBx, nQCx and nQDx will be forced high.

The 87322BI is characterized across the industrial temperature range and over the supply voltage range of 3V to 3.8V for LVPECL and -3.8V to -3V for LVECL/ECL. Guaranteed output and part to part skew characteristics make the 87322BI an excellent choice for clock generator and clock distribution applications demanding well defined performance and repeatability.

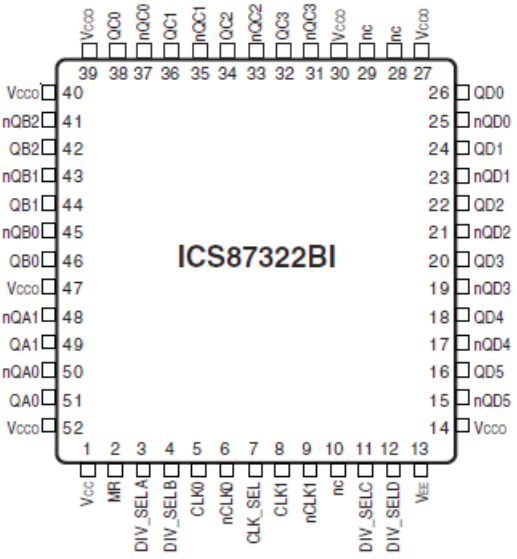
Features

- Fifteen differential LVPECL outputs
- Selectable LVPECL differential clock inputs
- CLK0, nCLK0 and CLK1, nCLK1 can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: 750MHz (maximum)
- Output skew: 180ps (maximum)
- Bank skew: 65ps (maximum)
- Part-to-part skew: 500ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 3V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -3V
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

Block Diagram



Pin Assignment



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

© 2019 Renesas Electronics Corporation

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CC}	Power		Core supply pin.
2	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
3	DIV_SELA	Input	Pulldown	Selects divide value for Bank A output as described in Table 3C. LVCMOS / LVTTL interface levels.
4	DIV_SELB	Input	Pulldown	Selects divide value for Bank B output as described in Table 3C. LVCMOS / LVTTL interface levels.
5	CLK0	Input	Pulldown	Non-inverting differential LVPECL clock input. LVPECL interface levels.
6	nCLK0	Input	Pullup	Inverting differential LVPECL clock input. LVPECL interface levels.
7	CLK_SEL	Input	Pulldown	Clock select. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levels.
8	CLK1	Input	Pulldown	Non-inverting differential LVPECL clock input. LVPECL interface levels.
9	nCLK1	Input	Pullup	Inverting differential LVPECL clock input. LVPECL interface levels.
10, 28, 29	nc	Unused		No connect.
11	DIV_SELC	Input	Pulldown	Selects divide value for Bank C output as described in Table 3C. LVCMOS / LVTTL interface levels.
12	DIV_SELD	Input	Pulldown	Selects divide value for Bank D output as described in Table 3C. LVCMOS / LVTTL interface levels.
13	V_{EE}	Power		Negative supply pin.
14, 27, 30, 39, 40, 47, 52	V_{CCO}	Power		Output supply pins.
15,16	nQD5, QD5	Output		Differential output pair. LVPECL interface levels.
17, 18	nQD4, QD4	Output		Differential output pair. LVPECL interface levels.
19, 20	nQD3, QD3	Output		Differential output pair. LVPECL interface levels.
21, 22	nQD2, QD2	Output		Differential output pair. LVPECL interface levels.
23, 24	nQD1, QD1	Output		Differential output pair. LVPECL interface levels.
25, 26	nQD0, QD0	Output		Differential output pair. LVPECL interface levels.
31, 32	nQC3, QC3	Output		Differential output pair. LVPECL interface levels.
33, 34	nQC2, QC2	Output		Differential output pair. LVPECL interface levels.
35, 36	nQC1, QC1	Output		Differential output pair. LVPECL interface levels.
37, 38	nQC0, QC0	Output		Differential output pair. LVPECL interface levels.
41, 42	nQB2, QB2	Output		Differential output pair. LVPECL interface levels.
43, 44	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
45, 46	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
48, 49	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
50, 51	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

© 2019 Renesas Electronics Corporation

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLKx, nCLKx			2		pF
		CLK_SEL, DIV_SELx, MR			4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ

Table 3A. Output Control Pin Function Table

Inputs		Outputs							
MR	CLK_SEL	QA0:QA1	nQA0:nQA1	QB0:QB2	nQB0:nQB2	QC0:QC3	nQC0:nQC3	QD0:QD5	nQD0:nQD5
1	X	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH
0	0	Active	Active	Active	Active	Active	Active	Active	Active
0	1	Active	Active	Active	Active	Active	Active	Active	Active

Table 3B. Input Control Function Table

Inputs	
CLK_SEL	Clock Input
0	CLK0, nCLK0
1	CLK1, nCLK1

Table 3C. Select Pin Function Table

Inputs				Outputs			
SEL_A	SEL_B	SEL_C	SEL_D	QAx	QBx	QCx	QDx
0	0	0	0	÷ 1	÷ 1	÷ 1	÷ 1
1	1	1	1	÷ 2	÷ 2	÷ 2	÷ 2

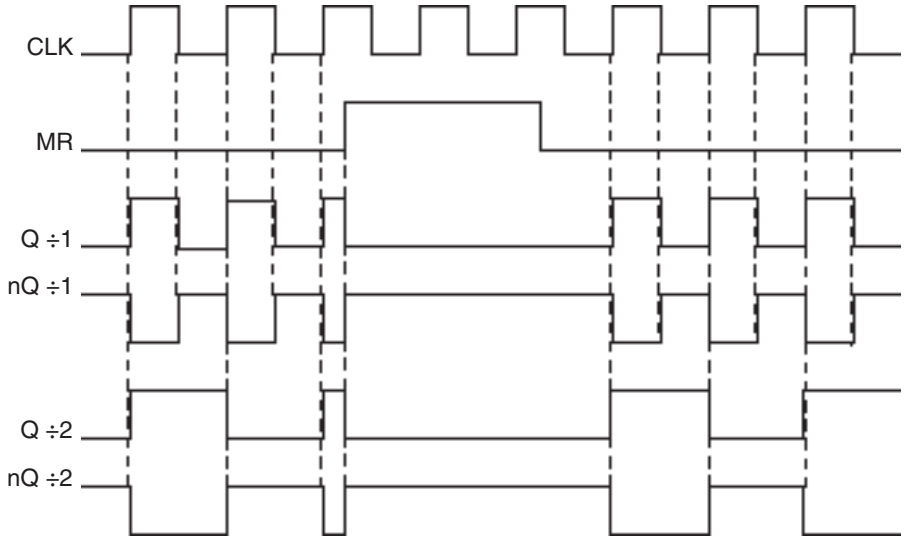


Figure 1. Timing Diagram

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO}$ = 3V to 3.8V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.0	3.3	3.8	V
V_{CCO}	Output Supply Voltage		3.0	3.3	3.8	V
I_{EE}	Power Supply Current				160	mA
I_{CCO}	Output Supply Current				98	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO}$ = 3V to 3.8V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	MR, CLK_SEL, F_SELA:F_SELD		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	MR, CLK_SEL, F_SELA:F_SELD				0.8	V
I_{IH}	Input High Current	MR, CLK_SEL, F_SELA:F_SELD	$V_{CC} = V_{IN}$ = 3.8V			150	µA
I_{IL}	Input Low Current	MR, CLK_SEL, F_SELA:F_SELD	V_{IN} = 0V, V_{CC} = 3.8V	-5			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCO}$ = 3V to 3.8V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{CC} = V_{IN}$ =3.8V			150	µA
		nCLK0, nCLK1	$V_{CC} = V_{IN}$ =3.8V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{IN} = 0V, V_{CC} = 3.8V	-5			µA
		nCLK0, nCLK1	V_{IN} = 0V, V_{CC} = 3.8V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 1.5		V_{CC}	V
V_{OH}	Output High Voltage, NOTE 3			V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage, NOTE 3			V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, CLK1 is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50W to V_{CCO} - 2V.

© 2019 Renesas Electronics Corporation

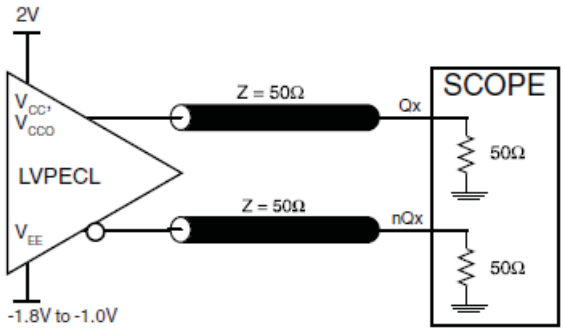
TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3V$ TO $3.8V$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				750	MHz
t_{PD}	Propagation Delay; NOTE 1		1.5		2.7	ns
tsk(o)	Output Skew; NOTE 2, 5				180	ps
		f = 212MHz			150	ps
tsk(b)	Bank Skew; NOTE 3, 5				65	ps
tsk(pp)	Part-to-Part Skew; NOTE 4, 5				500	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		600	ps

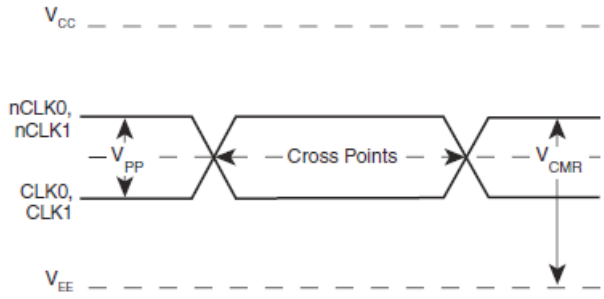
All parameters measured at $f \leq 750$MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2:Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CCO}/2$.
NOTE 3: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{CCO}/2$.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

© 2019 Renesas Electronics Corporation

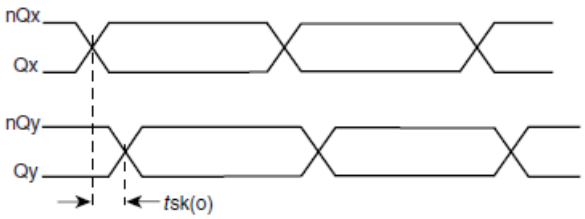
PARAMETER MEASUREMENT INFORMATION



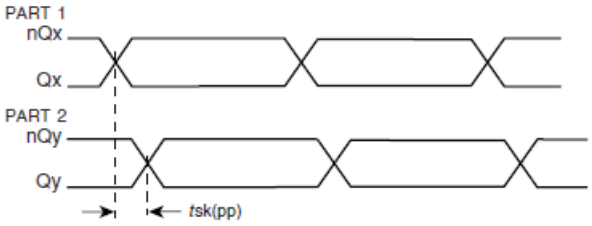
OUTPUT LOAD AC TEST CIRCUIT



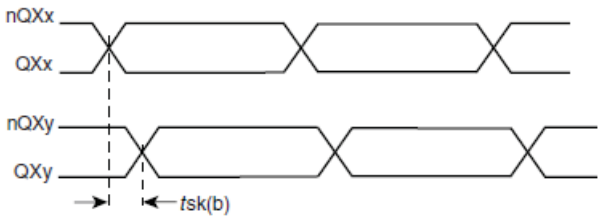
DIFFERENTIAL INPUT LEVEL



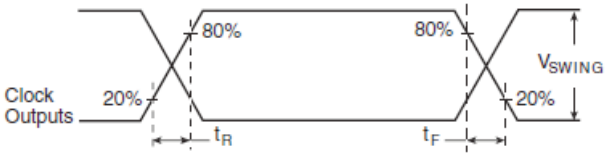
OUTPUT SKEW



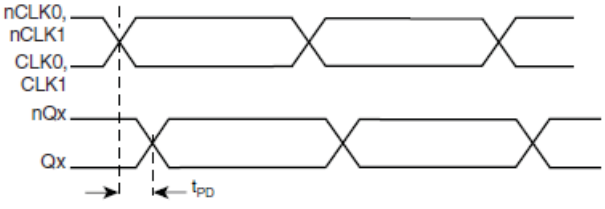
PART-TO-PART SKEW



BANK SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

© 2019 Renesas Electronics Corporation

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

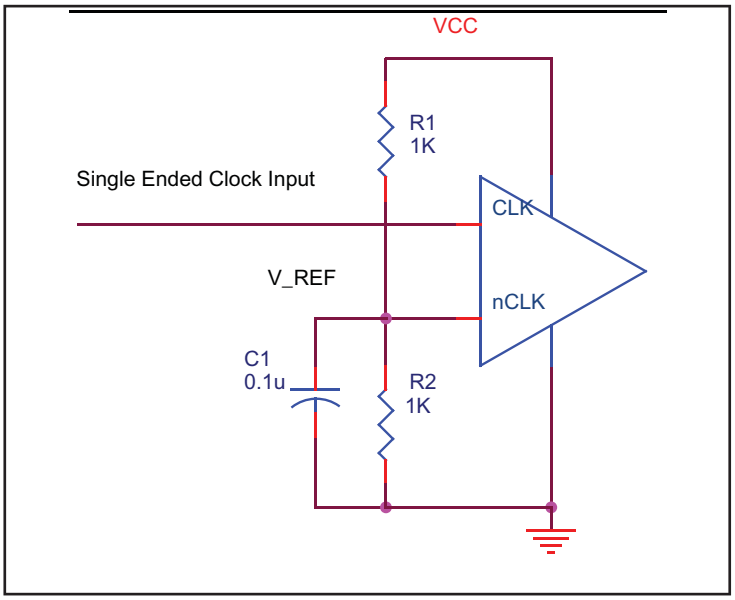


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

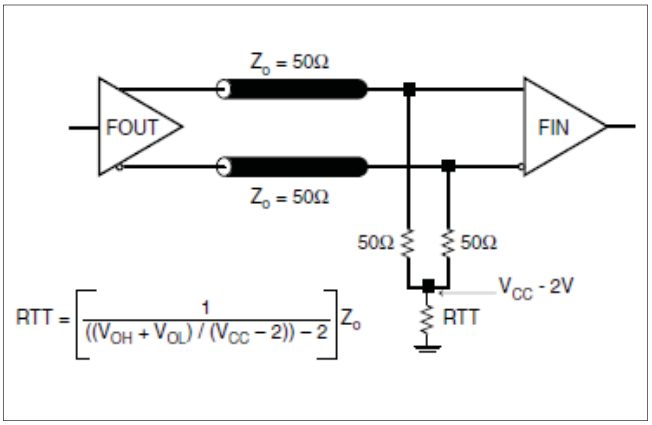


FIGURE 3A. LVPECL OUTPUT TERMINATION

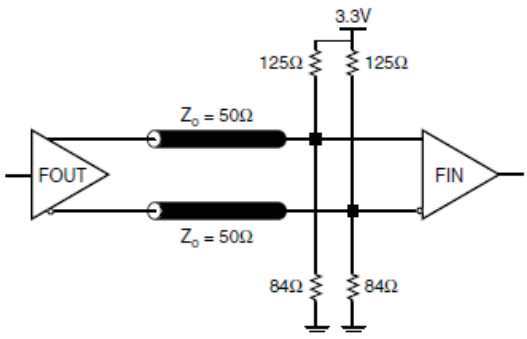


FIGURE 3B. LVPECL OUTPUT TERMINATION

© 2019 Renesas Electronics Corporation

LVPECL Clock Input Interface

The CLK /nCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

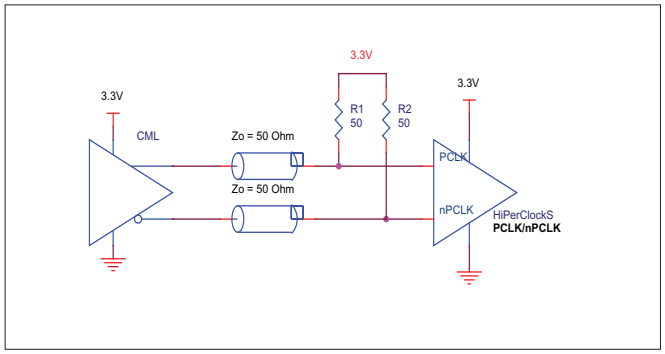


Figure 4A. CLK/nCLK Input Driven by a CML Driver

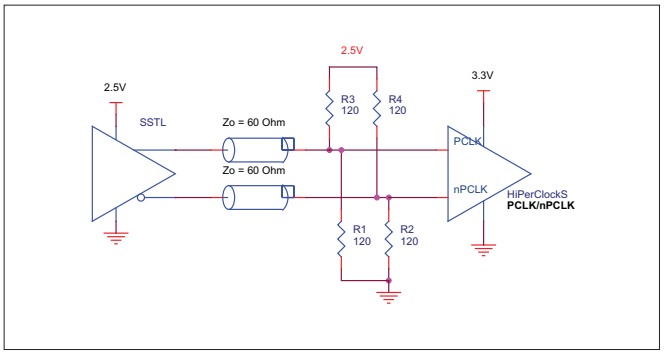


Figure 4B. CLK/nCLK Input Driven by an SSTL Driver

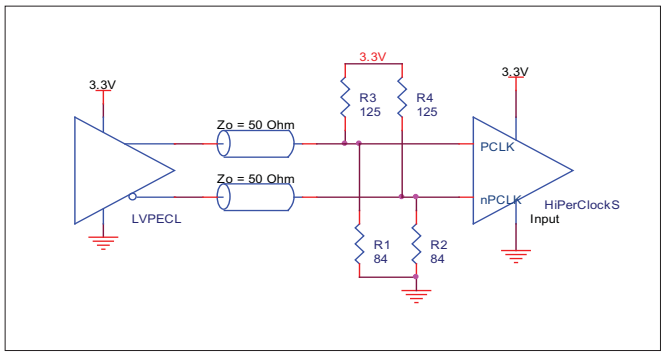


Figure 4C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

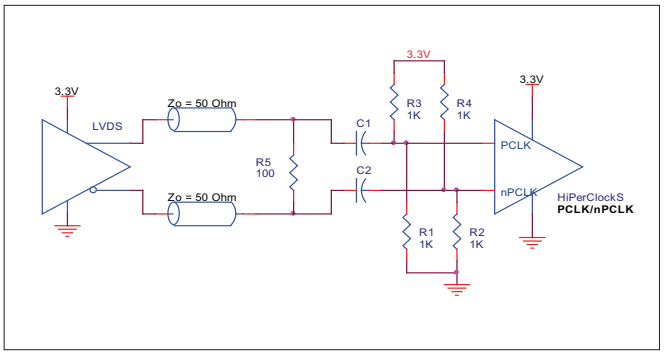


Figure 4D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

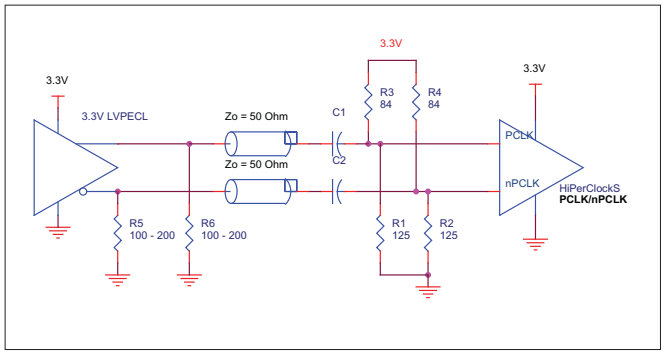


Figure 4E. CLK/nCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

© 2019 Renesas Electronics Corporation

Schematic Example

Figure 5 shows a schematic example of the 87322BI. In this example, the CLK0/nCLK0 input is selected. The input is driven by an LVPECL driver. All banks are set at ÷2. The decoupling capacitors should be physically located near the power pin. For 87322BI, the unused outputs can be left floating.

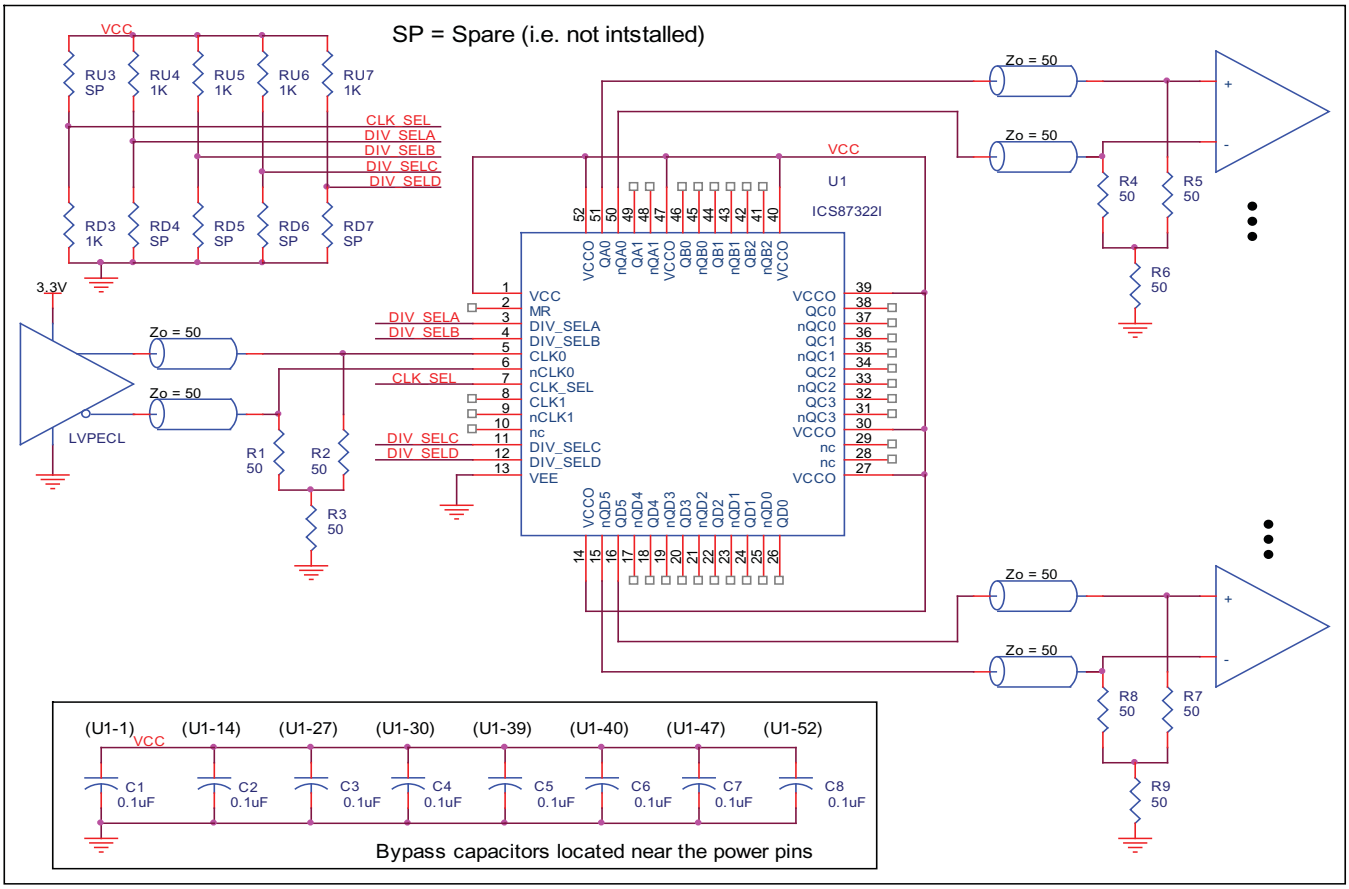


Figure 5. 87322BI Schematic Example

© 2019 Renesas Electronics Corporation

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 87322BI.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 87322BI is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.8V * 160mA = **608mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 15 * 30mW = **450mW**

Total Power$_{_MAX}$ (3.8V, with all outputs switching) = 608mW + 450mW = **1058mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 36.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 1.058W * 36.4°C/W = 123.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 52-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

© 2019 Renesas Electronics Corporation

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

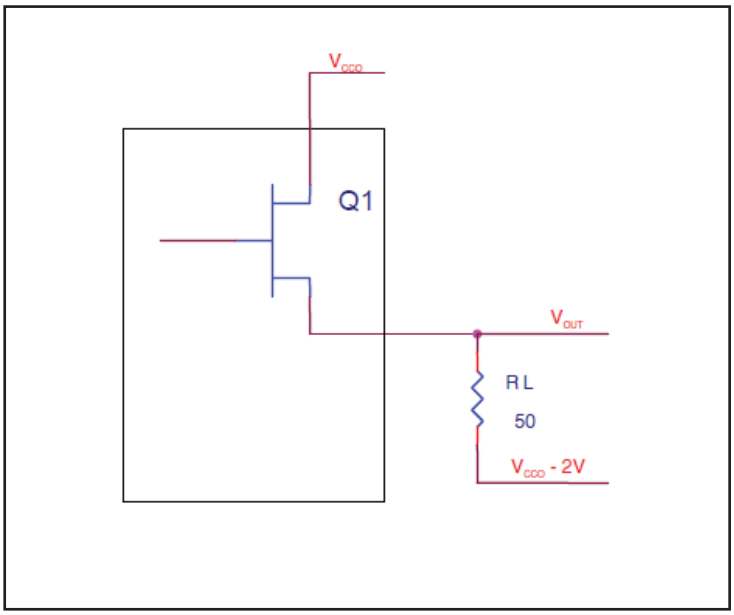


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CCO_MAX} – 0.9V}$

  $(V_{CCO_MAX} - V_{OH_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CCO_MAX} – 1.7V}$

  $(V_{CCO_MAX} - V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

© 2019 Renesas Electronics Corporation

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 87322BI is: 1331

© 2019 Renesas Electronics Corporation

Package Outline - Y Suffix for 52 Lead LQFP

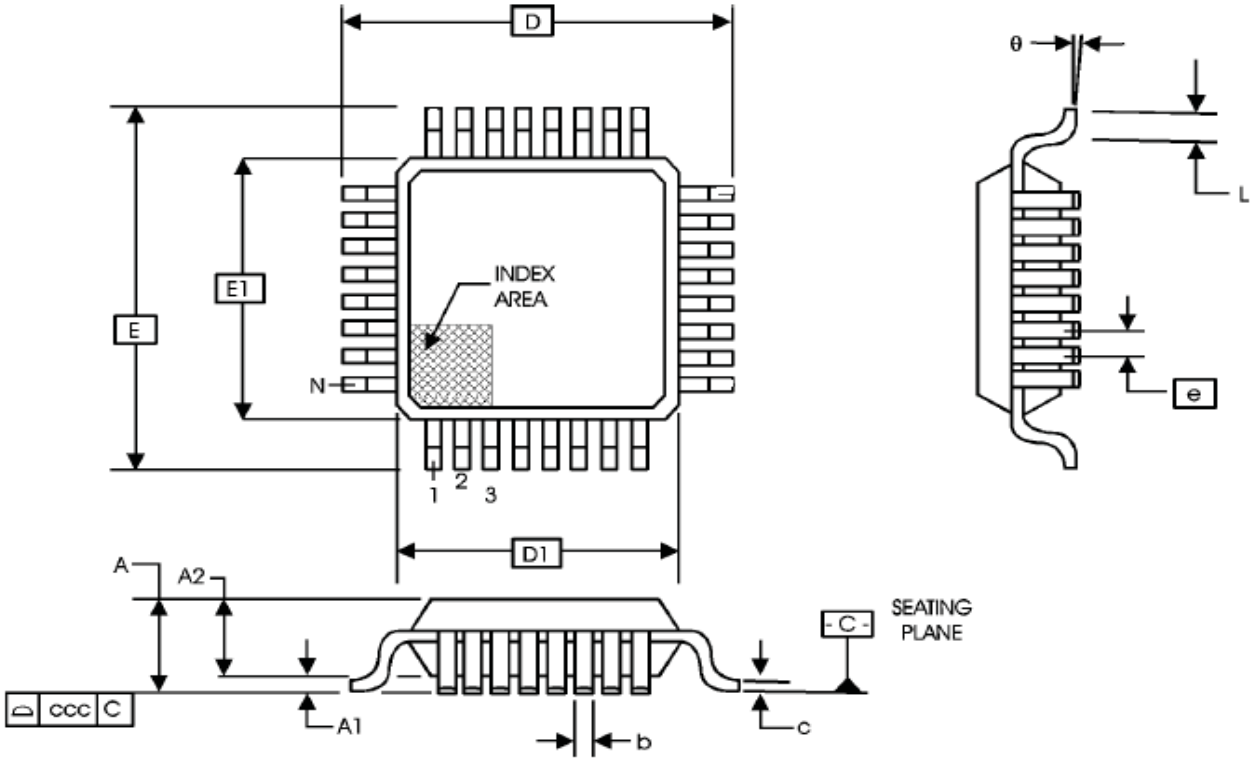


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

© 2019 Renesas Electronics Corporation

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87322BYILF	ICS87322BYILF	52 Lead “Lead-Free” LQFP	tray	-40°C to 85°C
87322BYILFT	ICS87322BYILF	52 Lead “Lead-Free” LQFP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” to the part number are the Pb-Free configuration and are RoHS compliant.

© 2019 Renesas Electronics Corporation

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4A T4B T4C T5B	 4 4 4 5 6 8 9	Changed input levels to LVPECL throughout data sheet. Changed operating supply range from 2.375V to 3V throughout data sheet. Power Supply table - changed V_{CC} & V_{CCO} from 2.375V min. to 3V min. LVCMOS table - deleted 2.625V test conditions. Changed Differential table to a LVPECL table. Deleted 2.625V test conditions. Revised V_{CMR} min. from V_{EE} + 0.5V to V_{EE} + 1.5V and max. from V_{CC} - 0.85V to V_{CC}. Deleted Table 5B, 2.5V AC Characteristics table. Revised Output Load AC Test Circuit Diagram, V_{EE}. Deleted Termination for 2.5V LVPECL Output. Changed Differential Clock Input Interface to LVPECL Clock Input Interface. (Now page 8.)	4/6/04
B	T2 T9	1 2 14	Features section - added Lead-Free bullet. Pin Description Table - added pin 30 (V_{CCO}). Ordering Information Table - added Lead-Free part number.	5/11/05
B	T9	14	Ordering Information Table - added Lead-Free marking.	6/9/05
B		6	Corrected Output Load AC Test Circuit Diagram - V_{EE} = -1.8V to 1.0V from ...to -0.375V.	6/20/05
C	T4C	4 10 - 11	LVPECL DC Characteristics Table -corrected V_{OH} max. from V_{CCO} - 1.0V to V_{CCO} - 0.9V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 4C.	4/13/07
C	T9	14 16	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	10/13/10
C	T9	14	Ordering Information - Removed leaded devices. Updated data sheet format.	11/16/15

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.