For Automotive, 40 V 150 mA 4ch Constant Current LED Driver

BD18347AEFV-M

General Description

BD18347AEFV-M are 40 V-withstanding constant current LED driver for automotive applications. It is a 4 channel LED driver with the built-in energy sharing control which can realize to make the board size small. High reliability can be realized with LED Open Detection, the OUTx (all later x=1 to 4) pin Short Circuit Protection, Over Voltage Mute and Thermal Shutdown Function.

Key Specifications

- Input Voltage Range: 5.5 V to 20.0 V
- Maximum Output Current: 150 mA/ch
- Output Current Accuracy: ±5 %
- Relative Channel Accuracy: ±5 %
- Operating Temperature Range: -40 °C to +125 °C

Package

	W (Typ) x D (Typ) x H (Max)
HTSSOP-B16	5.00 mm x 6.40 mm x 1.00 mm

Features

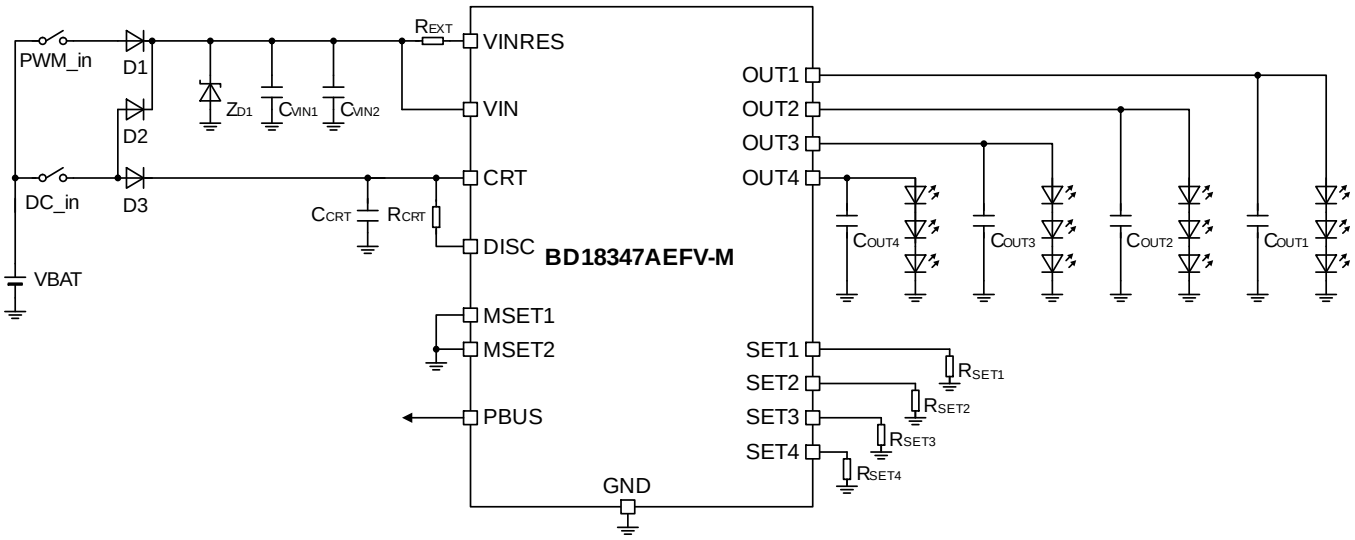
- AEC-Q100 Qualified(Note 1)
- Functional Safety Supportive Automotive Products
- Energy Sharing Control
- PWM Dimming Function
- License Lamp Mode
- LED Open Detection
- OUTx pin Short Circuit Protection (SCP)
- Over Voltage Mute Function (OVM)
- Disable LED Open Detection Function at Reduced-Voltage
- LED Failure Input / Output Functions (PBUS)

(Note 1) Grade1

Applications

- Automotive LED Exterior Lamp (Rear Lamp, License Lamp, DRL / Position Lamp, Fog Lamp etc.)
- Automotive LED Interior Lamp (Air Conditioner Lamp, Interior Lamp, Cluster Light etc.)

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

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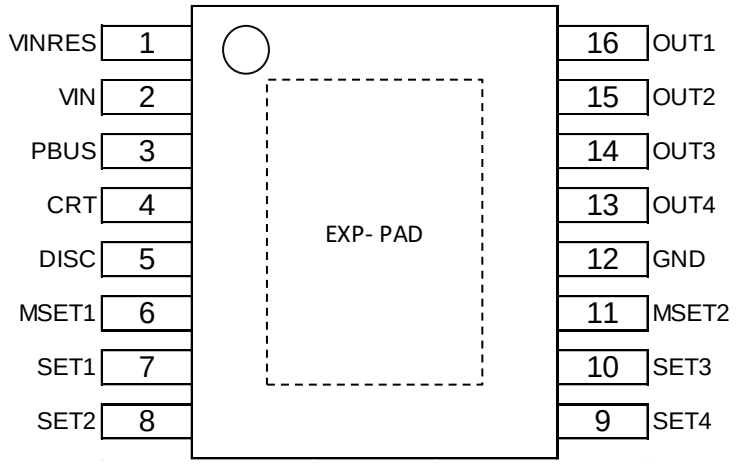
Pin Configuration



(TOP VIEW)

Pin Description

Pin No.	Pin Name	Function
1	VINRES	Energy sharing external resistor connection*(Note 1)*
2	VIN	Supply voltage input
3	PBUS	Output for fault flag / Input to disable output current
4	CRT	CR TIMER setting1*(Note 2)*
5	DISC	CR TIMER setting2*(Note 3)*
6	MSET1	Mode setting pin 1
7	SET1	Output current setting pin 1
8	SET2	Output current setting pin 2
9	SET4	Output current setting pin 4
10	SET3	Output current setting pin 3
11	MSET2	Mode setting pin 2
12	GND	GND
13	OUT4	Current output pin 4
14	OUT3	Current output pin 3
15	OUT2	Current output pin 2
16	OUT1	Current output pin 1
-	EXP-PAD	The EXP-PAD connect to GND.

(Note 1) Short the VINRES pin to the VIN pin when not in use.
(Note 2) Short the CRT pin to the VIN pin when not in use.
(Note 3) Open the DISC pin or connect it to GND when not in use.

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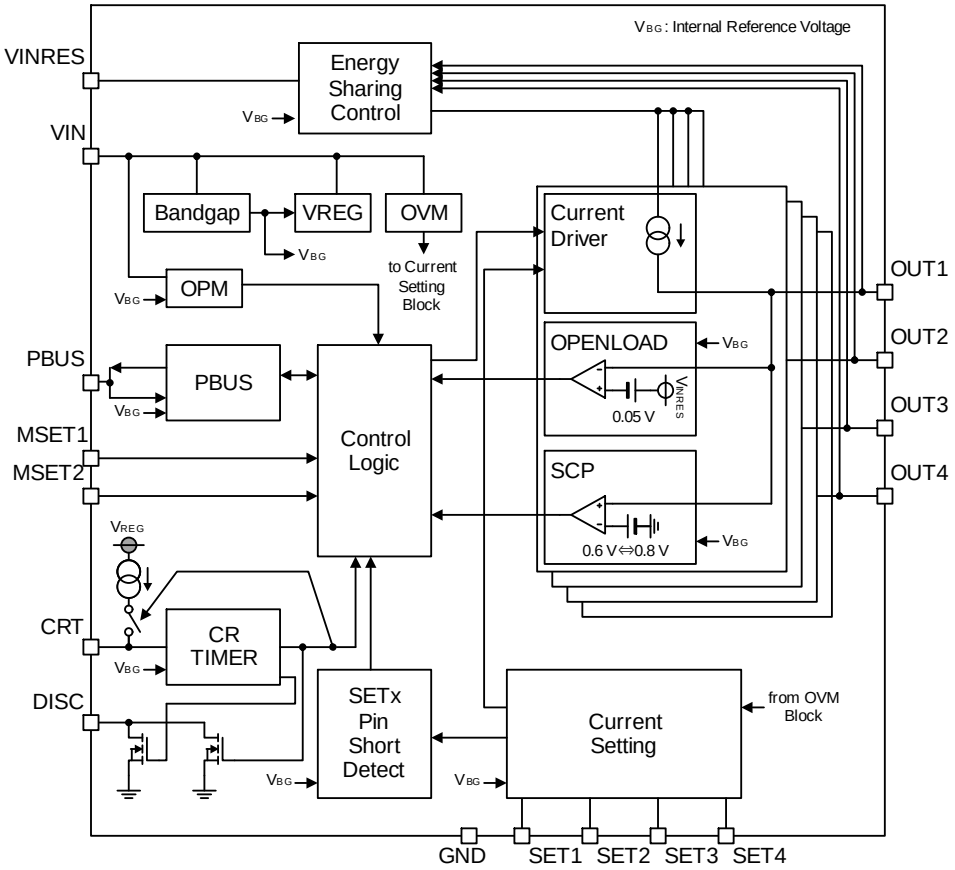
Block Diagram



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Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage (VIN)	V_{IN}	-0.3 to +40.0	V
Supply Voltage (VINRES)	V_{INRES}	-0.3 to +40.0 < V_{IN}	V
VIN to VINRES Pin Voltage	V_{VIN_VINRES}	-0.3 to +10.0	V
CRT, DISC Pin Voltage	V_{CRT}, V_{DISC}	-0.3 to +40.0	V
MSET1, MSET2 Pin Voltage	V_{MSET1}, V_{MSET2}	-0.3 to +20.0	V
OUT1,OUT2,OUT3,OUT4 Pin Voltage	V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}	-20.0 to V_{IN}+0.3V	V
VIN-OUTx Pin between Voltage	V_{IN_OUTx}	-0.3 ~ +40.0	V
PBUS Pin Voltage	V_{PBUS}	-0.3 to +20.0	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance(Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
HTSSOP-B16				
Junction to Ambient	θ_{JA}	113	36	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	13	9	°C/W

(Note 1) Based on JESD51-2A(Still-Air), using a BD18347AEFV-M Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (VIN)*(Note 1)*	V_{IN}	5.5	13.0	20.0	V
Output Current (each channel)	I_{OUTx}	-	-	150	mA
CR Timer Frequency	f_{PWM}	-	-	750	Hz
PWM Minimum Pulse Width	t_{MIN}	100	-	-	μs
Operating Temperature	Topr	-40	-	+125	°C

(Note 1) ASO should not be exceeded.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Capacitor Connecting VIN Pin 1	C_{VIN1}*(Note 2)*	1.0	-	μF
Capacitor Connecting VIN Pin 2	C_{VIN2}*(Note 2)*	0.047	-	μF
Capacitor Connecting LED Anode	C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}*(Note 2)*	0.01	0.47	μF
Capacitor for Setting CR Timer	C_{CRT}*(Note 2)*	0.01	0.22	μF
Resistor for Setting CR Timer	R_{CRT}	0.1	50	kΩ
Resistor for Setting Output Current	R_{SET1}, R_{SET2}, R_{SET3}, R_{SET4}	12	36	kΩ

(Note 2) Recommended ceramic capacitor.

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Electrical Characteristics (Unless otherwise specified, Ta=-40 °C to +125 °C, V_{IN}=13 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Circuit Current I_{VIN}]						
Circuit Current in Normal Mode	I_{VIN1}	-	4.0	7.0	mA	
Circuit Current when LED Open is Detected	I_{VIN2}	-	4.0	7.0	mA	at LED Open Detection
Circuit Current when PBUS is Low	I_{VIN3}	-	4.0	7.0	mA	V_{PBUS}=0 V
[Output Current I_{OUTx}]						
OUTx OFF Current	I_{OUTx_OFF}	-	-	1	µA	V_{CRT}=0 V, Ta=25 °C
VINRES-OUTx Pin Drop Voltage	V_{DR}	-	-	1.0	V	I_{OUTx}=100 mA
LED Open Detection Output Current	I_{OUTx_OPEN}	-	-	10	mA	V_{OUTx}=V_{INRES}-100 mV
[Energy Sharing Control]						
Energy Sharing Control Voltage	V_{ES}	1.0	1.5	2.5	V	V_{INRES}-V_{OUTx_MAX}, V_{IN}=13 V, V_{OUTx}=9 V
ON Resistance Between the VIN Pin and the VINRES Pin	R_{VIN_VINRES}	-	0.5	1.0	Ω	I_{VIN}=100 mA
[LED Open Detection]						
OUTx Pin LED Open Detection Voltage	V_{OPD}	20	50	100	mV	V_{INRES}-V_{OUTx}
[Disable LED Open Detection Function at Reduced-Voltage]						
VIN Pin Voltage	V_{IN_OPM}	7.30	7.65	8.00	V	
[OUTx pin Short Circuit Protection (SCP)]						
OUTx Pin Short Circuit Current	I_{OUTx_SCP}	0.1	0.3	1.0	mA	V_{OUTx}=0.9 V
OUTx Pin Short Circuit Protection Detection Voltage	V_{SCP}	1.1	1.2	1.3	V	
OUTx Pin Short Circuit Protection Release Voltage	V_{SCPR}	1.2	1.3	1.4	V	
SCP Detect Delay Time 1	t_{SCPD1}	10	60	150	µs	Refer to Figure 17
SCP Detect Delay Time 2	t_{SCPD2}	-	20	-	µs	Refer to Figure 17
SCP Release Delay Time	t_{SCPR}	-	40	-	µs	Refer to Figure 17
SCP Protection Disable Time at Power On	t_{SCPPON}	-	140	-	µs	Refer to Figure 17
[Output Current Setting]						
Output Current Setting Coefficient	K_{SET}	1710	1800	1890	-	R_{SETx}=12 kΩ to 18 kΩ, I_{OUTx}=K_{SET} / R_{SETx} [A]
		1620	1800	1980	-	R_{SETx}=18 kΩ to 36 kΩ, I_{OUTx}=K_{SET} / R_{SETx} [A]
SETx Pin Voltage	V_{SETx}	1.08	1.20	1.32	V	
SETx Pin Short Detection Resistance	R_{SETx_SHORT}	1.0	2.4	5.0	kΩ	

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Electrical Characteristics – continued (Unless otherwise specified, Ta=-40 °C to +125 °C, V_{IN}=13 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[CR TIMER]						
CRT Pin Charge Current	I_{CRT}	36	40	44	µA	
CRT Pin Charge Voltage	V_{CRT_CHA}	0.72	0.80	0.88	V	
CRT Pin Discharge Voltage 1	V_{CRT_DIS1}	1.80	2.00	2.20	V	
CRT Pin Discharge Voltage 2	V_{CRT_DIS2}	2.10	2.40	3.00	V	V_{CRT} > V_{CRT_DIS2} R_{DISC1} → R_{DISC2}
CRT Pin Charge Resistance	R_{CHA}	28.5	30.0	31.5	kΩ	
CRT Discharge Constant	V_{CRT_CHA} / V_{CRT_DIS1}	0.38	0.4	0.42	V / V	
DISC Pin ON Resistance 1	R_{DISC1}	20	50	100	Ω	I_{DISC}=10 mA
DISC Pin ON Resistance 2	R_{DISC2}	2.5	5	10	kΩ	I_{DISC}=100 µA
CRT Pin Leakage Current	I_{CRT_LEAK}	-	-	10	µA	V_{CRT}=V_{IN}
[Over Voltage Mute Function (OVM)]						
Over Voltage Mute Start Voltage	V_{OVMS}	20.0	22.0	24.0	V	ΔI_{OUTx}=-3 % ΔI_{OUTx}= I_{OUTx} (@V_{IN}=V_{OVM}) / I_{OUTx} (@V_{IN}=13 V) -1
Over Voltage Mute Gain	I_{OVMG}	-	-20	-	%/V	ΔI_{OUTx} / ΔV_{IN}
[PBUS]						
Input High Voltage	V_{PBUSH}	2.4	-	-	V	
Input Low Voltage	V_{PBUSL}	-	-	0.6	V	
PBUS Pin Source Current	I_{PBUS}	75	150	300	µA	
PBUS Pin Output Low Voltage	V_{PBUS_OL}	-	-	0.6	V	Source 3 mA to the PBUS pin
PBUS Pin Output High Voltage	V_{PBUS_OH}	3.5	4.5	5.5	V	Sink 10 µA from the PBUS pin
PBUS Pin Leakage Current	I_{PBUS_LEAK}	-	-	10	µA	V_{PBUS}=7 V
[UVLO VIN]						
UVLO VIN Detection Voltage	V_{UVLO_VIND}	4.50	4.75	5.00	V	V_{IN}: Sweep down
UVLO VIN Release Voltage	V_{UVLO_VINR}	5.00	5.25	5.50	V	V_{IN}: Sweep up
[UVLO VINRES]						
UVLO VINRES Detection Voltage	$V_{UVLO_VINRESD}$	1.25	1.50	1.75	V	V_{INRES}: Sweep down
UVLO VINRES Release Voltage	$V_{UVLO_VINRESR}$	1.75	2.00	2.25	V	V_{INRES}: Sweep up
[MSET1, MSET2]						
MSET1, MSET2 Input H Voltage	V_{MSETH}	2.4	-	-	V	
MSET1, MSET2 Input L Voltage	V_{MSETL}	-	-	0.6	V	
MSET1, MSET2 Pin Outflow Current	I_{MSET}	25	50	100	µA	V_{MSET1}=0 V, V_{MSET2}=0 V

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Typical Performance Curves (Reference Data)
(Unless otherwise specified, Ta=25 °C, V_{IN}=13 V)

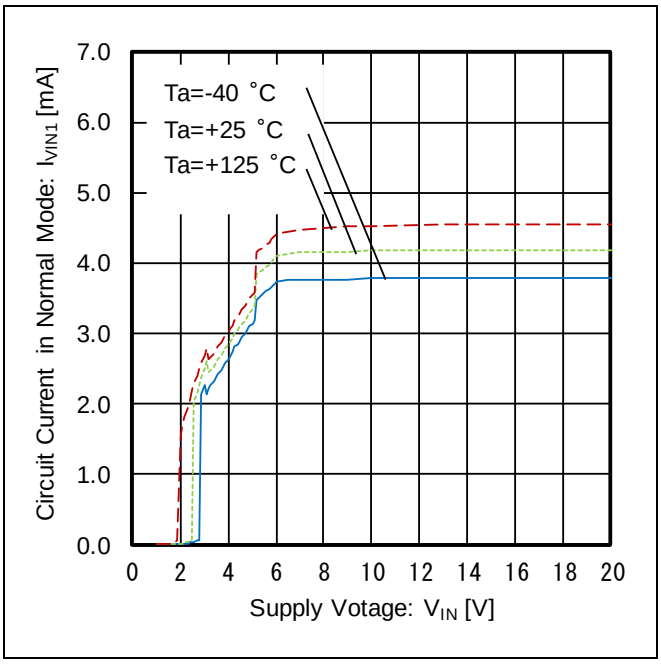

Figure 1. Circuit Current in Normal Mode vs Supply Voltage

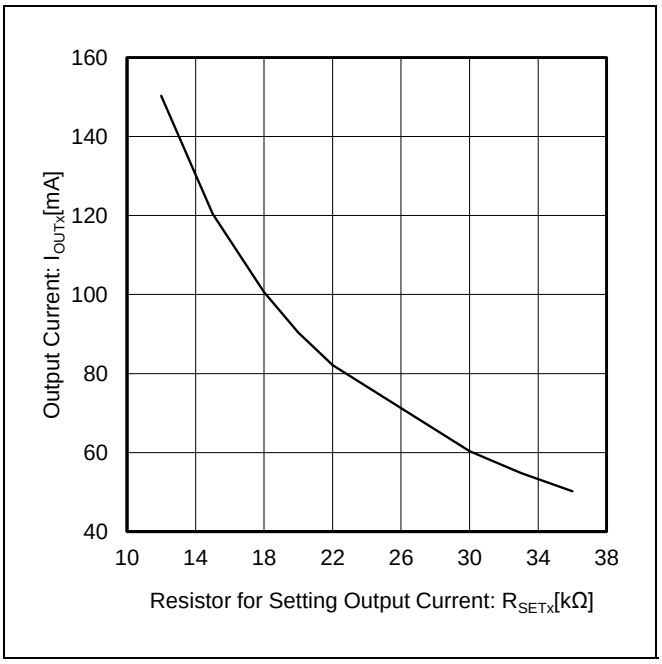

Figure 2. Output Current vs Resistor for Setting Output Current

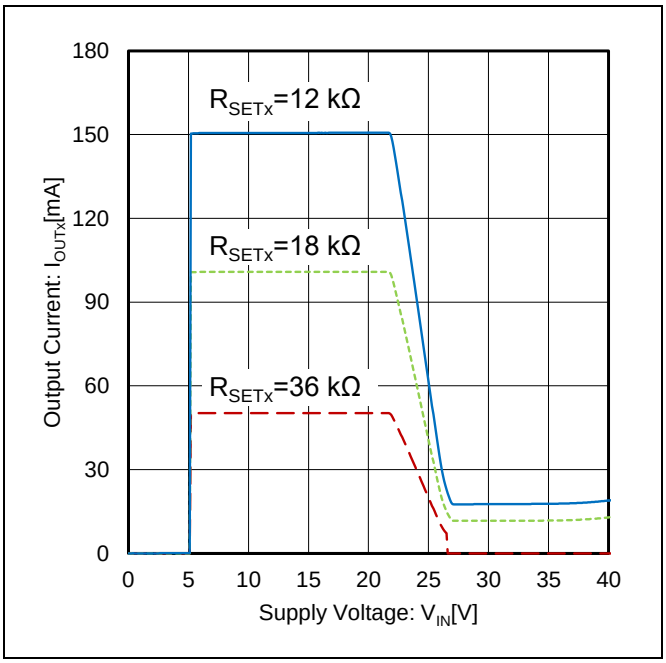

Figure 3. Output Current vs Supply Voltage

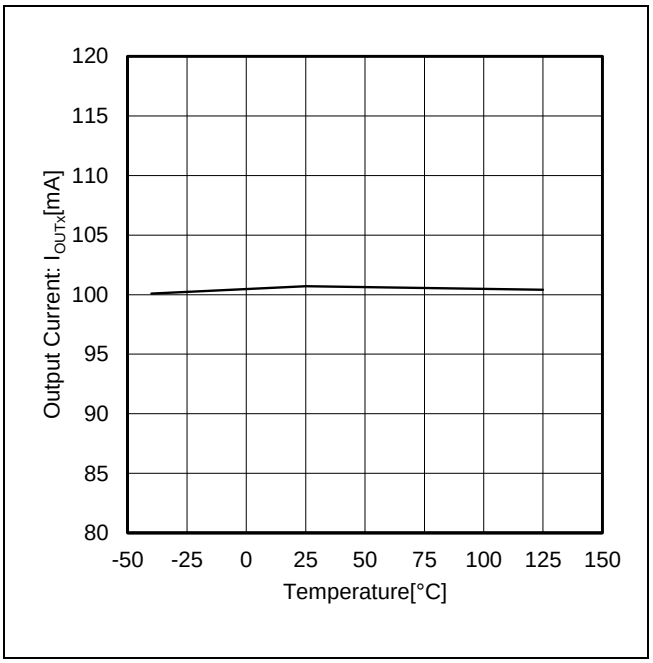

Figure 4. Output Current vs Temperature

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Typical Performance Curves (Reference Data) – continued
(Unless otherwise specified, Ta=25 °C, V_{IN}=13 V)

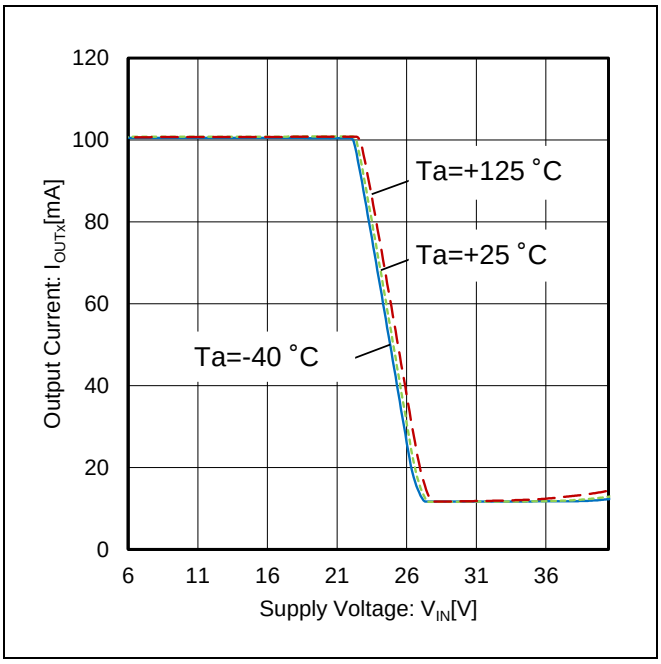

Figure 5. Output Current vs Supply Voltage

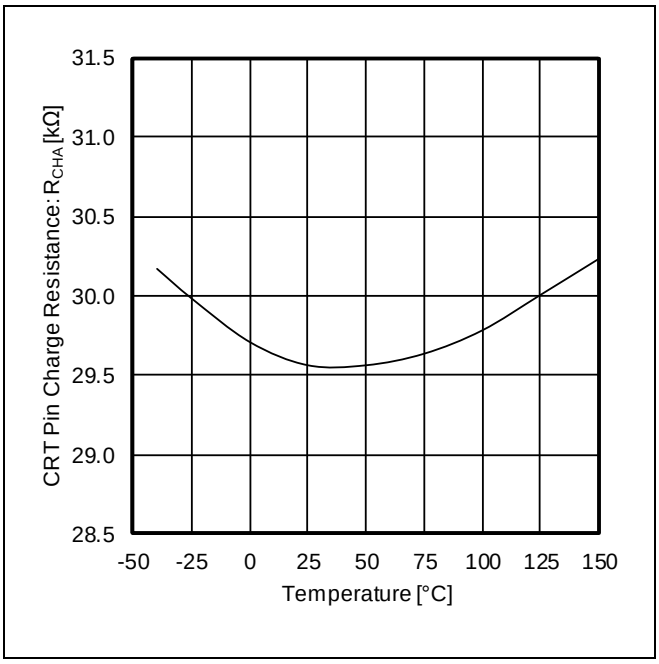

Figure 6. CRT Pin Charge Resistance vs Temperature

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Description of Function

(Unless otherwise specified, Ta=25 °C, V_{IN}=13 V)

1. Output Current Setting and Power Control

Output current I_{OUTx} can be set by the value of the output current setting resistor R_{SETx}.

$$I_{OUTx} = \frac{K_{SET}}{R_{SETx}} \quad [A]$$

where:
K_{SET} is the output current setting coefficient 1800 (Typ).
R_{SETx} is the output current setting resistor.

When not to use the OUTx pin, open the SETx pin.

●Required V_{IN} for set current to flow

Output Current I_{OUTx} and minimum V_{IN} should be set to satisfy the following relationship.

$$V_{IN} \geq V_{f_LED} \times N + V_{DR} + R_{VIN_VINRES} \times I_{OUTx_TOTAL} \quad [V]$$

where:

V_{IN}	is the VIN pin voltage.
V_{f_LED}	is the LED forward voltage.
N	is the number of LED.
V_{DR}	is the VINRES - OUTx drop voltage.
R_{VIN_VINRES}	is the ON resistance between the VIN pin and the VINRES pin.
I_{OUTx_TOTAL}	is the total output current.

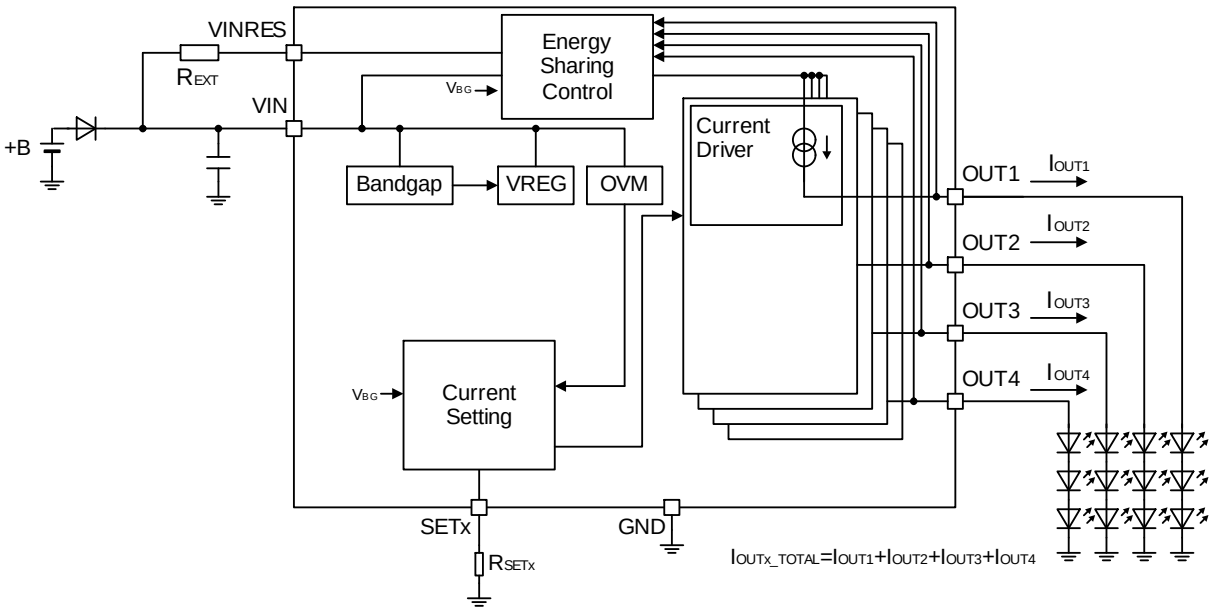

Figure 7. Output Current Setting

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Description of Function – continued

2. Energy Sharing Control

Energy sharing is performed by connecting external resistor R_{EXT} between the VIN and VINRES pins. It makes possible to distribute the heat generated by the IC to R_{EXT}. (When not in use, short the VINRES pin with the VIN pin.)
The IC controls the difference voltage to V_{ES} (1.5 V(Typ)) which is between the VINRES pin and the pin that has maximum voltage among OUT1 to OUT4 pins.
Insert resistor in the anode of the LED, when the following expression is not satisfied.

$$V_{UVLO_VINRESR} \leq V_{OUTx_MAX} + V_{ES}$$

$$V_{OUTx} = I_{OUTx} \times R_{OUTx} + V_{f_LED} \times N$$

where:

$V_{UVLO_VINRESR}$	is the VINRES pin UVLO release voltage, 2.00 V (Typ).
V_{OUTx_MAX}	is the maximum voltage among the OUT1 to OUT4 pins
V_{ES}	is the Energy Sharing control voltage, 1.5 V (Typ).
V_{OUTx}	is the OUTx pin voltage.
I_{OUTx}	is the OUTx pin current.
R_{OUTx}	is the resistor inserted in the anode of LED.
V_{f_LED}	is the LED forward voltage.
N	is the number of LED.

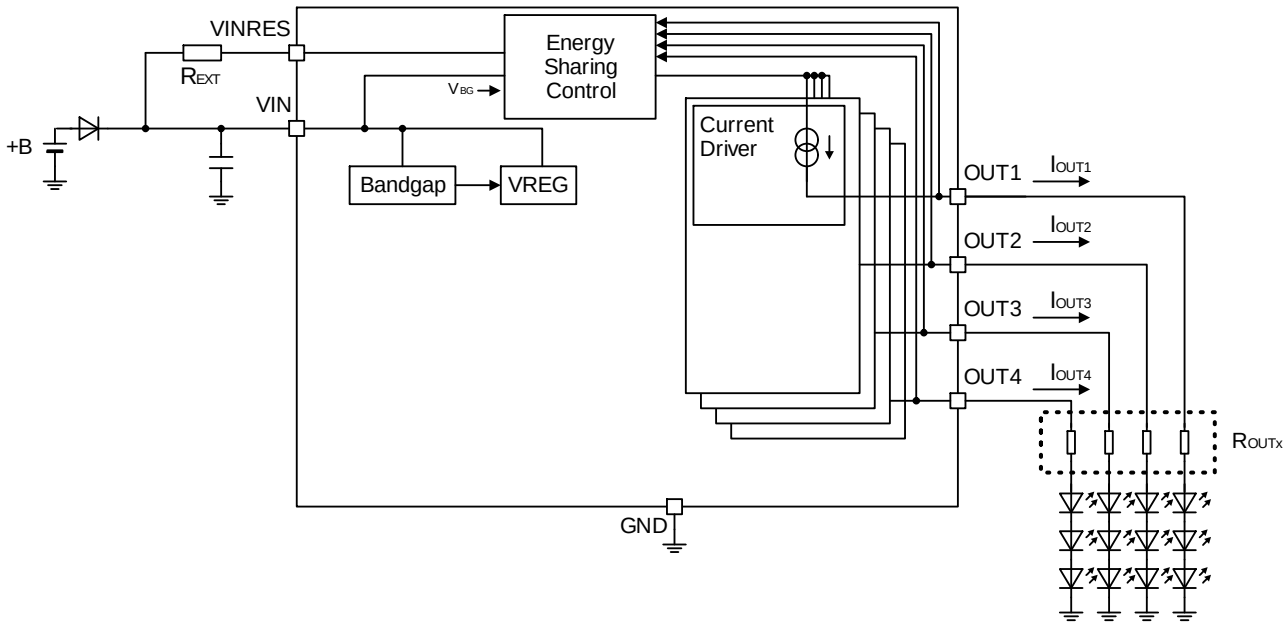

Figure 8. Energy Sharing Control

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2. Energy Sharing Control – continued

The power consumption(Pc) across the IC and R_{EXT} when I_{OUT_TOTAL}=200 mA, V_{OUTx}=6 V (x=1 to 4), R_{EXT}=30 Ω, 40 Ω or 50 Ω are shown below. (Reference data)

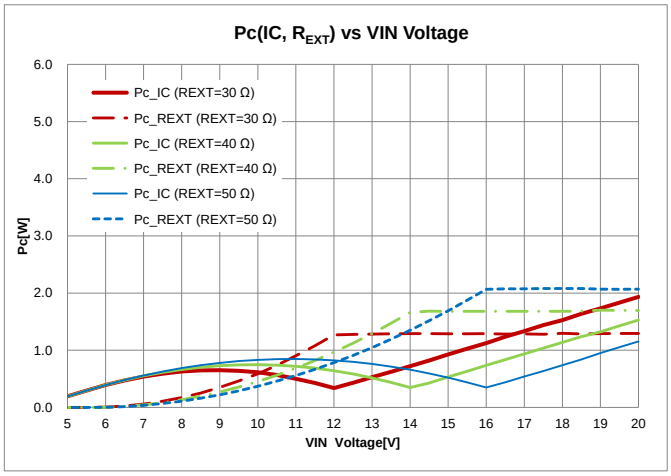

Figure 9. Energy Sharing Control Operation Example 1

The power consumption(Pc) across the IC and R_{EXT} when I_{OUT_TOTAL}=300 mA, V_{OUTx}=6 V (x=1 to 4), R_{EXT}=20 Ω, 30 Ω or 40 Ω are shown below. (Reference data)

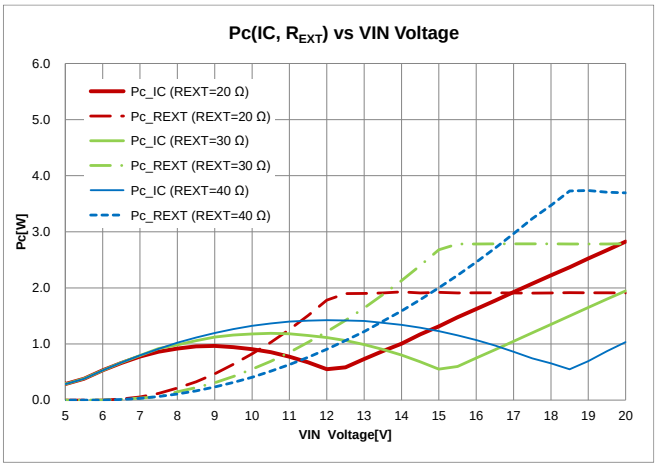

Figure 10. Energy Sharing Control Operation Example 2

The power consumption(Pc) across the IC and R_{EXT} when I_{OUT_TOTAL}=400 mA, V_{OUTx}=6 V (x=1 to 4), R_{EXT}=20 Ω, 25 Ω or 30 Ω are shown below. (Reference data)

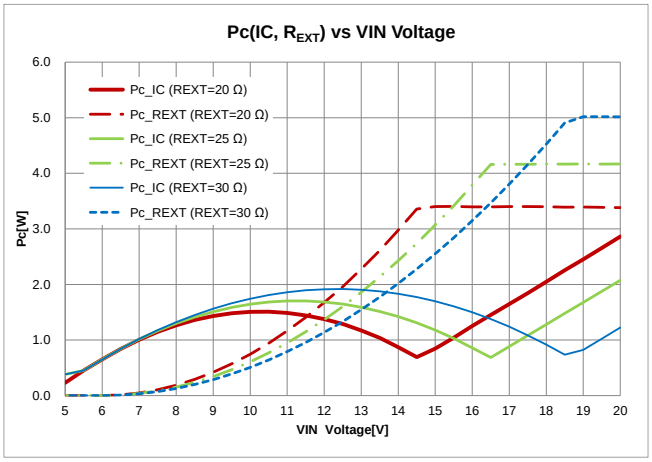

Figure 11. Energy Sharing Control Operation Example 3

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Description of Function – continued

3. Table of Operations

Depending on the CRT pin voltage, the IC switches between DC mode and PWM mode. Switching conditions are shown in the table below. When V_{IN} > 22.0 V, output current is limited to reduce power dissipation across the IC. Detect LED open and the OUTx pin short circuit then output current is turned OFF. When the PBUS pin is pulled low, all drivers are turned OFF. This IC also has inbuilt Under Voltage Lockout (UVLO) and Thermal Shutdown function (TSD). The correspondence table is given below. For details, refer to functional description of each block.

Operation Mode	CRT Pin	Detecting Condition		Output Current (I_{OUTx})	PBUS Pin
		[Detect]	[Release]		
DC	V_{CRT} ≥ 2.0 V (Typ)	-	-	50 mA to 150 mA	-
PWM Dimming	See Description of Function 4	-	-	See Description of Function 4	-
Over Voltage Mute (OVM)	-	V_{IN} > 22.0 V (Typ)	V_{IN} ≤ 22.0 V (Typ)	See Description of Function 13	-
LED Open Detection	-	V_{OUTx} ≥ V_{INRES} - 0.05 V (Typ) and V_{IN} ≥ V_{IN_OPM} (Typ)	V_{OUTx} < V_{INRES} - 0.05 V (Typ) or V_{IN} < V_{IN_OPM} (Typ)	See Description of Function 11	Low
OUTx Pin Short Circuit Protection (SCP)	-	V_{OUTx} ≤ 1.2 V (Typ)	V_{OUTx} ≥ 1.3 V (Typ)	See Description of Function 11	Low
SETx Pin Short Detection		R_{SET} ≤ 2.4 kΩ (Typ)	R_{SET} > 2.4 kΩ (Typ)	OFF	Low
PBUS Control OFF	-	V_{PBUS} ≤ 0.6 V	V_{PBUS} ≥ 2.4 V	OFF	V_{PBUS} ≤ 0.6 V input
Under Voltage Lockout (VIN UVLO)	-	V_{IN} ≤ 4.75 V (Typ)	V_{IN} ≥ 5.25 V (Typ)	OFF	High
Under Voltage Lockout (VINRES UVLO)	-	V_{INRES} ≤ 1.50 V (Typ)	V_{INRES} ≥ 2.00 V (Typ)	Power Control OFF	High
TSD	-	Tj ≥ 175 °C (Typ)	Tj ≤ 150 °C (Typ)	OFF	High

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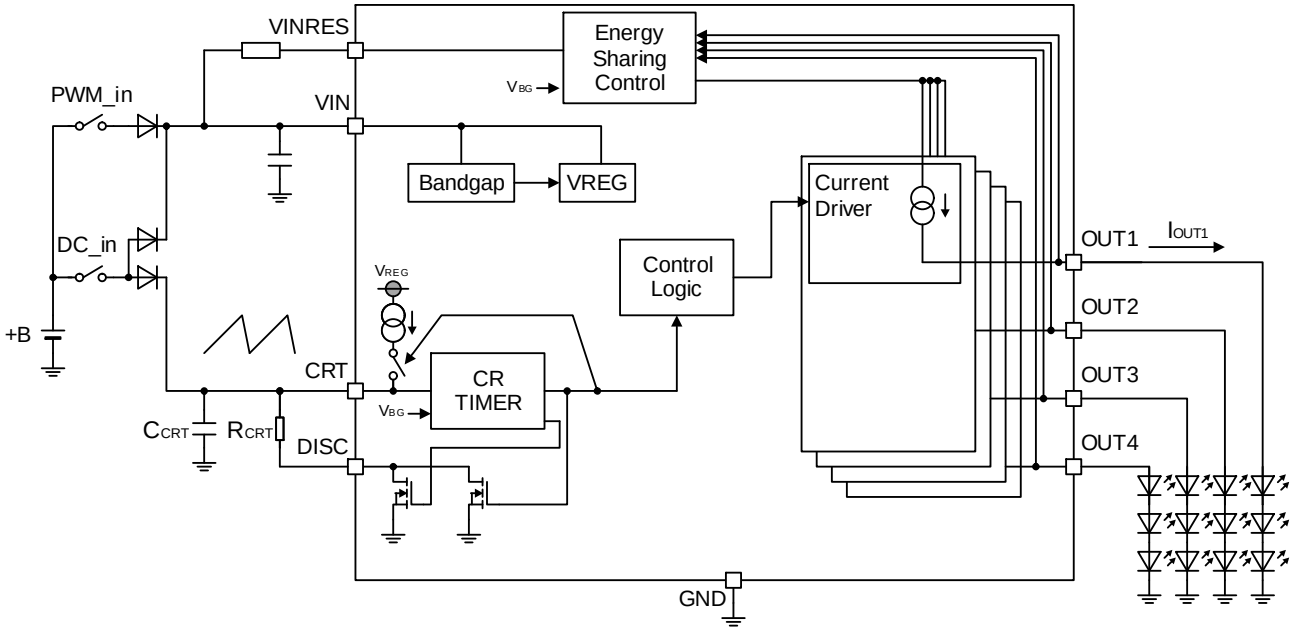
Description of Function – continued

4. PWM Dimming Operation

PWM Dimming is performed with the following circuit.
The dimming cycle and ON Duty Width can be set by values of the external components (C_{CRT}, R_{CRT}).
Connect the CRT pin to the VIN pin when not in use. Connect the DISC pin to GND or open when not in use.

The CR timer function is activated if DC SW is OPEN. To perform PWM dimming of output current, a triangular waveform is generated at the CRT pin. The output current (I_{OUTx}) is turned OFF while CRT voltage is ramp up, and output current (I_{OUTx}) is turned ON while CRT voltage is ramp down.

When $V_{CRT} \geq V_{CRT_DIS1}$ (2.0 V (Typ)), dimming mode turns to DC Control. When $V_{CRT} > V_{CRT_DIS2}$ (2.4 V (Typ)), the DISC pin ON resister changes from R_{DISC1} (50 Ω (Typ)) to R_{DISC2} (5 kΩ (Typ)), and the power consumption of the IC is reduced by reducing the inflow current of the DISC pin.



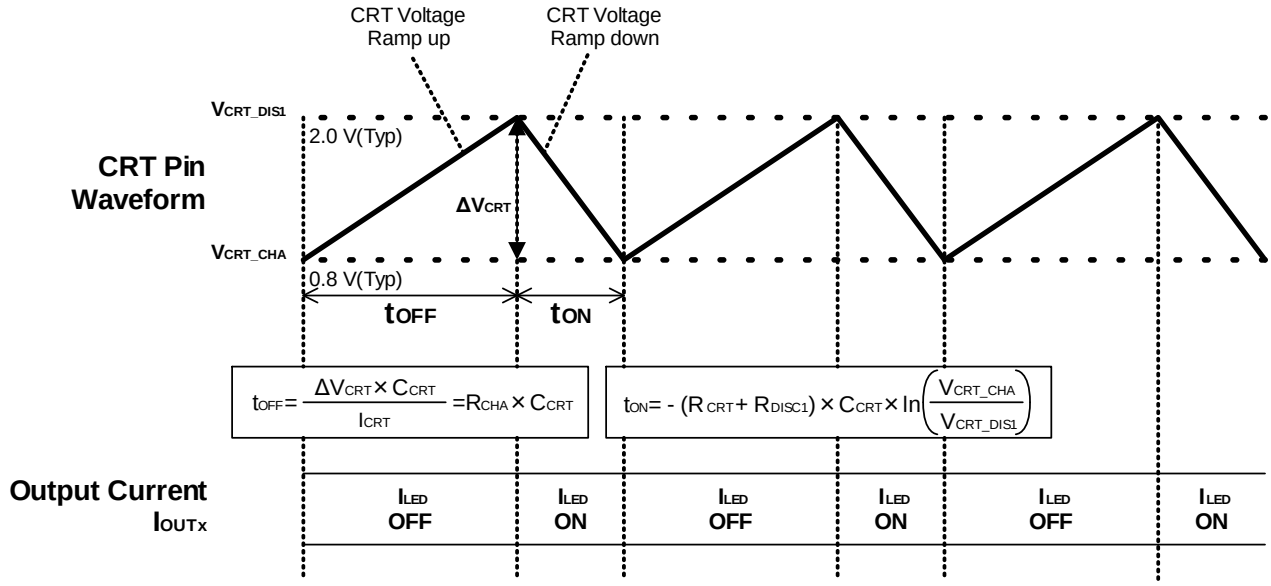


Figure 12. PWM Dimming Operation

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4. PWM Dimming Operation – continued

(1) CRT ramp up time t_{OFF} and CRT ramp down time t_{ON}
CRT ramp up time t_{OFF} and CRT ramp down time t_{ON} can be defined from the following equations.
Make sure that t_{ON} is set PWM Minimum Pulse Width t_{MIN} 100 µs or more.

$$t_{OFF} = \frac{\Delta V_{CRT} \times C_{CRT}}{I_{CRT}} = R_{CHA} \times C_{CRT} \quad [s]$$

$$t_{ON} = -(R_{CRT} + R_{DISC1}) \times C_{CRT} \times In\left(\frac{V_{CRT_CHA}}{V_{CRT_DIS1}}\right) \quad [s]$$

where:

I_{CRT}	is the CRT pin charge current, 40 µA (Typ).
R_{CHA}	is the CRT pin charge resistor, 30 kΩ (Typ).
R_{DISC1}	is the DISC pin ON resistor1, 50 Ω (Typ).
V_{CRT_CHA}	is the CRT pin charge voltage, 0.8 V (Typ).
V_{CRT_DIS1}	is the CRT pin discharge voltage1, 2.0 V (Typ).

(2) PWM Dimming Frequency (f_{PWM})
PWM Dimming Frequency is defined by t_{ON} and t_{OFF}.

$$f_{PWM} = \frac{1}{t_{ON} + t_{OFF}} \quad [Hz]$$

(3) ON Duty (D_{ON})
PWM ON duty is defined by t_{ON} and t_{OFF}.

$$D_{ON} = \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad [\%]$$

(Example) In case of R_{CRT}=3.6 kΩ, C_{CRT}=0.1 µF

$$t_{OFF} = R_{CHA} \times C_{CRT} = 30\ k\Omega \times 0.1\ \mu F = 3.0 \quad [ms]$$

$$t_{ON} = -(R_{CRT} + R_{DISC1}) \times C_{CRT} \times In(V_{CRT_CHA}/V_{CRT_DIS1})$$
$$= -(3.6\ k\Omega + 50\ \Omega) \times 0.1\ \mu F \times In(0.8\ V/2.0\ V) = 0.334 \quad [ms]$$

$$f_{PWM} = 1/(t_{ON} + t_{OFF}) = 1/(3.0\ ms + 0.334\ ms) = 300 \quad [Hz]$$

$$D_{ON} = t_{ON}/(t_{ON} + t_{OFF}) = 0.334\ ms/(3.0\ ms + 0.334\ ms) = 10.0 \quad [\%]$$

●PWM Dimming Operation Using External Signal
In case external PWM input to the CRT pin, make sure that input pulse high voltage ≥ 2.2 V and pulse low voltage ≤ 0.6 V. Also open the DISC pin or connect to GND.

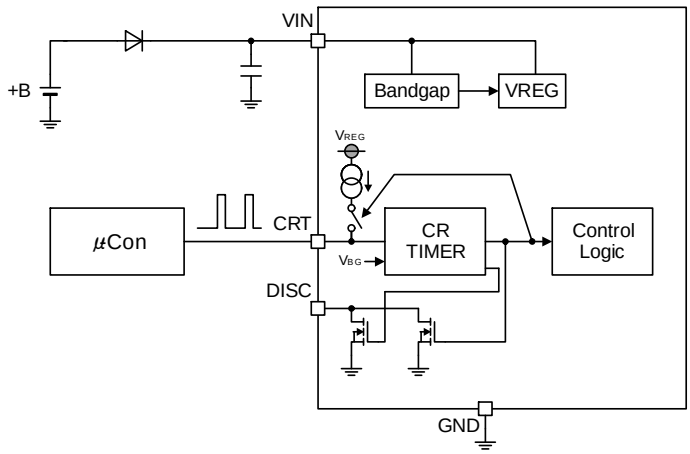

Figure 13. PWM Dimming Operation Using External Signal

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4. PWM Dimming Operation – continued

●About deviation of CRT ramp up/down time with a reverse connection protection diode

If this LSI is used to drive LED like below schematic, it is possible to occur CRT ramp up/down time deviation due to characteristics of reverse current Ir diode (D2, D3).
Consider to choose a diode (D2, D3) which is recommended by Rohm or Ir value 1 μA (Max) or less.
Since reverse current flows even with the recommended diodes, connect a resistor R_{DCIN} of 10 kΩ or less between point A and GND so that the voltage at point A does not rise.

Mechanism of deviation of CRT ramp up/down time from set values.

(1) During the PWM dimming operation mode, Point A on Figure 14 is Hi-Z.
↓
(2) Reverse current Ir of D2 and D3 goes to Point A.
(Power supply voltage is being input into the cathode of D2, so mainly reverse current of D2 goes into C1.)
→Reverse current Ir of D3 is added to the CRT pin charge current and discharge current, so CRT ramp up/down time deviates from the settings.
↓
(3) C1 gets charged, voltage at Point A rises.
↓
(4) Point A voltage ≥ the CRT pin voltage of each IC.
↓
(5) Vf occurs in the diodes D3.
↓
(6) D3 circulate forward current I_F
→Forward current I_F of D3 is added to the CRT pin charge current and discharge current, so CRT ramp up/down time deviates from the settings.
↓
(7) Repetition of (2) to (6).

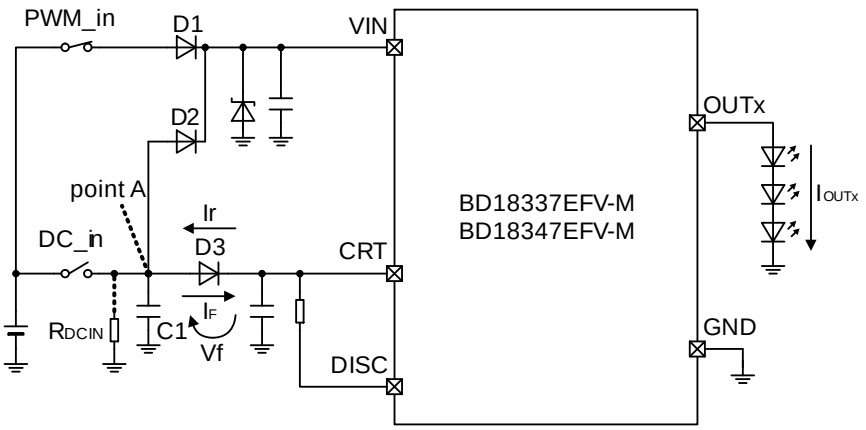

Figure 14. How Reverse Protection Diode Affects the CRT pin Ramp Up / Down Time

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Description of Function – continued

5. The SETx pin Short Detection Function

When the SETx pin is shorted to GND, the IC detects that the SETx pin current has increased and turns off the output current. The maximum resistance on the SETx pin short detection is R_{SETx} ≤ 5.0 kΩ (Max). Fault is indicated by pulling the PBUS pin low.

Note that the SETx pin short detection resistance value R_{SETx} is 5 kΩ or less when the over voltage mute function is active.

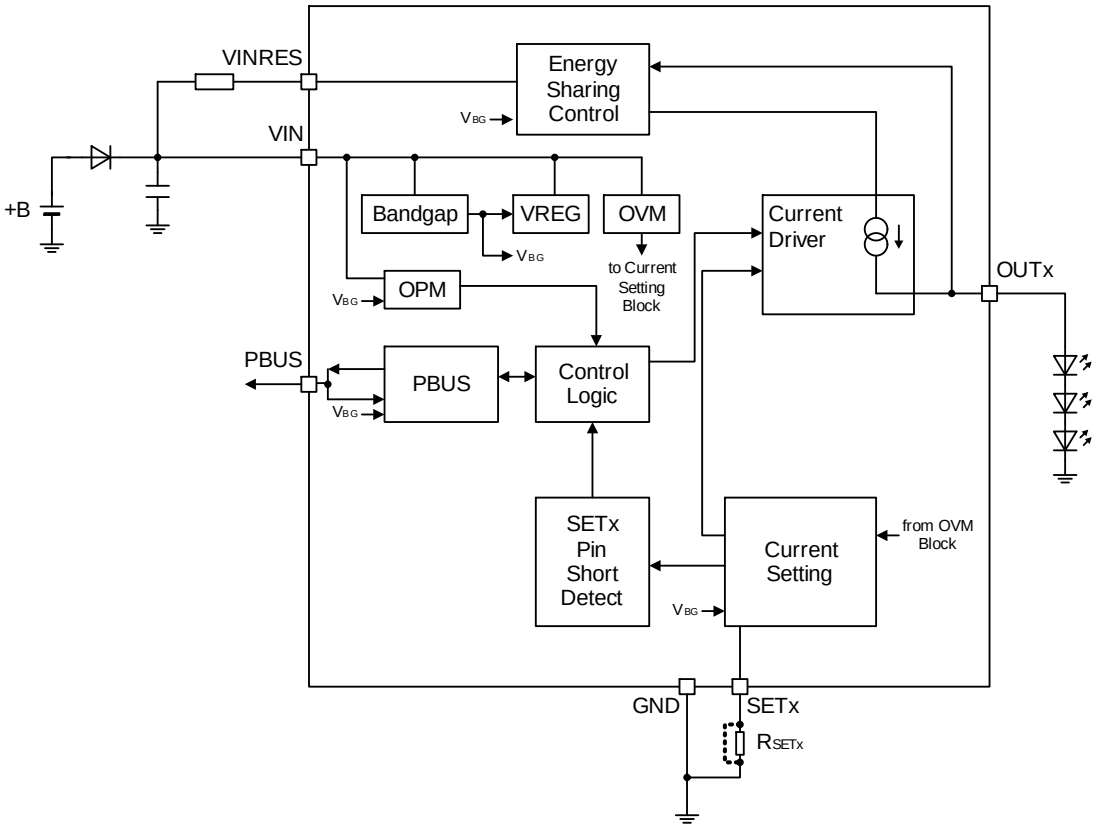

Figure 15. SETx pin Short Detection

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Description of Function – continued

6. LED Open Detection Function

When one of the LEDs is in the open state, the OUTx pin voltage rises. At $V_{OUTx} \geq V_{INRES}$ - 0.05 V (Typ), LED Open Detection operation is performed. In case of LED Open Detection, fault is indicated by pulling the PBUS pin low.

7. Disable LED Open Detection Function at Reduced-Voltage

Built-in disable LED Open Detection function prevents erroneous detection of LED Open during voltage ramp up or ramp down at the VIN pin. Open Detection is not performed until the VIN pin voltage is internal OPM threshold voltage (V_{IN_OPM}) or more. LED Open Detection remains disabled during power supply ramp up and ramp down, when $V_{IN} < V_{IN_OPM}$.
For disable LED Open Detection function to work properly, LEDs must be selected according to the following formula:

$$V_{f_LED_OPD} \times N + 100\ mV + R_{VIN_VINRES} \times 40\ mA < V_{IN_OPM} \quad [V]$$

where:

$V_{f_LED_OPD}$	is the LED Vf when $I_F = I_{OUT_OPEN}$ (I_{OUT_OPEN}=10 mA (Max))
R_{VIN_VINRES}	is the ON resistance between the VIN pin and the VINRES pin.
N	is the number of LED.

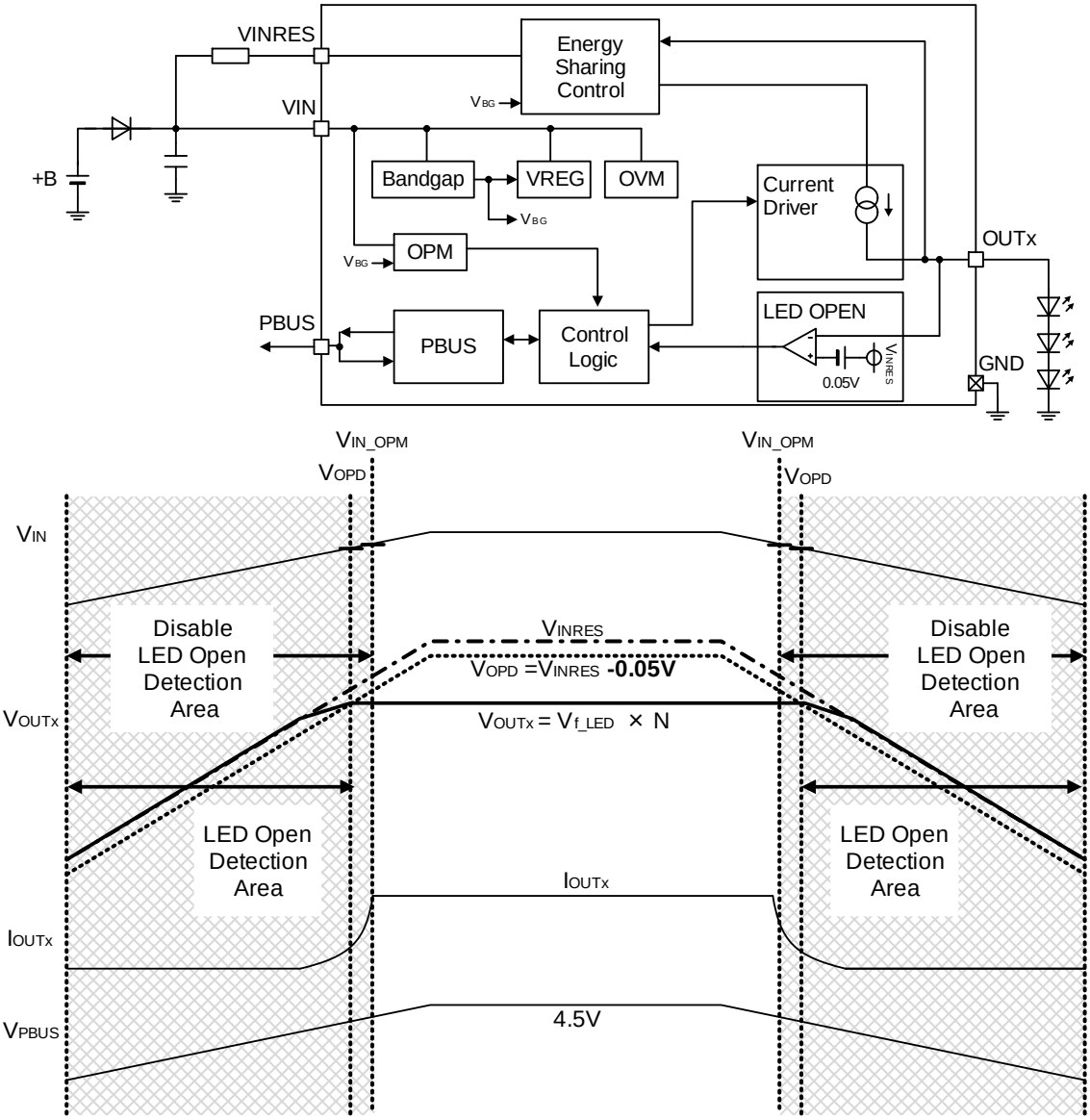

Figure 16. Disable LED Open Detection Voltage at Reduced-Voltage

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Description of Function – continued

8. OUTx pin Short Circuit Protection (SCP)

If the OUTx pin is shorted to GND, the OUTx voltage goes low. When the OUTx pin voltage V_{OUTx} ≤ 1.2 V (Typ), then SCP mechanism is enabled after a delay of t_{SCPD2} (20 µs (Typ)). In case of SCP, output current I_{OUT} is turned off to prevent thermal damage of the IC. Fault is indicated by pulling the PBUS pin low after a delay open t_{SCPD1} (60 µs (Typ)). To prevent false SCP at power supply startup, the output SCP is disabled until V_{CRT} > 2.0 V (Typ) once UVLO is released. In case of power supply ramping up with the OUTx pin short circuit condition (V_{OUTx} < 1.2 V (Typ)), SCP mechanism is enabled after t_{SCPPON} (140 µs (Typ)), only if UVLO is released and V_{CRT} > 2.0 V (Typ).

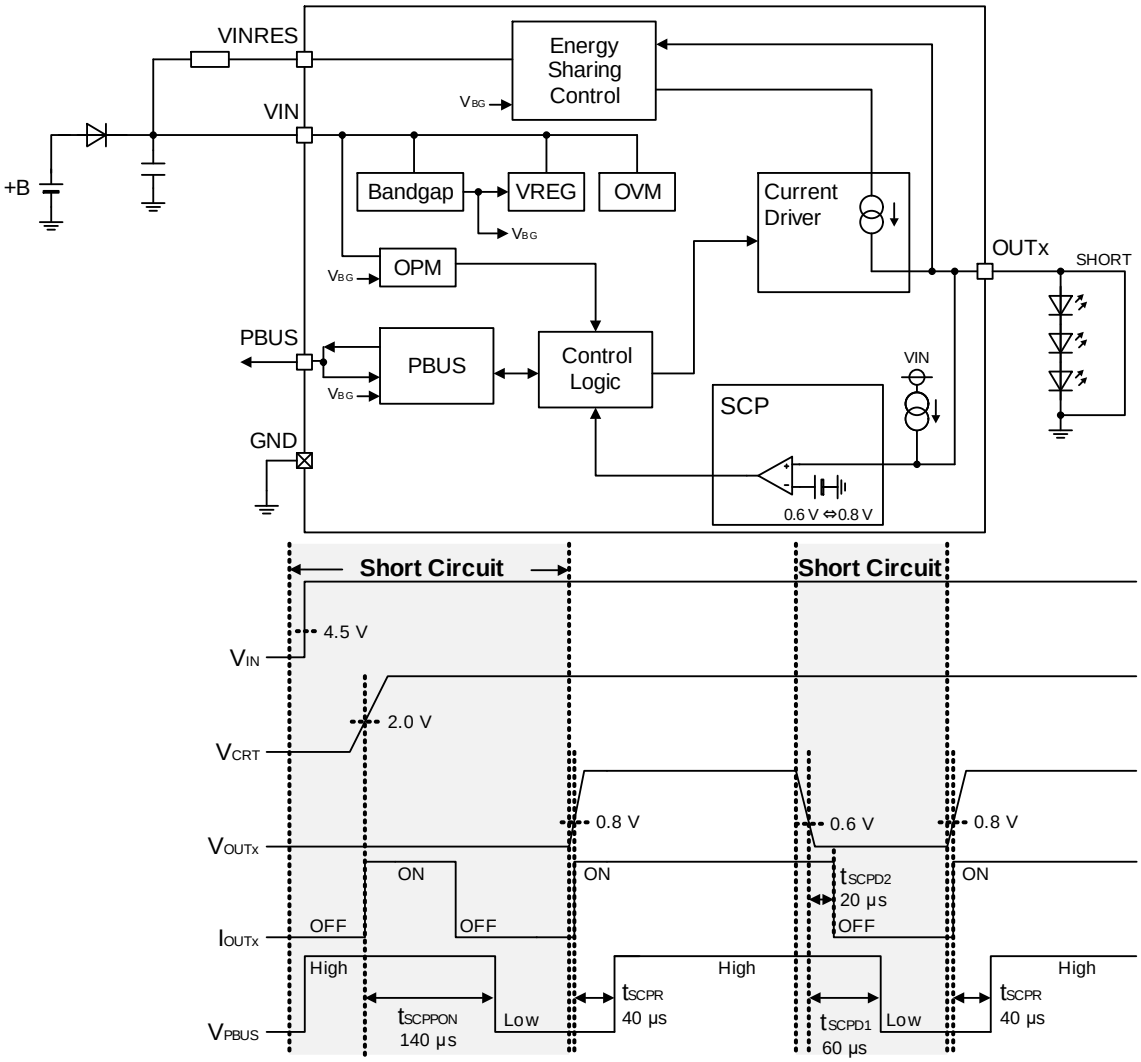

Figure 17. OUTx pin Short Circuit Protection (SCP)

●OUTx pin short circuit current

When V_{OUTx} < 1.3 V, the OUTx pin short circuit current I_{OUTx_SCP} flows to prevent malfunction of the OUTx pin short circuit protection mechanism.

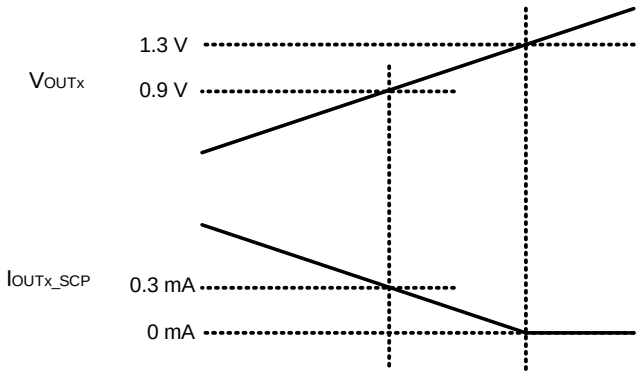

Figure 18. OUTx pin Short Circuit Current

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Description of Function – continued

9. Connection Method of LEDs to Output pins – Effect on Protection Functions

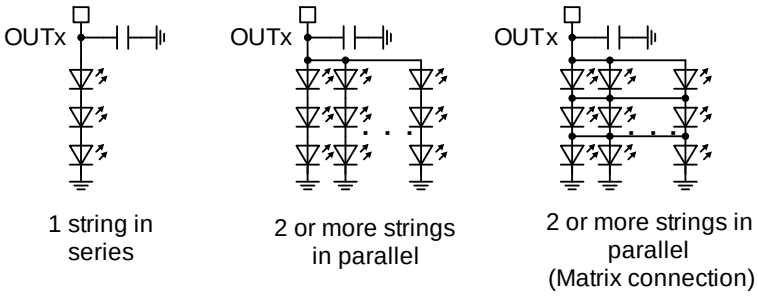

Figure 19. About the Capacitor of Connecting LED Anode

Connection method	Output SCP	LED Open Detection
1 string in Series	Detectable	Detectable
2 or more strings in parallel	Detectable	Not detectable*(Note 1)*
2 or more strings in parallel (Matrix connection)	Detectable	Not detectable*(Note 2)*

(Note 1) Detectable only when one or more LEDs are open in all columns.
(Note 2) Detectable only when all LEDs from any row are open.

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Description of Function – continued

10. LED Open Detection, SCP and OUTx pin Hi-Z in DC/PWM Dimming Modes

Operation of LED Open Detection and SCP sections differ in DC mode and PWM dimming mode.

In DC mode, LED Open Detection and SCP are enabled at all times.

In PWM dimming mode, the LED Open Detection function is valid only during the falling edge of CRT signal, whereas SCP is valid at all times. There is a possibility of the OUTx pin becoming Hi-Z. False SCP may occur if the OUTx pin voltage drops due to external noise(*Note 1*). Connect a capacitor (0.1 µF or more(*Note 2*)) to GND, close to the OUTx pin to avoid erroneous output.

(Note 1) Propagation noise, radiation noise, interference between wires, interference between connectors, etc.
(Note 2) When connecting 0.1 µF or more, evaluate the delay time from the start of VIN until the I_{OUTx} current flows. Also, evaluate the I_{OUTx} pulse width in the PWM dimming mode.

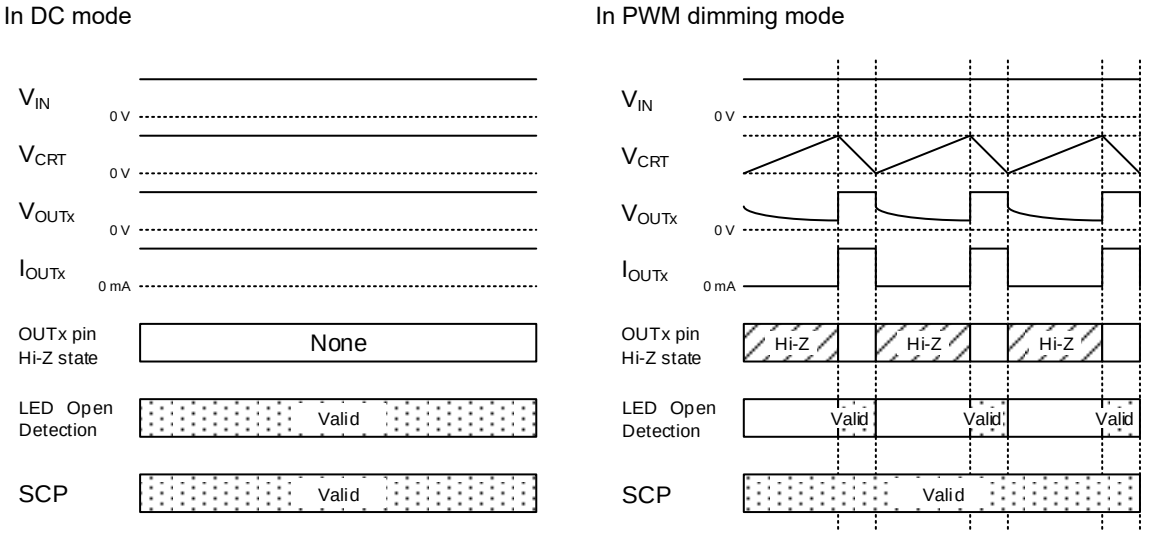

Figure 20. LED Open Detection, SCP and the OUTx pin Hi-Z

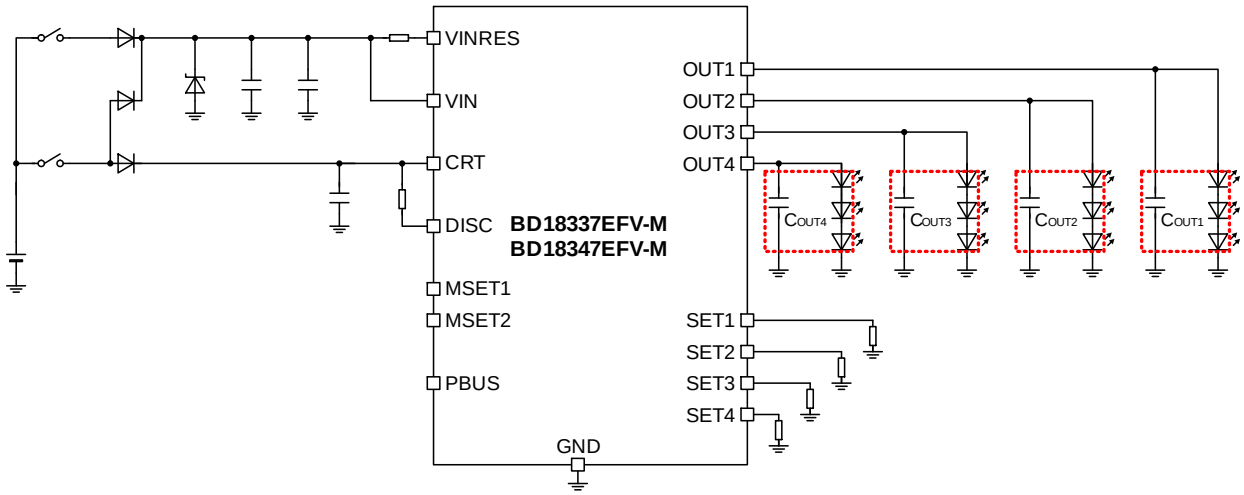

Figure 21. Capacitor Connected to the OUTx pin

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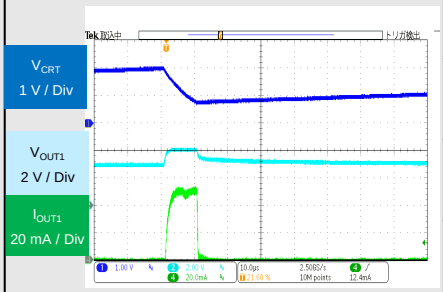
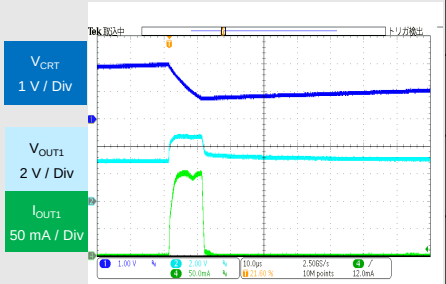
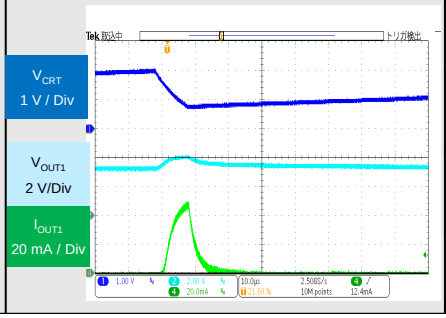
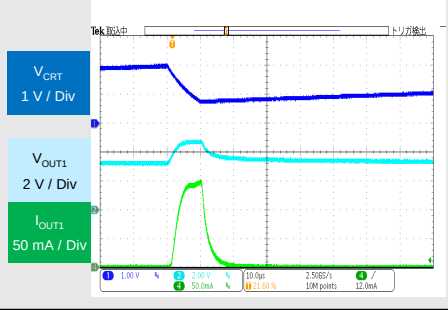
10. LED Open Detection, SCP and OUTx pin Hi-Z in DC/PWM Dimming Modes – continued

Evaluation example (I_{LED} pulse width at PWM Dimming operation)

Condition: +B=13 V
Ta=25 °C
LED=1 Strings
C_{CRT}=0.01 µF
R_{CRT}=1.0 kΩ
PWM Dimming Mode

	50 mA / ch		150 mA / ch	
C_{OUTx}=0.01 µF		Rise Time 3.5 µs Fall Time 0.8 µs		Rise Time 2.5 µs Fall Time 0.8 µs
C_{OUTx}=0.22 µF		Rise Time 7.7 µs Fall Time 12 µs		Rise Time 4.9 µs Fall Time 9.9 µs

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Description of Function – continued

11. Lamp Control Modes (MSET1, MSET2)

By connecting the MSET1 pin to ground or open, it is possible to change output channel operation mode on detecting an LED error. The MSET2 pin can also be used to control CH4 operation.
MSET1=L (GND short): If SCP or LED Open is detected in any one of 4 channels, all the channels are OFF.
MSET1=H (Pin open) : Remaining channels continue to operate even if one channel detects SCP or LED Open.
MSET2=L (GND short): CH4 operates in the same way as CH1 to CH3
MSET2=H (Pin open) : CH4 ignores the PWM signal generated by CRTIMER and are always in DC mode. When CH4 detects SCP or LED Open, PBUS : H is maintained and CH1 to CH3 continue to operate (License Lamp Mode).

Normal Mode (MSET2=L)

MSET1	MSET2	OUT1 to OUT3 OPEN Detect	OUT1 to OUT3 SCP	OUT4 OPEN Detect	OUT4 SCP	LED Error CH Output	Remaining CH1 to CH3 Output	CH4 Output	PBUS
L All CH OFF	**L** Normal Mode	Detect	-	-	-	ON	OFF	OFF	**L**
		-	Detect	-	-	OFF	OFF	OFF	
		-	-	Detect	-	ON	OFF	ON	
		-	-	-	Detect	OFF	OFF	OFF	
H IndividualCH OFF		Detect	-	-	-	ON	ON	ON	**L**
		-	Detect	-	-	OFF	ON	ON	
		-	-	Detect	-	ON	ON	ON	
		-	-	-	Detect	OFF	ON	OFF	

License Mode (MSET2=H)

MSET1	MSET2	OUT1 to OUT3 OPEN Detect	OUT1 to OUT3 SCP	OUT4 OPEN Detect	OUT4 SCP	LED Error CH Output	Remaining CH1 to CH3 Output	CH4 Output	PBUS
L All CH OFF	**H** License Mode	Detect	-	-	-	ON	OFF	OFF	**L**
		-	Detect	-	-	OFF	OFF	OFF	
		-	-	Detect	-	ON	ON	ON	**H**
		-	-	-	Detect	OFF	ON	OFF	
H IndividualCH OFF		Detect	-	-	-	ON	ON	ON	**L**
		-	Detect	-	-	OFF	ON	ON	
		-	-	Detect	-	ON	ON	ON	**H**
		-	-	-	Detect	OFF	ON	OFF	

Figure 22. Lamp Control Modes (MSET1, MSET2)

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Description of Function – continued

12. PBUS Function

The PBUS pin is the pin to input and output an error signal.
When abnormality such as LED Open or the OUTx pin short circuit occurs, it can notify the abnormality to the outside by changing the PBUS pin output from high to low. In addition, by externally controlling the PBUS pin from high to low, the output current is turned off. When using multiple LSIs to drive multiple LEDs, it is possible to turn off all LED lines at once by connecting the PBUS pins of each CH as shown in the figure below, even if LED Open or the OUTx pin short circuit occurs.

Caution of using the PBUS Pin
Do not connect to the PBUS pins other than below list items due to the difference of ratings, internal threshold voltages, and so on. (BD18340FV-M, BD18341FV-M, BD18342FV-M, BD18343FV-M, BD18345EFV-M, BD18337EFV-M, BD18347EFV-M)

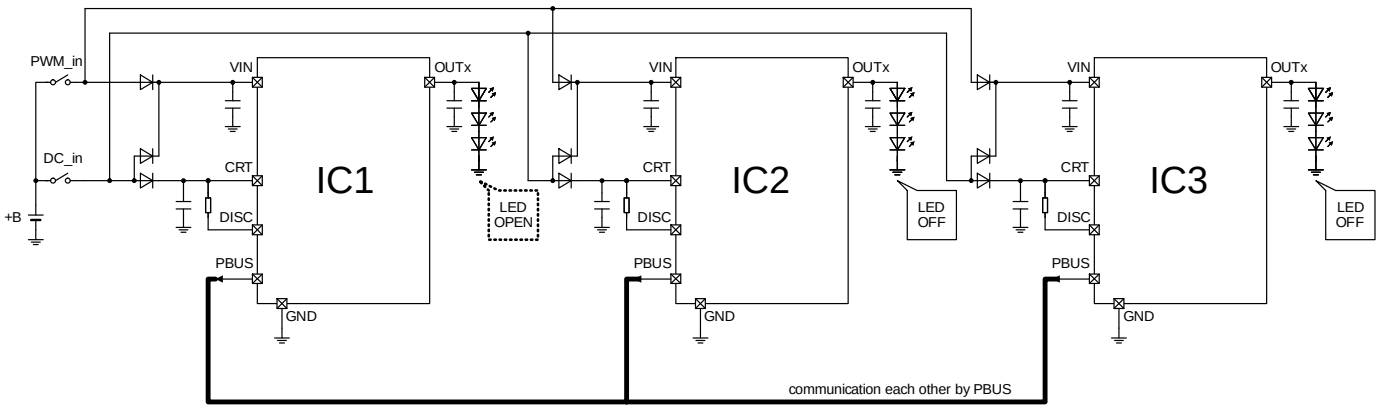

Figure 23. PBUS Function

▼Example of Protective Operation due to LED Open Circuit

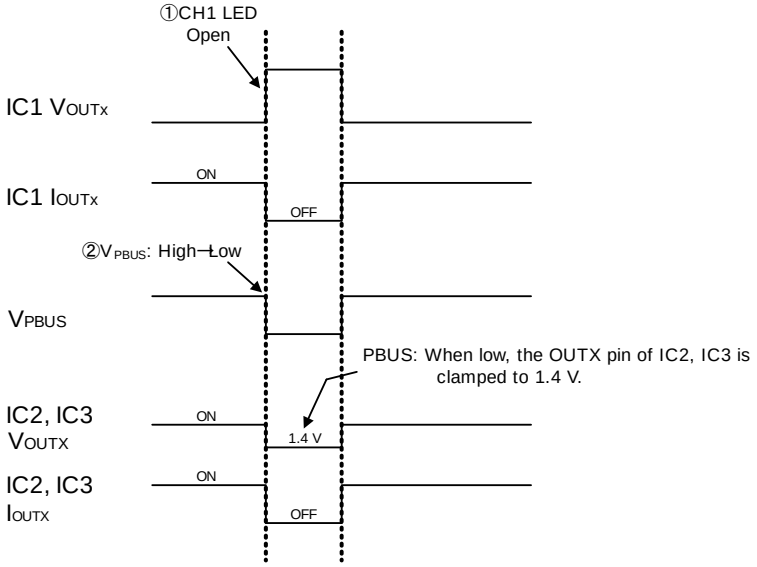

Figure 24. Example of Protective Operation

In case of LED Open, V_{PBUS} of IC1 goes from High to Low. As V_{PBUS} goes low, IC2 and IC3 LED drivers turn off their LEDs. When V_{PBUS} goes low, the OUTx pins are clamped to 1.4 V (Typ), in order to prevent output ground protection operation.

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Description of Function – continued

13. Over Voltage Mute Function (OVM)

When the VIN pin voltage exceeds 22.0 V (Typ), Over Voltage Mute function is activated to prevent thermal deterioration to the IC. This is done by attenuating the output current (I_{OUTx}). The output current (I_{OUTx}) is attenuated at -20 %/V (Typ). If the output current is attenuated less than 10 mA (Typ), output current is turned OFF.

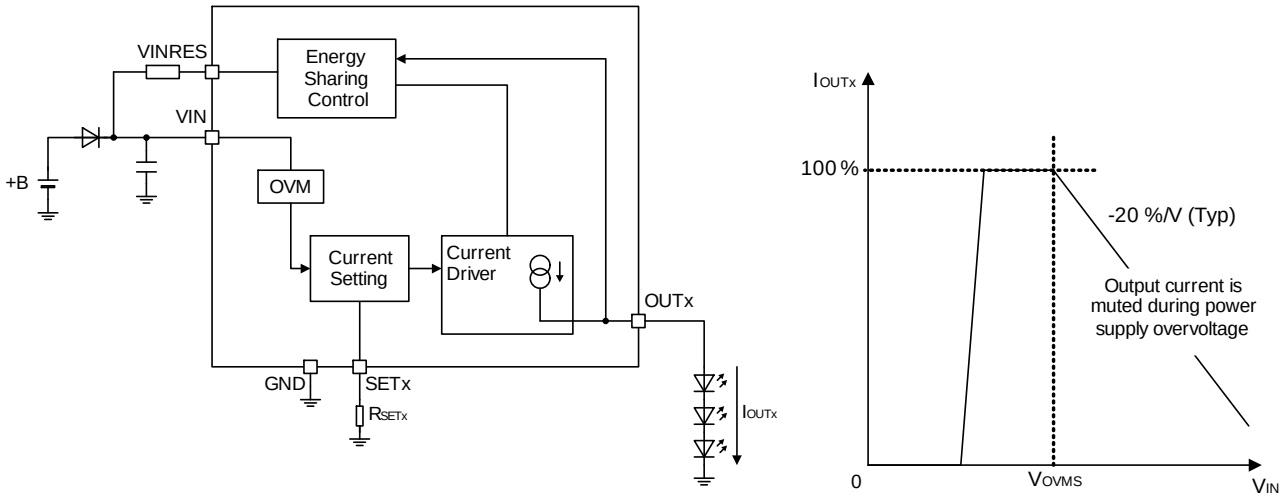

Figure 25. Over Voltage Mute Function (OVM)

14. Under Voltage Lockout (UVLO)

UVLO circuit prevents the IC malfunction during times of power supply ramp up, ramp down or instantaneous power interruptions. When the VIN pin voltage is 4.75 V (Typ) or less, VIN UVLO is activated and output current (I_{OUTx}) is turned OFF, and when the VIN pin voltage increases to 5.25 V (Typ) or more, VIN UVLO is deactivated and normal operation resumes. The VINRES pin voltage is 1.50 V (Typ) or less, VINRES UVLO is activated and power control function is turned OFF, and when The VINRES pin voltage increases to 2.00V (Typ) or more, VINRES UVLO is deactivated and power control function is turned ON.

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Application Examples

1. I_{OUTx}=75 mA/ch License MODE,
PWM ON Duty:10 %, Pulse Width=0.334 ms, PWM Frequency=300 Hz

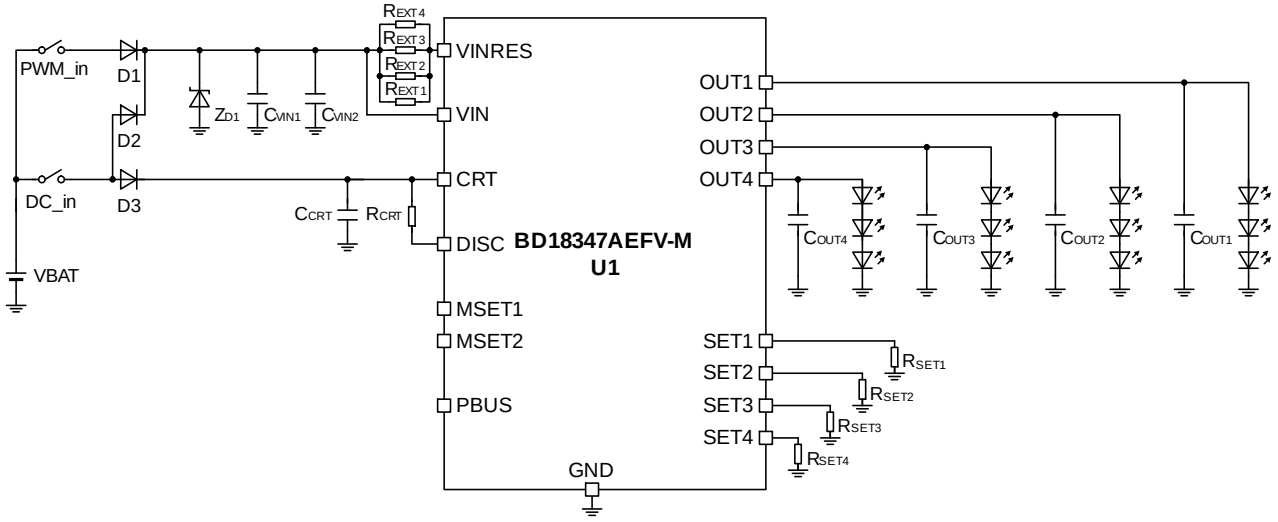

Figure 26. Application Example 1

Recommended Parts List 1

Parts	No.	Parts Name	Value	Unit	Product Maker
IC	U1	BD18347AEFV-M	-	-	ROHM
Diode	D1, D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Resistor	R_{SET1}, R_{SET2}, R_{SET3}, R_{SET4}	MCR03EZPFX2402	24	kΩ	ROHM
	R_{EXT1}, R_{EXT2}, R_{EXT3}, R_{EXT4}	LTR100JZPJ101	100	Ω	ROHM
	R_{CRT}	MCR03EZPFX3601	3.6	kΩ	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	μF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	μF	murata
	C_{CRT}	GCM155R71H104KE37	0.1	μF	murata
	C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}	GCM155R71H104KE37	0.1	μF	murata

About Z_{D1}, place according to test standard of battery line.

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Application Examples – continued

2. I_{OUTx}=100 mA/ch, Tail / Stop application with MSET1=L
PWM ON Duty=10 %, Pulse Width=0.334 ms, PWM Frequency=300 Hz

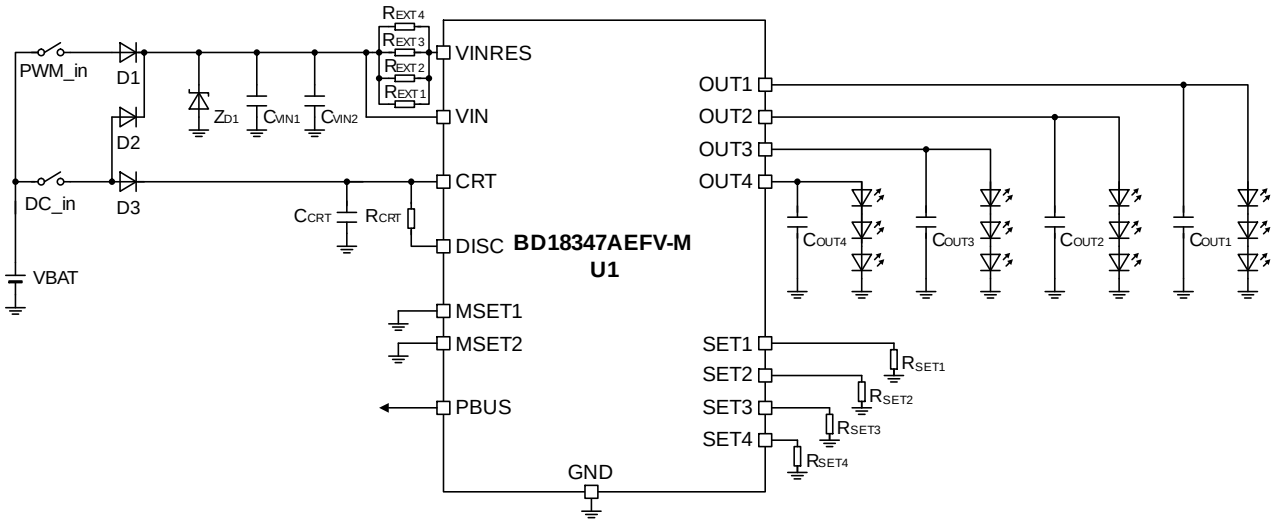

Figure 27. Application Example 2

Recommended Parts List 2

Parts	No.	Parts Name	Value	Unit	Product Maker
IC	U1	BD18347AEFV-M	-	-	ROHM
Diode	D1, D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Resistor	R_{SET1}, R_{SET2}, R_{SET3}, R_{SET4}	MCR03EZPFX2402	18	kΩ	ROHM
	R_{EXT1}, R_{EXT2}, R_{EXT3}, R_{EXT4}	LTR100JZPJ101	100	Ω	ROHM
	R_{CRT}	MCR03EZPFX3601	3.6	kΩ	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	μF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	μF	murata
	C_{CRT}	GCM155R71H104KE37	0.1	μF	murata
	C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}	GCM155R71H104KE37	0.1	μF	murata

About Z_{D1}, place according to test standard of battery line.

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Application Examples – continued

3. I_{OUTx}=100 mA/ch, PWM Control Each Channel from External Signal

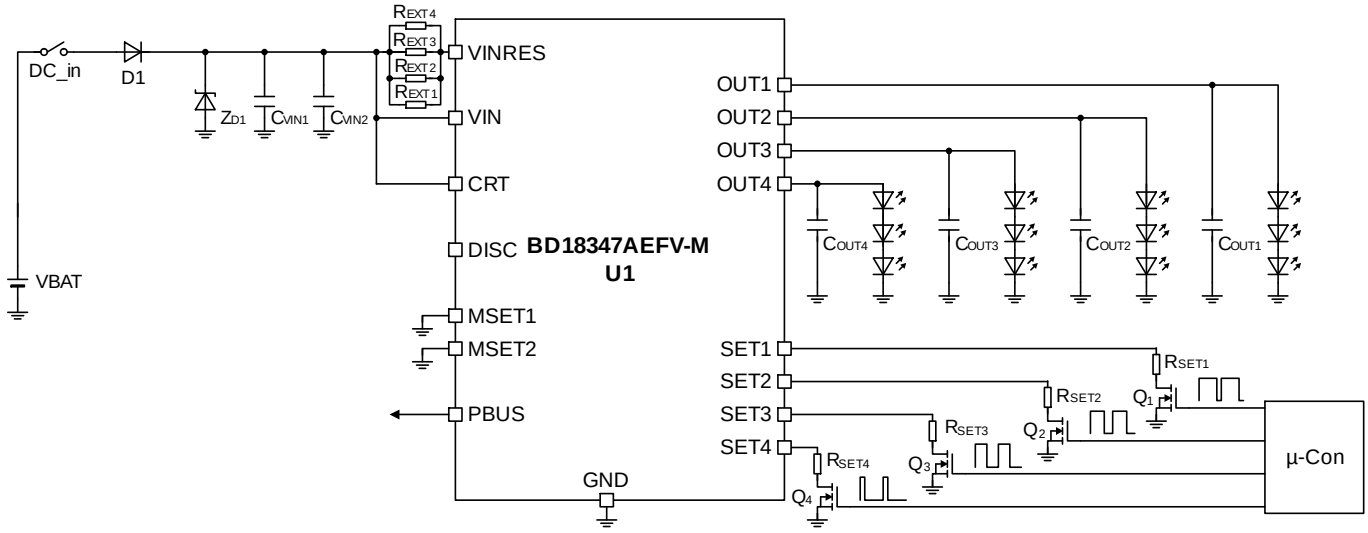

Figure 28. Application Example 3

Recommended Parts List 3

Parts	No.	Parts Name	Value	Unit	Product Maker
IC	U1	BD18347AEFV-M	-	-	ROHM
MOSFET	Q1 to Q4	RJU003N03FRAT106	-	-	ROHM
Diode	D1	RFN2LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Resistor	R_{SET1}, R_{SET2}, R_{SET3}, R_{SET4}	MCR03EZPFX2402	18	kΩ	ROHM
	R_{EXT1}, R_{EXT2}, R_{EXT3}, R_{EXT4}	LTR100JZPJ101	100	Ω	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	µF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	µF	murata
	C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}	GCM155R71H104KE37	0.1	µF	murata

About Z_{D1}, place according to test standard of battery line.

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Power Dissipation

Thermal design should meet the following equation.

$$P_d > P_C$$

$$P_d = \left(1/\theta_{JA}\right) \times \left(T_{jmax} - T_a\right) or \left(1/\Psi_{JT}\right) \times \left(T_{jmax} - T_T\right)$$

When don't use Energy Sharing Control, refer to below equation.

$$P_C = (V_{IN} \times (I_{VIN1} + I_{DISC}) + (V_{IN} - V_{OUT1}) \times I_{OUT1} + (V_{IN} - V_{OUT2}) \times I_{OUT2} + (V_{IN} - V_{OUT3}) \times I_{OUT3} + (V_{IN} - V_{OUT4}) \times I_{OUT4}$$

When use Energy Sharing Control, refer to page 11 and 12.

where:

P_d	is the power dissipation.
P_C	is the power consumption.
V_{IN}	is the VIN pin voltage.
I_{VIN1}	is the circuit current at normal mode.
I_{DISC}	is the DISC pin input current.
I_{OUT1} to I_{OUT4}	is the output current through each channel.
V_{OUT1} to V_{OUT4}	is the OUTx pin voltage each channel.
θ_{JA}	is the thermal resistance of junction to ambient.
Ψ_{JT}	is the thermal characterization parameter of junction to center case surface.
T_{jmax}	is the maximum junction temperature (150 °C).
T_a	is the ambient temperature.
T_T	is the case surface temperature.

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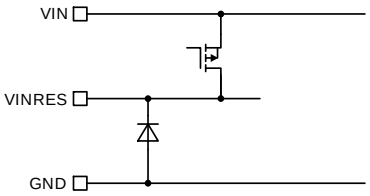
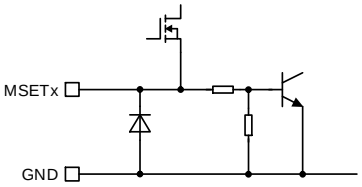
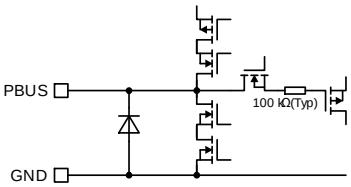
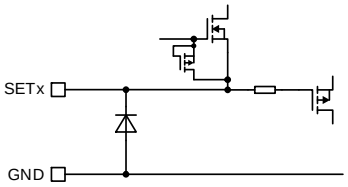
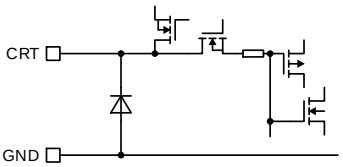
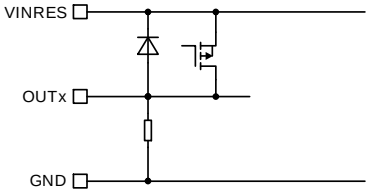
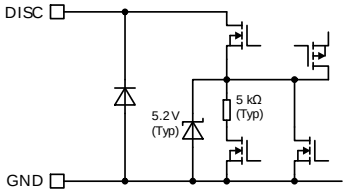
I/O Equivalence Circuits

No.	Pin Name	I/O Equivalence Circuit	No.	Pin Name	I/O Equivalence Circuit
1	VINRES		6,11	MSET1 MSET2	
3	PBUS		7 to 10	SET1 SET2 SET3 SET4	
4	CRT		13 to 16	OUT1 OUT2 OUT3 OUT4	
5	DISC				

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

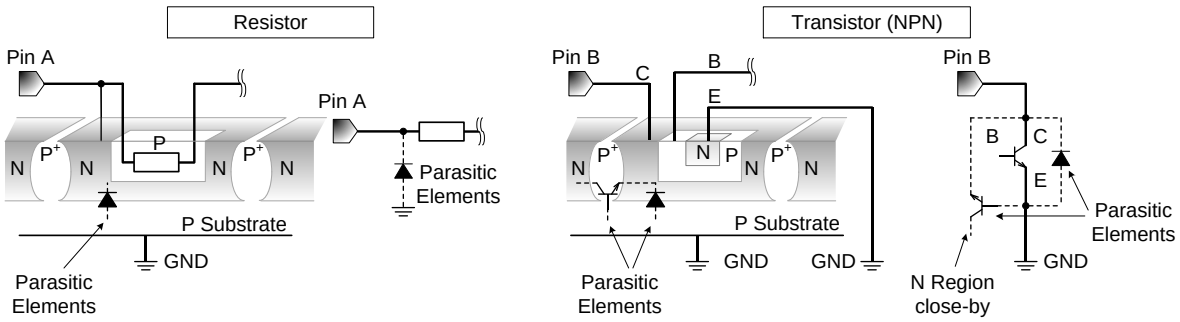

Figure 29. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.
"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

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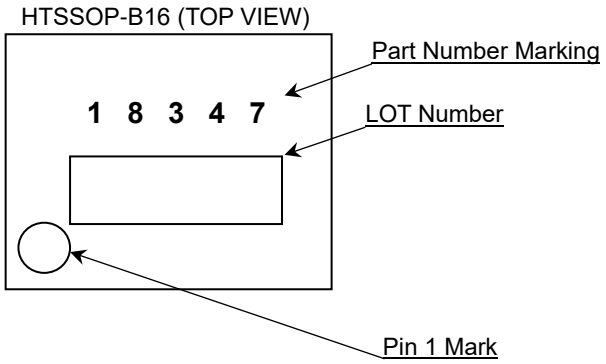
Ordering Information

B	D	1	8	3	4	7	A	E	F	V	-	M	E	2

Package
EFV:
HTSSOP-B16

Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



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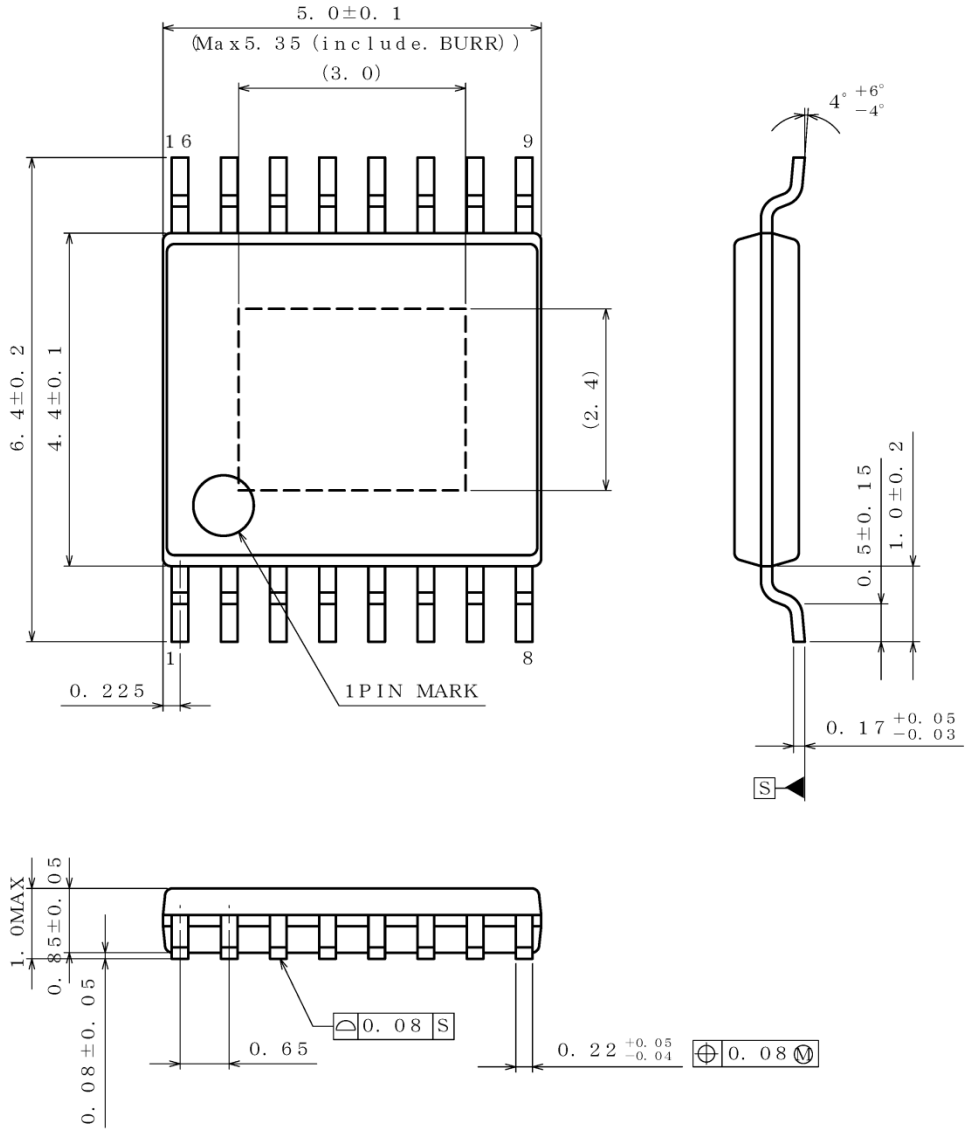
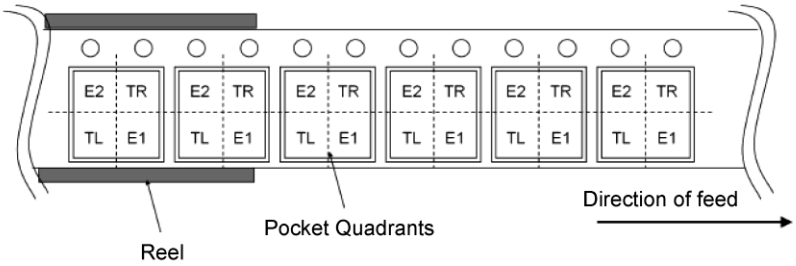
Physical Dimension and Packing Information

Package Name	HTSSOP-B16



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
20.Nov.2020	001	New Release

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Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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