TEXAS INSTRUMENTS

THS6043EVM

User's Guide

August 2002

High Performance Linear Products

SLOU139

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This manual provides information about the EVM used to evaluate the THS6043 high-speed amplifier. Additionally, this document provides a good example of PCB design for high-speed applications. The user should keep in mind the following points.

It is recommended that the user initially review the data sheet of the device under test.

- It is helpful to review the schematic and layout of the THS6043EVM to determine the design techniques used in the evaluation board.
- The design of the high-speed amplifier PCB is a sensitive process. The user must approach high speed PCB design with care and awareness.

How to Use This Manual

This document contains the following chapters:

- Chapter 1: Introduction and Description
- Chapter 2: Using the THS6043EVM
- Chapter 3: THS6043EVM Applications
- Chapter 4: High-Speed Amplifier PCB Layout Tips
- Chapter 5: EVM Hardware Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Electrostatic Sensitive Components

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on poroper handling, refere to SSYA008.

Related Documentation From Texas Instruments

The URLs below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS6043 data sheet (literature number SLOS264)
- Application report (literature number SLMA002), *Power Pad Thermally Enhanced Package*, http://www−s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report (literature number SLMA004), *Power Pad Made Easy*, http://www−s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report (literature number SSYA008), *Electrostatic Discharge (ESD)*, http://www−s.ti.com/sc/psheets/ssya008/ssya008.pdf

- Application report (literature number SLOA100), *Active Output Impedance for ADSL Line Drivers*, http://www−s.ti.com/sc/psheets/sloa100/sloa100.pdf

Trademarks

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Chapter 1

Introduction and Description

The Texas Instruments THS6043 evaluation module (EVM) helps designers evaluate the performance of the THS6043 operational amplifier. Also, this EVM is a good example of high-speed PCB design.

This document details the THS6043EVM. It includes a list of EVM features, a brief description of the module illustrated with a series of schematic diagrams, EVM specifications, details on connecting and using the EVM, and a discussion of high-speed amplifier design considerations.

This EVM enables the user to implement various circuits to clarify the available configurations presented by the schematic of the EVM. The user is not limited to the circuit configurations presented here. The EVM provides enough hardware hooks that the only limitation should be the creativity of the user.

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1.1 Description

The THS6043EVM provides a platform for developing high-speed op amp application circuits. It contains the THS6043 high-speed dual op amp, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations. The PC board measures 4.21 by 2.88 inches.

1.2 Evaluation Module Features

THS6043 high-speed operational amplifier EVM features include:

- ❑ Differential noninverting gain configuration for DSL
- ❑ Active termination capability (R6 and R11)
- ❑ Snubber circuit (R19 and C5), for use with active termination
- ❑ HPF function (C3 and R7)
- ❑ Hooks for a receive path signal (TP1 through TP4)
- ❑ Virtual ground capability (JP1, R20, R21)
- ❑ Power down capability (R25, R26, R27, JP2)
- ❑ Single supply capability (R4, R14, R20, R21, C9, JP1, Z1, Z2)
- ❑ Single-ended noninverting gain stage capability (R8, R9, R23, R24, Z3)
- ❑ Single-ended inverting gain stage capability (R3, R4, R14, R15)
- ❑ Power supply decoupling components (C6−C15, FB1, FB2)
- ❑ Short-loop length for the power supply differential high-frequency path (C8)

1.3 THS6043EVM Operating Conditions

Supply voltage range, $\pm V_{CC}$	±5 V to ±15 V (see the device data sheet)
Supply current, I_{CC}	(see the device data sheet)

For complete THS6043 amplifier IC specifications, parameter measurement information, and additional application information, see the THS6043 data sheet, TI literature number SLOS264.

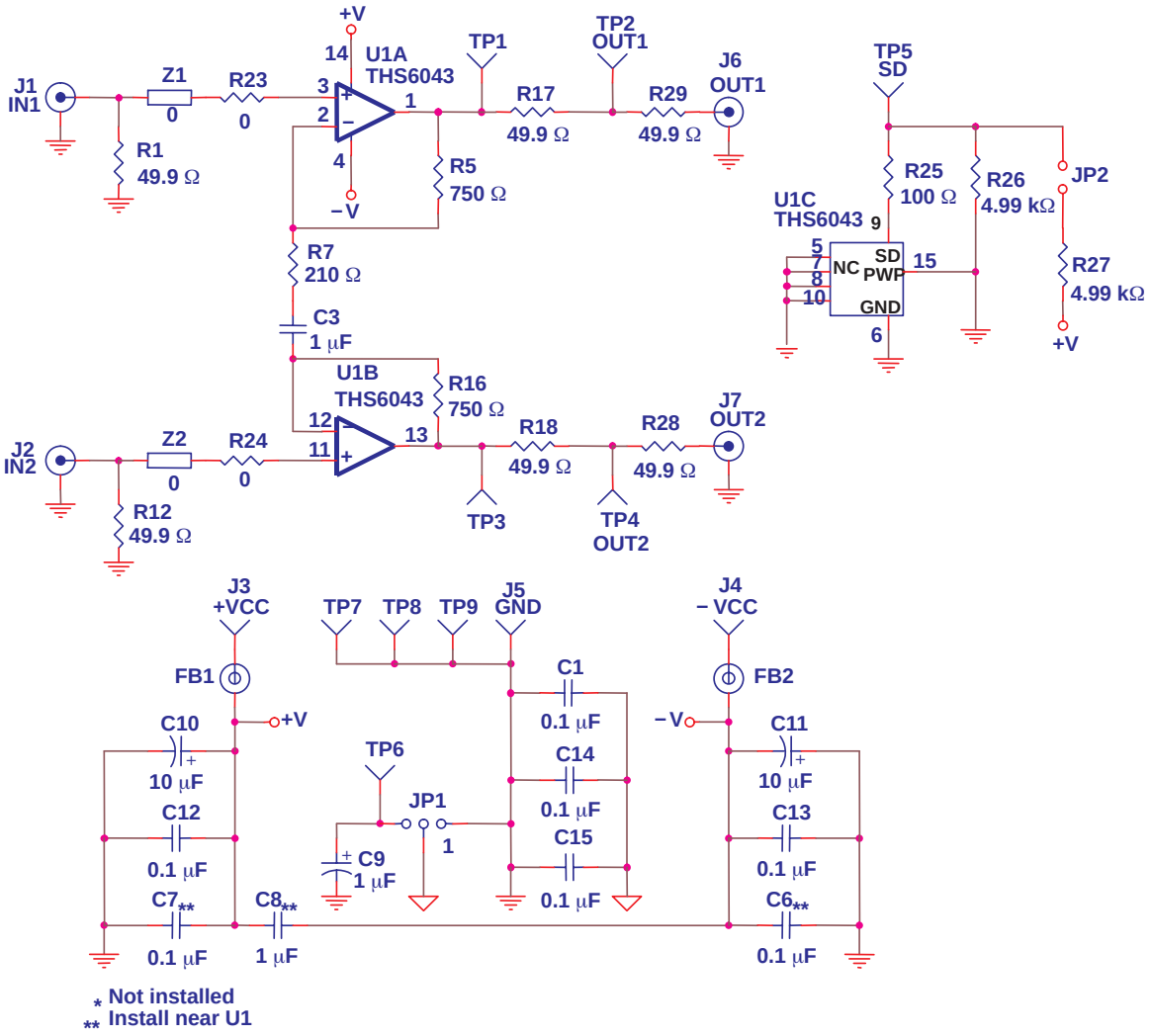
1.4 EVM Default Configuration

The EVM has a fully functional example circuit; just add power supplies, a signal source, and monitoring instrument. See Figure 1−1 for the default schematic diagram. The complete EVM schematic in Chapter 5 shows all component locations.

The default configuration assumes a differential gain, as determined by R5, R16, and R7 in combination with series matching resistors R17 and R18, and assumes a 50-Ω load on the outputs at J6 and J7.

Some components such as R10, R25 through R27, C6 through C15, FB1, FB2, JP1, J3, J4, and J5 are omitted on the application schematics of Chapter 3 for clarity.

Figure 1−1. Schematic of the Populated Circuit on the EVM (Default Configuration)



Chapter 2

Using the THS6043EVM

This section describes how to connect the THS6043EVM to test equipment. It is recommended that the user connect the EVM as described in this section to avoid damage to the EVM or the THS6043 installed on the board.

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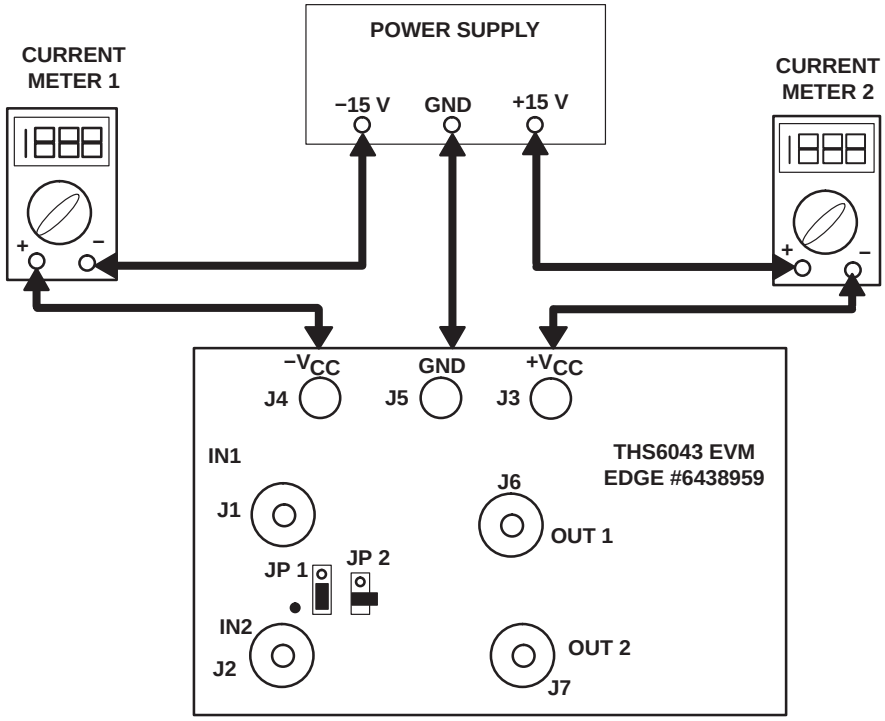
2.1 Test Equipment Required

- ❑ Dual dc output power supply (± 15 V, 200 mA output minimum)
- ❑ Two dc current meters with resolution to 1 mA and capable of the maximum current supplied by the dc power source. *Note: Some power supplies incorporate current meters which may be applicable to this test.*
- ❑ 50-Ω source impedance function generator (1 MHz, 10 V_{pp} sine wave)
- ❑ Oscilloscope (50 MHz bandwidth minimum, 50-Ω terminated BNC Input)

2.2 Power Supply Setup (See Figure 2−1)

- ❑ Set the dc power supply to ±15 V. If available, set the current limit on the dc power supply to 200 mA.
- ❑ Make sure the dc power supply is turned off before proceeding.
- ❑ Connect the +15 V supply to the + input on current meter 2 (if applicable).
- ❑ Connect the – input on current meter 2 to J3 (+Vcc) on the EVM.
- ❑ Connect the –15V supply to the − input on current meter 1 (if applicable).
- ❑ Connect the + input on current meter 1 to J4 (–Vcc) on the EVM.
- ❑ Make sure both dc current meters are set to at least 1 mA resolution and can withstand the maximum output current of the power supplies.
- ❑ Connect the ground(s) of the +15 V and –15 V power supply to J5 (GND) on the EVM.
- ❑ Verify JP1 is connected to the 1−2 position (lower posts).
- ❑ Verify JP2 is not shorting the header pins (connect to only one post).

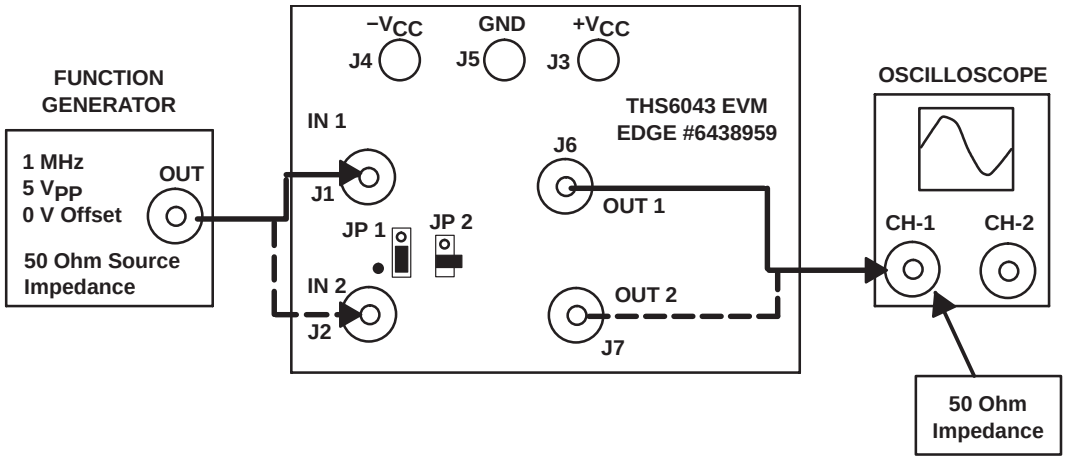
Figure 2−1. Power Supply Connection



2.3 Input and Output Test Setup (See Figure 2−2)

- ❑ Set the function generator to a 1 MHz, ±2.5 V (5 V_{pp}) sine wave with no dc offset.
- ❑ Turn off the function generator before proceeding to the next step.
- ❑ Using a BNC cable, connect the function generator to J1 (IN1 BNC) on the EVM.
- ❑ Using a BNC cable, connect the oscilloscope to J6 (OUT1 BNC) on the EVM. Set the oscilloscope to 1 V/Division and a time base of 0.2 µSec/Division. *Note : The Oscilloscope must be set to 50-Ω termination for proper operation.*

Figure 2−2. Signal Connections



Chapter 3

THS6043EVM Applications

Example applications are presented in this chapter. These applications demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. That, after all, is the function of an evaluation board.

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3.1 Standard Gain Configuration

The THS6043EVM default configuration is a fully differential input, fully differential output gain stage as shown in Figure 3−1. This gain is calculated according an equation that is similar to the one that describes an instrumentation amplifier:

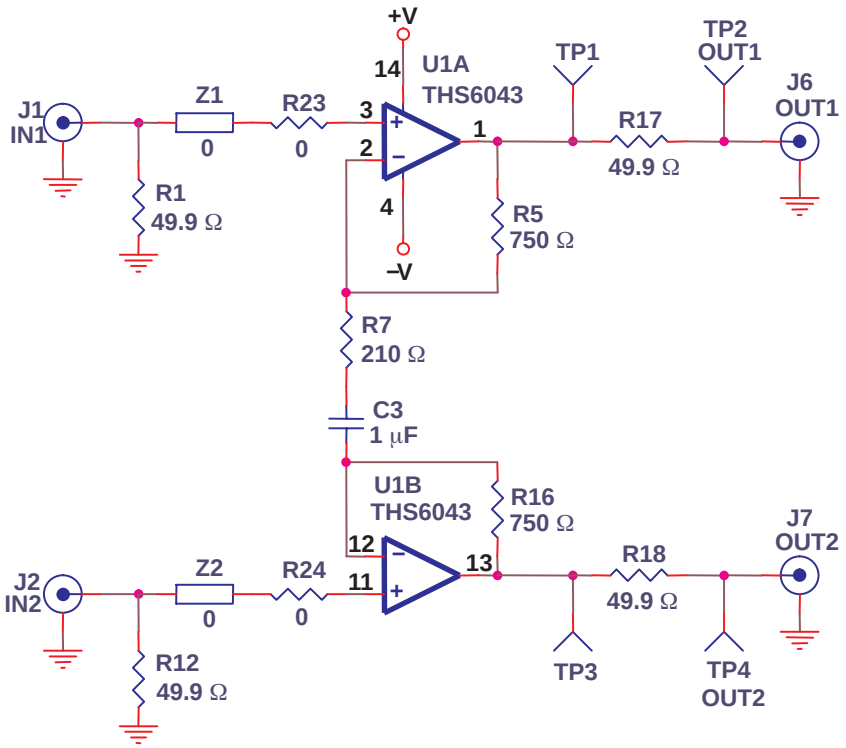
$$\text{Differential gain} = \frac{V_O(\text{diff})}{V_I(\text{diff})} = 1 + \frac{2 \times R5}{R7} \quad (1)$$

Where:

R5 = R16

Series resistors R17 and R18 affect output voltage at J6 and J7. Designers need to take the voltage divider law into account for their load impedance and R17/R18.

Figure 3−1. Default Configuration Operation



3.2 Single Supply Operation

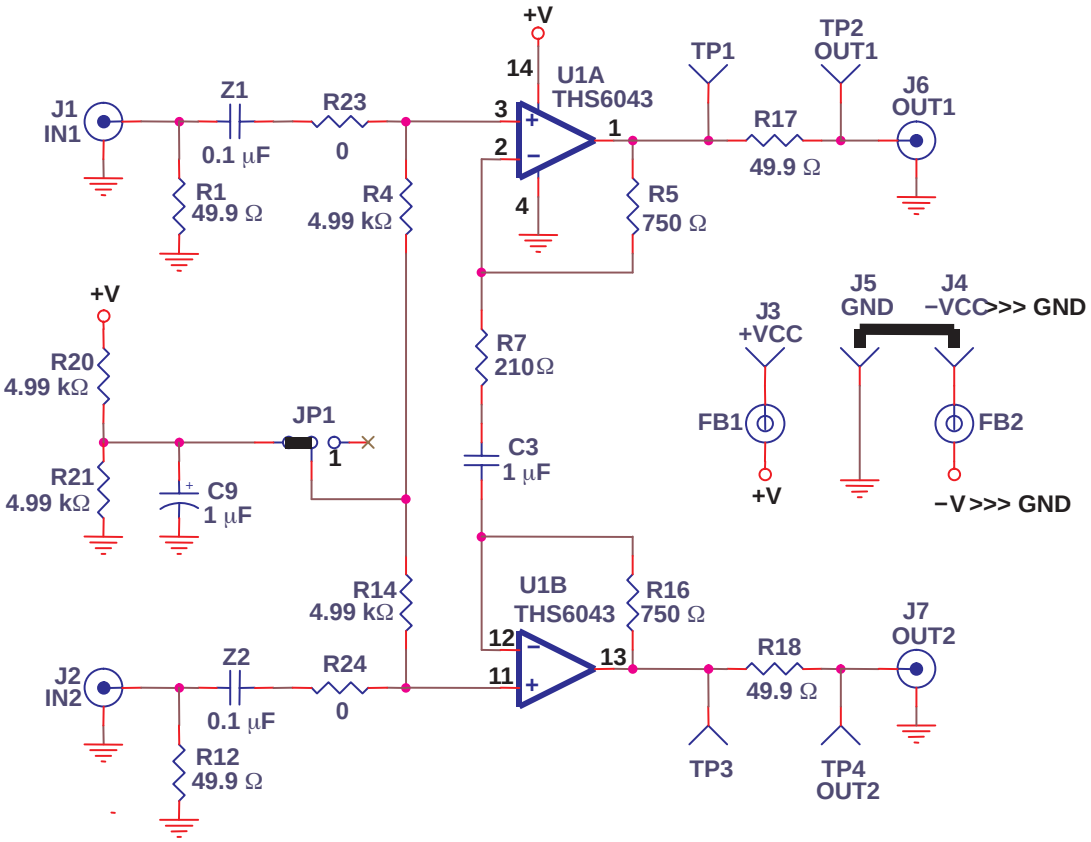
Many designs use single supply voltages, and the THS6043EVM allows single supply operation. The THS6043EVM can be reconfigured for single supply operation as shown in Figure 3−2. To convert to single supply operation:

- ❑ Connect ground from the power supply to both J5 (GND) and J4 ($-V_{CC}$).
- ❑ Jumper pins 2 and 3 of JP1 together with a jumper plug. This enables connection to a *half supply* voltage divider.
- ❑ Populate R4, R14, R20, and R21, with 4.99 kΩ 1% resistors. R20 and R21 create the *half supply* potential (virtual ground for the stage). R4 and R14 sum this potential into the noninverting inputs of the op amps.

The *half-supply* virtual ground potential is also present on the output of the op amps. No provision has been made on the EVM for output dc-blocking capacitors. When the outputs are monitored with equipment that has 50-Ω inputs, 75 mW is dissipated through R17, R18, and the input resistors of the measuring equipment.

- ❑ Remove the zero Ω jumpers located at Z1 and Z2 and replace them with dc-blocking capacitors.

Figure 3−2. Single-Supply Operation



3.3 Active Termination

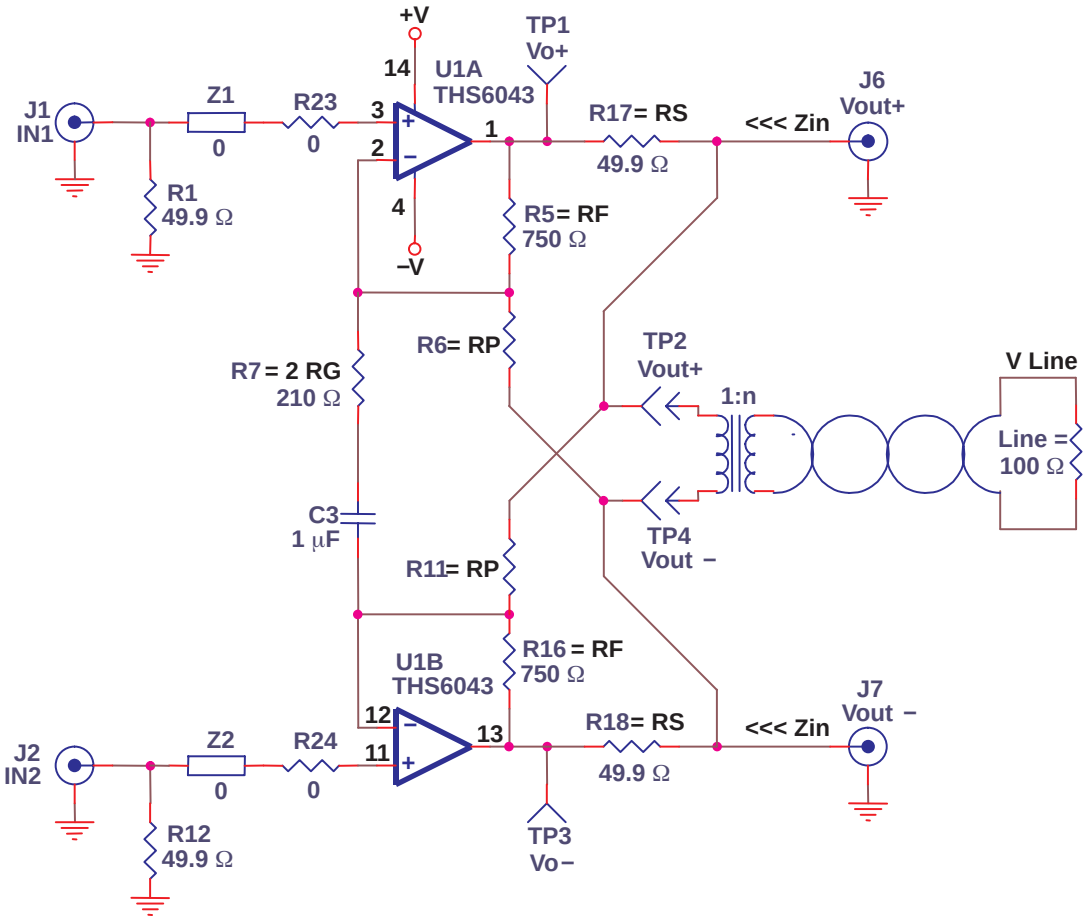
Active termination is a technique that allows the designer to use a small value resistor for the series resistance (R17 or R18). The circuit then uses positive feedback to make the impedance of this resistor appear much larger, when looking from the line side. This accomplishes two things:

1) A very small resistance is evident when the line driver amplifier transmits signals to the line. This lowers the driver stage output voltage swing range requirement.

2) Proper matching impedance when looking from the line to the amplifier

Figure 3−3 shows the basic circuit for differential positive feedback.

Figure 3−3. Differential Positive Feedback



Active feedback creates larger impedance (Z) than what is actually placed there by series resistors R_S:

$$Z(\Omega) = \frac{R_S}{1 - \frac{R_F}{R_P}} \qquad (2)$$

The important thing to consider is that regardless of the forward gain from Vin to Vo, the active impedance (Z) value remains constant.

Now that the return impedance is corrected, forward voltage gain from input to output is calculated. Equation 3 shows the simplified forward gain from Vin to Vo.

$$A_V = \frac{V_O \pm}{V_{in} \pm} = \frac{1 + \left(\frac{R_F}{R_G \| R_P}\right)}{1 - \left(\frac{R_F}{R_P}\right)\left(\frac{R_L}{R_L + R_S}\right)} \text{ iff } R_L << R_P \quad (3)$$

Where:

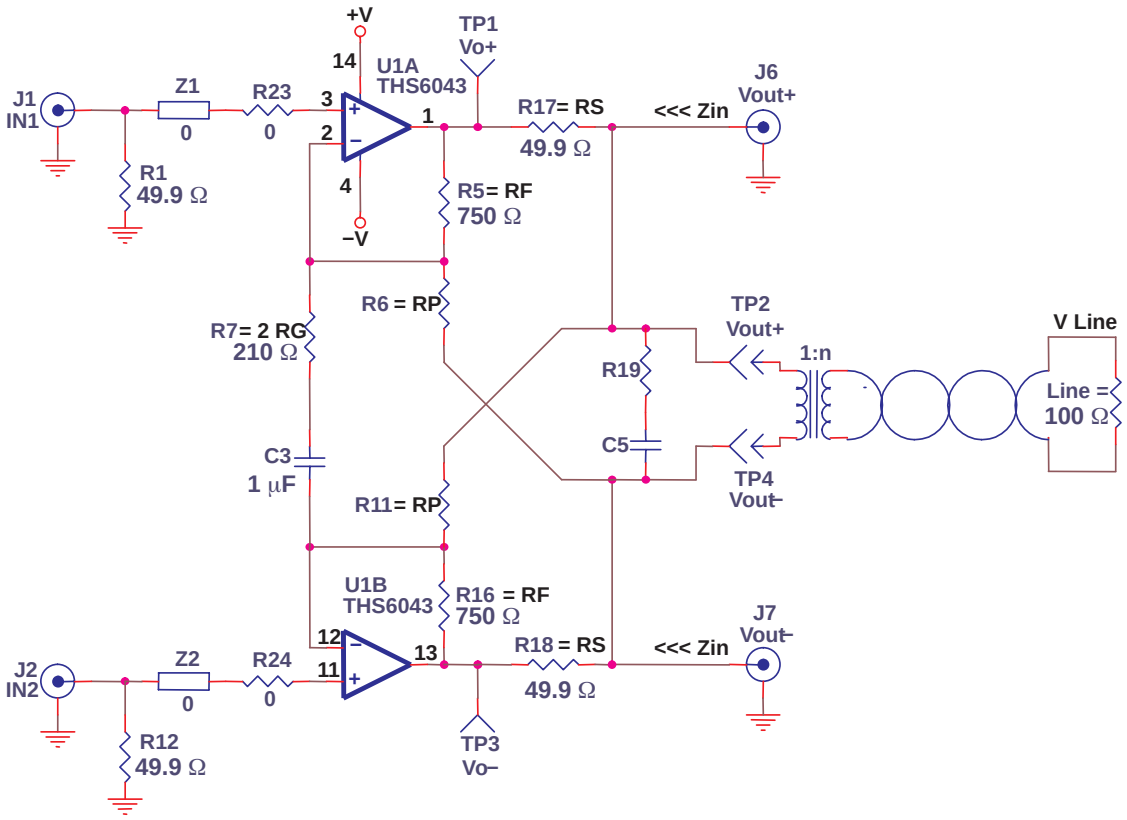
$$R_L = \frac{R_{LINE}}{2\,n^2} \quad (4)$$

Where n is the turn ratio of the transformer.

The reader is cautioned that active termination is a very complex topic, with many considerations. Carefully read the Texas Instruments application report *Active Output Impedance for ADSL Line Drivers*, SLOA100 to gain a more complete understanding of the topic and all of the subtle implications of active termination.

3.4 Snubber Circuit

Figure 3−4. Addition of Snubber Circuit to Active Termination



R19 and C5 are located on the EVM so that a snubber circuit may be implemented. Some transformers have a high resonance frequency (as low as 25 MHz but as high as 150 MHz). When using traditional termination (just R17 and R18—no active termination), there is typically no reason to use these components. But, when active termination is used, the effective impedance of these two resistor values drops substantially. Thus, there can be very small resistor isolation between the amplifier—and a resonance problem. Couple this with the feedback path of R6 and R11, and this can cause the amplifier to oscillate. The snubber is utilized to eliminate this oscillation. As a rule of thumb, use the following calculations to select the proper snubber values:

$$R19 = 2 \times \frac{R_{LINE}}{n^2} \tag{5}$$

Then select C5:

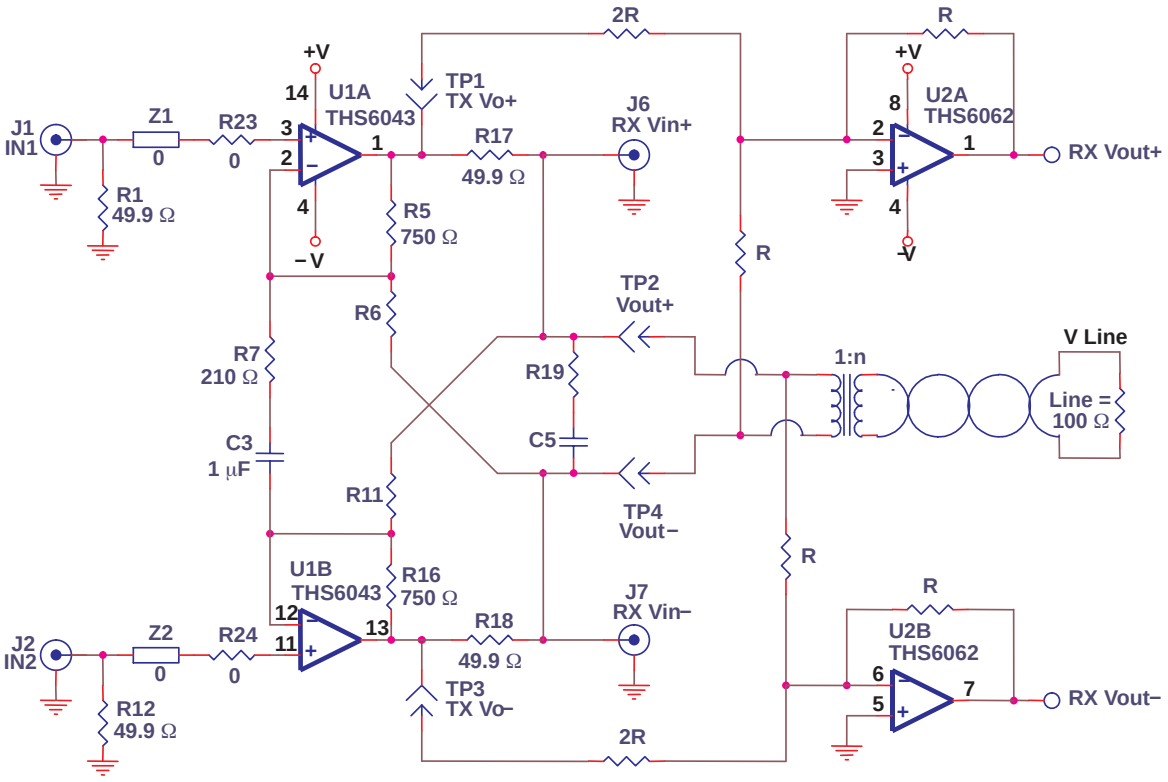
$$C5 = \frac{1}{2 \times \pi \times R19 \times F_C} \tag{6}$$

where F_C = at least 10 X the highest operating frequency (1.104MHz is the highest ADSL operating frequency). 20X or even larger may be preferable.

3.5 Receive Path Implementation

Test points TP1 through TP4 are located on the EVM to facilitate the addition of the receive signal path to the signal chain as shown in Figure 3−5. When implementing the receive path, a *hybrid* must be used since ADSL is full duplex. The hybrid cancels out the TX signal and allows the RX signal from the line to come through. The THS6043EVM does not include receive or *hybrid* circuitry. Texas Instruments assumes that customers prefer to implement their own propriety hybrid design. This makes sense as each customer knows their nominal line impedance characteristics, and is able to match them better. Texas Instruments does have an EVM that contains a THS6062 ADSL receiver, and this EVM can be purchased separately to facilitate construction of a complete ADSL transmit/receive interface.

Figure 3−5. Implementation of the Receive Signal Path

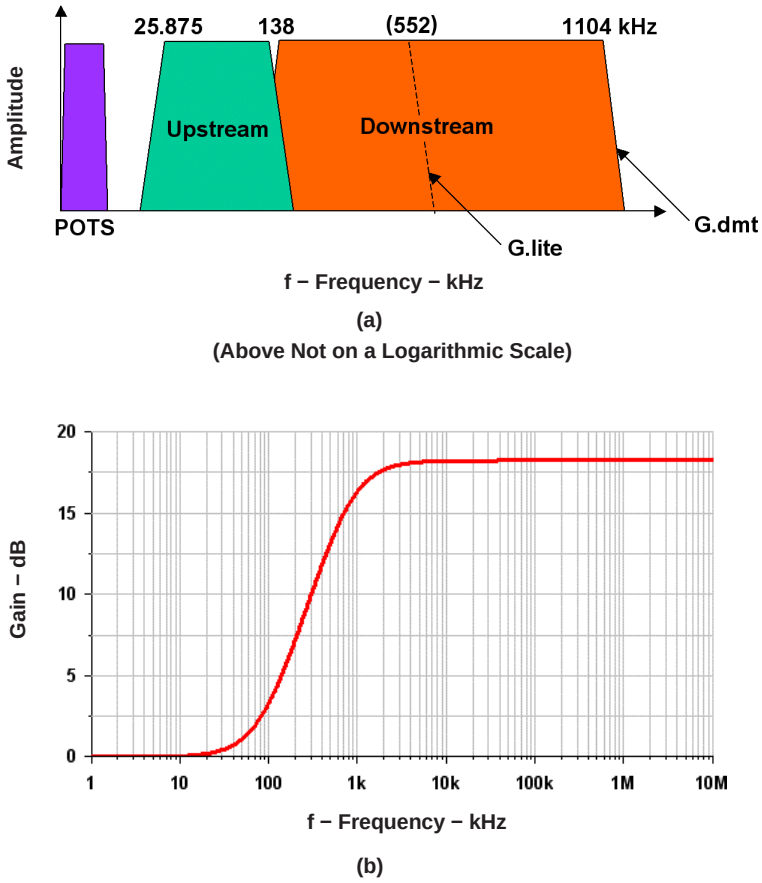


3.6 High-Pass Filter

Because ADSL CPE is designed to transmit from 25.875 kHz to 138 kHz, C3 and R7 can be used to implement an HPF function. These are selected to be 20X lower than 25 kHz (1.25 kHz) or so. Some designs use a capacitor—some do not. This path allows for a common gain setting between the two channels. This helps (but does not assure) that the signals are truly differential.

Figure 3−6 compares the frequency spectrum of ADSL to a simulation of the high-pass filter on the THS6043EVM.

Figure 3−6. ADSL Spectrum and High-Pass Filter Response



Note that the high-pass filter function is not a true high pass filter. C3 in series with R7 creates a zero at about 10 Hz. As the frequency decreases from about 3 kHz to 10 Hz, the circuit changes from a gain stage into two unity gain buffers.

3.7 Noninverting Single-Ended Gain Stages

Although ADSL is the obvious application for the THS6043EVM, it can also be configured for other applications.There are component locations on the EVM that allow various dc- and ac-coupled gain stages to be constructed.

Referring to Figure 3−7, for example, two dc-coupled noninverting gain stages could be formed by:

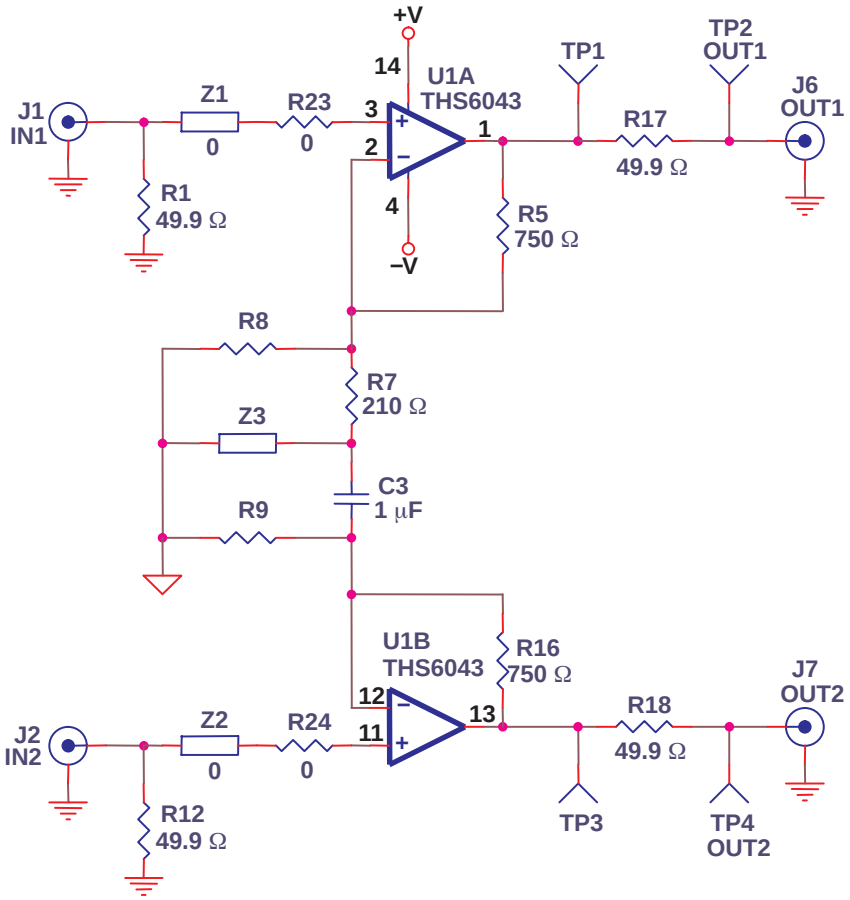
- ❑ Removing R7 and C3
- ❑ Making R8 and R9 gain resistors for the two individual stages.

An ac-coupled gain stage for the top amplifier can be constructed by:

- ❑ Removing R7 and C3
- ❑ Making R8 and R9 gain resistors for the two individual stages.
- ❑ Using a dc blocking capacitor at locations Z1 and Z3

There are many possibilites—these suggestions are not meant to limit the options of the user.

Figure 3−7. Independent Single-Ended Noninverting Gain Configuration

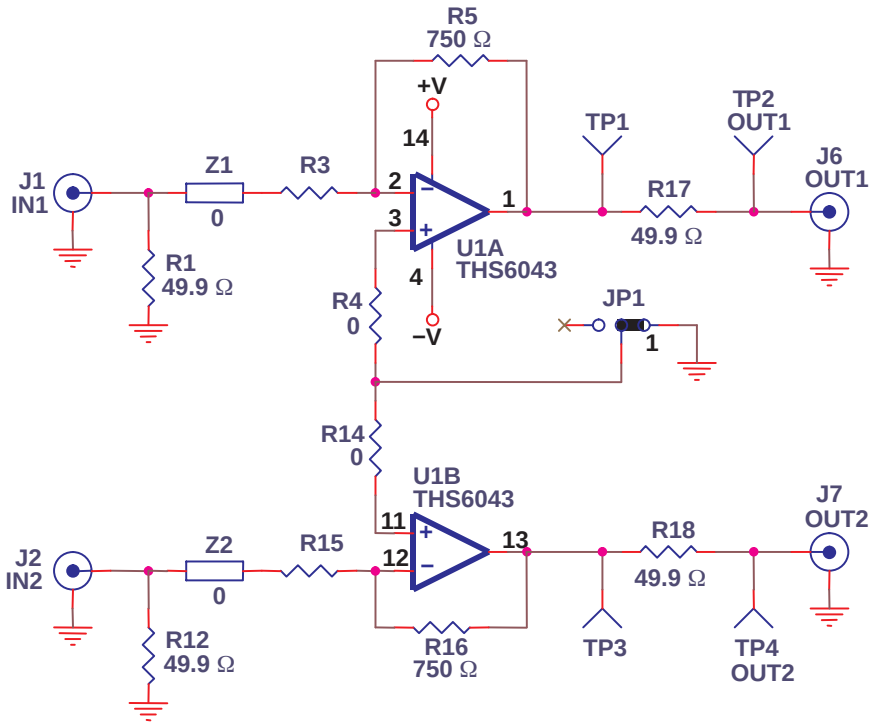


3.8 Independent Single-Ended Inverting Gain Stages

Two independent inverting gain stages can be created by:

- ❑ Removing R7, R23, R24, and C3
- ❑ Adding zero Ω jumpers at R4 and R14
- ❑ Jumper pins 1 and 2 of JP1
- ❑ Adding gain resistors (Rg) at R3 and R15. Gain (Av) for each stage is calculated by –Rf / Rg (−R5 / R3 and –R16 / R15).

Figure 3−8. Independent Single-Ended Inverting Gain Configuration

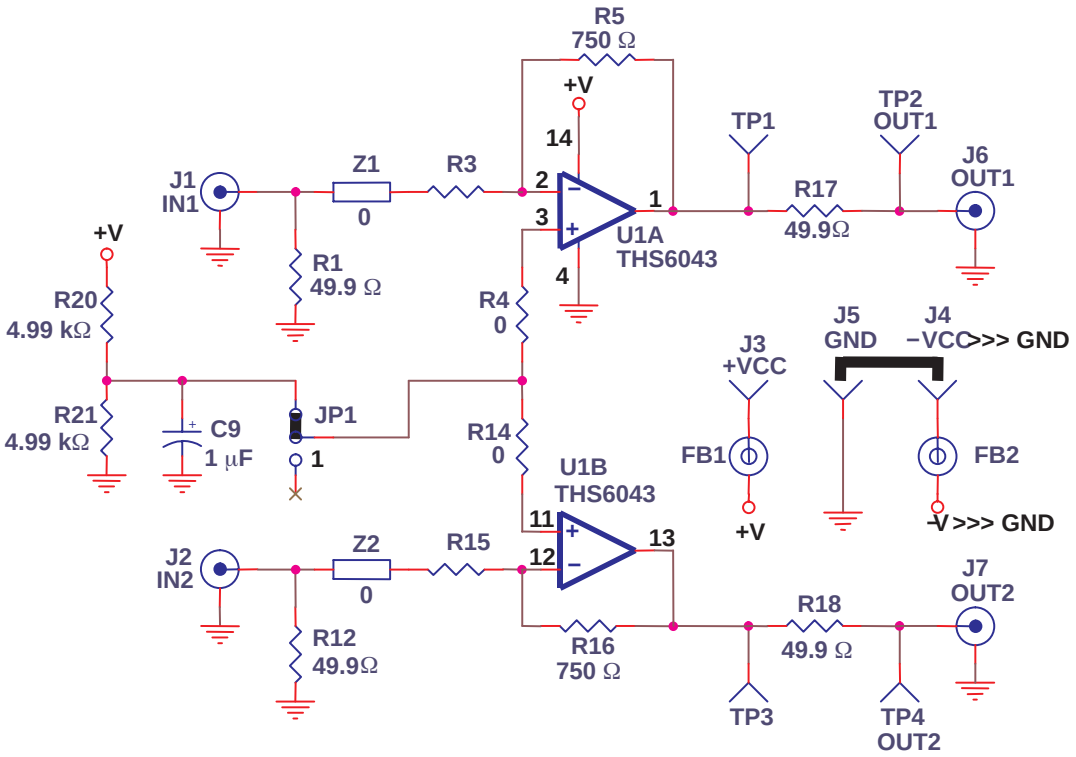


3.9 Independent Single-Supply Single-Ended Inverting Gain Stages

Two independent inverting gain stages can be created by:

- ❑ Connecting the $-V_{CC}$ supply (J4) to GND (J5)
- ❑ Removing R7, R23, R24, and C3
- ❑ Addinging zero Ω jumpers at R4 and R14
- ❑ Installing 4.99 kΩ resistors at locations R20 and R21
- ❑ Jumpering pins 2 and 3 of JP1
- ❑ Adding gain resistors (Rg) at R3 and R15. Gain (Av) for each stage is calculated by –Rf / Rg (−R5 / R3 and –R16 / R15).

Figure 3−9. Independent Single−Ended Single−Supply Inverting Gain Configuration



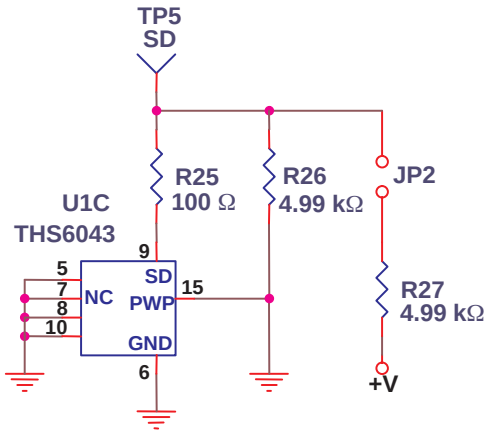
3.10 Shutdown Operation (Channels 1 and 2)

The output of channels 1 and 2 can both be shut down simultaneously when a voltage above 2 Vdc is applied to the shutdown input (JP2 on the EVM—see Figure 3−10). In shutdown mode, the output goes to ground. Normal operation is restored for voltages below 0.8 V on the shutdown (SD) input.

When no jumper is installed in position JP2, the SD input is pulled to ground through R26. When a jumper is installed in position JP2, a voltage

divider is formed by R26 and R27, taking the SD input to +V/2, which disables the outputs of the EVM. Please note that due to the low-value input and feedback resistors, some signal leaks from the inputs to the outputs of the EVM.

Figure 3−10. Shutdown Operation



Chapter 4

High-Speed Amplifier PCB Layout Tips

The THS6043EVM layout has been designed for use with high-speed signals and can be used as an example when designing PCBs incorporating the THS6043. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregarding these basic design considerations could result in less than optimum performance of the THS6043 high-speed operational amplifier. Surface-mount components are selected because of the extremely low lead inductance associated with this technology. This helps minimize both stray inductance and capacitance. Also, because surface-mount components are physically small, the layout can be very compact.

Tantalum power supply bypass capacitors at the power input pads help filter switching transients from the laboratory power supply. Power supply bypass capacitors are placed as close as possible to the IC power input pins in order to minimize the return path impedance. This improves high frequency bypassing and reduces harmonic distortion. The GND side of these capacitors should be located close to each other, minimizing the differential current loops associated with differential output currents. If poor high frequency performance is observed, replace the 0.1-μF capacitors with microwave capacitors with a self-resonance at the frequency that produces trouble. A proper ground plane on both sides of the PCB should be used with high-speed circuit design. This provides low-inductive ground connections for return current paths.

In the area of the amplifier input pins, however, the ground plane has been removed to minimize stray capacitance and to reduce ground plane noise coupling into these pins. This is especially important for the inverting input pin. As low as 1 pF capacitance at the inverting input can significantly affect the response of the amplifier or even cause oscillation.

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Such a signal line must also be properly terminated with an appropriate resistor.

The printed-circuit board that is used with PowerPAD packages must have features included in the design to remove the heat from the package efficiently. As a minimum, there must be an area of solder-tinned-copper underneath the PowerPAD package. This area is called the thermal land. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed in http://www−s.ti.com/sc/techlit/slma002 and http://www−s.ti.com/sc/techlit/slma004.

Finally, all inputs and outputs must be properly terminated, either in the layout or in the load instrumentation. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in the amplifier's phase−margin and improves the amplifier stability resulting in reduced peaking and settling times.

On boards operated from dual power supplies, it is helpful to place a capacitor directly across the positive and negative power supplies. This helps the fully differential drive.

Chapter 5

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed circuit board layout.

Table 5−1. THS6043EVM Bill of Materials

Item	Description	Reference Designator	PCB QTY	Manufacturer's Part Number	Distributor's Part Number
1	Bead, Ferrite, 3A, 80 Ω, SMD size 1206	FB1, FB2	2	(Steward) HI1206N800R−00	(Digi-Key) 240−1010−1−ND
2	Open, size 1206	C5	1		
3	Cap, 1.0 µF, tantalum, 35 V, SMT size B	C9	1	(AVX) TAJB105K035R	(Garrett) TAJB105K035R
4	Cap, 10 µF, tantalum, 35 V, SMT, size D	C10, C11	2	(AVX) TAJD106K035R	(Garrett) TAJD106K035R
5	Cap, 1.0 µF, ceramic, +80% − 20%, 50 V, SMD size 1210	C8	1	(AVX) 12105G105ZAT2A	
6	Cap, 1.0 µF, ceramic, X7R, 25 V, SMD size 1206	C3	1	(AVX) 1063C105KAT2A	(TTI) 1063C105KAT2A
7	Cap, 0.1 µF, ceramic, X7R, 50 V, SMD size 0805	C1, C6, C7, C12, C13, C14, C15	7	(AVX) 08055C104DAT2A	(Garrett) 08055C104KAT2A
8	Resistor, 0 Ω, SMD size 0805	R23, R24	2	(KOA) RM73Z2A000	(Garrett) RM73Z2A000
9	Resistor, 100 Ω, 1/8 W, 1%, SMD size 0805	R25	1	(Phycomp) 9C08052A1000KHFT	(Garrett) 9C08052A4990FKHFT
10	Resistor, 210 Ω, 1/8 W, 1%, SMD size 0805	R7	1	(Phycomp) 9C08052A2100FKHFT	(Garrett) 9C08052A2100FKHFT
11	Resistor, 750 Ω, 1/8 W, 1%, SMD size 0805	R5, R16	2	(Phycomp) 9C08052A7500FKHFT	(Garrett) 9C08052A7500FKHFT
12	Resistor, 4.99 KΩ, 1/8 W, 1%, SMD size 0805	R26, R27	2	(Phycomp) 9C08052A4991FKHFT	(Phycomp) 9C08052A4991FKHFT
13	Open, size 0805	R3, R4, R6, R8, R9, R11, R14, R15, R20, R21, Z3	11		
14	Open, size 1206	R19	1		
15	Resistor, 0 Ω, size 1206	Z1, Z12,	2	(KOA) RM73Z2B000	(Garrett) RM73Z2B000
16	Resistor, 49.9 Ω, 1/4 W, 1% SMD size 1206	R1, R12, R17, R18, R28, R29	6	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT

17	Header, 0.1” centers, 0.025” square pins	JP1, JP2	2	(Sullins) PZC36SAAN	(Digi-Key) S1011−36−ND
18	Shunts	JP1, JP2	2	(Sullins) SSC02SYAN	(Digi-Key) S9002−ND
19	Test points (red)	TP1 − TP6	6	(Keystone) 5000	(Allied) 839−3600
20	Test points (black)	TP7 − TP9	3	(Keystone) 5001	(Allied) 839−3601
21	Jack, banana receptacle, 0.25” diameter hole	J3, J4, J5	3	(HH Smith) 101	(Newark) 35F865
22	Connector, BNC, vertical, PCB	J1, J2, J6, J7	4	(Amphenol) 31−5329	(Allied) 713−7160 (Newark) 89F2885
23	Standoff, 4−40 hex, 0.625” length		4	(Keystone) 1804	(Allied) 839−2089
24	Screw, Phillips, 4−40, 0.250”		4		
25	IC, THS6043 PWP	U1	1	(TI) THS6043CPWP	
26	PCB,		1	(TI) EDGE #6438959	

Figure 5−1. Top Layer 1 of THS6043EVM

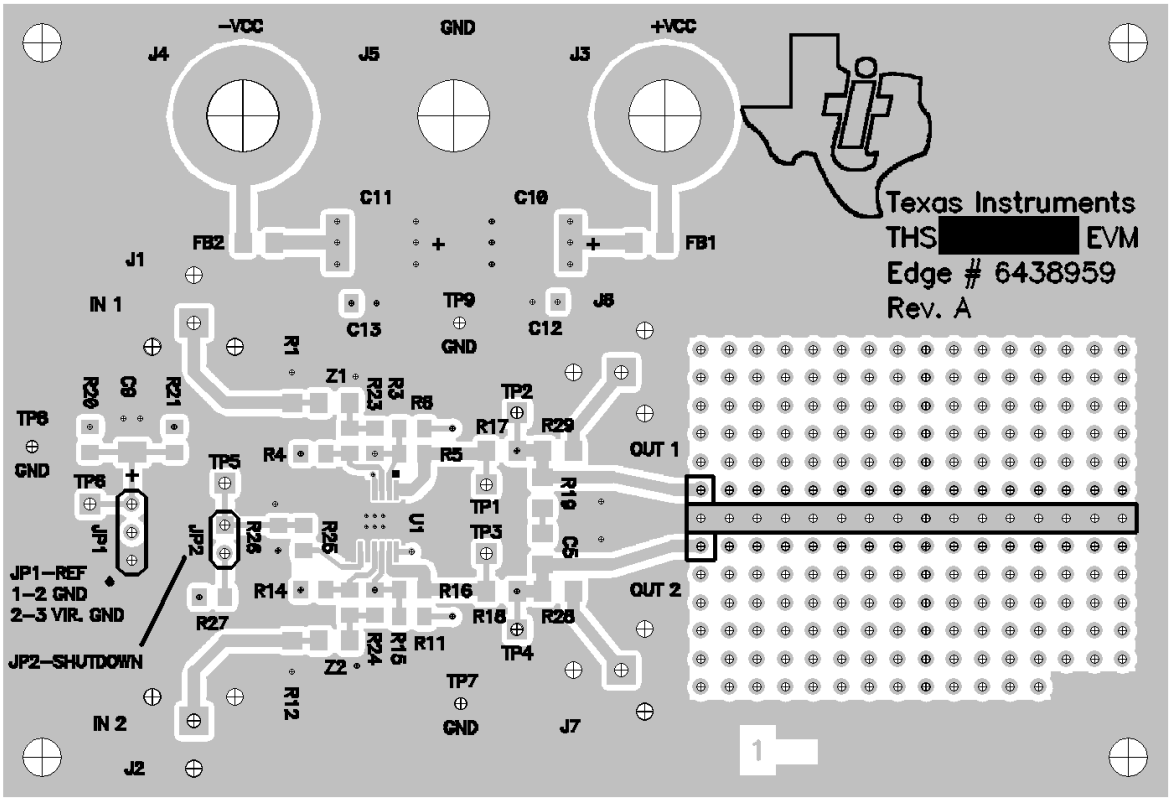


Figure 5−2. Internal Plane (Layer 2)

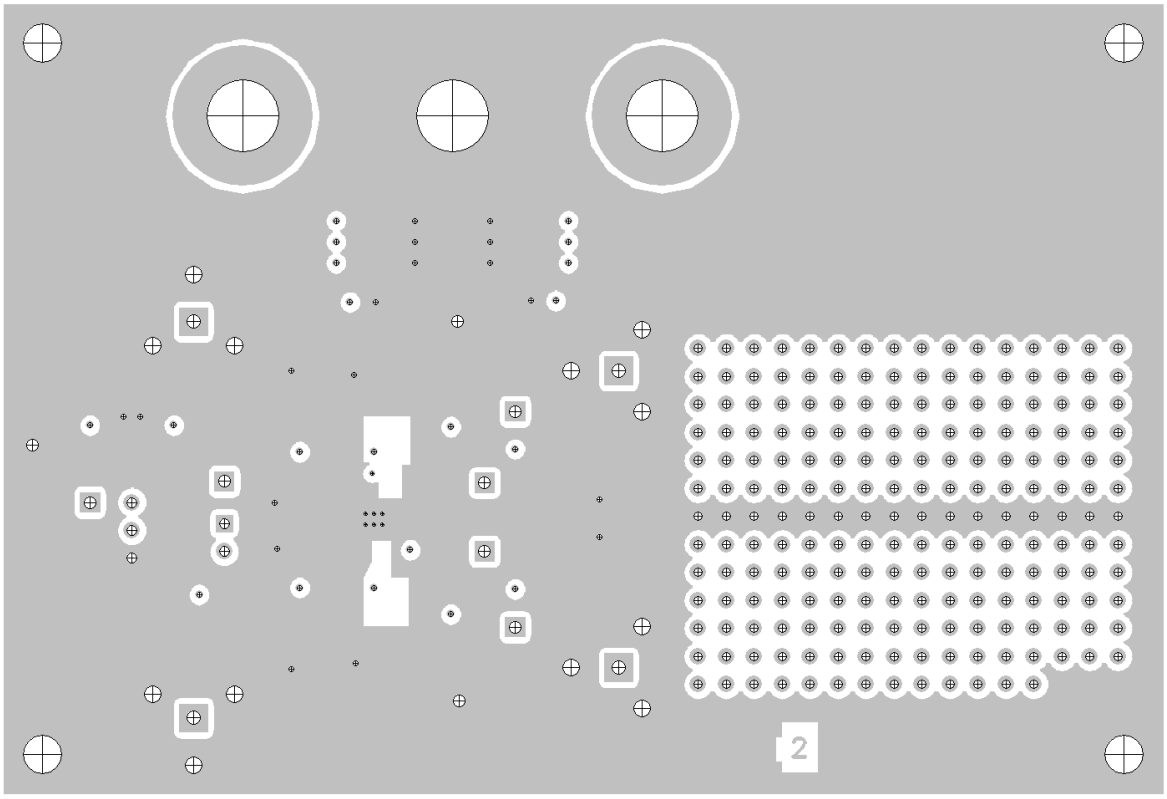


Figure 5−3. Internal Plane (Layer 3)

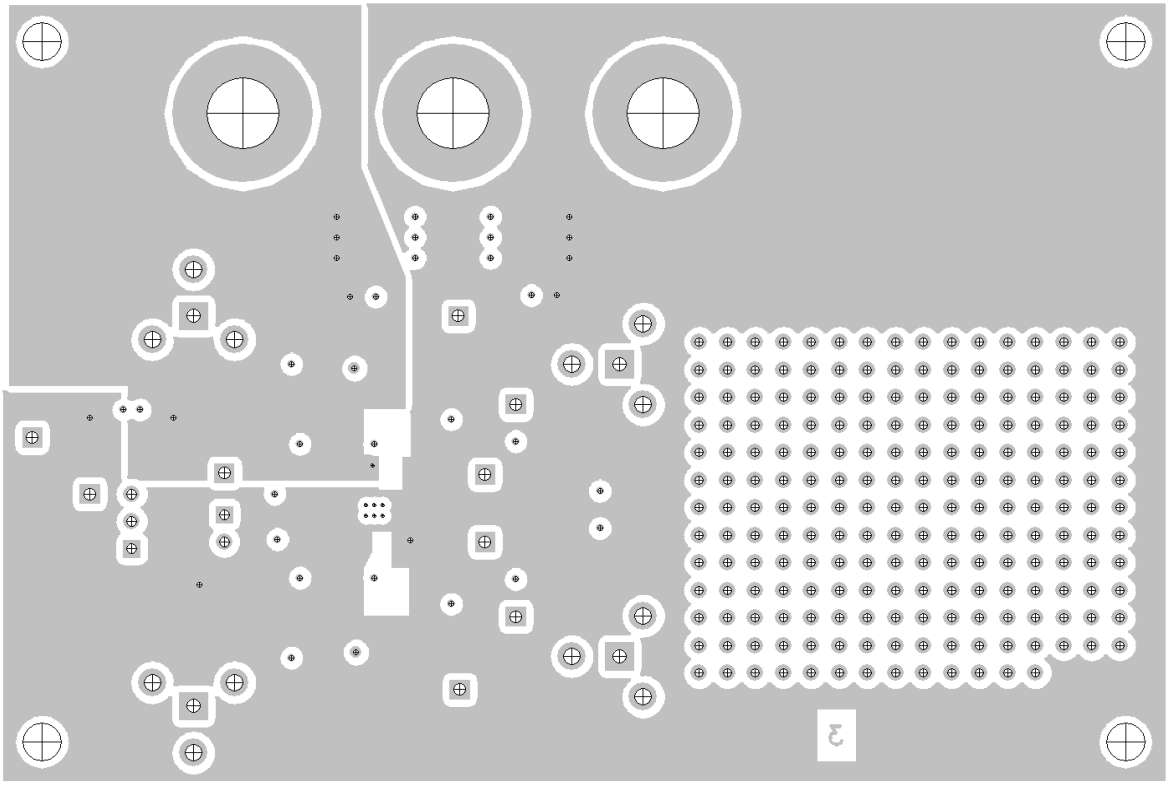


Figure 5−4. Bottom (Layer 4)

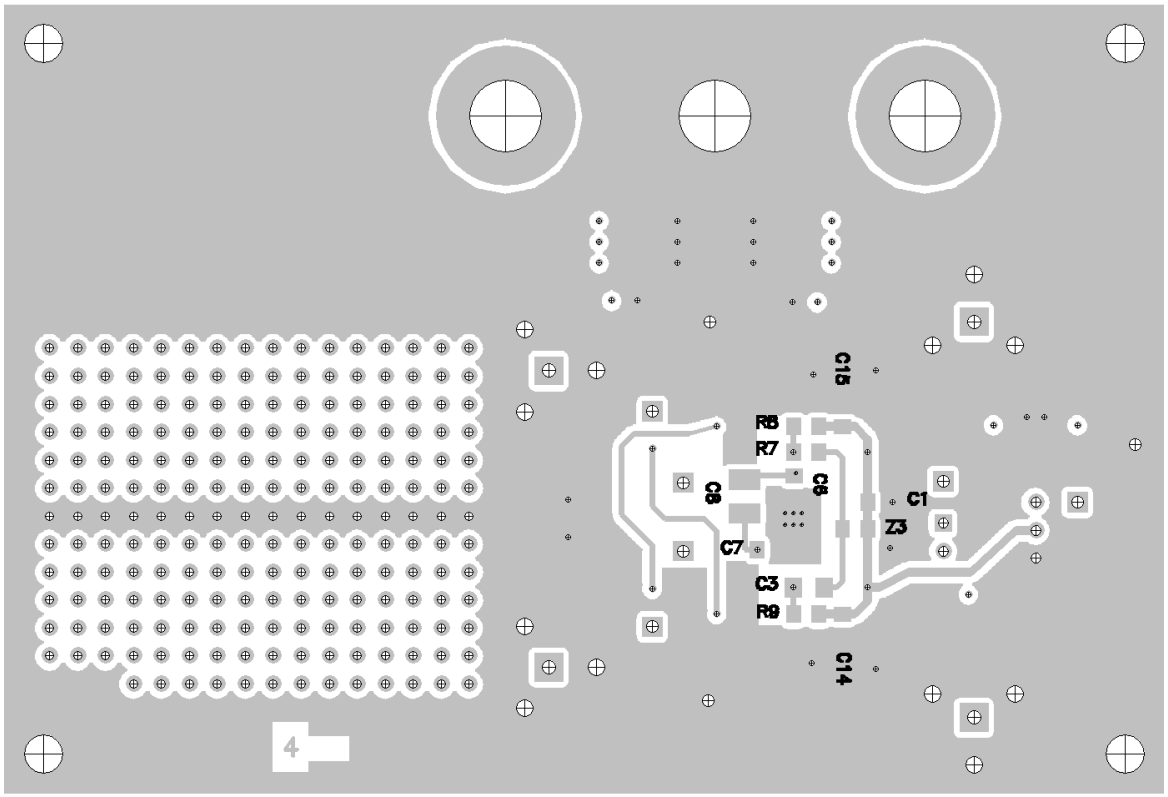
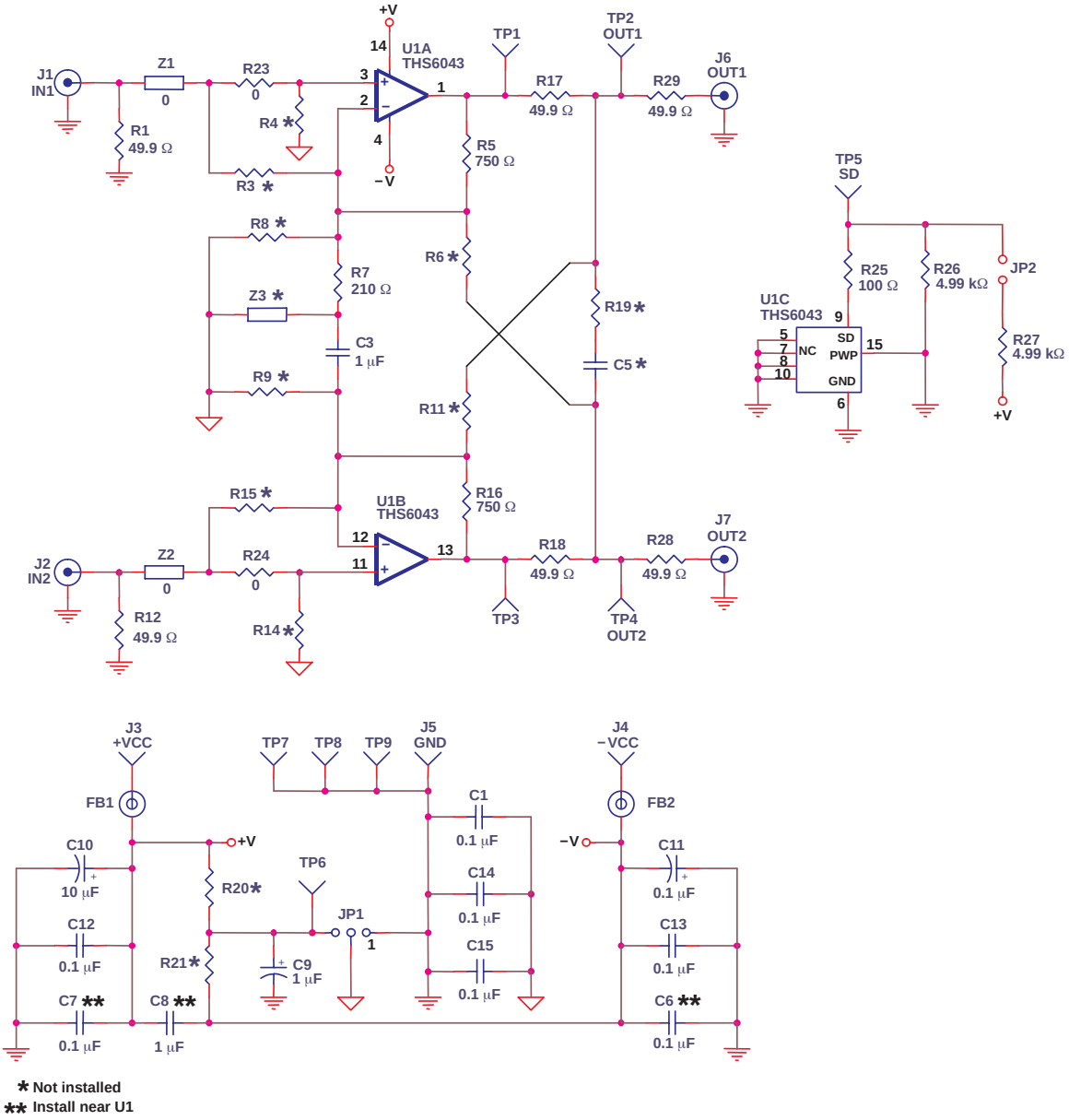


Figure 5−5. Full Schematic of the THS6043EVM



* Not installed
** Install near U1