MP6506

2.7V-to-15V, 500mA, Bipolar Stepper-Motor Driver with Integrated MOSFETs

The Future of Analog IC Technology

DESCRIPTION

The MP6506 is a bipolar stepper-motor driver with dual, built-in full-bridges consisting of N-channel power MOSFETs.

It operates from a supply voltage range of 2.7V to 15V, and can deliver motor current up to 500mA per channel. The internal safety features include under-voltage lockout and thermal shutdown. An over-temperature output flag is available to indicate thermal shutdown.

The MP6506 is available in a 3mm×3mm QFN package with an exposed thermal pad on the back.

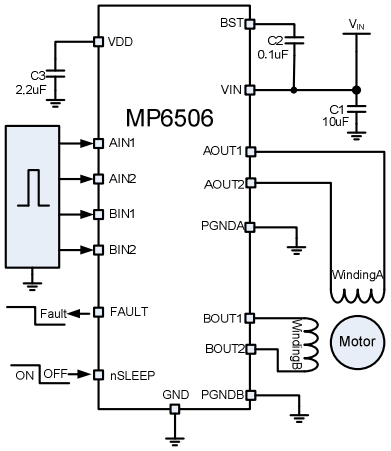
FEATURES

- Wide 2.7V-to-15V Input Voltage Range
- Two Internal Full-Bridge Drivers
- Low MOSFET On Resistance (HS: 500mΩ; LS: 500 mΩ)
- Internal Charge Pump for the High-Side Driver
- Low Quiescent Current: 1.1mA
- Low Sleep Current: 1μA
- Thermal Shutdown and Under-Voltage Lockout Protection
- Over-Temperature Output Flag
- Thermally-Enhanced Surface-Mount Package

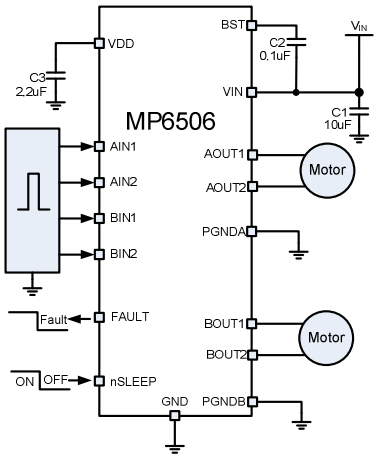
APPLICATIONS

- POS Printers
- Video Security Camera
- Digital Still Cameras
- Battery Powered Toys

TYPICAL APPLICATION



Stepper Motor Application



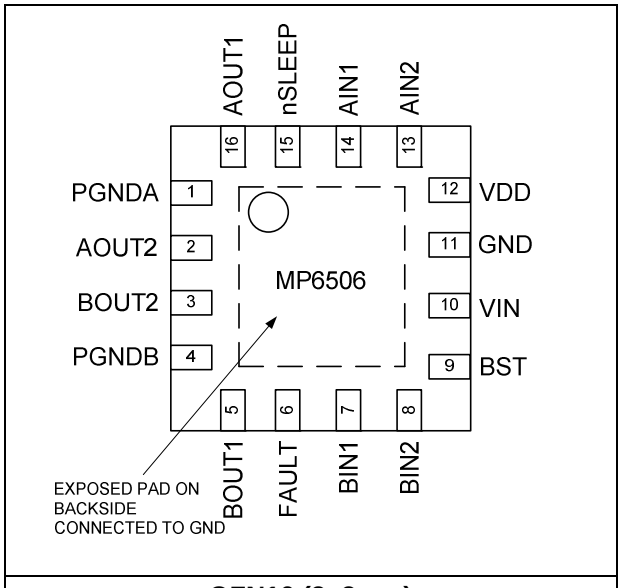
Dual DC Motor Application

ORDERING INFORMATION

Part Number	Package	Top Marking
MP6506GQ*	QFN16 (3×3mm)	AJU

* For Tape & Reel, add suffix –Z (e.g. MP6506GQ–Z);

PACKAGE REFERENCE



QFN16 (3×3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... -0.3V to 18V
AOUTx Voltage V_{AOUTx} .....-0.3V to V_{IN}+1V
BOUTx Voltage V_{BOUTx} .....-0.3V to V_{IN}+1V
BST Voltage V_{BST}.....-0.3V to V_{IN}+7V
All Other Pins..... -0.3V to 6.5V
Junction Temperature.....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A = +25°C) (2)
QFN16 (3×3mm).....2.1W
Operating Temperature.....-40°C to +85°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 15V
Output Current $I_{A/BOUT}$.....500mA
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN16(3×3mm) .....60 ..... 12 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} =2.7V to 15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Type	Max	Units
Power Supply						
Input Supply Voltage	V_{IN}		2.7		15	V
Quiescent Current	I_{IN}	nSLEEP=1, I_{OUT}=0, Output disable			1.1	mA
	I_{IN_SLEEP}	nSLEEP=0, V_{IN}=5V			1	μA
Integrated MOSFETs						
Output On Resistance	R_{HS}	I_{OUT}=500mA, V_{IN}=5V T_J=25°C		460		mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=25°C		565	600	mΩ
		I_{OUT}=500mA, V_{IN}=5V T_J=85°C		570		mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=85°C		700		mΩ
	R_{LS}	I_{OUT}=500mA, V_{IN}=5V T_J=25°C		395		mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=25°C		515	600	mΩ
		I_{OUT}=500mA, V_{IN}=5V T_J=85°C		490		mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=85°C		650		mΩ
Body-Diode Forward Voltage	V_F	I_{OUT}=500mA			1	V
Control Logic						
UVLO Threshold (Rising)	V_{IN_RISE}				2.5	V
UVLO Hysteresis	V_{HYS}			70		mV
Input Logic ‘Low’ Threshold	V_{IL}				0.6	V
Input Logic ‘High’ Threshold	V_{IH}		2			V
nSLEEP Logic, Low	V_{SLEEP_L}				0.4	V
nSLEEP Logic, High	V_{SLEEP_H}		2			V
Fault Output Logic, Low	V_{FAULT_L}	Flag triggered by OTP 1mA Current.			200	mV
Fault Output Leakage Current	I_{LEAK_FAULT}	V_{FAULT}=5V			1	μA
Propagation Delay Time (On)	T_{ON_DELAY}	INx high to OUTx on 10mA Source Current	50	150	250	ns
Propagation Delay Time (Off)	T_{OFF_DELAY}	INx low to OUTx off	50	150	250	ns

ELECTRICAL CHARACTERISTICS *(continued)*

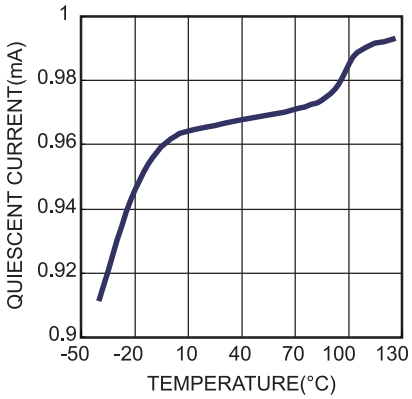
V_{IN} =2.7V to 15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Type	Max	Units
Cross Over Delay	T_{CROSS}	HS off to LS on or LS off to HS on for one bridge arm	200	425	650	ns
Sleep Mode Wakeup Time	T_{WAKE}	Sleep inactive high to full bridge turn on (V_{BST}=100nF)			1.5	ms
Protection Circuitry						
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				15		°C

TYPICAL CHARACTERISTICS

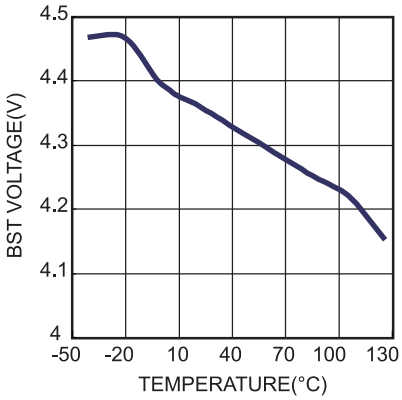
Quiescent Current vs. Temperature

V_{IN}=15V



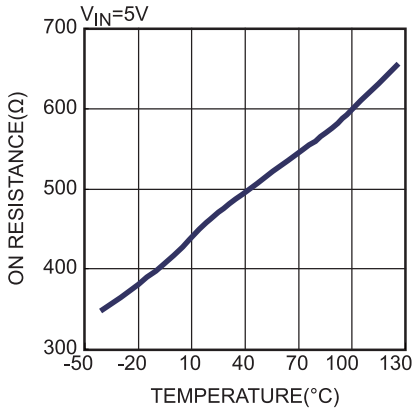
BST Voltage vs. Temperature

V_{IN}=9V



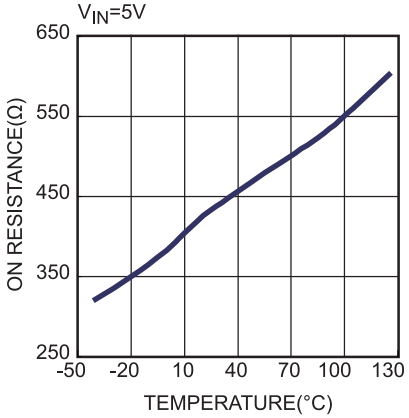
Bridge A HS ON RESIGTANCE vs. Temperature

V_{IN}=5V

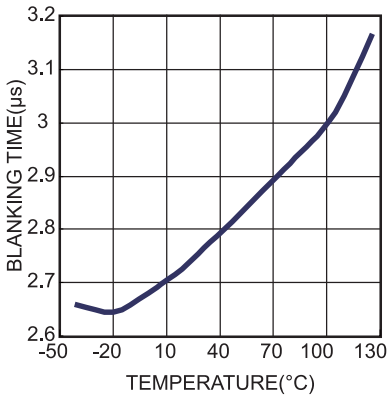


Bridge B HS ON RESISTANCE vs. Temperature

V_{IN}=5V

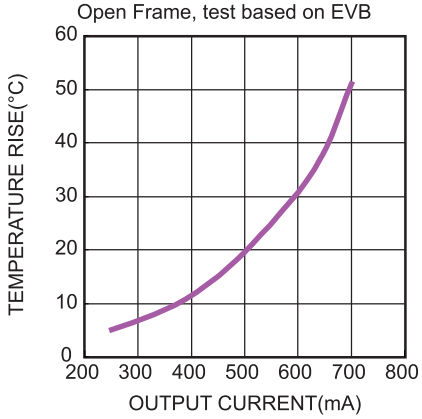


Blanking Time vs. Temperature

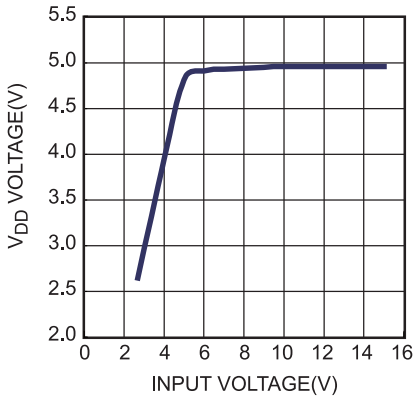


Temperature Rise vs. Output Current

V_{IN}=9V, Full Step(100Hz), T_A=25°C, Open Frame, test based on EVB



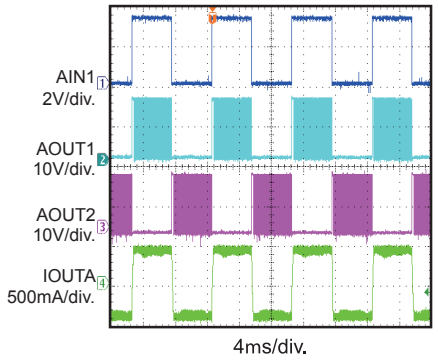
V_{DD} Voltage vs. Input Voltage



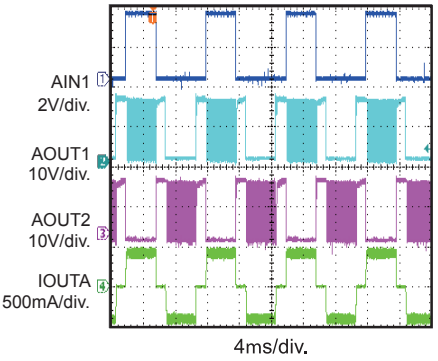
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. I_{OUT}=500mA, F_{STEP}=100Hz, T_A=25°C, unless otherwise noted.

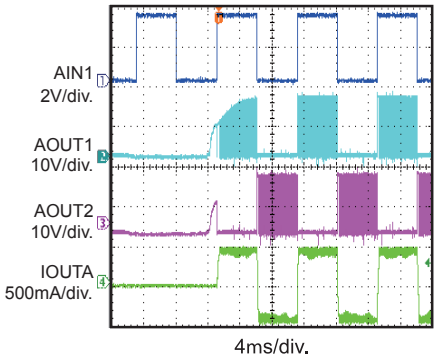
Steady State-Full Step
V_{IN}=15V



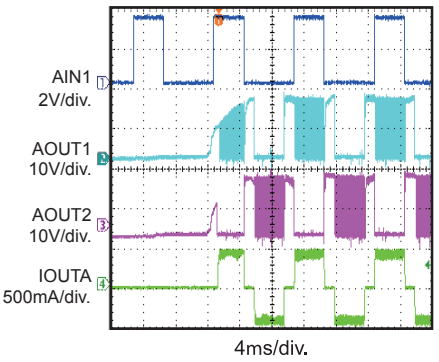
Steady State-Half Step
V_{IN}=15V



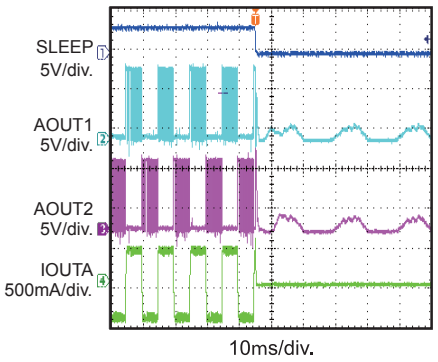
Power Ramp Up-Full Step
V_{IN}=15V



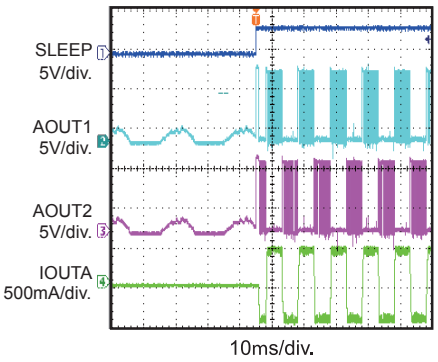
Power Ramp Up-Half Step
V_{IN}=15V



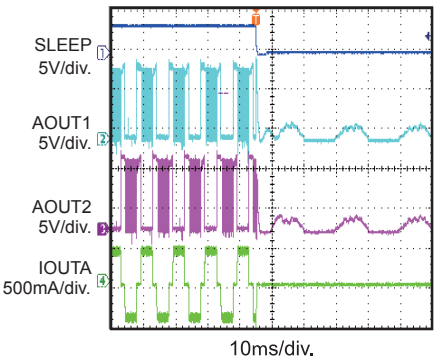
Sleep Entry-Full Step
V_{IN}=9V



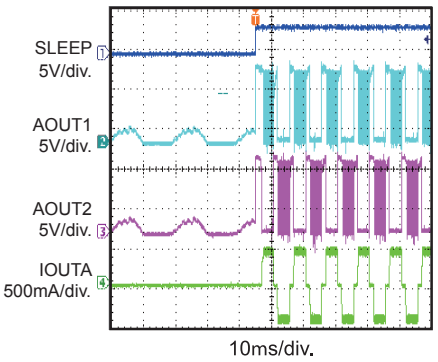
Sleep Recovery-Full Step
V_{IN}=9V



Sleep Entry-Half Step
V_{IN}=9V



Sleep Recovery-Half Step
V_{IN}=9V



PIN FUNCTIONS

QFN16 Pin #	Name	Description
1	PGNDA	Channel A Power Ground.
2	AOUT2	Connect to motor winding A.
3	BOUT2	Connect to motor winding B.
4	PGNDB	Channel B Power Ground.
5	BOUT1	Connect to motor winding B.
6	FAULT	Logic low when in over-temperature fault condition.
7	BIN1	Gate signal input to control BOUT1.
8	BIN2	Gate signal input to control BOUT2.
9	BST	Charge Pump Output. Connect a 10nF-to-100nF ceramic capacitor to VIN.
10	VIN	Power Supply Input. Ranges from 2.7V to 15V.
11	GND	Ground.
12	VDD	Internal control and logic supply voltage.
13	AIN2	Gate signal input to control AOUT2.
14	AIN1	Gate signal input to control AOUT1.
15	nSLEEP	Sleep Logic Input. Logic low for sleep mode and logic high to enable the device.
16	AOUT1	Connect to motor winding A.

BLOCK DIAGRAM

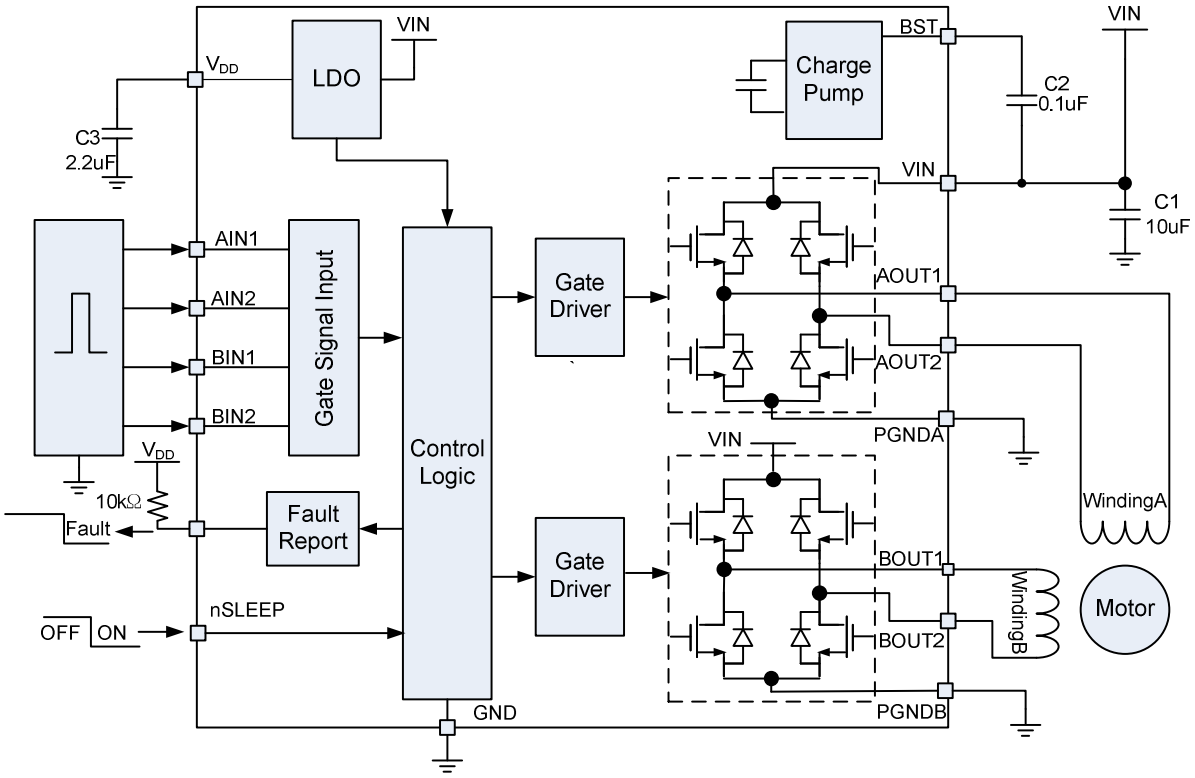


Figure 1: Function Block Diagram

OPERATION

The MP6506 is a motor driver that integrates 8 N-channel power MOSFETs for dual, internal full-bridges with 500mA output current capability over an input voltage range of 2.7V to 15V. It can drive a stepper motor, or two DC motors.

The motor output current can be controlled by an external pulse width modulator (PWM).

The MP6506 includes the following fault protections: under-voltage lockout (UVLO) and over-temperature protection (OTP).

It also provides a low-power sleep mode.

External PWM Current Control

The motor current can be regulated by applying external PWM signals on the input pins AIN1, AIN2, BIN1 and BIN2. For phase A, the AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2; similarly for phase B, thee BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2.

Table 1 shows the input signal logic and bridge output state.

Table 1: Full-Bridge Gate Logic

A/BIN1	A/BIN2	A/BOUT1	A/BOUT2
L	L	High Impedance	High Impedance
L	H	GND	VIN
H	L	VIN	GND
H	H	GND	GND

The winding's inductive current ramps up when the high-side MOSFET is on and freewheels during the high-side MOSFET's off time to cause the recirculation current.

There are two modes for this recirculation current: slow decay and fast decay, both of which are shown in Figure 2 for forward operation and Figure 3 for reverse operation.

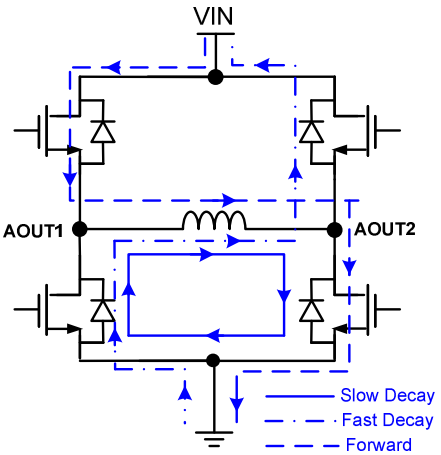


Figure 2: Forward Operation

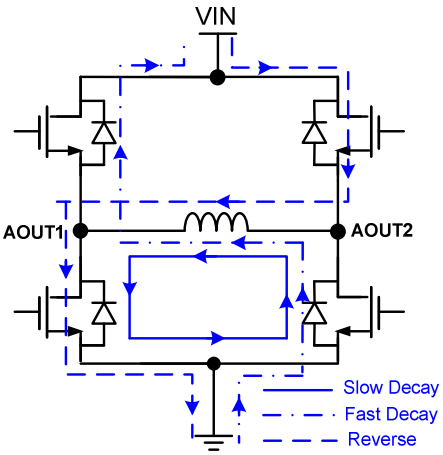


Figure 3: Reverse Operation

For slow decay mode, the current circulates through the two low-side MOSFETs. For fast decay mode, the current flows through the body diodes of the other diagonal two MOSFETS.

To configure the MP6506 for fast decay mode, apply the PWM signal to one input pin and keep the other input pin low; for slow decay mode, apply the PWM signal to one input pin and keep the other input pin high. See Table 2 for more configuration details and Figure 4 for detailed waveforms.

Table 2: PWM Control

A/BIN1	A/BIN2	Mode
H (PWM)	L	Forward
L (PWM)	L	Fast Decay
L	H (PWM)	Reverse
L	L (PWM)	Fast Decay
H	L (PWM)	Forward
H	H (PWM)	Slow Decay
L (PWM)	H	Reverse
H (PWM)	H	Slow Decay

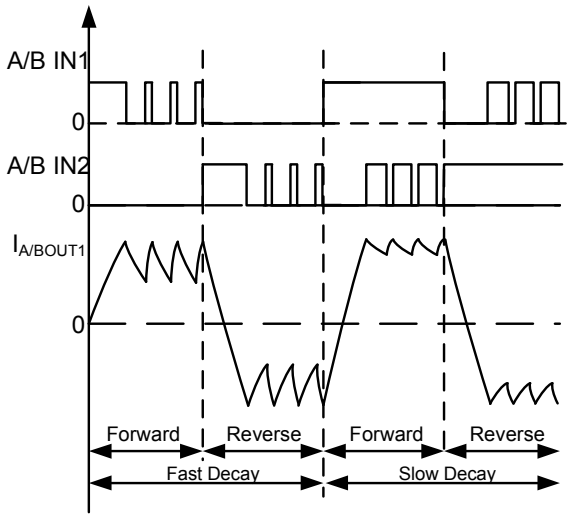


Figure 4: External PWM Current Control Waveform

Sleep Mode

The MP6506 provides low-power standby sleep mode.

Connect the nSLEEP pin to logic low to enable a low-power sleep state. In this state, the two full bridges are disabled and the internal circuits such as the gate drive, internal regulator, and charge pump all shut down. Connect the nSLEEP pin to logic high to wake up the MP6506 from sleep mode, though there is a delay time of ~1ms until the internal circuitry stabilizes.

Enable

If all the inputs (AIN1, AIN2, BIN1 and BIN2) are logic low, the MP6506's outputs are disabled while the charger pump and internal regulator remain active.

Thermal Shutdown

The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 165ºC), the converter is shut down (the fault pin goes low) and recoveries once the junction temperature drops to about 150ºC (15ºC hysteresis).

UVLO protection

The MP6506 has UVLO protection. When the VIN exceeds the UVLO rising threshold, the MP6506 powers up. It shuts off when VIN drops below the UVLO falling threshold.

APPLICATION INFORMATION

Driver Mode:

The MP6506 could be configured for both full-step and half-step modes by sequentially energizing the two windings.

Full-step drive energizes two winding phases at any given time. The stator windings are energized as per the sequence shown in Table 3. There are a total of four steps for one cycle in the sequence [5]: AB→$\overline{A}$B→$\overline{A\,B}$→A$\overline{B}$.

Half-step energizes the stator windings as per the sequence shown in Table 4 There are a total of 8 steps for one cycle: AB→B→$\overline{A}$B→$\overline{A}$→$\overline{A\,B}$ →$\overline{B}$→A$\overline{B}$→A.

Figure 5 shows the operating waveforms for both full and half step drives.

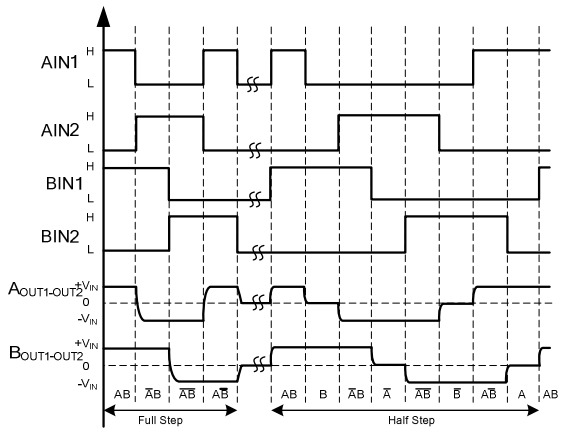


Figure 5: Signal Logic Sequences for Full-Step and Half-Step

Table 3[6]: Full-Step Drive Sequence

Sequence (Full Step)	1	2	3	4
A	+			+
B	+	+		
$\overline{A}$		+	+	
$\overline{B}$			+	+

Table 4[6]: Half-Step Drive Sequence

Sequence (Half Step)	1	2	3	4	5	6	7	8
A	+						+	+
B	+	+	+					
$\overline{A}$			+	+	+			
$\overline{B}$					+	+	+	

Note:

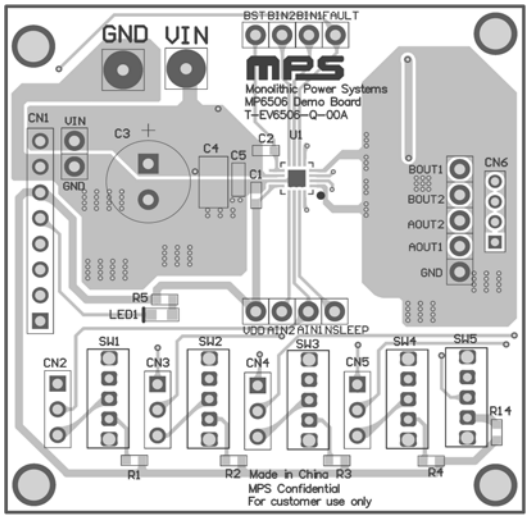
5) A means +VIN between AOUT1 and AOUT2 for winding A, while $\overline{A}$ means -VIN between AOUT1 and AOUT2. The same applies to winding B.

6) "+" item is the selected winding voltage.

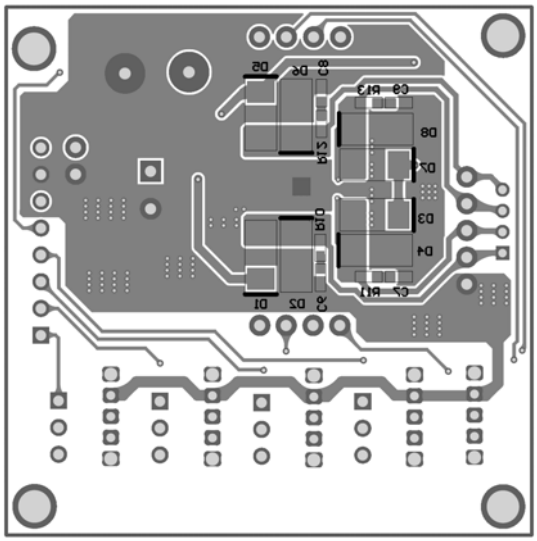
PCB Layout Guide

The printed circuit board (PCB) should use a heavy ground-plane. The MP6506 must be soldered directly onto the board for better electrical and thermal performance.

The MP6506 uses an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to copper on the PCB. Thermal vias are often used to transfer heat to other layers of the PCB.



Top Layer

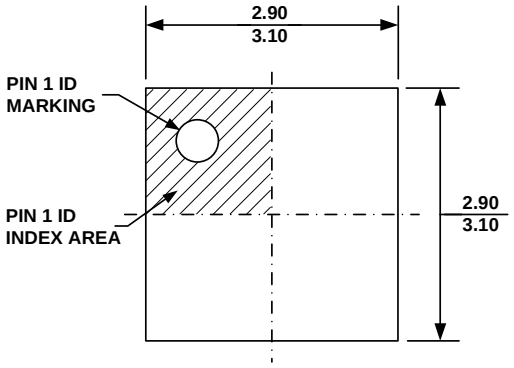


Bottom Layer

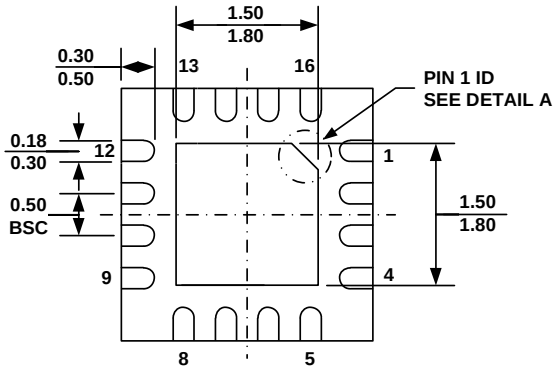
Figure 7: PCB Layout

PACKAGE INFORMATION

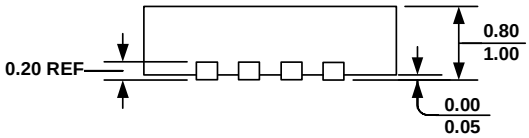
QFN 16 (3×3mm)



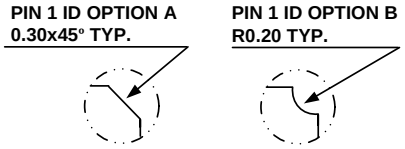
TOP VIEW



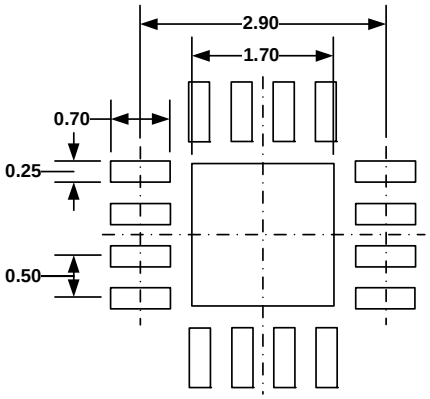
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VEED-4.
5) DRAWING IS NOT TO SCALE.