ISL62773

Multiphase PWM Regulator for AMD Fusion™ Desktop CPUs Using SVI 2.0

FN8263
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The ISL62773 is fully compliant with AMD Fusion™ SVI 2.0 and provides a complete solution for desktop microprocessor and graphics processor core power. The ISL62773 controller supports two Voltage Regulators (VRs) with three integrated gate drivers and two optional external drivers for maximum flexibility. The Core VR can be configured for 3-, 2-, or 1-phase operation while the Northbridge VR supports 2- or 1-phase configurations. The two VRs share a serial control bus to communicate with the AMD CPU and achieve lower cost and smaller board area compared with two-chip solutions.

The PWM modulator is based on Intersil's Robust Ripple Regulator R3™ technology. Compared to traditional modulators, the R3 modulator can automatically change switching frequency for faster transient settling time during load transients and improved light-load efficiency.

The ISL62773 has several other key features. Both outputs support DCR current sensing with a single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. Both outputs utilize remote voltage sense, adjustable switching frequency, OC protection and power-good.

Applications

- AMD Fusion CPU/GPU core power
- Desktop computers

Features

- Supports AMD SVI 2.0 serial data bus interface
  - Serial VID clock frequency range 100kHz to 25MHz
- Dual output controller with integrated drivers
  - Two dedicated core drivers
  - One programmable driver for either core or Northbridge
- Precision voltage regulation
  - 0.5% system accuracy over-temperature
  - 0.5V to 1.55V in 6.25mV steps
  - Enhanced load line accuracy
- Supports multiple current sensing methods
  - Lossless inductor DCR current sensing
  - Precision resistor current sensing
- Programmable 1-, 2- or 3-phase for the core output and 1- or 2-phase for the Northbridge output
- Adaptive body diode conduction time reduction
- Superior noise immunity and transient response
- Output current monitor and thermal monitor
- Differential remote voltage sensing
- High efficiency across entire load range
- Programmable slew rate, VID offset, droop and switching frequency on both outputs
- OCP/WOC, OVP, PGOOD and thermal monitor
- Small footprint 48 Ld 6x6 QFN Package
  - Pb-free (RoHS compliant)

Core Performance

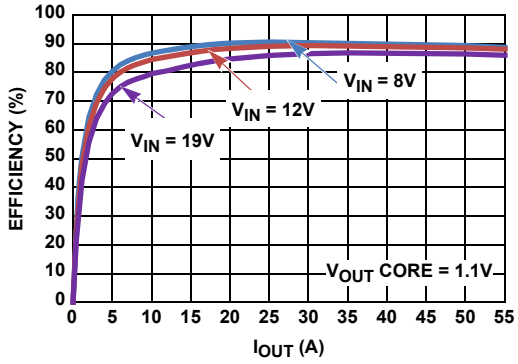

FIGURE 1. EFFICIENCY vs LOAD

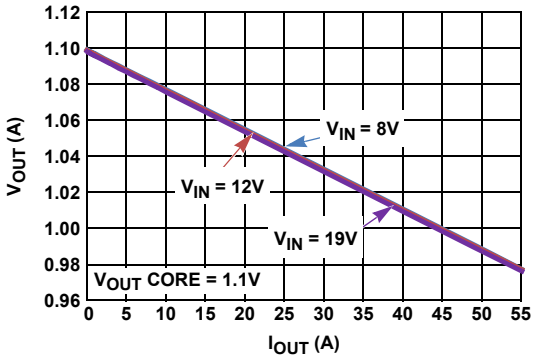

FIGURE 2. V_{OUT} vs LOAD

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Simplified Application Circuit for High Power CPU Core

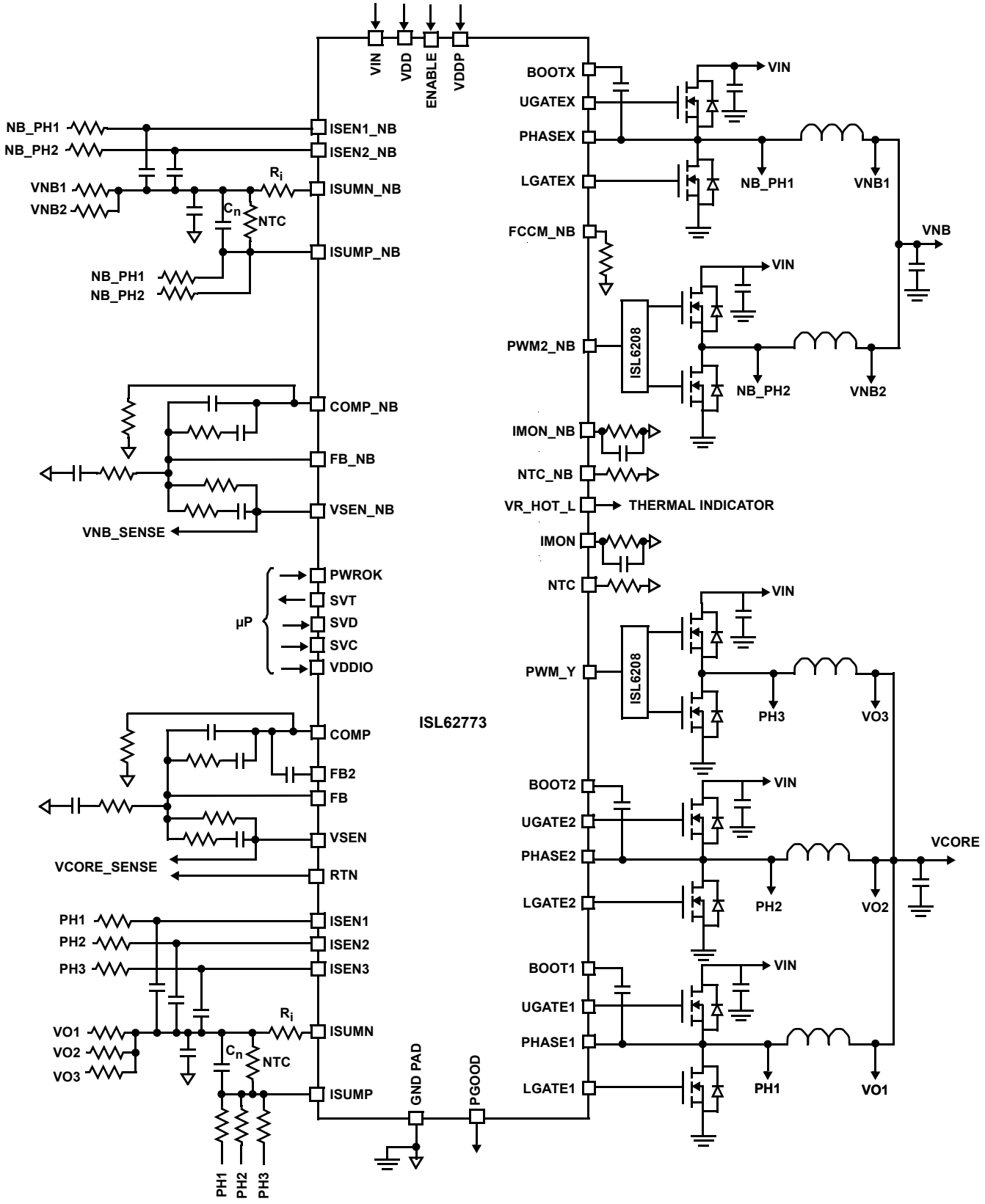


FIGURE 3. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit with 3 Internal Drivers Used for Core

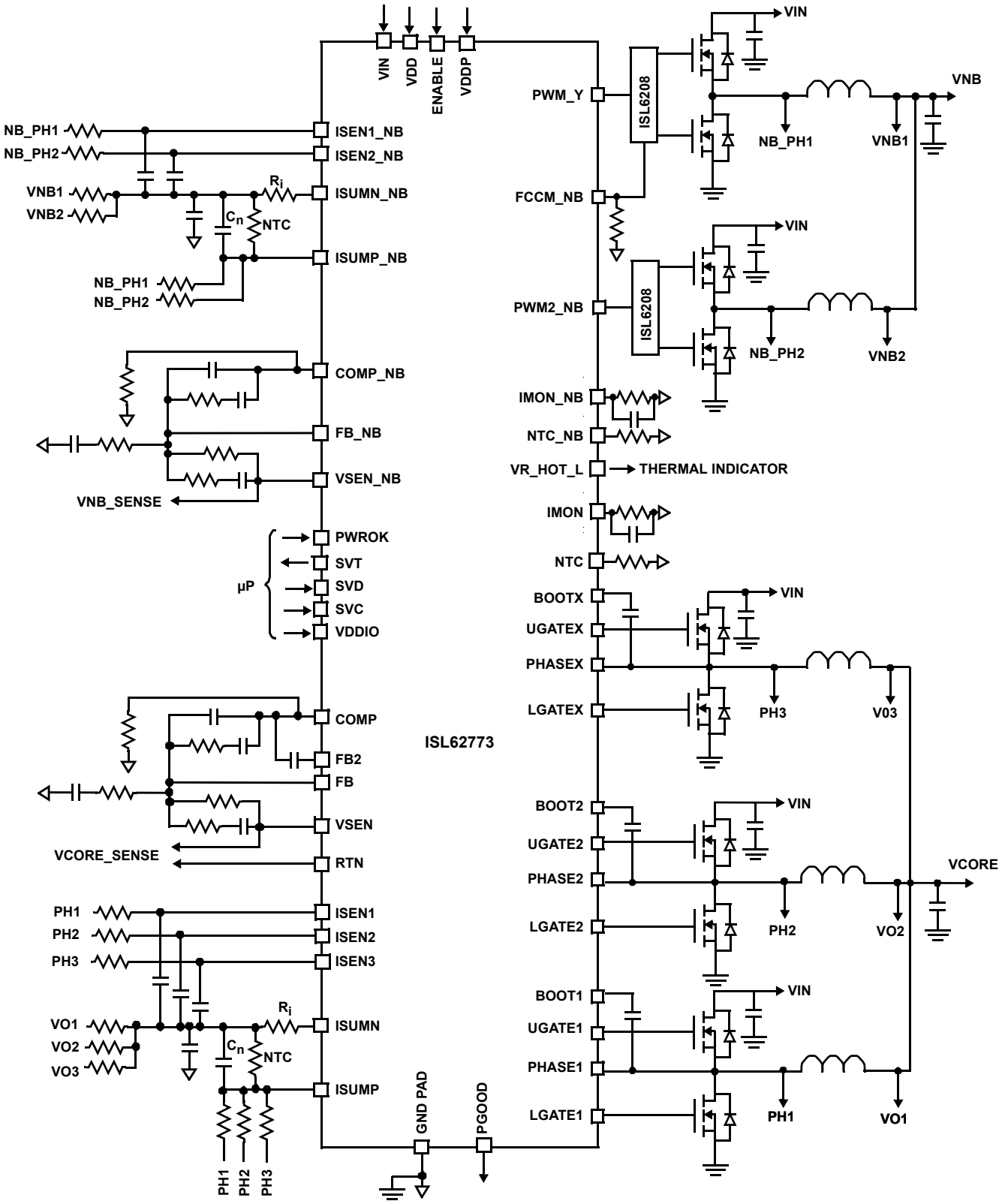


FIGURE 4. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit for Mid-Power CPUs [2+1 Configuration]

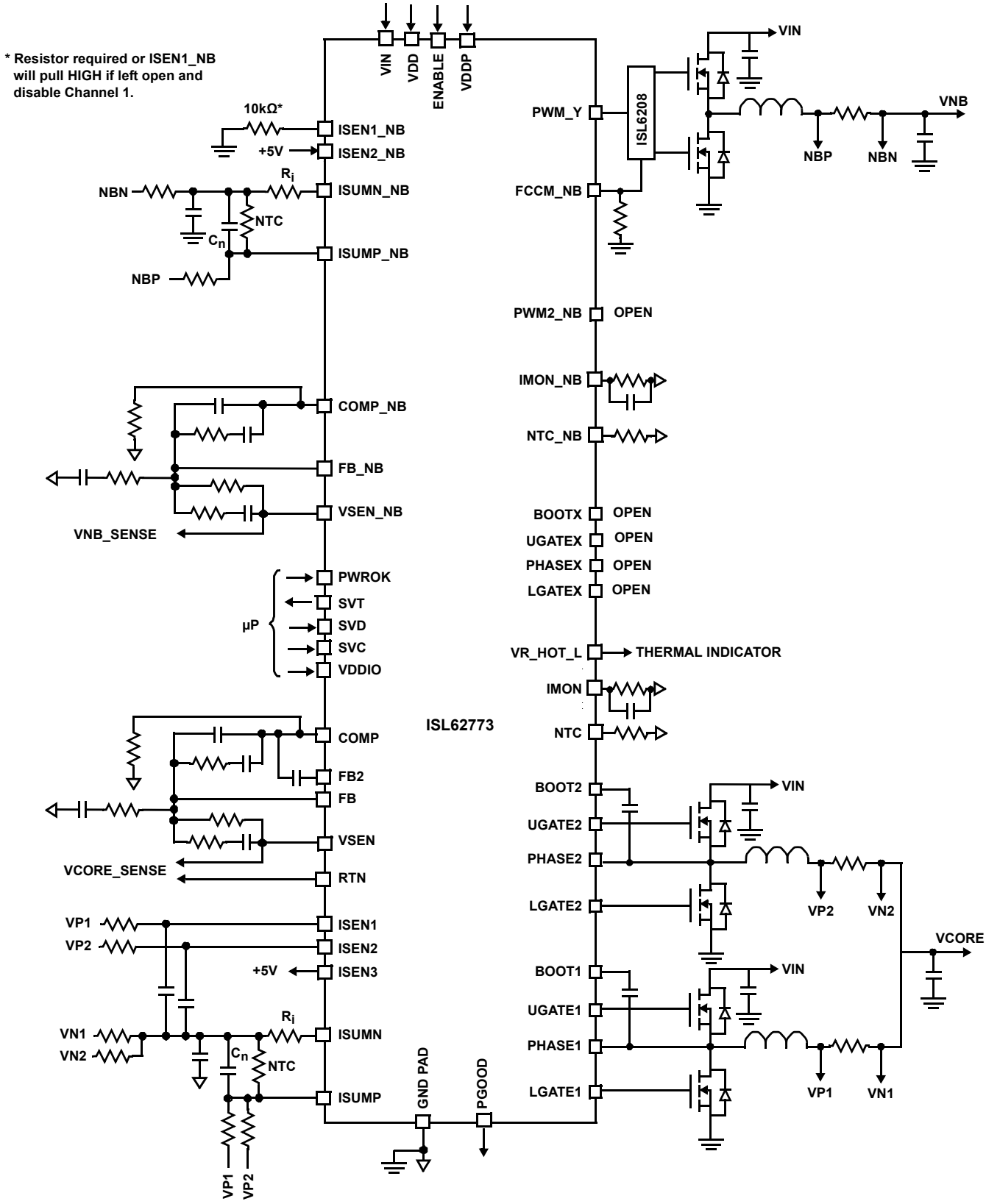


FIGURE 5. TYPICAL APPLICATION CIRCUIT USING RESISTOR SENSING

Simplified Application Circuit for Low Power CPUs [1+1 Configuration]

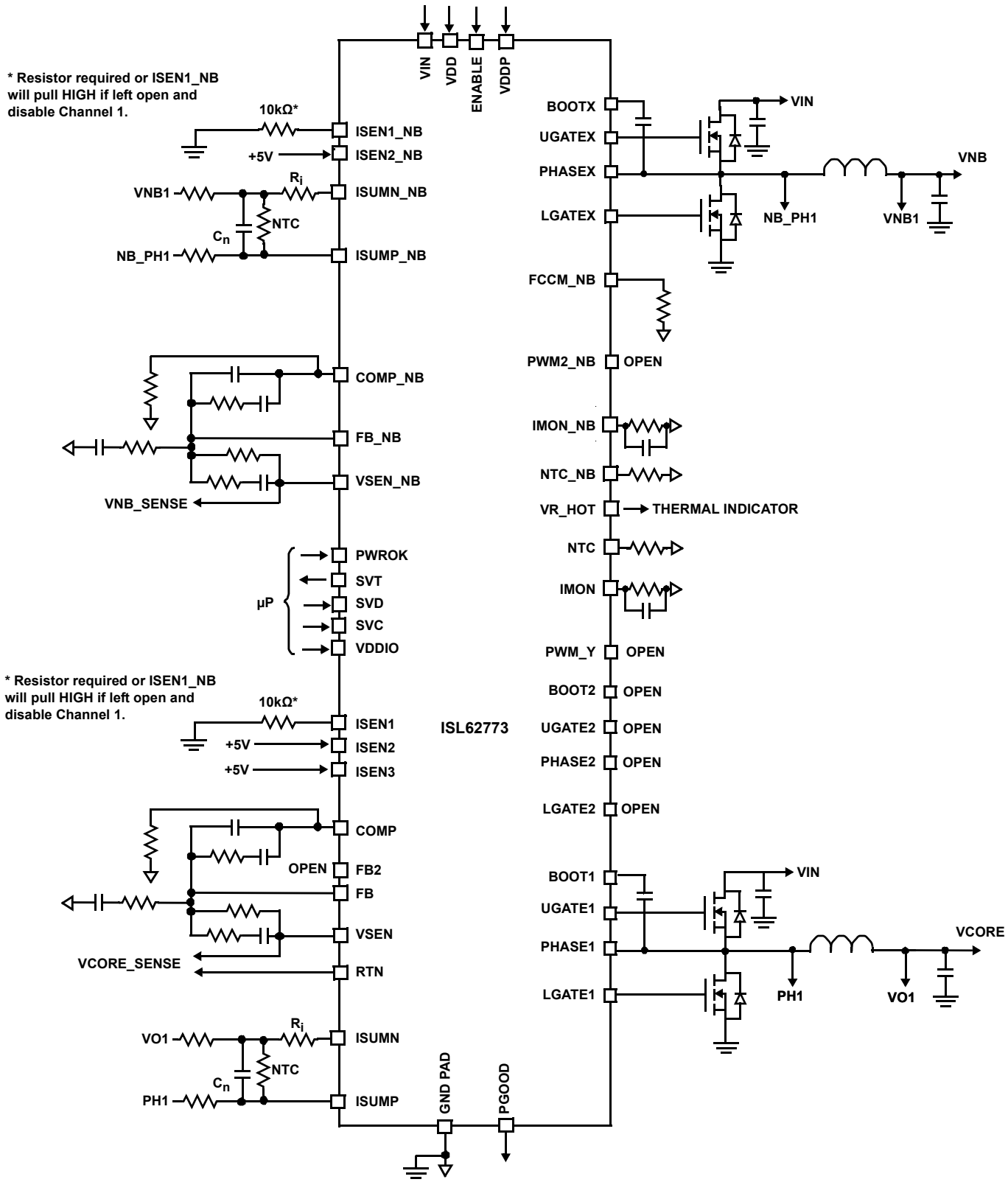


FIGURE 6. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Block Diagram

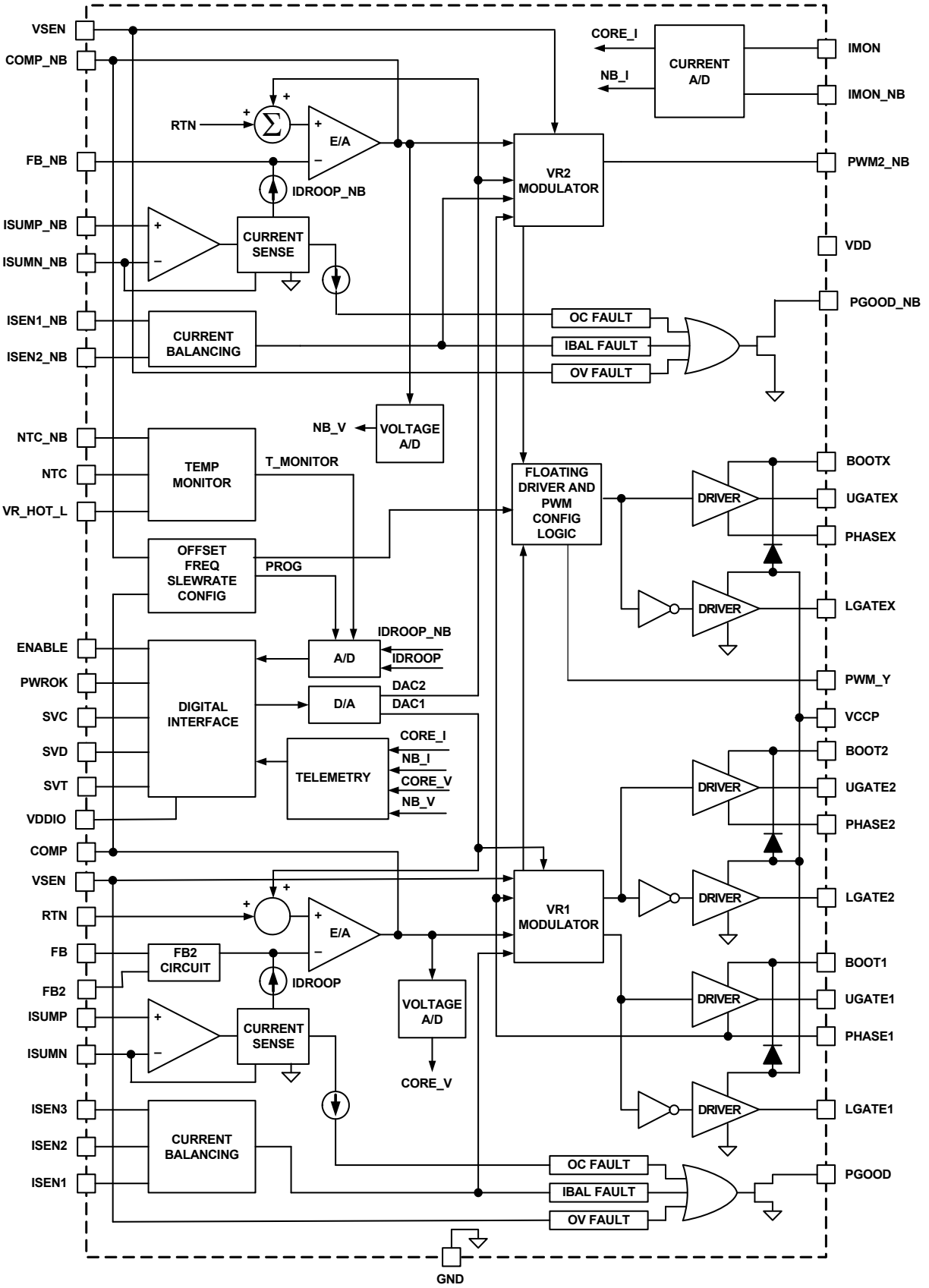
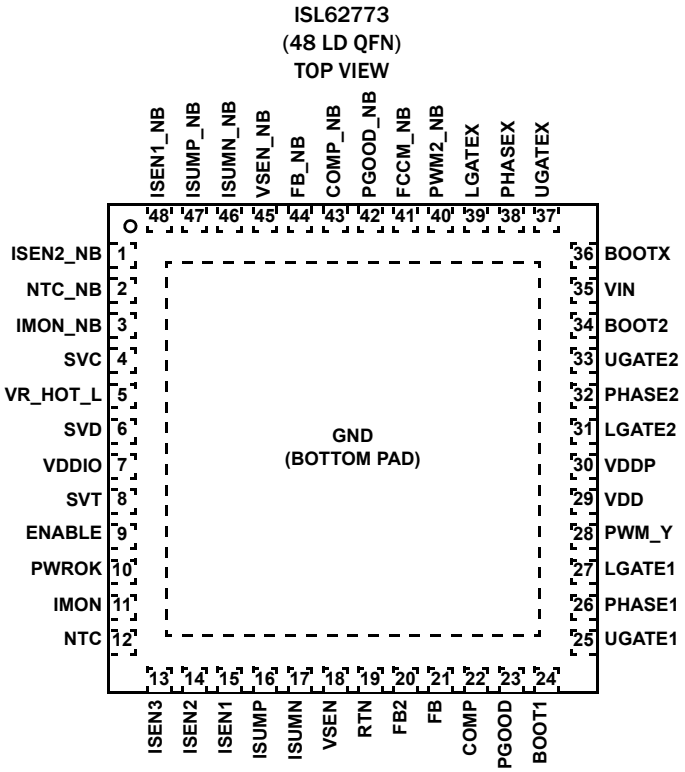


FIGURE 7. BLOCK DIAGRAM

Pin Configuration



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	ISEN2_NB	Individual current sensing for Channel 2 of the Northbridge VR. When ISEN2_NB is pulled to +5V, the controller will disable Channel 2 and the Northbridge VR will run single-phase.
2	NTC_NB	Thermistor input to VR_HOT_L circuit to monitor Northbridge VR temperature.
3	IMON_NB	Northbridge output current monitor. A current proportional to the Northbridge VR output current is sourced from this pin.
4	SVC	Serial VID clock input from the CPU processor master device.
5	VR_HOT_L	Thermal indicator signal to AMD CPU. Thermal overload open-drain output indicator active LOW.
6	SVD	Serial VID data bidirectional signal from the CPU processor master device to the VR.
7	VDDIO	VDDIO is the processor memory interface power rail and this pin serves as the reference to the controller IC for this processor I/O signal level.
8	SVT	Serial VID Telemetry (SVT) data line input to the CPU from the controller IC. Telemetry and VID-on-the-fly complete signal provided on from this pin.
9	ENABLE	Enable input. A high level logic on this pin enables both VRs.
10	PWROK	System power-good input. When this pin is high, the SVI 2 interface is active and the I^2C protocol is running. While this pin is low, the SVC and SVD input states determine the pre-PWROK metal VID. This pin must be low prior to the ISL62773 PGOOD output going high per the AMD SVI 2.0 Controller Guidelines.
11	IMON	Core output current monitor. A current proportional to the Core VR output current is sourced from this pin.
12	NTC	Thermistor input to VR_HOT_L circuit to monitor Core VR temperature.
13	ISEN3	ISEN3 is the individual current sensing for Channel 3. When ISEN3 is pulled to +5V, the controller disables Channel 3 and the Core VR runs in two-phase mode.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
14	ISEN2	Individual current sensing for Channel 2 of the Core VR. When ISEN2 is pulled to +5V, the controller disables Channel 2 and the Core VR runs in single-phase mode.
15	ISEN1	Individual current sensing for Channel 1 of the Core VR. If ISEN2 is tied to +5V, this pin cannot be left open and must be tied to GND with a 10kΩ resistor. If ISEN1 is tied to +5V, the Core portion of the IC is shutdown.
16	ISUMP	Noninverting input of the transconductance amplifier for current monitor and load line of Core output.
17	ISUMN	Inverting input of the transconductance amplifier for current monitor and load line of Core output.
18	VSEN	Output voltage sense pin for the Core controller. Connect to the +sense pin of the microprocessor die.
19	RTN	Output voltage sense return pin for both Core VR and Northbridge VR. Connect to the -sense pin of the microprocessor die.
20	FB2	There is a switch between the FB2 pin and the FB pin. The switch is on in 2-phase or 3-phase mode and is off in 1-phase mode. The components connecting to FB2 are used to adjust the compensation in 1-phase mode of the Core VR to achieve optimum performance.
21	FB	Output voltage feedback to the inverting input of the Core controller error amplifier.
22	COMP	Core controller error amplifier output. A resistor from COMP to GND sets the Core VR offset voltage.
23	PGOOD	Open-drain output to indicate the Core portion of the IC is ready to supply regulated voltage. Pull up externally to VDD or 3.3V through a resistor.
24	BOOT1	Connect an MLCC capacitor across the BOOT1 and the PHASE1 pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOT1 pin, each time the PHASE1 pin drops below VDDP minus the voltage dropped across the internal boot diode.
25	UGATE1	Output of the Phase 1 high-side MOSFET gate driver of the Core VR. Connect the UGATE1 pin to the gate of the Phase 1 high-side MOSFET(s).
26	PHASE1	Current return path for the Phase 1 high-side MOSFET gate driver of VR1. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Phase 1.
27	LGATE1	Output of the Phase 1 low-side MOSFET gate driver of the Core VR. Connect the LGATE1 pin to the gate of the Phase 1 low-side MOSFET(s).
28	PWM_Y	Floating PWM output used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR depending on the FCCM_NB resistor connected between FCCM_NB and GND.
29	VDD	5V bias power. A resistor [2Ω] and a decoupling capacitor should be used from the +5V supply. A high quality, X7R dielectric MLCC capacitor is recommended.
30	VDDP	Input voltage bias for the internal gate drivers. Connect +5V to the VDDP pin. Decouple with at least 1µF of capacitance to GND. A high quality, X7R dielectric MLCC capacitor is recommended.
31	LGATE2	Output of the Phase 2 low-side MOSFET gate driver of the Core VR. Connect the LGATE2 pin to the gate of the Phase 2 low-side MOSFET(s).
32	PHASE2	Current return path for the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Phase 2.
33	UGATE2	Output of the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the UGATE2 pin to the gate of the Phase 2 high-side MOSFET(s).
34	BOOT2	Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOT2 pin, each time the PHASE2 pin drops below VDDP minus the voltage dropped across the internal boot diode.
35	VIN	Battery supply voltage, used for feed-forward.
36	BOOTX	Boot connection of the programmable internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Connect an MLCC capacitor across the BOOT1X and the PHASEX pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOTX pin, each time the PHASEX pin drops below VDDP minus the voltage dropped across the internal boot diode.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
37	UGATEX	High-side MOSFET gate driver portion of the programmable internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Connect the UGATEX pin to the gate of the high-side MOSFET(s) for either Phase 3 of the Core VR or Phase 1 of the Northbridge VR based on the configuration state selected.
38	PHASEX	Phase connection of the programmable internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Current return path for the high-side MOSFET gate driver of the floating internal driver. Connect the PHASEX pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of either Phase 3 of the Core VR or Phase 1 of the Northbridge VR based on the configuration state selected.
39	LGATEX	Low-side MOSFET gate driver portion of floating internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Connect the LGATEX pin to the gate of the low-side MOSFET(s) for either Phase 3 of the Core VR or Phase 1 of the Northbridge VR based on the configuration state selected.
40	PWM2_NB	PWM output for Channel 2 of the Northbridge VR. Disabled when ISEN2_NB is tied to +5V.
41	FCCM_NB	Diode emulation control signal for Intersil MOSFET Drivers. When FCCM_NB is LOW, diode emulation at the driver this pin connects to is allowed. A resistor from FCCM_NB pin to GND configures the PWM_Y and floating internal gate driver [BOOTX, UGATEX, PHASEX, LGATEX pins] to support Phase 3 of the Core VR and Phase 1 of the Northbridge VR. The FCCM_NB resistor value also is used to set the slew rate for the Core VR and Northbridge VR.
42	PGOOD_NB	Open-drain output to indicate the Northbridge portion of the IC is ready to supply regulated voltage. Pull up externally to VDDP or 3.3V through a resistor.
43	COMP_NB	Northbridge VR error amplifier output. A resistor from COMP_NB to GND sets the Northbridge VR offset voltage and is used to set the switching frequency for the Core VR and Northbridge VR.
44	FB_NB	Output voltage feedback to the inverting input of the Northbridge controller error amplifier.
45	VSEN_NB	Output voltage sense pin for the Northbridge controller. Connect to the +sense pin of the microprocessor die.
46	ISUMN_NB	Inverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
47	ISUMP_NB	Noninverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
48	ISEN1_NB	Individual current sensing for Channel 1 of the Northbridge VR. If ISEN2_NB is tied to +5V, this pin cannot be left open and must be tied to GND with a 10kΩ resistor. If ISEN1_NB is tied to+5V, the Northbridge portion of the IC is shutdown.
	GND (Bottom Pad)	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL62773HRZ	ISL62773 HRZ	-10 to +100	48 Ld 6x6 QFN	L48.6x6B
ISL62773IRZ	ISL62773 IRZ	-40 to +85	48 Ld 6x6 QFN	L48.6x6B

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL62773. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

Supply Voltage, V_{DD}, V_{DDP} . . . . . -0.3V to +7V
Battery Voltage, V_{IN} . . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE) . . . . . -0.3V to +7V (DC)
. . . . . -0.3V to +9V (<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHA SE - 0.3V (DC) to BOOTPHASE - 5V
. . . . . (<20ns Pulse Width, 10µJ) to BOOT LGATE Voltage
. . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
All Other Pins . . . . . -0.3V to (VDD + 0.3V)
Open-Drain Outputs, PGOOD, PGOOD_NB, VR_HOT_L. . . . . -0.3V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN Package (Notes 4, 5)	29	3.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . +5V ±5%
Battery Voltage, V_{IN} . . . . . +4.5V to 25V
Ambient Temperature
HRZ. . . . . -10°C to +100°C
IRZ . . . . . -40°C to +85°C
Junction Temperature . . . . . -10°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +85°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	ENABLE = 1V		8	11	mA
		ENABLE = 0V			5	µA
Battery Supply Current	I_{VIN}	ENABLE = 0V			1	µA
V_{IN} Input Resistance	R_{VIN}	ENABLE = 1V		620		kΩ
POWER-ON-RESET THRESHOLDS						
VDD POR Threshold	VDD_POR_r	V_{DD} rising		4.35	4.5	V
	VDD_POR_f	V_{DD} falling	4.00	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	HRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V,	-0.5		+0.5	%
		VID = 0.25V to 0.74375V	-10		+10	mV
	IRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V	-0.8		+0.8	%
		VID = 0.25V to 0.74375V	-12		+12	mV
Maximum Output Voltage	$V_{OUT(max)}$	VID = [00000000]		1.55		V
Minimum Output Voltage	$V_{OUT(min)}$	VID = [11111111]		0.0		V
CHANNEL FREQUENCY						
Nominal Channel Frequency	$f_{SW(nom)}$		280	300	320	kHz
Adjustment Range			300		450	kHz

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +85°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
AMPLIFIERS						
Current-Sense Amplifier Input Offset	HRZ	I_{FB} = 0A	-0.15		+0.15	mV
	IRZ	I_{FB} = 0A	-0.20		+0.20	mV
Error Amp DC Gain	A_{VO}			119		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		17		MHz
ISEN						
Input Bias Current				20		nA
POWER-GOOD (PGOOD AND PGOOD_NB) AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA			0.4	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	-1		1	µA
PWROK High Threshold				750		mV
VR_HOT_L Pull-Down				11		W
PWROK Leakage Current					1	µA
VR_HOT_L Leakage Current					1	µA
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA source current		1.0	1.5	W
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance	R_{UGPD}	250mA sink current		1.0	1.5	W
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA source current		1.0	1.5	W
LGATE Source Current	I_{LGSRC}	LGATE - VSSP = 2.5V		2.0		A
LGATE Sink Resistance	R_{LGPD}	250mA sink current		0.5	0.9	W
LGATE Sink Current	I_{LGSNK}	LGATE - VSSP = 2.5V		4.0		A
UGATE to LGATE Dead Time	t_{UGFLGR}	UGATE falling to LGATE rising, no load		23		ns
LGATE to UGATE Dead Time	t_{LGFUGR}	LGATE falling to UGATE rising, no load		28		ns
PROTECTION						
Overvoltage Threshold	OV_H	VSEN rising above setpoint for >1µs	275	325	375	mV
Undervoltage Threshold	OV_H	VSEN falls below setpoint for >1µs	275	325	375	mV
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
Way Overcurrent Trip Threshold [IMONx Current Based Detection]	$IMONx_{WOC}$	All states, I_{DROOP} = 60µA, R_{IMON} = 135kΩ		15		µA
Overcurrent Trip Threshold [IMONx Voltage Based Detection]	V_{IMONx_OCP}	All states, I_{DROOP} = 45µA, I_{IMONx} = 11.25µA, R_{IMON} = 135kΩ	1.485	1.510	1.535	V
LOGIC THRESHOLDS						
ENABLE Input Low	V_{IL}				1	V
ENABLE Input High	V_{IH}	HRZ	1.6			V
	V_{IH}	IRZ	1.65			V
ENABLE Leakage Current	I_{ENABLE}	ENABLE = 0V	-1	0	1	µA
		ENABLE = 1V		18	35	µA

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +85°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SVT Impedance				50		W
SVC, SVD Input Low	V_{IL}	% of VDDIO			30	%
SVC, SVD Input High	V_{IH}	% of VDDIO	70			%
SVC, SVD Leakage		ENABLE = 0V, SVC, SVD = 0V and 1V	-1		1	µA
		ENABLE = 1V, SVC, SVD = 1V	-5		1	µA
		ENABLE = 1V, SVC, SVD = 0V	-35	-20	-5	µA
PWM						
PWM Output Low	V_{0L}	Sinking 5mA			1.0	V
PWM Output High	V_{0H}	Sourcing 5mA	3.5			V
PWM Tri-State Leakage		PWM = 2.5V			0.5	µA
THERMAL MONITOR						
NTC Source Current		NTC = 0.6V	27	30	33	µA
NTC Thermal Warning Voltage			600	640	680	mV
NTC Thermal Warning Voltage Hysteresis				20		mV
NTC Thermal Shutdown Voltage			530	580	630	mV
SLEW RATE						
VID-on-the-Fly Slew Rate		Maximum programmed	16	20	24	mV/µs
		Minimum programmed	8	10	12	mV/µs

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Gate Driver Timing Diagram

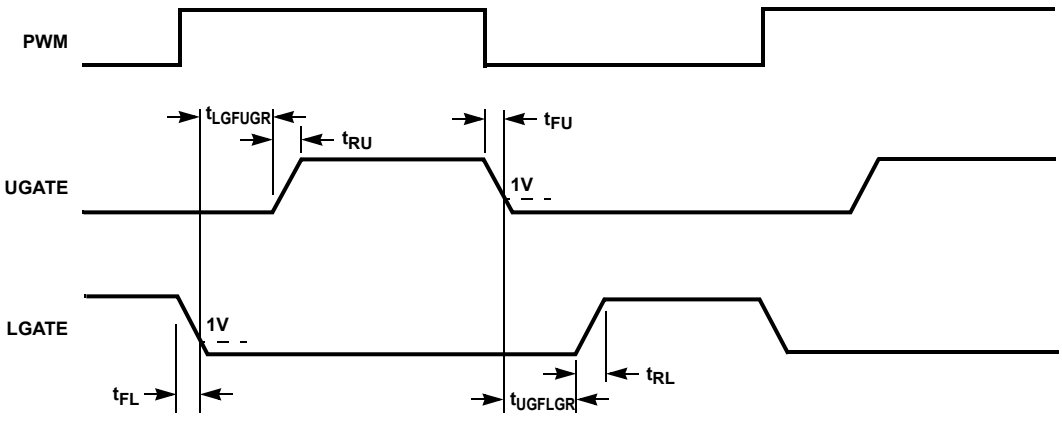


FIGURE 8. GATE DRIVER TIMING DIAGRAM

Theory of Operation

Multiphase R3™ Modulator

The ISL62773 is a multiphase regulator implementing two voltage regulators, CORE VR and Northbridge (NB) VR, on one chip controlled by AMD's™ SVI2™ protocol. The CORE VR can be programmed for 1-, 2- or 3-phase operation. The Northbridge VR can be configured for 1- or 2-phase operation. Both regulators use the Intersil patented R3™ (Robust Ripple Regulator) modulator. The R3™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 9 conceptually shows the multiphase R3™ modulator circuit and Figure 10 shows the operation principles.

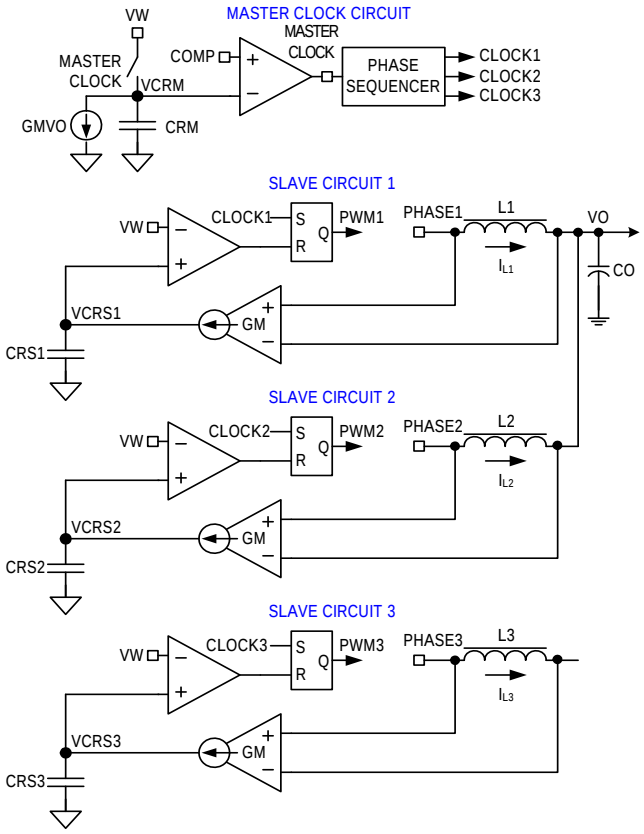


FIGURE 9. R3™ MODULATOR CIRCUIT

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. C_{rm} voltage V_{CRM} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If the CORE VR is in 3-phase mode, the master clock signal is distributed to the three phases and the Clock 1~3 signals will be 120° out-of-phase. If the Core VR is in 2-phase mode, the master clock signal is distributed to Phases 1 and 2 and the Clock1 and Clock2 signals will be 180° out-of-phase. If the Core VR is in 1-phase mode, the master clock signal will be distributed to Phase 1 only and be the Clock1 signal.

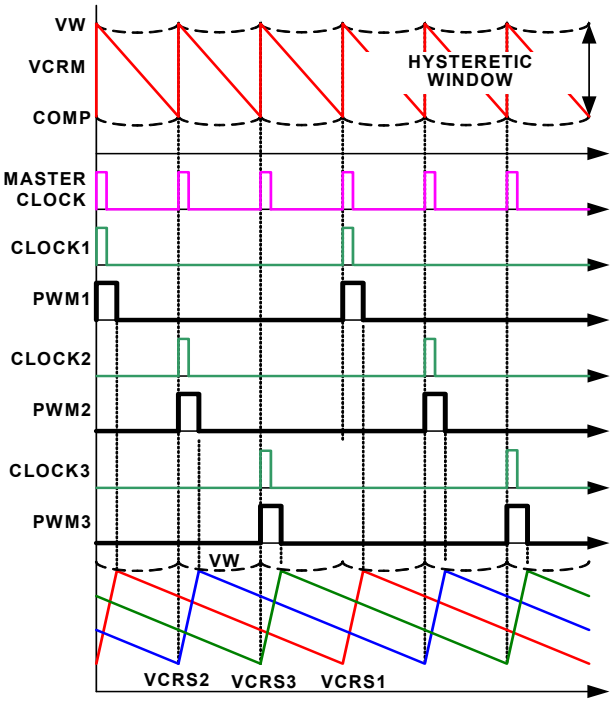


FIGURE 10. R3™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

Each slave circuit has its own ripple capacitor C_{rs}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse upon receiving the clock signal and the current source charges C_{rs}. When C_{rs} voltage V_{Crs} hits VW, the slave circuit turns off the PWM pulse and the current source discharges C_{rs}.

Since the controller works with V_{crs}, which are large amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the error amplifier allows the ISL62773 to maintain a 0.5% output voltage accuracy.

Figure 11 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency. This allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL62773 excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

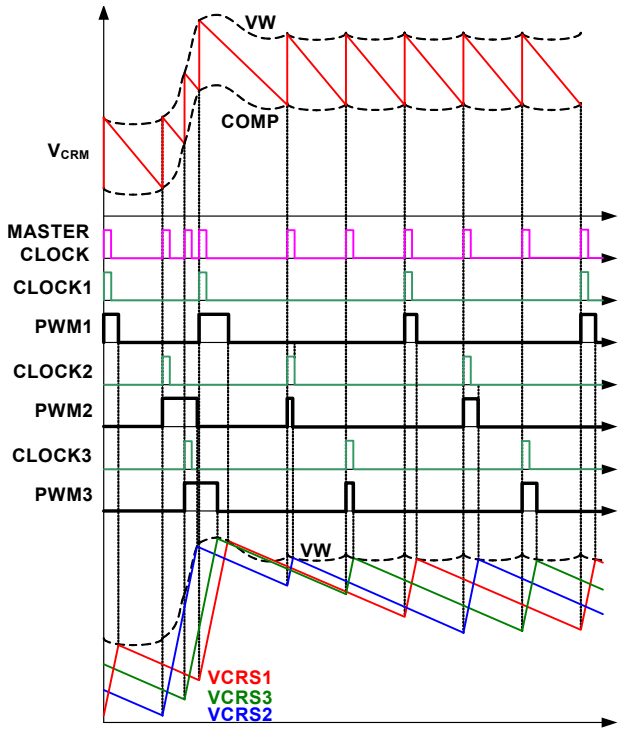


FIGURE 11. R3™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

Diode Emulation and Period Stretching

The ISL62773 can operate in diode emulation (DE) mode to improve light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and does not allow reverse current, thus emulating a diode. Figure 12 shows that when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL62773 monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

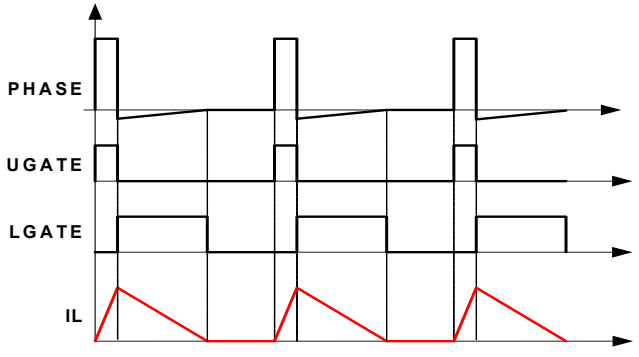


FIGURE 12. DIODE EMULATION

If the load current is light enough, as Figure 12 shows, the inductor current reaches and stays at zero before the next phase node pulse and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A and the regulator is in CCM, although the controller is in DE mode.

Figure 13 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, making the inductor current triangle the same in the three cases. The ISL62773 clamps the ripple capacitor voltage V_{CRS} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{CRS}, naturally stretching the switching period. The inductor current triangles move farther apart, such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

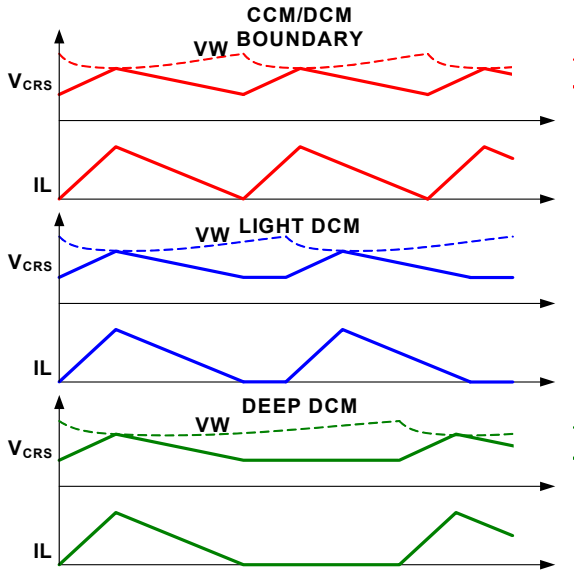


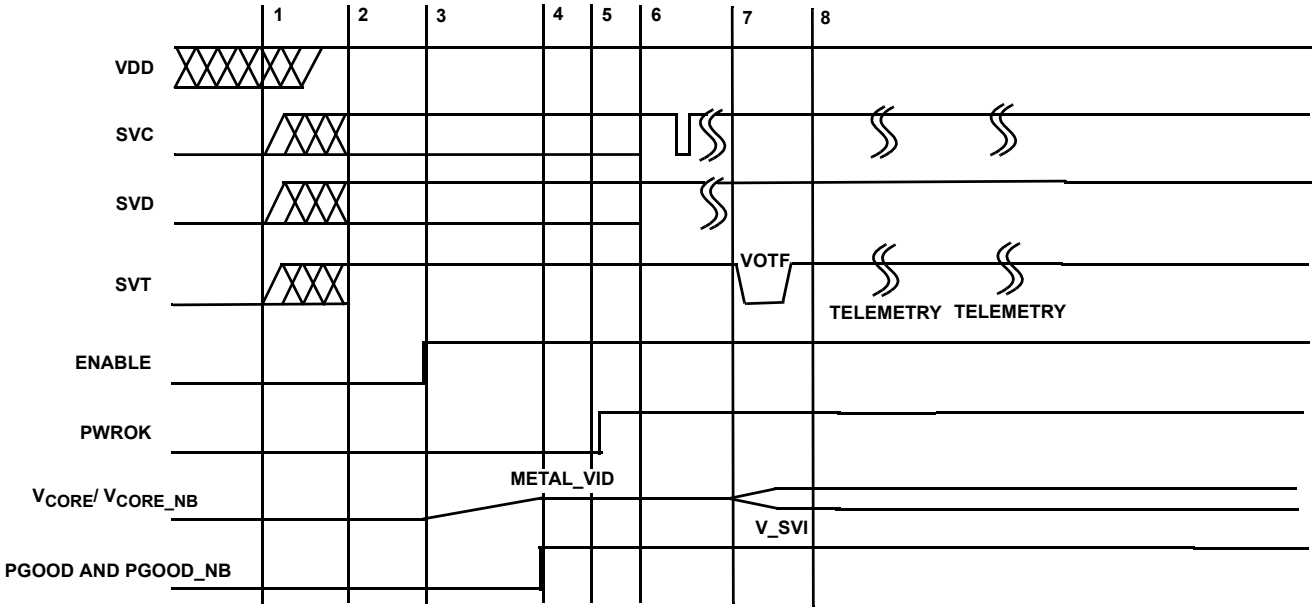
FIGURE 13. PERIOD STRETCHING

Channel Configuration

Individual PWM channels of either VR can be disabled by connecting the ISENx pin of the channel not required to +5V. For example, placing the controller in a 2+1 configuration (Figure 5), requires ISEN3 of the Core VR and ISEN2 of the Northbridge VR to be tied to +5V. This disables Channel 3 of the Core VR and Channel 2 of the Northbridge VR. ISEN1_NB must be tied through a 10kΩ resistor to GND to prevent this pin from pulling high and disabling the channel. Connecting ISEN1 or ISEN1_NB to +5V will disable the corresponding VR output. This feature allows debug of individual VR outputs.

Power-On Reset

Before the controller has sufficient bias to guarantee proper operation, the ISL62773 requires a +5V input supply tied to VDD and VDDP to exceed the VDD rising power-on reset (POR) threshold. Once this threshold is reached or exceeded, the ISL62773 has enough bias to check the state of the SVI inputs once ENABLE is taken high. Hysteresis between the rising and the falling threshold on VDD POR assure the ISL62773 does not inadvertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 11). Note that VIN must be present for the controller to drive the output voltage.



Interval 1 to 2: ISL62773 waits to POR.

Interval 2 to 3: SVC and SVD are externally set to pre-Metal VID code.

Interval 3 to 4: ENABLE locks pre-Metal VID code. Both outputs soft-start to this level.

Interval 4 to 5: PGOOD signal goes HIGH, indicating proper operation.

Interval 5 to 6: PGOOD and PGOOD_NB high is detected and PWROK is taken high. The ISL62773 is prepared for SVI commands.

Interval 6 to 7: SVC and SVD data lines communicate change in VID code.

Interval 7 to 8: ISL62773 responds to VID-ON-THE-FLY code change and issues a VOTF for positive VID changes.

Post 8: Telemetry is clocked out of the ISL62773.

FIGURE 14. SVI INTERFACE TIMING DIAGRAM: TYPICAL PRE-PWROK METAL VID START-UP

Start-Up Timing

With VDD above the POR threshold, the controller start-up sequence begins when ENABLE exceeds the logic high threshold. Figure 15 shows the typical soft-start timing of the Core and Northbridge VRs. Once the controller registers ENABLE as a high, the controller checks that state of a few programming pins during the typical 8ms delay prior to beginning soft-starting the Core and Northbridge outputs. The pre-PWROK Metal VID is read from the state of the SVC and SVD pins and programs the DAC, the programming resistors on COMP, COMP_NB and FCCM_NB are read to configure internal drivers, switching frequency, slew rate and output offsets. These programming resistors are discussed in subsequent sections. The ISL62773 uses a digital soft-start to ramp up the DAC to the Metal VID level programmed. The soft-start slew rate is programmed by the FCCM_NB resistor, which is used to set the VID-on-the-Fly slew rate as well. See "VID-on-the-Fly Slew Rate Selection" on page 21 for more details on selecting the FCCM_NB resistor. PGOOD is asserted high at the end of the soft-start ramp.

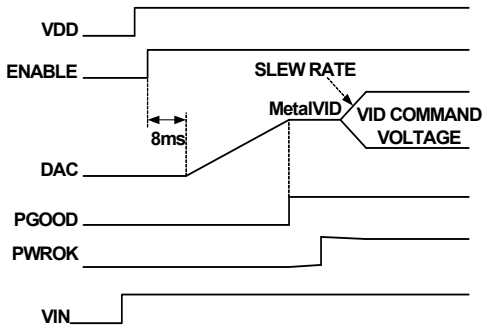


FIGURE 15. TYPICAL SOFT-START WAVEFORMS

Voltage Regulation and Load Line Implementation

After the soft-start sequence, the ISL62773 regulates the output voltages to the pre-PWROK metal VID programmed, see Table 6. The ISL62773 controls the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.55V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

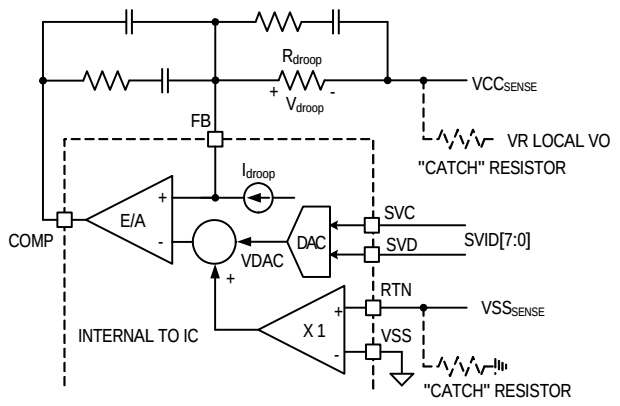


FIGURE 16. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage droops from the VID programmed value by an amount proportional to the load current, to achieve the load line. The ISL62773 can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors (see Figures 3 and 4) or through resistors in series with the inductors (see Figure 5). In both methods, capacitor C_n voltage represents the total inductor current. A droop amplifier converts C_n voltage into an internal current source with the gain set by resistor R_i. The current source is used for load line implementation, current monitoring and overcurrent protection.

Figure 16 shows the load line implementation. The ISL62773 drives a current source (I_{droop}) out of the FB pin, as described by Equation 1.

$$I_{droop} = \frac{V_{Cn}}{R_i} \quad \text{(EQ. 1)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding, thus sustaining the load line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 2.

$$V_{droop} = R_{droop} \times \left(I_{droop} \times \frac{5}{4}\right) \quad \text{(EQ. 2)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can change the load line slope. Since I_{droop} also sets the overcurrent protection level, it is recommended to first scale I_{droop} based on OCP requirement. Next, select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Sensing

Figure 16 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. The error amplifier regulates the inverting and noninverting input voltages to be equal as shown in Equation 3:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 3)}$$

Rewriting Equation 3 and substituting Equation 2 gives Equation 4 is the exact equation required for load line implementation.

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times (I_{droop} \times 5/4) \quad \text{(EQ. 4)}$$

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback is open circuit in the absence of the processor. As Figure 16 shows, it is recommended to add a “catch” resistor to feed the VR local output voltage back to the compensator and to add another “catch” resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, provide voltage feedback if the system is powered up without a processor installed.

Phase Current Balancing

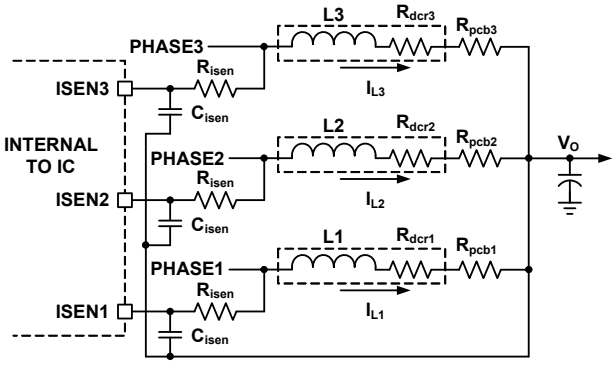


FIGURE 17. CURRENT BALANCING CIRCUIT

The ISL62773 monitors individual phase average current by monitoring the ISEN1, ISEN2 and ISEN3 voltages. Figure 17 shows the recommended current balancing circuit for DCR sensing. Each phase node voltage is averaged by a low-pass filter consisting of R_{isen} and C_{isen} and is presented to the corresponding ISEN pin. R_{isen} should be routed to the inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 5 through 7 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 5)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 6)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 7)}$$

Where R_{dcr1}, R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2} and I_{L3} are inductor average currents.

The ISL62773 will adjusts the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using the same components for L1, L2 and L3 provides a good match of R_{dcr1}, R_{dcr2} and R_{dcr3}. Board layout determines R_{pcb1}, R_{pcb2} and R_{pcb3}. It is recommended to have a symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

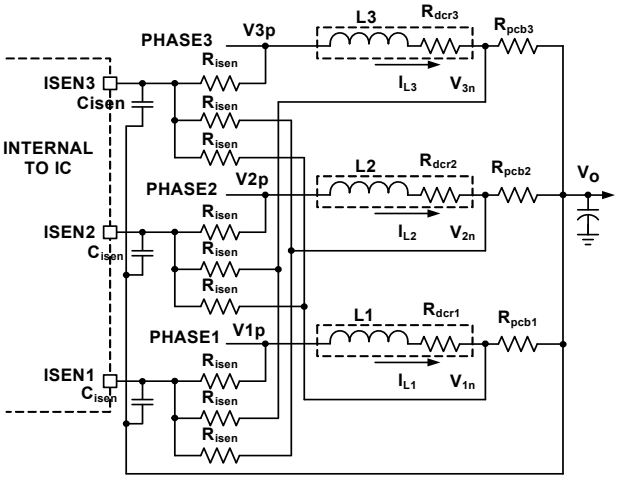


FIGURE 18. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

At times, it is difficult to implement symmetrical layout. For the circuit shown in Figure 17, asymmetric layout causes different R_{pcb1}, R_{pcb2} and R_{pcb3} values, thus creating a current imbalance. Figure 18 shows a differential sensing current balancing circuit recommended for ISL62773. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own, phase inductor phase-node pad and the other two phases inductor output side pads. Equations 8 through 10 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad \text{(EQ. 8)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 9)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 10)}$$

The ISL62773 will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as shown in Equations 11 and 12:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 11)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 12)}$$

Rewriting Equation 11 gives Equation 13:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 13)}$$

Rewriting Equation 12 gives Equation 14:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 14)}$$

Combining Equations 13 and 14 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 15)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 16)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) is achieved when $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2} and R_{pcb3} do not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, the R3™ modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 19 shows the current balancing performance of the evaluation board with load transient of 12A/51A at different repetition rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at a low repetition rate, but cannot keep up when the repetition rate gets into the hundred-kHz range, where it is out of the control loop bandwidth. The controller achieves excellent current balancing in all cases installed.

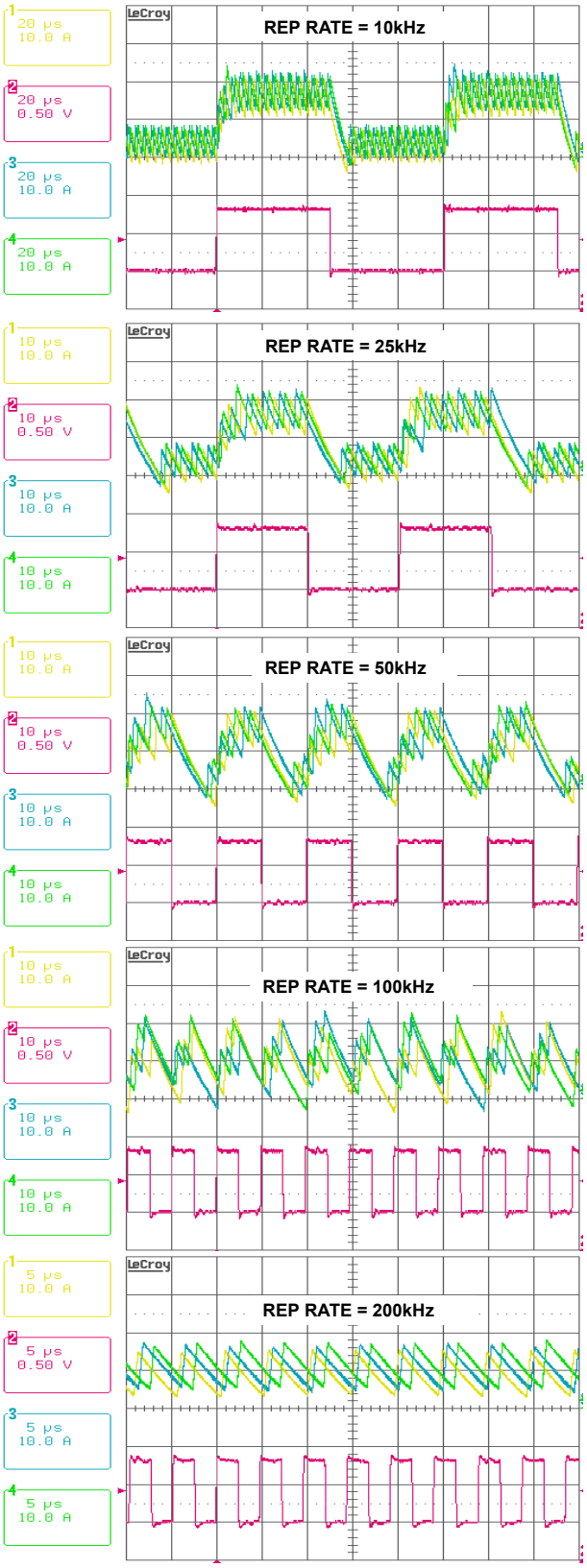


FIGURE 19. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: I_{L1}, CH2: I_{LOAD}, CH3: I_{L2}, CH4: I_{L3}

Modes of Operation

TABLE 1. CORE VR MODES OF OPERATION

CONFIG.	ISEN3	ISEN2	PSL0_L AND PSI1_L	MODE	OCP THRESHOLD (µA)
3-phase Core VR Config.	To Power Stage	To Power Stage	11	3-phase CCM	45
			01	2-phase CCM	
			00	1-phase DE	
2-phase Core VR Config.	Tied to 5V	To Power Stage	11	2-phase CCM	45
			01	1-phase CCM	
			00	1-phase DE	
1-phase Core VR Config.	Tied to 5V	Tied to 5V	11	1-phase CMM	45
			01		
			00	1-phase DE	

The Core VR can be configured for 3, 2- or 1-phase operation. Table 1 shows Core VR configurations and operational modes, programmed by the ISEN3 and ISEN2 pin status and the PSL0_L and PSL1_L commands via the SVI 2 interface, see Table 9 on page 25.

For a 2-phase configuration, tie the ISEN3 pin to 5V. In this configuration, phases 1 and 2 are active. To select a 1-phase configuration, tie the ISEN3 pin and the ISEN2 pin to 5V. In this configuration, only phase-1 is active.

In a 3-phase configuration, the Core VR operates in 3-phase CCM, with PSI0_L and PSI_L both high. If PSI0_L is taken low via the SVI 2 interface, the Core VR drops phase 3 and continues to operate in CCM. When both PSI0_L and PSI1_L are taken low, the Core VR drops phase 2 and enters 1-phase DE mode.

For 2-phase configurations, the Core VR operates in 2-phase CCM with PSI0_L and PSI_L both high. If PSI0_L is taken low via the SVI 2 interface, the Core VR drops phase 2 and continues to operate in 1-phase CCM. When both PSI0_L and PSI1_L are taken low, the Core VR enters 1-phase DE mode.

In a 1-phase configuration, the Core VR operates in 1-phase CCM and enters 1-phase DE when both PSI0_L and PSI1_L are low.

The Core VR can be disabled completely by connecting ISEN1 to +5V.

TABLE 2. NORTHBRIDGE VR MODES OF OPERATION

ISEN2_NB	CONFIG.	PSL0_L AND PSI1_L	MODE	OCP THRESHOLD
To Power Stage	2-phase NB VR Config.	11	2-phase CCM	45µA
		01	1-phase CCM	
		00	1-phase DE	
Tied to 5V	1-phase NB VR Config.	11	1-phase CCM	45µA
		01	1-phase CCM	
		00	1-phase DE	

ISL62773 Northbridge VR can be configured for 2- or 1-phase operation. Table 2 shows the Northbridge VR configurations and operational modes, which are programmed by the ISEN2_NB pin status and the PSI0_L and PSI1_L bits of the SVI 2 command.

In a 1-phase configuration, the ISEN2_NB pin is tied to +5V. The Northbridge VR operates in 1-phase CCM and enters 1-phase DE when both PSI0_L and PSI1_L are low.

The Northbridge VR can be disabled completely by tying ISEN1_NB to 5V.

Dynamic Operation

Core VR and Northbridge VR behave the same during dynamic operation. The controller responds to VID-on-the-fly changes by slewing to the new voltage at the slew rate programmed, see Table 4. During negative VID transitions, the output voltage decays to the lower VID value at the slew rate determined by the load.

The R3™ modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

FB2 Function

The Core VR features an FB2 pin. The FB2 function is only available when the Core VR is in a 2-phase configuration.

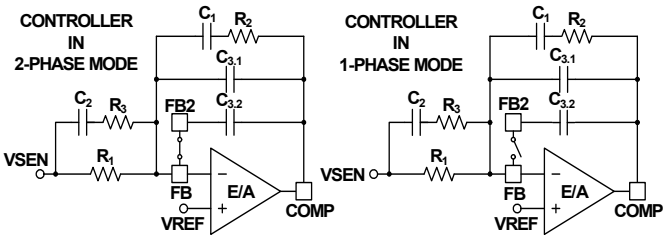


FIGURE 20. FB2 FUNCTION

Figure 20 shows the FB2 function. A switch (called FB2 switch) turns on to short the FB and the FB2 pins when the controller is in 2-phase mode. Capacitors $C_{3.1}$ and $C_{3.2}$ are in parallel, serving as part of the compensator. When the controller enters 1-phase mode, the FB2 switch turns off, removing $C_{3.2}$ and leaving only $C_{3.1}$ in the compensator. The compensator gain increases with the removal of $C_{3.2}$. By properly sizing $C_{3.1}$ and $C_{3.2}$, the compensator can be optimal for both 2-phase mode and 1-phase mode.

When the FB2 switch is off, $C_{3.2}$ is disconnected from the FB pin. However, the controller still actively drives the FB2 pin voltage to follow the FB pin voltage such that $C_{3.2}$ voltage always follows $C_{3.1}$ voltage. When the controller turns on the FB2 switch, $C_{3.2}$ is reconnected to the compensator smoothly.

The FB2 function ensures excellent transient response in both 2-phase and 1-phase mode. If the FB2 function is not used, populate $C_{3.1}$ only.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it will flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it will flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET. To minimize the body diode-related loss, the controller also adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns.

Resistor Configuration Options

The ISL62773 uses the COMP, COMP_NB and FCCM_NB pins to configure some functionality within the IC. Resistors from these pins to GND are read during the first portion of the soft-start sequence. The following sections outline how to select the resistor values for each of these pins to correctly program the output voltage offset of each output, the configuration of the floating DriverX and PWM_Y output, VID-on-the-Fly slew rate and switching frequency used for both VRs.

VR Offset Programming

A positive or negative offset is programmed for the Core VR using a resistor to ground from the COMP pin and the Northbridge in a similar manner from the COMP_NB pin. Table 3 provides the resistor value to select the desired output voltage offset

TABLE 3. COMP AND COMP_NB OUTPUT VOLTAGE OFFSET SELECTION

RESISTOR VALUE [kΩ]	COMP $V_{CORE\ OFFSET}$ [mV]	COMP_NB OFFSET [mV]
5.62	-43.75	18.75
9.53	-37.5	31.25
13.3	-31.25	43.76
16.9	-25	50
21.0	-18.75	37.5
26.7	-12.5	25
34.0	-6.25	12.5
41.2	6.25	0
57.6	18.75	18.75
73.2	31.25	31.25
95.3	43.76	43.76
121	50	50
154	37.5	37.5
182	25	25
221	12.5	12.5
OPEN	0	0

Floating DriverX and PWM_Y Configuration

The ISL62773 allows for one internal driver and one PWM output to be configured to opposite VRs depending on the desired configuration of the Northbridge VR. Internal DriverX can be used as Channel 1 of the Northbridge VR with PWM_Y used for Channel 3 of the Core VR. Using this partitioning, a 2+1 or 1+1 configured ISL62773 would not require an external driver.

If routing of the driver signals would be a cause of concern due to having an internal driver on the Northbridge VR, then the ISL62773 can be configured to use PWM_Y as Channel 1 on the Northbridge VR. DriverX would then be used as Channel 3 of the Core VR. This allows the placement of the external drivers for the Northbridge VR to be closer to the output stage(s) depending on the number of active Phases. Providing placement and layout flexibility to the Northbridge VR.

TABLE 4. FCCM_NB RESISTOR SELECTION

RESISTOR VALUE [kΩ]	SLEW RATE FOR CORE AND NORTHBRIDGE [mV/µs]	DriverX	PWM_Y
5.62	20	Core VR Channel 3	NB VR Channel 1
9.53	15		
13.3	12.5		
16.9	10		
21.0	20		
26.7	15		
34.0	12.5		
41.2	10		
57.6	20	NB VR Channel 1	Core VR Channel 3
73.2	15		
95.3	12.5		
121	10		
154	20		
182	15		
221	12.5		
OPEN	10		

VID-on-the-Fly Slew Rate Selection

The FCCM_NB resistor is also used to select the slew rate for VID changes commanded by the processor. Once selected, the slew rate is locked in during soft-start and is not adjustable during operation. The lowest slew rate which can be selected is 10mV/µs, which is above the minimum of 7.5mV/µs required by the SVI2 specification. The slew rate selected sets the slew rate for both Core and Northbridge VRs, thus they cannot be independently selected.

CCM Switching Frequency

The Core and Northbridge VR switching frequency is set by the programming resistors on COMP_NB and FCCM_NC. When the ISL62773 is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the R3™ modulator. As explained in the "Multiphase R3™ Modulator" on page 14, the effective switching frequency increases during load insertion and decreases during load release to achieve fast response. Thus, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 10% and does not have any significant effect on output voltage ripple magnitude. Table 5 defines the switching frequency based on the resistor values used to program the COMP_NB and FCCM_NB pins. Use Tables 3 and 4 to determine the correct resistor value in these ranges to program the desired output offset, Slew Rate and DriverX/PWM_Y configuration.

TABLE 5. SWITCHING FREQUENCY SELECTION

FREQUENCY [kHz]	COMP_NB RANGE [kΩ]	FCCM_NB RANGE [kΩ]
300	57.6 to OPEN	21.0 to 41.2 or 154 to OPEN
350	5.62 to 41.2	21.0 to 41.2 or 154 to OPEN
400	57.6 to OPEN	5.62 to 16.9 or 57.6 to 121
450	5.62 to 41.2	5.62 to 16.9 or 57.6 to 121

The controller monitors SVI commands to determine when to enter power-saving mode, implement dynamic VID changes and shut down individual outputs.

AMD Serial VID Interface 2.0

The on-board Serial VID Interface 2.0 (SVI 2) circuitry allows the AMD processor to directly control the Core and Northbridge voltage reference levels within the ISL62773. Once the PWROK signal goes high, the IC begins monitoring the SVC and SVD pins for instructions. The ISL62773 uses a digital-to-analog converter (DAC) to generate a reference voltage based on the decoded SVI value. See Figure 14 on page 16 for a simple SVI interface timing diagram.

Pre-PWROK Metal VID

Typical motherboard start-up begins with the controller decoding the SVC and SVD inputs to determine the pre-PWROK Metal VID setting (see Table 6). Once the ENABLE input exceeds the rising threshold, the ISL62773 decodes and locks the decoded value into an on-board hold register.

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Once the programming pins are read, the internal DAC circuitry begins to ramp Core and Northbridge VRs to the decoded pre-PWROK Metal VID output level. The digital soft-start circuitry ramps the internal reference to the target gradually at a fixed rate of approximately 5mV/µs until the output voltage reaches ~250mV and then at the programmed slew rate. The controlled ramp of all output voltage planes reduces in-rush current during the soft-start interval. At the end of the soft-start interval, the PGOOD and PGOOD_NB outputs transition high, indicating both output planes are within regulation limits.

If the ENABLE input falls below the enable falling threshold, the ISL62773 tri-states both outputs. PGOOD and PGOOD_NB are pulled low with the loss of ENABLE. The Core and Northbridge VR output voltages decay, based on output capacitance and load leakage resistance. If bias to VDD falls below the POR level, the ISL62773 responds in the manner previously described. Once VDD and ENABLE rise above their respective rising thresholds, the internal DAC circuitry reacquires a pre-PWROK metal VID code and the controller soft-starts.

SVI Interface Active

Once the Core and Northbridge VRs have successfully soft-started and PGOOD and PGOOD_NB signals transition high, PWROK can be asserted externally to the ISL62773. Once PWROK is asserted to the IC, SVI instructions can begin as the controller actively monitors the SVI interface. Details of the SVI Bus protocol are provided in the “AMD Serial VID Interface 2.0 (SVI2) Specification”. See AMD publication #48022.

Once a VID change command is received, the ISL62773 decodes the information to determine which VR is affected and the VID target is determined by the byte combinations in Table 7. The internal DAC circuitry steps the output voltage of the VR commanded to the new VID level. During this time, one or more of the VR outputs could be targeted. In the event either VR is commanded to power-off by serial VID commands, the PGOOD signal remains asserted.

If the PWROK input is deasserted, then the controller steps both the Core and the Northbridge VRs back to the stored pre-PWROK metal VID level in the holding register from initial soft-start. No attempt is made to read the SVC and SVD inputs during this time. If PWROK is reasserted, then the ISL62773 SVI interface waits for instructions.

If ENABLE goes low during normal operation, all external MOSFETs are tri-stated and both PGOOD and PGOOD_NB are pulled low. This event clears the pre-PWROK metal VID code and forces the controller to check SVC and SVD upon restart, storing the pre-PWROK metal VID code found on restart.

A POR event on either VCC or VIN during normal operation shuts down both regulators and both PGOOD outputs are pulled low. The pre-PWROK metal VID code is not retained.

VID-on-the-Fly Transition

Once PWROK is high, the ISL62773 detects this flag and begins monitoring the SVC and SVD pins for SVI instructions. The microprocessor follows the protocol outlined in the following sections to send instructions for VID-on-the-fly transitions. The ISL62773 decodes the instruction and acknowledges the new VID code. For VID codes higher than the current VID level, the ISL62773 begins stepping the commanded VR outputs to the new VID target with the slew rate programmed by the FCCM_NB resistor.

When the VID codes are lower than the current VID level, the ISL62773 checks the state of power state bits in the SVI command. If power state bits are not active, the controller begins stepping the regulator output to the new VID target. If the power state bits are active, the controller allows the output voltage to decay and slowly steps the DAC down with the natural decay of the output. This allows the controller to quickly recover and move to a high VID code if commanded.

SVI Data Communication Protocol

The SVI WIRE protocol is based on the I^2C bus concept. Two wires [serial clock (SVC) and serial data (SVD)], carry information between the AMD processor (master) and VR controller (slave) on the bus. The master initiates and terminates SVI transactions and drives the clock, SVC, during a transaction. The AMD processor is always the master and the voltage regulators are the slaves. The slave receives the SVI transactions and acts accordingly. Mobile SVI WIRE protocol timing is based on high-speed mode I^2C. See AMD publication #48022 for additional details.

TABLE 7. SERIAL VID CODES

SVID[7:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)
0000_0000	1.55000	0010_0000	1.35000	0100_0000	1.15000	0110_0000	0.95000
0000_0001	1.54375	0010_0001	1.34375	0100_0001	1.14375	0110_0001	0.94375
0000_0010	1.53750	0010_0010	1.33750	0100_0010	1.13750	0110_0010	0.93750
0000_0011	1.53125	0010_0011	1.33125	0100_0011	1.13125	0110_0011	0.93125
0000_0100	1.52500	0010_0100	1.32500	0100_0100	1.12500	0110_0100	0.92500
0000_0101	1.51875	0010_0101	1.31875	0100_0101	1.11875	0110_0101	0.91875
0000_0110	1.51250	0010_0110	1.31250	0100_0110	1.11250	0110_0110	0.91250
0000_0111	1.50625	0010_0111	1.30625	0100_0111	1.10625	0110_0111	0.90625
0000_1000	1.50000	0010_1000	1.30000	0100_1000	1.10000	0110_1000	0.90000
0000_1001	1.49375	0010_1001	1.29375	0100_1001	1.09375	0110_1001	0.89375
0000_1010	1.48750	0010_1010	1.28750	0100_1010	1.08750	0110_1010	0.88750
0000_1011	1.48125	0010_1011	1.28125	0100_1011	1.08125	0110_1011	0.88125
0000_1100	1.47500	0010_1100	1.27500	0100_1100	1.07500	0110_1100	0.87500
0000_1101	1.46875	0010_1101	1.26875	0100_1101	1.06875	0110_1101	0.86875
0000_1110	1.46250	0010_1110	1.26250	0100_1110	1.06250	0110_1110	0.86250
0000_1111	1.45625	0010_1111	1.25625	0100_1111	1.05625	0110_1111	0.85625
0001_0000	1.45000	0011_0000	1.25000	0101_0000	1.05000	0111_0000	0.85000
0001_0001	1.44375	0011_0001	1.24375	0101_0001	1.04375	0111_0001	0.84375
0001_0010	1.43750	0011_0010	1.23750	0101_0010	1.03750	0111_0010	0.83750
0001_0011	1.43125	0011_0011	1.23125	0101_0011	1.03125	0111_0011	0.83125
0001_0100	1.42500	0011_0100	1.22500	0101_0100	1.02500	0111_0100	0.82500
0001_0101	1.41875	0011_0101	1.21875	0101_0101	1.01875	0111_0101	0.81875
0001_0110	1.41250	0011_0110	1.21250	0101_0110	1.01250	0111_0110	0.81250
0001_0111	1.40625	0011_0111	1.20625	0101_0111	1.00625	0111_0111	0.80625
0001_1000	1.40000	0011_1000	1.20000	0101_1000	1.00000	0111_1000	0.80000
0001_1001	1.39375	0011_1001	1.19375	0101_1001	0.99375	0111_1001	0.79375
0001_1010	1.38750	0011_1010	1.18750	0101_1010	0.98750	0111_1010	0.78750
0001_1011	1.38125	0011_1011	1.18125	0101_1011	0.98125	0111_1011	0.78125
0001_1100	1.37500	0011_1100	1.17500	0101_1100	0.97500	0111_1100	0.77500
0001_1101	1.36875	0011_1101	1.16875	0101_1101	0.96875	0111_1101	0.76875
0001_1110	1.36250	0011_1110	1.16250	0101_1110	0.96250	0111_1110	0.76250
0001_1111	1.35625	0011_1111	1.15625	0101_1111	0.95625	0111_1111	0.75625
1000_0000	0.75000	1010_0000	0.55000*	1100_0000	0.35000*	1110_0000	0.15000*
1000_0001	0.74375	1010_0001	0.54375*	1100_0001	0.34375*	1110_0001	0.14375*
1000_0010	0.73750	1010_0010	0.53750*	1100_0010	0.33750*	1110_0010	0.13750*
1000_0011	0.73125	1010_0011	0.53125*	1100_0011	0.33125*	1110_0011	0.13125*
1000_0100	0.72500	1010_0100	0.52500*	1100_0100	0.32500*	1110_0100	0.12500*
1000_0101	0.71875	1010_0101	0.51875*	1100_0101	0.31875*	1110_0101	0.11875*
1000_0110	0.71250	1010_0110	0.51250*	1100_0110	0.31250*	1110_0110	0.11250*
1000_0111	0.70625	1010_0111	0.50625*	1100_0111	0.30625*	1110_0111	0.10625*

TABLE 7. SERIAL VID CODES (Continued)

SVID[7:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)	SVID[6:0]	VOLTAGE (V)
1000_1000	0.70000	1010_1000	0.50000*	1100_1000	0.30000*	1110_1000	0.10000*
1000_1001	0.69375	1010_1001	0.49375*	1100_1001	0.29375*	1110_1001	0.09375*
1000_1010	0.68750	1010_1010	0.48750*	1100_1010	0.28750*	1110_1010	0.08750*
1000_1011	0.68125	1010_1011	0.48125*	1100_1011	0.28125*	1110_1011	0.08125*
1000_1100	0.67500	1010_1100	0.47500*	1100_1100	0.27500*	1110_1100	0.07500*
1000_1101	0.66875	1010_1101	0.46875*	1100_1101	0.26875*	1110_1101	0.06875*
1000_1110	0.66250	1010_1110	0.46250*	1100_1110	0.26250*	1110_1110	0.06250*
1000_1111	0.65625	1010_1111	0.45625*	1100_1111	0.25625*	1110_1111	0.05625*
1001_0000	0.65000	1011_0000	0.45000*	1101_0000	0.25000*	1111_0000	0.05000*
1001_0001	0.64375	1011_0001	0.44375*	1101_0001	0.24375*	1111_0001	0.04375*
1001_0010	0.63750	1011_0010	0.43750*	1101_0010	0.23750*	1111_0010	0.03750*
1001_0011	0.63125	1011_0011	0.43125*	1101_0011	0.23125*	1111_0011	0.03125*
1001_0100	0.62500	1011_0100	0.42500*	1101_0100	0.22500*	1111_0100	0.02500*
1001_0101	0.61875	1011_0101	0.41875*	1101_0101	0.21875*	1111_0101	0.01875*
1001_0110	0.61250	1011_0110	0.41250*	1101_0110	0.21250*	1111_0110	0.01250*
1001_0111	0.60625	1011_0111	0.40625*	1101_0111*	0.20625*	1111_0111	0.00625*
1001_1000	0.60000*	1011_1000	0.40000*	1101_1000	0.20000*	1111_1000	OFF*
1001_1001	0.59375*	1011_1001	0.39375*	1101_1001	0.19375*	1111_1001	OFF*
1001_1010	0.58750*	1011_1010	0.38750*	1101_1010	0.18750*	1111_1010	OFF*
1001_1011	0.58125*	1011_1011	0.38125*	1101_1011	0.18125*	1111_1011	OFF*
1001_1100	0.57500*	1011_1100	0.37500*	1101_1100	0.17500*	1111_1100	OFF*
1001_1101	0.56875*	1011_1101	0.36875*	1101_1101	0.16875*	1111_1101	OFF*
1001_1110	0.56250*	1011_1110	0.36250*	1101_1110	0.16250*	1111_1110	OFF*
1001_1111	0.55625*	1011_1111	0.35625*	1101_1111	0.15625*	1111_1111	OFF*

NOTES:

7. *Indicates a VID not required for AMD Family 10h processors
8. *Loosened AMD requirements at this levels.

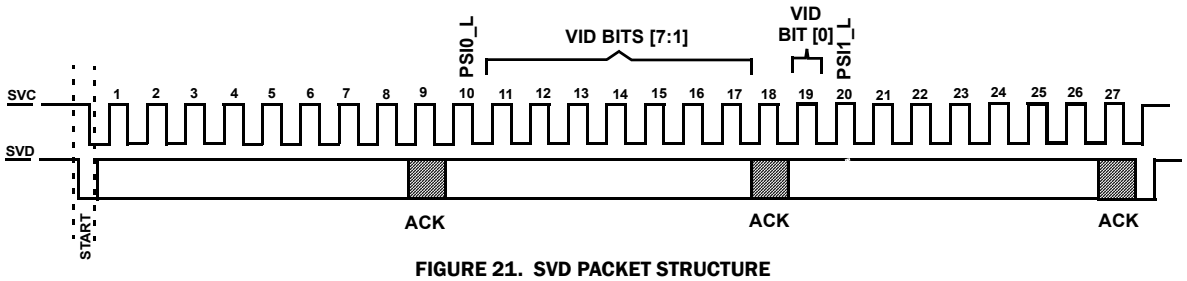


FIGURE 21. SVD PACKET STRUCTURE

SVI Bus Protocol

The AMD processor bus protocol is compliant with SMBus send byte protocol for VID transactions. The AMD SVD packet structure is shown in Figure 21. The description of what each bit of the three bytes that make up the SVI command are shown in Table 8. During a transaction, the processor sends the start sequence followed by each of the three bytes, which end with an optional acknowledge bit. The ISL62773 does not drive the SVD line during the ACK bit. Finally, the processor sends the stop sequence. After the ISL62773 has detected the stop, it can then proceed with the commanded action from the transaction.

TABLE 8. SVD DATA PACKET

BITS	DESCRIPTION
1:5	Always 11000b
6	Core domain selector bit, if set then the following data byte contains VID, power state, telemetry control, load line trim and offset trim apply to the Core VR.
7	Northbridge domain selector bit, if set then the following data byte contains VID, power state, telemetry control, load line trim and offset trim apply to the Northbridge VR.
8	Always 0b
9	Acknowledge bit
10	PSI0_L
11:17	VID code bits [7:1]
18	Acknowledge Bit
19	VID code bit [0]
20	PSI1_L
21	TFN (telemetry functionality)
22:24	Load line slope trim
25:26	Offset trim [1:0]
27	Acknowledge bit

Power States and Telemetry

SVI2 defines two power state indicator levels, see Table 9. As processor current consumption is reduces the power state indicator level increases starting with 0.

For the Core VR operating in 3-phase mode, when PSI0_L is asserted Channel 3 is tri-stated to boost efficiency. When PSI1_L is asserted, Channel 2 is tri-stated and Channel 1 enters diode emulation mode to further boost efficiency. In 2-phase mode, when PSI0_L is asserted, Channel 2 is tri-stated. Asserting PSI1_L in this mode results in Channel 1 entering diode emulation mode.

For the Northbridge VR operating in 2-phase mode, when PSI0_L is asserted Channel 2 is tri-stated to boost efficiency. When PSI1_L is asserted Channel 1 enters diode emulation mode to further boost efficiency.

It is possible for the processor to assert or deassert PSI0_L and PSI1_L out of order. PSI0_L takes priority over PSI1_L. If PSI0_L is deasserted while PSI1_L is still asserted, the ISL62773 will return the selected VR back full channel CCM operation.

TABLE 9. PSI0_L, PSI1_L AND TFN DEFINITION

FUNCTION	BIT	DESCRIPTION
PSI0_L	10	Power State Indicate level 0. When this signal is asserted (active Low) the processor is in a low enough power state for the ISL62773 to take action to boost efficiency by dropping phases.
PSI1_L	20	Power State Indicate level 1. When this signal is asserted (active Low) the processor is in a low enough power state for the ISL62773 to take additional action to boost efficiency beyond that taken with PSI0_L asserted.
TFN	21	Telemetry Functionality. This is an active high signal that allows the processor to control the telemetry functionality of the VR.

The TFN bit along with the Core and Northbridge domain selector bits are used by the processor to change the functionality of telemetry, see Table 10 for more information.

TABLE 10. TFN TRUTH TABLE

TFN, CORE, NB BITS [21,6,7]	DESCRIPTION
1,0,1	Telemetry is in voltage and current mode. Therefore, voltage and current are sent for VDD and VDDNB domains by the controller.
1,0,0	Telemetry is in voltage mode only. Only the voltage of VDD and VDDNB domains is sent by the controller.
1,1,0	Telemetry is disabled.
1,1,1	Reserved

Dynamic Load Line Slope Trim

The ISL62773 supports the SVI2 ability for the processor to manipulate the load line slope of the Core and Northbridge VRs independently using the serial VID interface. The slope manipulation applies to the initial load line slope. A load line slope trim will typically coincide with a VOTF change. Refer to Table 11 for more information about the load line slope trim feature of the ISL62773.

TABLE 11. LOAD LINE SLOPE TRIM DEFINITION

LOAD LINE SLOPE TRIM [2:0]	DESCRIPTION
000	Disable LL
001	-40% mΩ Change
010	-20% mΩ Change
011	No change
100	+20% mΩ Change
101	+40% mΩ Change
110	+60% mΩ Change
111	+80% mΩ Change

Dynamic Offset Trim

The ISL62773 supports the SVI2 ability for the processor to manipulate the output voltage offset of the Core and Northbridge VRs. This offset is in addition to any output voltage offset set via the COMP resistor reader. The dynamic offset trim can disable the COMP resistor programmed offset of either output when Disable All Offset is selected.

TABLE 12. OFFSET TRIM DEFINITION

OFFSET TRIM [1:0]	DESCRIPTION
00	Disable All Offset
01	-25mV Change
10	0mV Change
11	+25mV Change

Protection Features

Core VR and Northbridge VR both provide overcurrent, current-balance, undervoltage and overvoltage fault protections. The controller also provides over-temperature protection. The following discussion is based on Core VR and also applies to the Northbridge VR.

Overcurrent

Overcurrent protection is triggered when the voltage across the IMON resistor is 1.5V. Within 2µs of detecting the IMON voltage, the controller asserts VR_HOT_L low to communicate to the AMD CPU to throttle back. A fault timer begins counting while IMON is at or above the 1.5V threshold. The fault timer lasts 7.5µs to 11µs and then flags an OCP fault. The controller then tri-states the active channels and goes into shutdown. PGOOD is taken low and a fault flag from this VR is sent to the other VR and it is shut down within 10µs. If the IMON voltage drops below the 1.5V threshold prior to the fault timer count finishing, the fault timer is cleared and VR_HOT_L is taken high.

The ISL62773 also features a Way-Overcurrent [WOC] feature, which immediately takes the controller into shutdown. This protection is also referred to as fast overcurrent protection for short-circuit protection. If the IMON current reaches 15µA, WOC is triggered. Active channels are tri-stated and the controller is placed in shutdown and PGOOD is pulled low. There is no fault timer on the WOC fault, the controller takes immediate action. The other controller output is also shut down within 10µs.

Designing the current feedback components and setting the OCP level require knowing the $I_{DDSpike}$ value (EDC) outlined for the AMD CPU under consideration. AMD specifications will outline a TDC current level and an EDC current level for each CPU. The EDC current is the maximum current the CPU can demand for a short, thermally insignificant time. When selecting the components for the current feedback design or using an Intersil design spreadsheet, the EDC current is used as the full load current. The reasoning is that the AMD CPU will view reaching the EDC current as 100% loading. The desired droop current at full load must be set to 45µA. The controller generates a current across the IMON resistor that is ¼ of the average value of the I_{sum} current. The droop current is 5/4 greater than the I_{sum} current, so for a droop current of 45µA the I_{sum} current is 36µA. The recommended IMON resistor value is 133kΩ, 1% tolerance. At full load current, EDC level, the resulting IMON voltage will be 1.2V and telemetry will report 100%. If the load current continues to increase, then the IMON voltage will continue to rise, but the telemetry will still report 100% loading. Once the I_{sum} current reaches 45µA, the corresponding current out of the IMON pin is 11.25µA and the voltage on the IMON resistor will be 1.5V and the controller will report an OC trip. The load current at this point is 25% higher than the EDC current used for setting full load droop current. This additional margin allows the AMD CPU to enter and exit the $I_{DDSpike}$ performance mode without issue unless the load current is out of line with the $I_{DDSpike}$ expectation.

Current-Balance

The controller monitors the ISENx pin voltages to determine current-balance protection. If the ISENx pin voltage difference is greater than 9mV for 1ms, the controller will declare a fault and latch off.

Undervoltage

If the VSEN voltage falls below the output voltage VID value plus any programmed offsets by -325mV, the controller declares an undervoltage fault. The controller deasserts PGOOD and tri-states the power MOSFETs.

Overvoltage

If the VSEN voltage exceeds the output voltage VID value plus any programmed offsets by +325mV, the controller declares an overvoltage fault. The controller deasserts PGOOD and turns on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value. Once the output voltage is below this level, the lower gate is tri-stated. If the output voltage rises above the overvoltage threshold again, the protection process is repeated when all power MOSFETs are turned off. This behavior provides the maximum amount of protection

against shorted high-side power MOSFETs while preventing output ringing below ground.

Thermal Monitor [NTC, NTC_NB]

The ISL62773 features two thermal monitors, which use an external resistor network that includes an NTC thermistor to monitor motherboard temperature and alert the AMD CPU of a thermal issue. Figure 22 shows the basic thermal monitor circuit on the Core VR NTC pin. The Northbridge VR features the same thermal monitor. The controller drives a 30µA current out of the NTC pin and monitors the voltage at the pin. The current flowing out of the NTC pin creates a voltage that is compared to a warning threshold of 640mV. When the voltage at the NTC pin falls to this warning threshold or below, the controller asserts VR_HOT_L to alert the AMD CPU to throttle back load current to stabilize the motherboard temperature. A thermal fault counter begins counting toward a minimum shutdown time of 100µs. The thermal fault counter is an up/down counter, so if the voltage at the NTC pin rises above the warning threshold, it will count down and extend the time for a thermal fault to occur. The warning threshold does have 20mV of hysteresis.

If the voltage at the NTC pin continues to fall down to the shutdown threshold of 580mV or below, the controller goes into shutdown and triggers a thermal fault. The PGOOD pin is pulled low and tri-states the power MOSFETs. A fault on either side will shutdown both VRs.

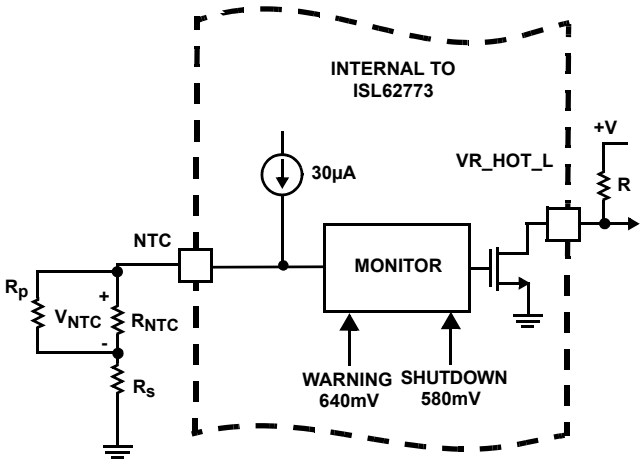


FIGURE 22. CIRCUITRY ASSOCIATED WITH THE THERMAL MONITOR FEATURE OF THE ISL62773

As the board temperature rises, the NTC thermistor resistance decreases and the voltage at the NTC pin drops. When the voltage on the NTC pin drops below the over-temperature trip threshold, then VR_HOT is pulled low. The VR_HOT signal is used to change the CPU operation and decrease power consumption. With the reduction in power consumption by the CPU, the board temperature decreases and the NTC thermistor voltage rises. Once the over-temperature threshold is tripped and VR_HOT is taken low, the over-temperature threshold changes to the reset level. The addition of hysteresis to the over-temperature threshold prevents nuisance trips. Once both pin voltages exceed the over-temperature reset threshold, the pull-down on VR_HOT is released. The signal changes state and the CPU resumes normal operation. The over-temperature threshold returns to the trip level.

Table 13 summarizes the fault protections.

TABLE 13. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	7.5µs to 11.5µs	PWM tri-state, PGOOD latched low	ENABLE toggle or VDD toggle
Phase Current Unbalance	1ms		
Way-Overcurrent (1.5xOC)	Immediately		
Undervoltage -325mV		PGOOD latched low. PWM tri-state.	
Overvoltage +325mV		PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-state.	
NTC Thermal	100µs min	PGOOD latched low. PWM tri-state.	

Fault Recovery

All of the previously described fault conditions can be reset by bringing ENABLE low or by bringing VDD below the POR threshold. When ENABLE and VDD return to their high operating levels, the controller resets the faults and soft-start occurs.

Interface Pin Protection

The SVC and SVD pins feature protection diodes which must be considered when removing power to VDD and VDDIO, but leaving it applied to these pins. Figure 23 shows the basic protection on the pins. If SVC and/or SVD are powered but VDD is not, leakage current will flow from these pins to VDD.

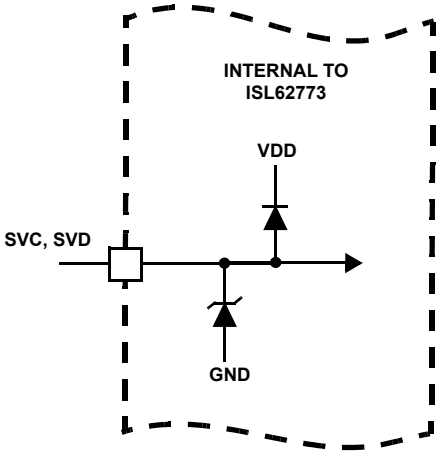


FIGURE 23. PROTECTION DEVICES ON THE SVC AND SVD PINS

Key Component Selection

Inductor DCR Current-Sensing Network

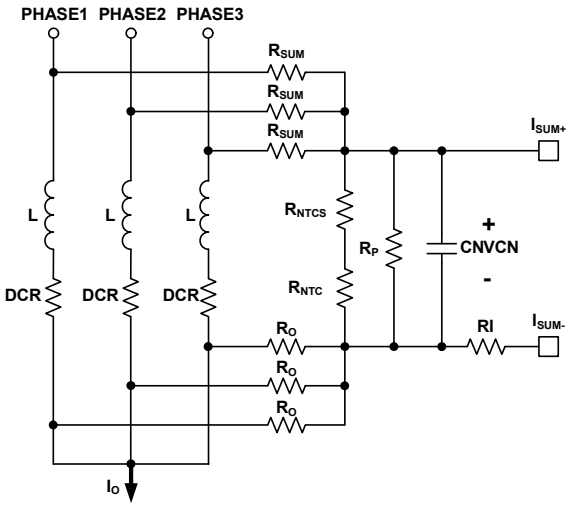


FIGURE 24. DCR CURRENT-SENSING NETWORK

Figure 24 shows the inductor DCR current-sensing network for a 3-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to temperature compensate the inductor DCR change.

The inductor output side pads are electrically shorted in the schematic but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use 1Ω~10Ω R_o to create quality signals. Since R_o value is much smaller than the rest of the current sensing circuit, the following analysis ignores it.

The summed inductor current information is presented to the capacitor C_n. Equations 17 through 21 describe the frequency domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 17)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 18)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 19)}$$

Where N is the number of phases.

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 20)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 21)}$$

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC R_{ntc} value decrease as its temperature decreases. Proper selection of R_{sum}, R_{ntcs}, R_p and R_{ntc} parameters ensures that V_{Cn} represents the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of V_{cn} to the inductor DCR voltage so the droop circuit has a higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole w_{sns} and a zero w_L. One needs to match w_L and w_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing w_L equal to w_{sns} and solving for the solution, Equation 22 gives Cn value.

$$C_n = \frac{L}{\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 22)}$$

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ and L = 0.36µH, Equation 22 gives C_n = 0.406µF.

Assuming the compensator design is correct, Figure 25 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{core} also has a square response.

If C_n value is too large or too small, $V_{Cn}(s)$ does not accurately represent real-time $I_o(s)$ and worsens the transient response. Figure 26 shows the load transient response when C_n is too small. V_{core} sags excessively upon load insertion and may create a system failure. Figure 27 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value.

There is excessive overshoot if load insertion occurs during this time, which may negatively affect the CPU reliability.

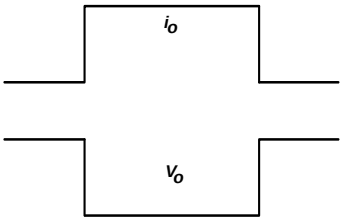


FIGURE 25. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

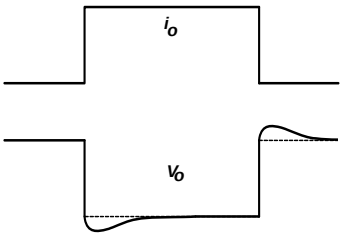


FIGURE 26. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

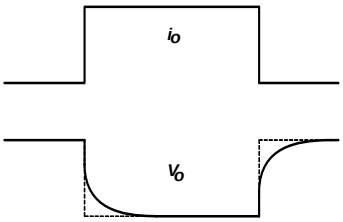


FIGURE 27. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

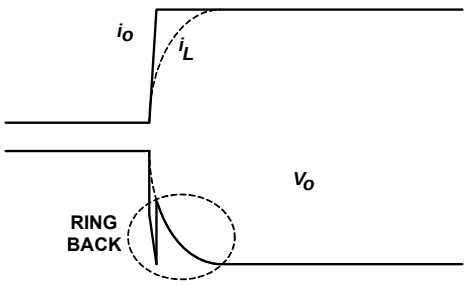


FIGURE 28. OUTPUT VOLTAGE RINGBACK PROBLEM

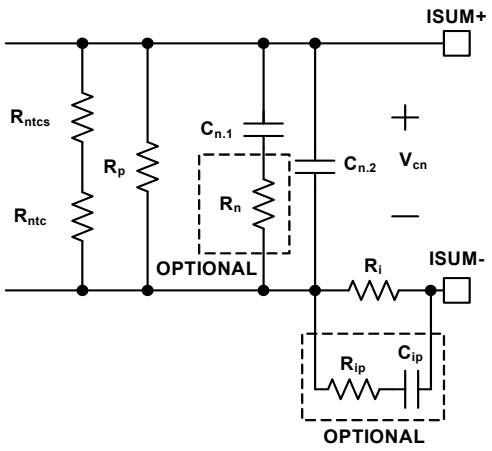


FIGURE 29. OPTIONAL CIRCUITS FOR RINGBACK REDUCTION

Figure 28 shows the output voltage ringback problem during load transient response. The load current i_o has a fast step change, but the inductor current i_L cannot accurately follow. Instead, i_L responds in first-order system fashion due to the nature of the current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_o dip quickly upon load current change. However, the controller regulates V_o according to the droop current i_{droop}, which is a real-time representation of i_L; therefore, it pulls V_o back to the level dictated by i_L, causing the ringback problem. This phenomenon is not observed when the output capacitor has very low ESR and ESL, as is the case with all ceramic capacitors.

Figure 29 shows two optional circuits for reduction of the ring-back. C_n is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 29 shows that two capacitors ($C_{n.1}$ and $C_{n.2}$) are in parallel. Resistor R_n is an optional component to reduce the V_o ringback. At steady state, $C_{n.1} + C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 26 shows, V_o tends to dip when C_n is too small and this effect reduces the V_o ring-back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. The R_n value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and R_n values should be determined through tuning the load transient response waveforms on an actual board.

R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of i_o change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L and V_o will not ring back. The recommended value for R_{ip} is 100Ω. C_{ip} should be determined through tuning the load transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF. However, it should be noted that the R_{ip} -C_{ip} branch may distort the i_{droop} waveform. Instead of being triangular as the real inductor current, i_{droop} may have sharp spikes, which may adversely affect i_{droop} average value detection and therefore may affect OCP accuracy. User discretion is advised.

Resistor Current-Sensing Network

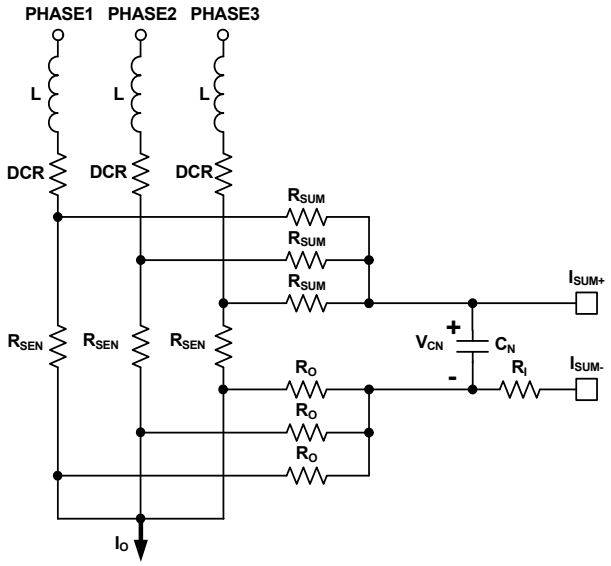


FIGURE 30. RESISTOR CURRENT-SENSING NETWORK

Figure 30 shows the resistor current-sensing network for a 3-phase solution. Each inductor has a series current sensing resistor, R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a filter for noise attenuation. Equations 23 through 25 give the $V_{Cn}(s)$ expression.

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 23)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 24)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 25)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor R_{sen} value does not have significant variation over-temperature, so there is no need for the NTC network.

The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

Overcurrent Protection

Refer to Equation 1 on page 17 and Figures 24, 28 and 30; resistor R_i sets the droop current, I_{droop}. Tables 1 and 2 on page 19 show the internal OCP threshold. It is recommended to design I_{droop} without using the R_{comp} resistor.

For example, the OCP threshold is 1.5V on the IMON pin. This translates to 45µA of I_{sum} current or 56.25µA of droop current. I_{droop} is designed to be 45µA at full load, so the OCP trip level is 1.25x of the full load current.

For inductor DCR sensing, Equation 26 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$:

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 26)}$$

Substitution of Equation 26 into Equation 1 gives Equation 27:

$$I_{droop} = \frac{1}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 27)}$$

Therefore:

$$R_i = \frac{R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{droop}} \quad \text{(EQ. 28)}$$

Substitution of Equation 18 and application of the OCP condition in Equation 28 gives Equation 29:

$$R_i = \frac{\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{droopmax}} \quad \text{(EQ. 29)}$$

Where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.9mΩ, I_{omax} = 65A and $I_{droopmax}$ = 45µA. Equation 29 gives R_i = 359Ω.

For resistor sensing, Equation 30 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 30)}$$

Substitution of Equation 30 into Equation 1 gives Equation 31:

$$I_{droop} = \frac{1}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 31)}$$

Therefore:

$$R_i = \frac{R_{sen} \times I_o}{N \times I_{droop}} \quad \text{(EQ. 32)}$$

Substitution of Equation 32 and application of the OCP condition in Equation 28 gives Equation 33:

$$R_i = \frac{R_{sen} \times I_{omax}}{N \times I_{droopmax}} \quad \text{(EQ. 33)}$$

Where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sen} = 1mΩ, I_{omax} = 65A and $I_{droopmax}$ = 45µA, Equation 33 gives R_i = 481Ω.

Load Line Slope

See Figure 16 for load line implementation.

For inductor DCR sensing, substitution of Equation 27 into Equation 2 gives the load line slope expression in Equation 34:

$$LL = \frac{V_{droop}}{I_o} = \frac{R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \quad \text{(EQ. 34)}$$

For resistor sensing, substitution of Equation 31 into Equation 2 gives the load line slope expression in Equation 35:

$$LL = \frac{V_{droop}}{I_o} = \frac{R_{sen} \times R_{droop}}{N \times R_i} \quad \text{(EQ. 35)}$$

Substitution of Equation 28 and rewriting Equation 34, or substitution of Equation 32 and rewriting Equation 35, gives the same result as in Equation 36:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad \text{(EQ. 36)}$$

One can use the full-load condition to calculate R_{droop}. For example, given I_{omax} = 65A, $I_{droopmax}$ = 45µA and LL = 2.1mΩ, Equation 36 gives R_{droop} = 3.03kΩ.

It is recommended to start with the R_{droop} value calculated by Equation 36 and fine-tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Compensator

Figure 25 on page 29 shows the desired load transient response waveforms. Figure 31 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e., a constant output impedance, then in the entire frequency range, V_o will have a square response when I_o has a square change.

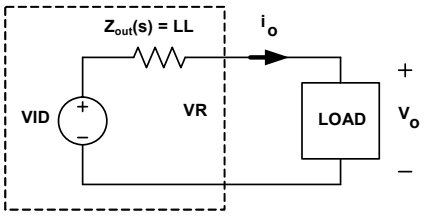


FIGURE 31. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network so that VR achieves constant output impedance as a stable system.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop, which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 32 conceptually shows T1(s) measurement setup and Figure 33 conceptually shows T2(s) measurement setup. The VR senses the inductor current, multiplies it by a gain of the load line slope, adds it on top of the sensed output voltage and then feeds it to the compensator. T1 is measured after the summing node and T2 is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can actually be measured on an ISL62773 regulator.

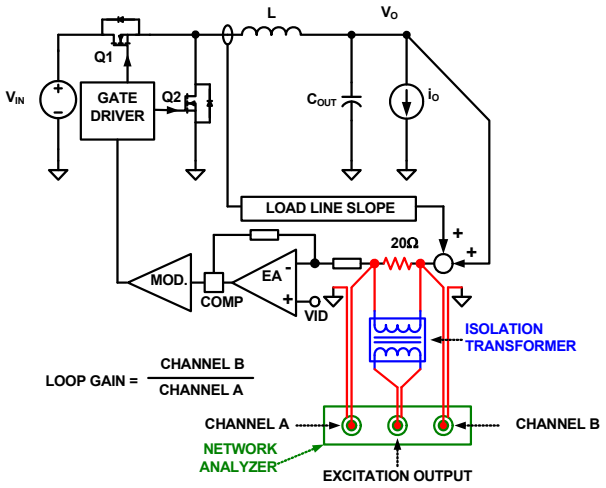


FIGURE 32. LOOP GAIN T1(s) MEASUREMENT SETUP

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s), therefore has a higher impact on system stability.

T2(s) is the voltage loop gain with closed droop loop, thus having a higher impact on output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin and an output impedance equal to or smaller than the load line slope.

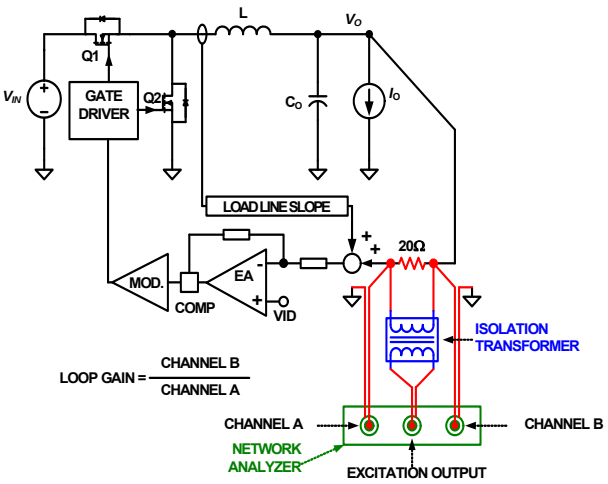


FIGURE 33. LOOP GAIN T2(s) MEASUREMENT SETUP

Current Balancing

Refer to Figures 17 through 24 for information on current balancing. The ISL62773 achieves current balancing through matching the ISEN pin voltages. R_{isen} and C_{isen} form filters to remove the switching ripple of the phase node voltages. It is recommended to use a rather long $R_{isen}C_{isen}$ time constant such that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are R_s = 10kΩ and C_s = 0.22µF.

Thermal Monitor Component Selection

The ISL62773 features two pins, NTC and NTC_NB, which are used to monitor motherboard temperature and alert the AMD CPU if a thermal issues arises. The basic function of this circuitry is outlined in the "Thermal Monitor [NTC, NTC_NB]" on page 27. Figure 34 shows the basic configuration of the NTC resistor, R_{NTC} and offset resistor, R_S, used to generate the warning and shutdown voltages at the NTC pin.

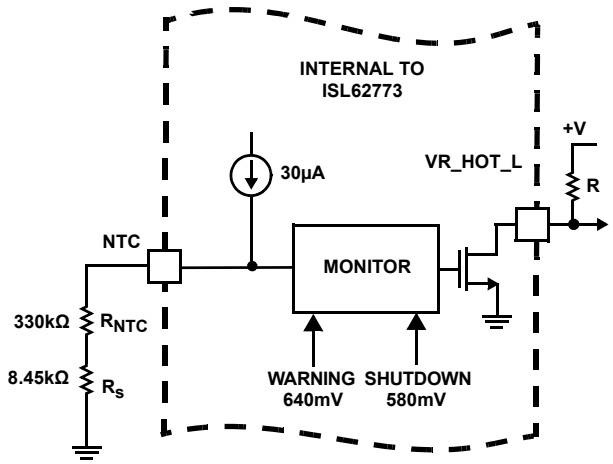


FIGURE 34. THERMAL MONITOR FEATURE OF THE ISL62773

As the board temperature rises, the NTC thermistor resistance decreases and the voltage at the NTC pin drops. When the voltage on the NTC pin drops below the thermal warning threshold of 0.640V, then VR_HOT_L is pulled low. When the AMD CPU detects that VR_HOT_L has gone low, it will begin throttling back load current on both outputs to reduce the board temperature.

If the board temperature continues to rise, the NTC thermistor resistance will drop further and the voltage at the NTC pin could drop below the thermal shutdown threshold of 0.580V. Once this threshold is reached, the ISL62773 shuts down both Core and Northbridge VRs indicating a thermal fault has occurred prior to the thermal fault counter triggering a fault.

Selection of the NTC thermistor can vary depending on how the resistor network is configured. The equivalent resistance at the typical thermal warning threshold voltage of 0.64V is defined in Equation 37.

$$\frac{0.64V}{30\mu A} = 21.3k\Omega \quad \text{(EQ. 37)}$$

The equivalent resistance at the typical thermal shutdown threshold voltage of 0.58V required to shutdown both outputs is defined in Equation 38.

$$\frac{0.58V}{30\mu A} = 19.3k\Omega \quad \text{(EQ. 38)}$$

The NTC thermistor value correlates to the resistance change between the warning and shutdown thresholds and the required temperature change. If the warning level is designed to occur at a board temperature of +100°C and the thermal shutdown level at a board temperature of +105°C, then the resistance change of the thermistor can be calculated. For example, a Panasonic NTC thermistor with B = 4700 has a resistance ratio of 0.03939 of its nominal value at +100°C and 0.03308 of its nominal value at +105°C. Taking the required resistance change between the thermal warning threshold and the shutdown threshold and dividing it by the change in resistance ratio of the NTC thermistor at the two temperatures of interest, the required resistance of the NTC is defined in Equation 39.

$$\frac{(21.3k\Omega - 19.3k\Omega)}{(0.03939 - 0.03308)} = 317k\Omega \quad \text{(EQ. 39)}$$

The closest standard thermistor to the value calculated with B = 4700 is 330kΩ. The NTC thermistor part number is ERTJ0EV334J. The actual resistance change of this standard thermistor value between the warning threshold and the shutdown threshold is calculated in Equation 40.

$$(330k\Omega \cdot 0.03939) - (330k\Omega \cdot 0.03308) = 2.082k\Omega \quad \text{(EQ. 40)}$$

Since the NTC thermistor resistance at +105°C is less than the required resistance from Equation 38, additional resistance in series with the thermistor is required to make up the difference. A standard resistor, 1% tolerance, added in series with the thermistor will increase the voltage seen at the NTC pin. The additional resistance required is calculated in Equation 41.

$$19.3k\Omega - 10.916k\Omega = 8.384k\Omega \quad \text{(EQ. 41)}$$

The closest, standard 1% tolerance resistor is 8.45kΩ.

The NTC thermistor is placed in a hot spot on the board, typically near the upper MOSFET of Channel 1 of the respective output. The standard resistor is placed next to the controller.

Layout Guidelines

PCB Layout Considerations

POWER AND SIGNAL LAYERS PLACEMENT ON THE PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board. The ground-plane layer should be adjacent to the signal layer to provide shielding.

COMPONENT PLACEMENT

There are two sets of critical components in a DC/DC converter; the power components and the small signal components. The power components are the most critical because they switch large amount of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors and the inductor. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each power train. Symmetrical layout allows heat to be dissipated equally across all power trains. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, PGND, PHASE and BOOT.

When placing MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as

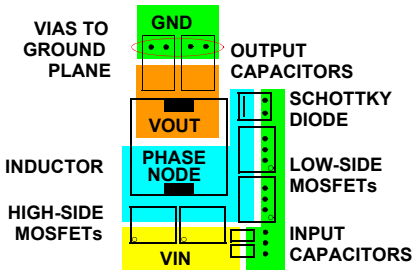


FIGURE 35. TYPICAL POWER COMPONENT PLACEMENT

thermally possible (see Figure 35). Input high-frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High-frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target (microprocessor), making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

Table 14 shows layout considerations for the ISL62773 controller by pin.

TABLE 14. LAYOUT CONSIDERATIONS FOR THE ISL62773 CONTROLLER

PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through a low impedance path. A minimum of 5 vias are recommended to connect this pad to the internal ground plane layers of the PCB
1	ISEN2_NB	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN_NB, then through another capacitor (Cvsumn_nb) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: 1. ISEN1_NB pin to ISEN2_NB pin 2. Any ISENx_NB pin to GND
2	NTC_NB	The NTC thermistor must be placed close to the thermal source that is monitored to determine Northbridge thermal throttling. Placement at the hottest spot of the Northbridge VR is recommended. Additional standard resistors in the resistor network on this pin should be placed near the IC.
3	IMON_NB	Place the IMON_NB resistor close to this pin and make keep a tight GND connection.
4	SVC	Use good signal integrity practices and follow AMD recommendations.
5	VR_HOT_L	Follow AMD recommendations. Placement of the pull-up resistor near the IC is recommended.
6	SVD	Use good signal integrity practices and follow AMD recommendations.
7	VDDIO	Use good signal integrity practices and follow AMD recommendations.
8	SVT	Use good signal integrity practices and follow AMD recommendations.
9	ENABLE	No special considerations.
10	PWROK	Use good signal integrity practices and follow AMD recommendations.
11	IMON	Place the IMON resistor close to this pin and make keep a tight GND connection.
12	NTC	The NTC thermistor must be placed close to the thermal source that is monitored to determine Core thermal throttling. Placement at the hottest spot of the Core VR is recommended. Additional standard resistors in the resistor network on this pin should be placed near the IC.

TABLE 14. LAYOUT CONSIDERATIONS FOR THE ISL62773 CONTROLLER (Continued)

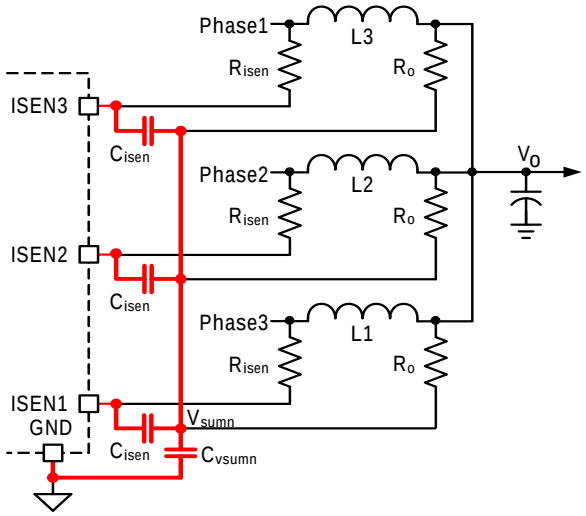
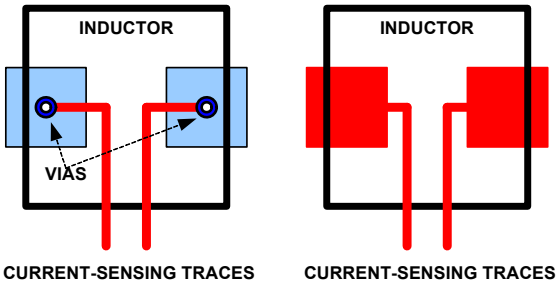
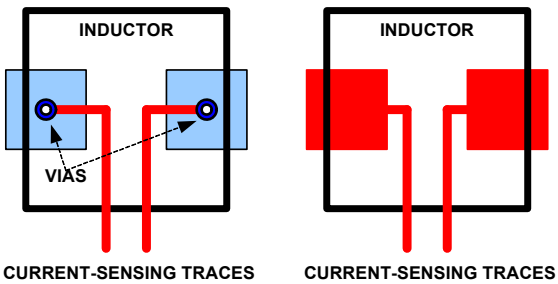
PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
13	ISEN3	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN and then through another capacitor (C_{vsumn}) to GND. Place Cisen capacitors as close as possible to the controller and keep the following loops small: 1. Any ISEN pin to another ISEN pin 2. Any ISEN pin to GND The red traces in the following drawing show the loops to be minimized. 
14	ISEN2	
15	ISEN1	
16	ISUMP	Place the current sensing circuit in general proximity of the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to Core VR Channel 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUMP and VSUMN signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. 
17	ISUMN	
18	VSEN	Place the filter on these pins in close proximity to the controller for good coupling.
19	RTN	
20	FB2	Place the compensation components in general proximity of the controller.
21	FB	
22	COMP	
23	PGOOD	No special consideration.
24	BOOT1	Use a wide trace width (>30mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
25	UGATE1	These two signals should be routed together in parallel. Each trace should have sufficient width (>30mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE1 to the Core VR Channel 1 high-side MOSFET source pin instead of a general connection to PHASE1 copper is recommended for better performance.
26	PHASE1	

TABLE 14. LAYOUT CONSIDERATIONS FOR THE ISL62773 CONTROLLER (Continued)

PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
27	LGATE1	Use sufficient trace width (>30mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.
28	PWM_Y	No special considerations.
29	VDD	A high quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin with the filter resistor nearby the IC.
30	VDDP	A high quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin.
31	LGATE2	Use sufficient trace width (>30mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.
32	PHASE2	These two signals should be routed together in parallel. Each trace should have sufficient width (>30mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE2 to the Core VR Channel 2 high-side MOSFET source pin instead of a general connection to PHASE2 copper is recommended for better performance.
33	UGATE2	
34	BOOT2	Use a wide trace width (>30mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
35	VIN	Place the decoupling capacitor in close proximity to the pin with a short connection to the internal GND plane.
36	BOOTX	Use a wide trace width (>30mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
37	UGATEX	These two signals should be routed together in parallel. Each trace should have sufficient width (>30mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASEX to the high-side MOSFET source pin instead of a general connection to the PHASEX copper is recommended for better performance.
38	PHASEX	
39	LGATEX	Use sufficient trace width (>30mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.
40	PWM2_NB	No special considerations.
41	FCCM_NB	
42	PGOOD_NB	No special consideration.
43	COMP_NB	Place the compensation components in general proximity of the controller.
44	FB_NB	
45	VSEN_NB	Place the filter on this pin in close proximity to the controller for good coupling.
46	ISUMN_NB	Place the current sensing circuit in general proximity of the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to Core VR Channel 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUMP and VSUMN signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. 
47	ISUMP_NB	
48	ISEN1_NB	

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 16, 2015	FN8263.1	On page 1 under Features, added "Serial VID clock frequency range 100kHz to 25MHz" below "Supports AMD SVI 2.0 serial data bus interface". Updated Products section to About Intersil content.
March 7, 2012	FN8263.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

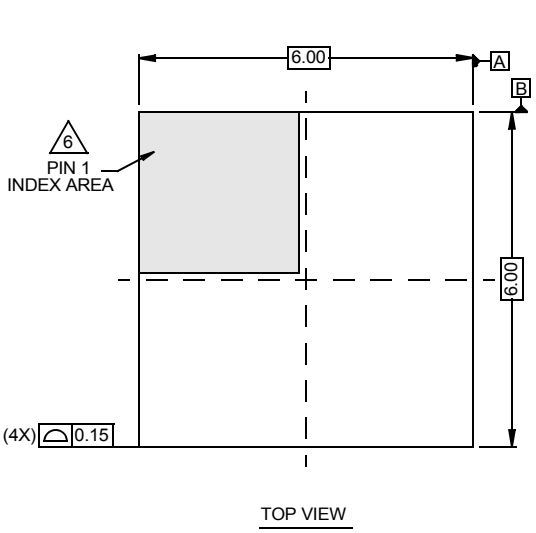
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

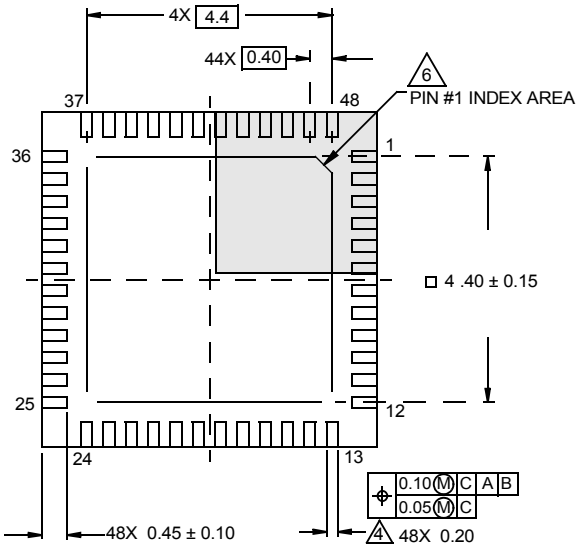
L48.6x6B

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

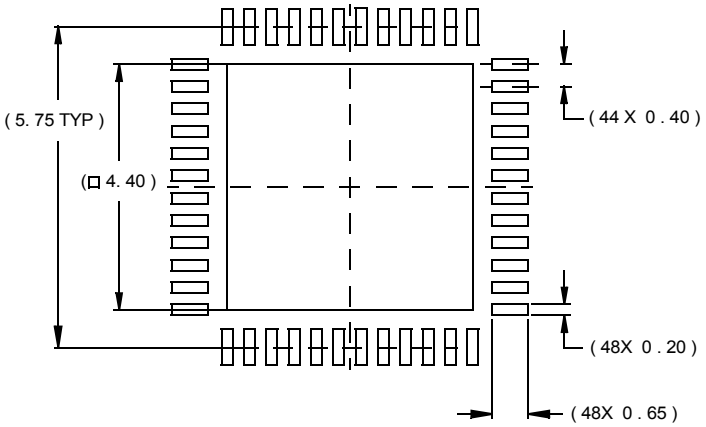
Rev 0, 9/09



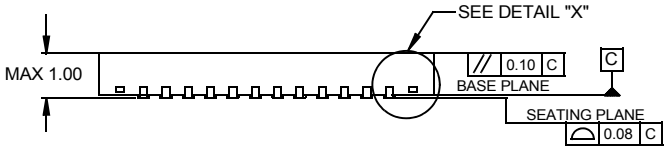
TOP VIEW



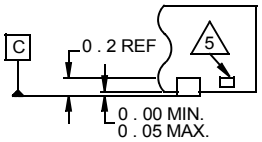
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.