

CAB008M12GM3

1200 V, 8 mΩ All-Silicon Carbide Half-Bridge Module

| | |
|--------------|---------------|
| V_{DS} | 1200 V |
| $R_{DS(on)}$ | 8 mΩ |

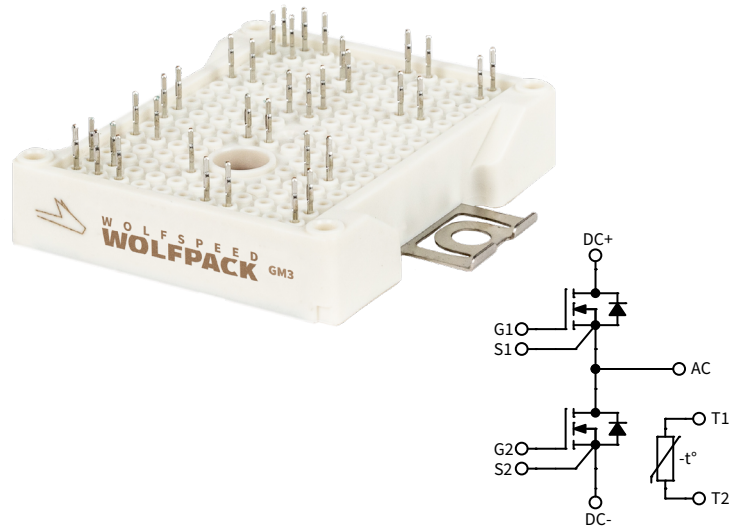
Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation

Applications

- EV Chargers
- Solar
- High-Efficiency Converters / Inverters
- Motor & Traction Drives
- Smart-Grid / Grid-Tied Distributed Generation

Package



System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Maximum Parameters (Verified by Design)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|-------------------|---|------|------|------|------------------|--|---------|
| $V_{DS\ max}$ | Drain-Source Voltage | | | 1200 | V | | |
| $V_{GS\ max}$ | Gate-Source Voltage, Maximum Value | -8 | | +19 | | Transient, <100 ns | Fig. 33 |
| $V_{GS\ op}$ | Gate-Source Voltage, Recommended | -4 | | +15 | | Static | |
| I_D | DC Continuous Drain Current ($T_{VJ} \leq 150\ ^\circ\text{C}$) | | 146 | | A | $V_{GS} = 15\ \text{V}, T_{HS} = 50\ ^\circ\text{C}, T_{VJ} \leq 150\ ^\circ\text{C}$ | Fig. 20 |
| | DC Continuous Drain Current ($T_{VJ} \leq 175\ ^\circ\text{C}$) | | 154 | | | $V_{GS} = 15\ \text{V}, T_{HS} = 50\ ^\circ\text{C}, T_{VJ} \leq 175\ ^\circ\text{C}$ | |
| $I_{SD\ BD}$ | DC Source-Drain Current (Body Diode) | | 79 | | | $V_{GS} = -4\ \text{V}, T_{HS} = 50\ ^\circ\text{C}, T_{VJ} \leq 175\ ^\circ\text{C}$ | |
| $I_{D\ (pulsed)}$ | Maximum Pulsed Drain Current | | | 308 | | t_{Pmax} limited by T_{VJ-max} $V_{GS} = 15\ \text{V}, T_{HS} = 50\ ^\circ\text{C}$ | |
| $T_{VJ\ op}$ | Maximum Virtual Junction Temperature under Switching Conditions | -40 | | 150 | $^\circ\text{C}$ | Operation | |
| | | -40 | | 175 | $^\circ\text{C}$ | Intermittent with Reduced Life | |

MOSFET Characteristics (Per Position) ($T_{VJ} = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---------------|--|------|-------|------|---------------------------|---|--------------------|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 1200 | | | V | $V_{GS} = 0\text{ V}, T_{VJ} = -40^\circ\text{C}$ | |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.8 | 2.5 | 3.6 | | $V_{DS} = V_{GS}, I_D = 46\text{ mA}$ | |
| | | | 2.1 | | | $V_{DS} = V_{GS}, I_D = 46\text{ mA}, T_{VJ} = 150^\circ\text{C}$ | |
| I_{DSS} | Zero Gate Voltage Drain Current | | 5 | 80 | μA | $V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$ | |
| I_{GSS} | Gate-Source Leakage Current | | 0.05 | 1.5 | | $V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$ | |
| $R_{DS(on)}$ | Drain-Source On-State Resistance (Devices Only) | | 8.0 | 10.4 | m Ω | $V_{GS} = 15\text{ V}, I_D = 150\text{ A}$ | Fig. 2 Fig. 3 |
| | | | 12.8 | | | $V_{GS} = 15\text{ V}, I_D = 150\text{ A}, T_{VJ} = 150^\circ\text{C}$ | |
| | | | 14.4 | | | $V_{GS} = 15\text{ V}, I_D = 150\text{ A}, T_{VJ} = 175^\circ\text{C}$ | |
| g_{fs} | Transconductance | | 107 | | S | $V_{DS} = 20\text{ V}, I_{DS} = 150\text{ A}$ | Fig. 4 |
| | | | 101 | | | $V_{DS} = 20\text{ V}, I_{DS} = 150\text{ A}, T_{VJ} = 150^\circ\text{C}$ | |
| E_{On} | Turn-On Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$ | | 2.98 | | mJ | $V_{DD} = 600\text{ V},$ $I_D = 150\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(OFF)} = 0.0\ \Omega, R_{G(ON)} = 1.5\ \Omega,$ $L = 40\ \mu\text{H}$ | Fig. 11 Fig. 13 |
| | | | 3.26 | | | | |
| | | | 3.44 | | | | |
| E_{Off} | Turn-Off Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$ | | 0.26 | | | | |
| | | | 0.28 | | | | |
| | | | 0.28 | | | | |
| $R_{G(int)}$ | Internal Gate Resistance | | 1.68 | | Ω | $f = 100\text{ kHz}, V_{AC} = 25\text{ mV}$ | |
| C_{iss} | Input Capacitance | | 13.6 | | nF | $V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$ | Fig. 9 |
| C_{oss} | Output Capacitance | | 0.56 | | | | |
| C_{rss} | Reverse Transfer Capacitance | | 43 | | | | |
| Q_{GS} | Gate to Source Charge | | 160 | | nC | $V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 150\text{ A}$ Per IEC60747-8-4 pg 21 | |
| Q_{GD} | Gate to Drain Charge | | 136 | | | | |
| Q_G | Total Gate Charge | | 472 | | | | |
| R_{thJH} | FET Thermal Resistance, Junction to Heatsink | | 0.363 | | $^\circ\text{C}/\text{W}$ | | Fig. 17 |



Diode Characteristics (Per Position) ($T_{VJ} = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|-----------|--|------|------|------|---------------|---|---------|
| V_{SD} | Body Diode Forward Voltage | | 5.3 | | V | $V_{GS} = -4\text{ V}, I_{SD} = 150\text{ A}$ | Fig. 7 |
| | | | 4.8 | | | $V_{GS} = -4\text{ V}, I_{SD} = 150\text{ A}, T_{VJ} = 150^\circ\text{C}$ | |
| | | | 4.7 | | | $V_{GS} = -4\text{ V}, I_{SD} = 150\text{ A}, T_{VJ} = 175^\circ\text{C}$ | |
| t_{rr} | Reverse Recovery Time | | 28 | | ns | $V_{GS} = -4\text{ V}, I_{SD} = 150\text{ A}, V_R = 600\text{ V}$ $di/dt = 17.5\text{ A/ns}, T_{VJ} = 150^\circ\text{C}$ | Fig. 32 |
| Q_{RR} | Reverse Recovery Charge | | 2.8 | | μC | | |
| I_{RRM} | Peak Reverse Recovery Current | | 200 | | A | | |
| E_{RR} | Reverse Recovery Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$ | | 0.24 | | mJ | $V_{DD} = 600\text{ V}, I_D = 150\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G(ON)} = 1.5\ \Omega,$ $L = 40\ \mu\text{H}$ | Fig. 14 |
| | | | 0.59 | | | | |
| | | | 0.85 | | | | |

Module Physical Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------|------------------------------------|------|------|------|------------------|--|
| R_{HS} | Package Resistance, M1 (High-Side) | | 1.02 | | m Ω | $T_C = 25^\circ\text{C}, I_D = 150\text{ A}, \text{Note 1}$ |
| | | | 1.43 | | | $T_C = 125^\circ\text{C}, I_D = 150\text{ A}, \text{Note 1}$ |
| R_{LS} | Package Resistance, M2 (Low-Side) | | 0.94 | | m Ω | $T_C = 25^\circ\text{C}, I_D = 150\text{ A}, \text{Note 1}$ |
| | | | 1.30 | | | $T_C = 125^\circ\text{C}, I_D = 150\text{ A}, \text{Note 1}$ |
| L_{Stray} | Stray Inductance | | 7.4 | | nH | Between DC- and DC+, $f = 10\text{ MHz}$ |
| T_C | Case Temperature | -40 | | 125 | $^\circ\text{C}$ | |
| W | Weight | | 39 | | g | |
| M_S | Mounting Torque | | 2.0 | 2.3 | N-m | M4 bolts |
| V_{isol} | Case Isolation Voltage | | 3 | | kV | AC, 50 Hz, 1 min |
| CTI | Comparative Tracking Index | 200 | | | | |
| | Clearance Distance | | 5.0 | | mm | Terminal to Terminal |
| | | | 10.0 | | | Terminal to Heatsink |
| | Creepage Distance | | 6.3 | | mm | Terminal to Terminal |
| | | | 11.5 | | | Terminal to Heatsink |

Note 1 Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

NTC Thermistor Characterization

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|------------------|--|------|------|------|------------|------------------------------|---------|
| R_{NTC} | Rated Resistance | | 5.0 | | k Ω | $T_{NTC} = 25^\circ\text{C}$ | Fig. 23 |
| $\Delta R/R$ | Resistance Tolerance at 25°C | -5 | | 5 | % | | |
| $\beta_{25/50}$ | Beta Value ($T_2 = 50^\circ\text{C}$) | | 3380 | | K | | |
| $\beta_{25/80}$ | Beta Value ($T_2 = 80^\circ\text{C}$) | | 3468 | | K | | |
| $\beta_{25/100}$ | Beta Value ($T_2 = 100^\circ\text{C}$) | | 3523 | | K | | |
| P_{Max} | Power Dissipation | | | 10 | mW | $T_{NTC} = 25^\circ\text{C}$ | |

Typical Performance

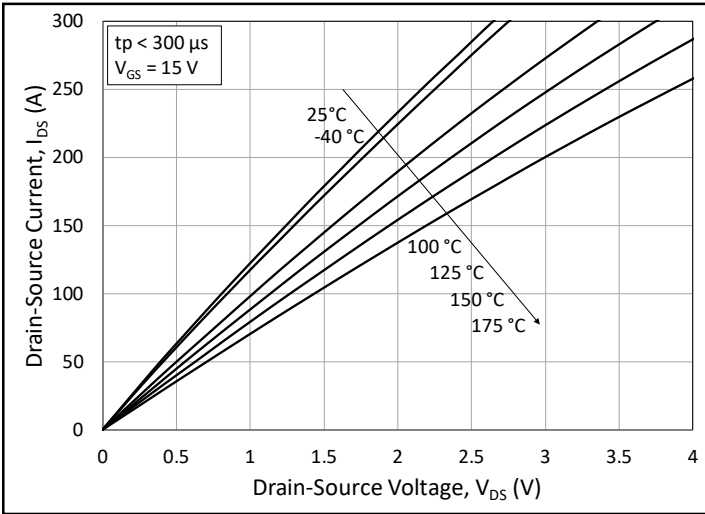


Figure 1. Output Characteristics for Various Junction Temperatures

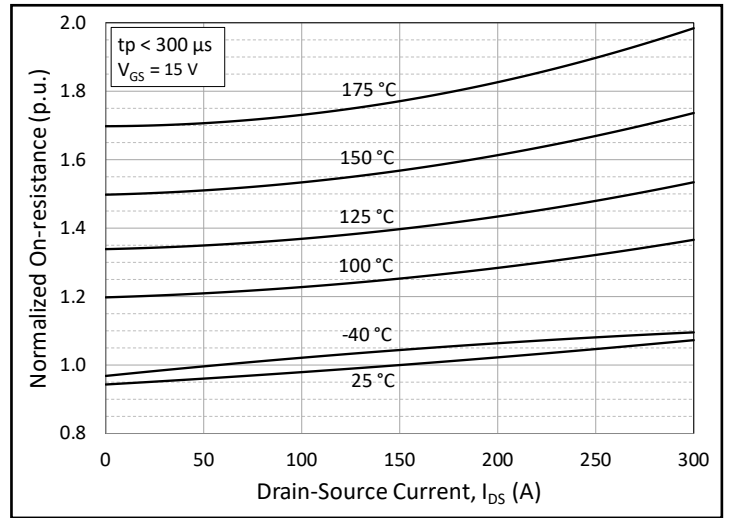


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

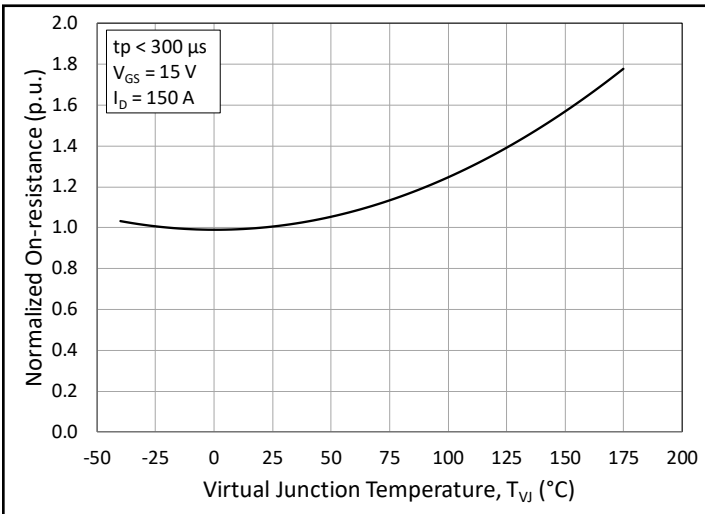


Figure 3. Normalized On-State Resistance vs. Junction Temperature

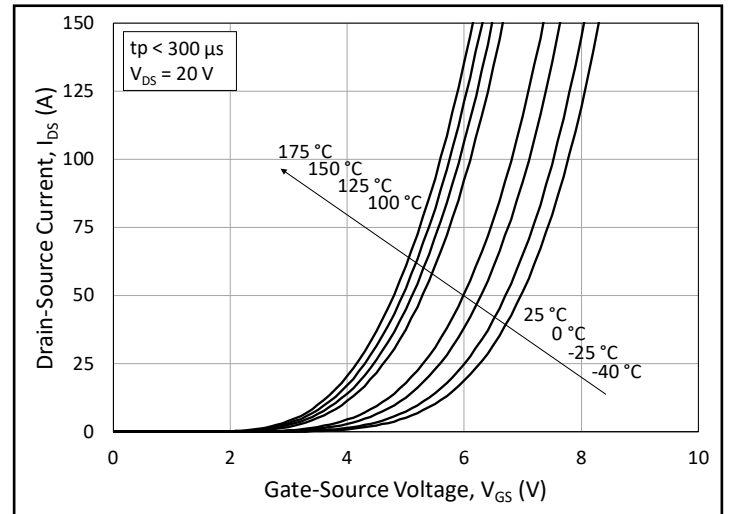


Figure 4. Transfer Characteristic for Various Junction Temperatures

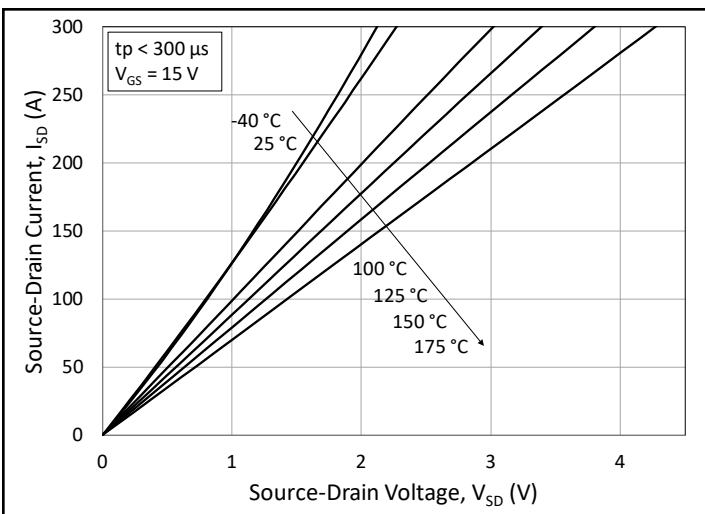


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15\text{ V}$

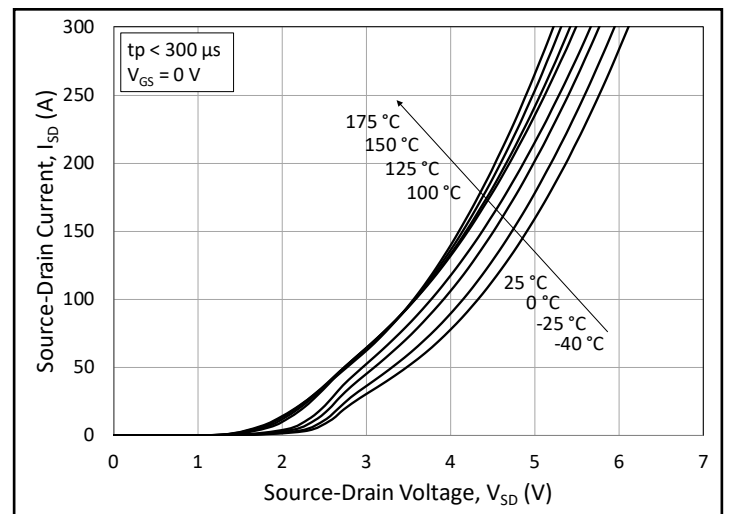


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0\text{ V}$ (Body Diode)

Typical Performance

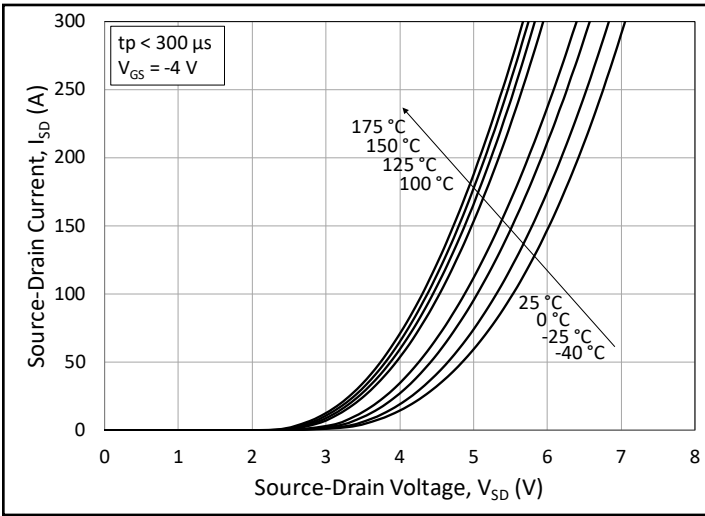


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4$ V (Body Diode)

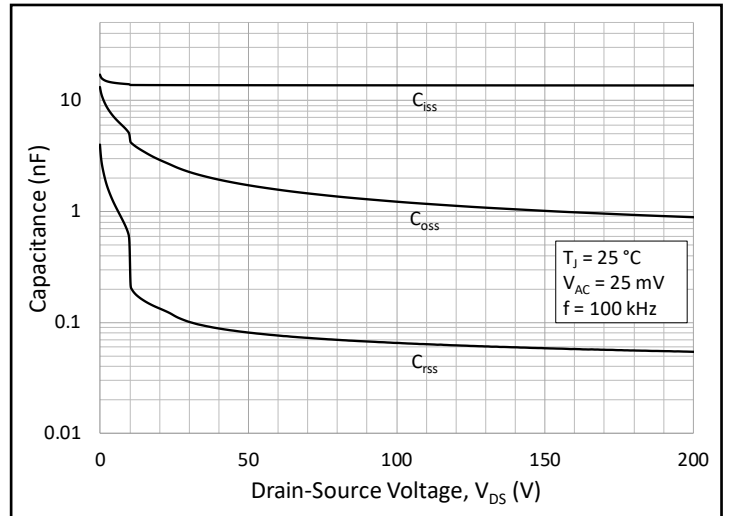


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

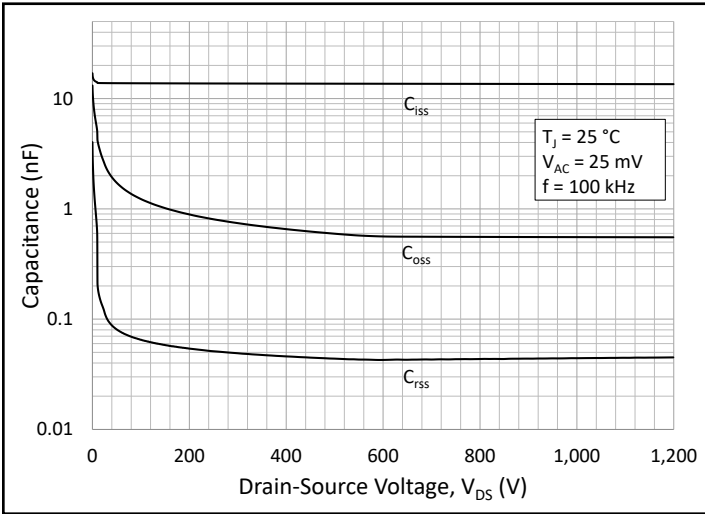


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

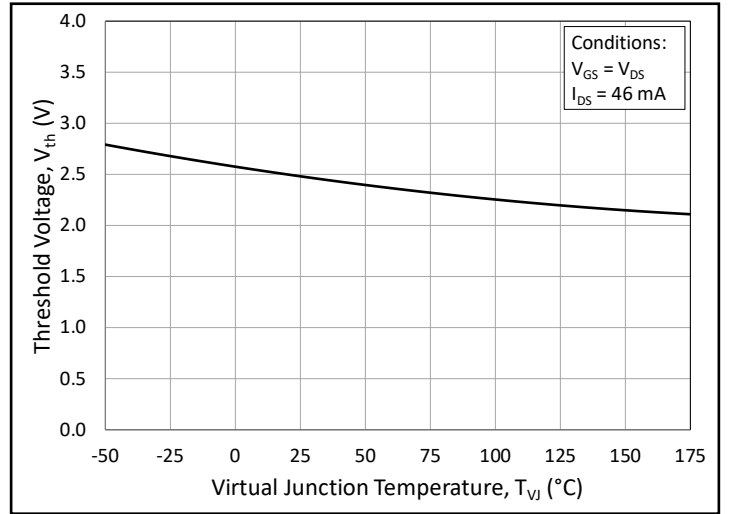


Figure 10. Threshold Voltage vs. Junction Temperature

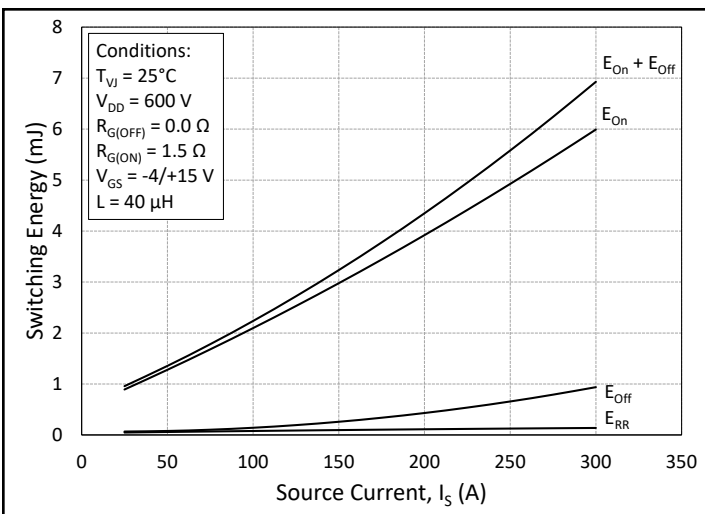


Figure 11. Switching Energy vs. Drain Current ($V_{DS} = 600$ V)

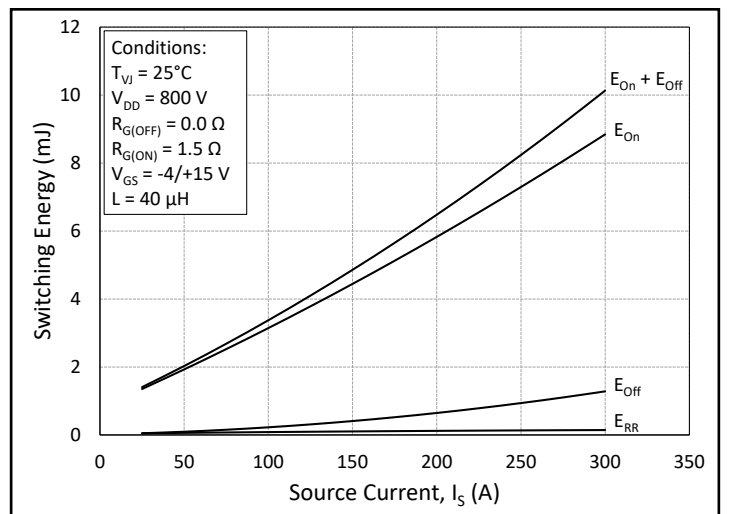


Figure 12. Switching Energy vs. Drain Current ($V_{DS} = 800$ V)

Typical Performance

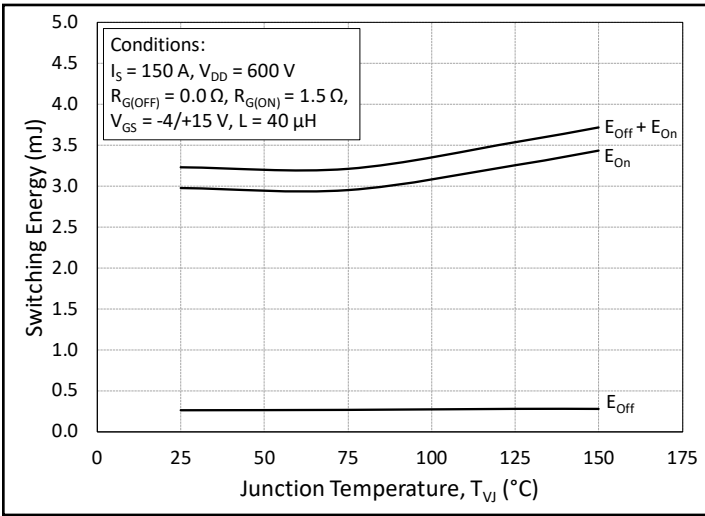


Figure 13. MOSFET Switching Energy vs. Junction Temperature

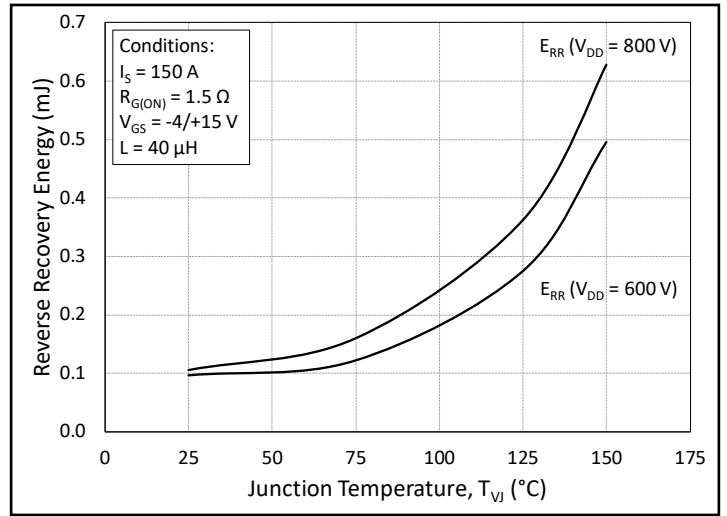


Figure 14. Reverse Recovery Energy vs. Junction Temperature

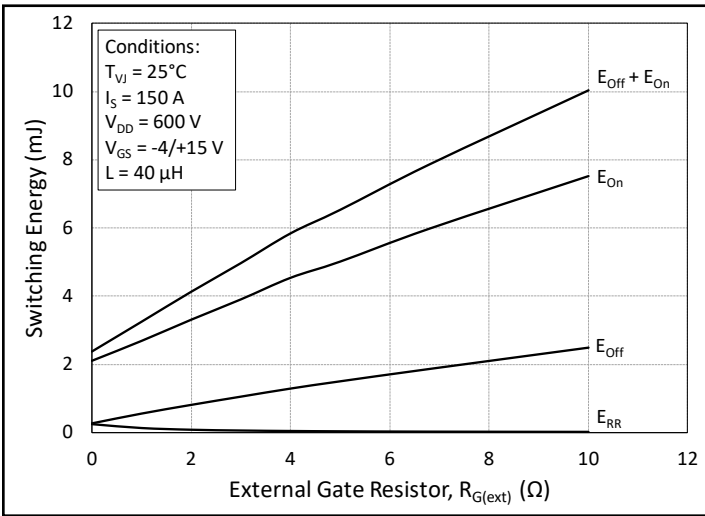


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

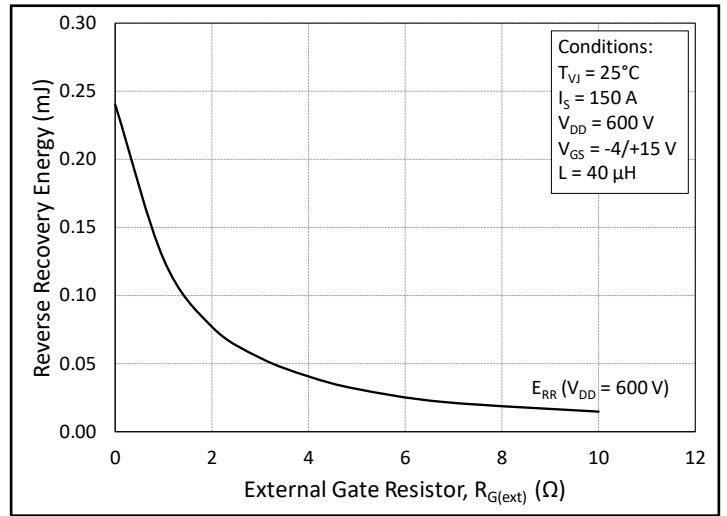


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

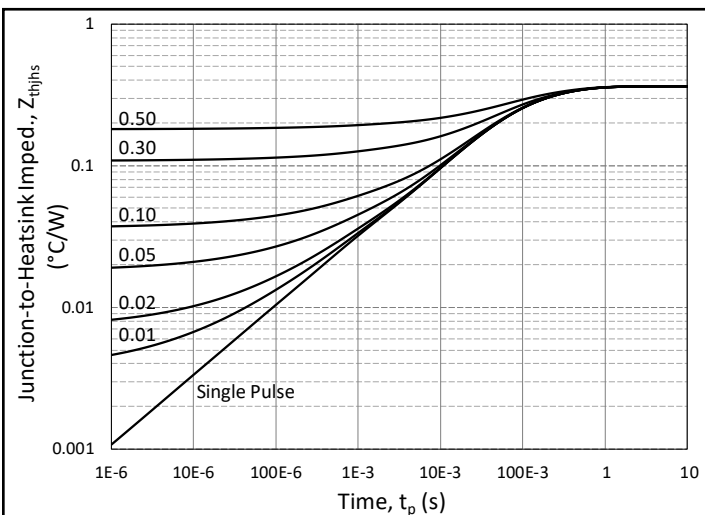


Figure 17. MOSFET Junction to Heatsink Transient Thermal Impedance, $Z_{th\ JHS}$ ($^{\circ}C/W$)

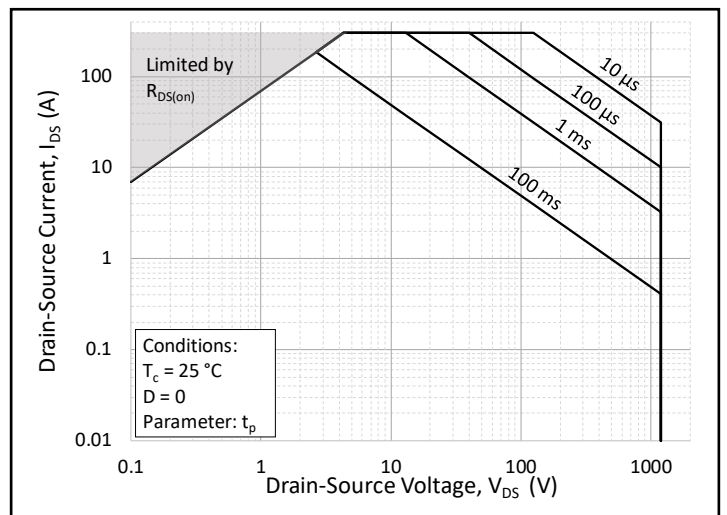


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

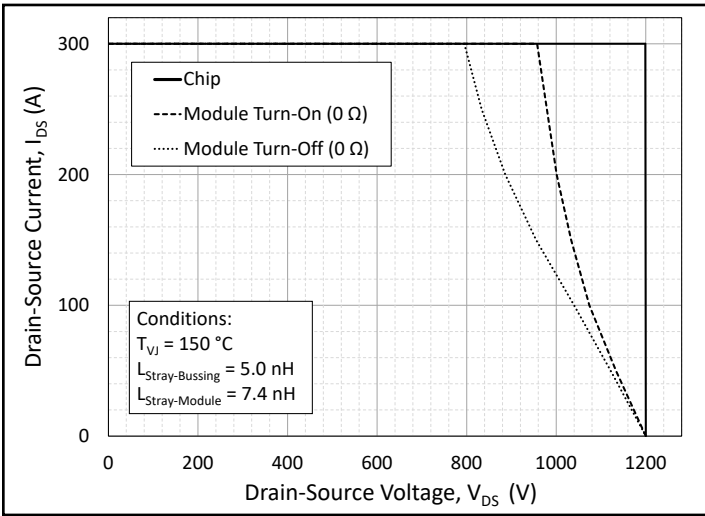


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

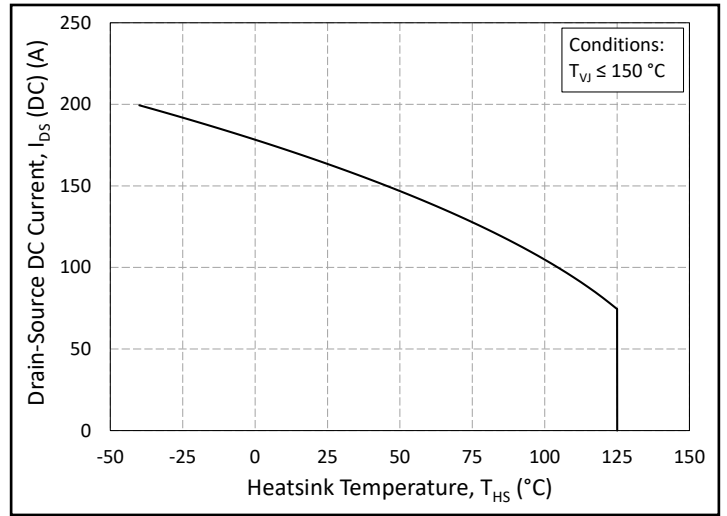


Figure 20. Continuous Drain Current Derating vs. Heatsink Temperature

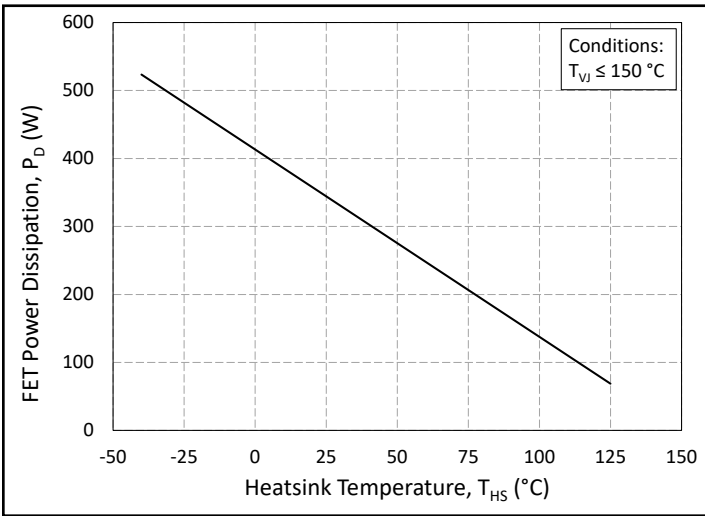


Figure 21. Maximum Power Dissipation Derating vs. Heatsink Temperature

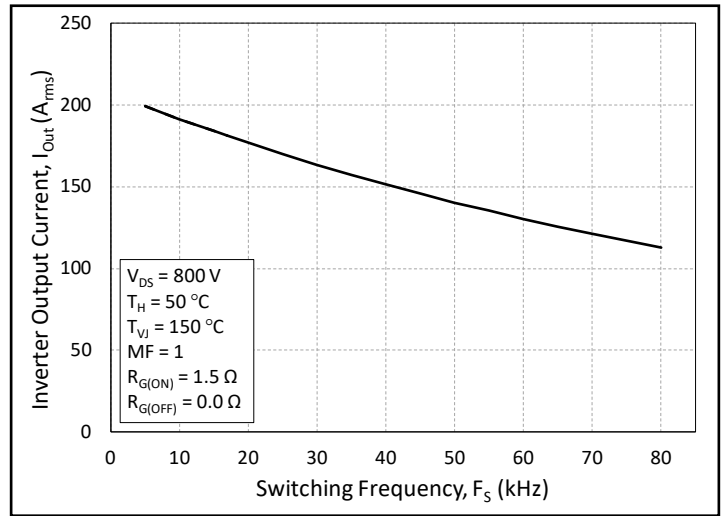


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

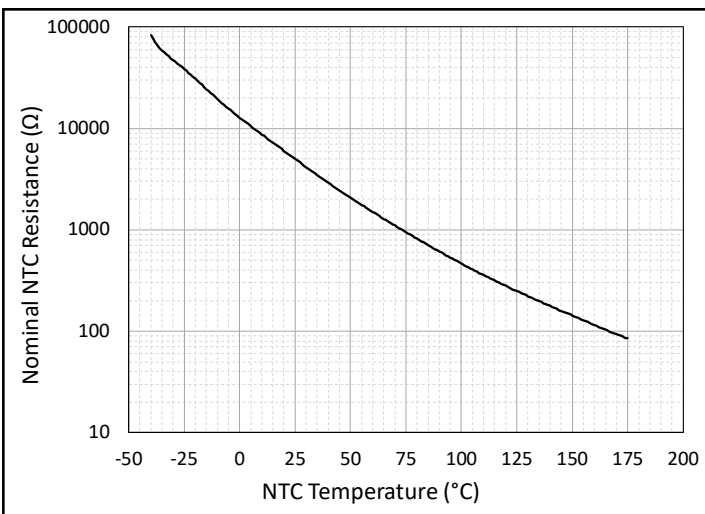


Figure 23. Nominal NTC Resistance vs. NTC Temperature



Timing Characteristics

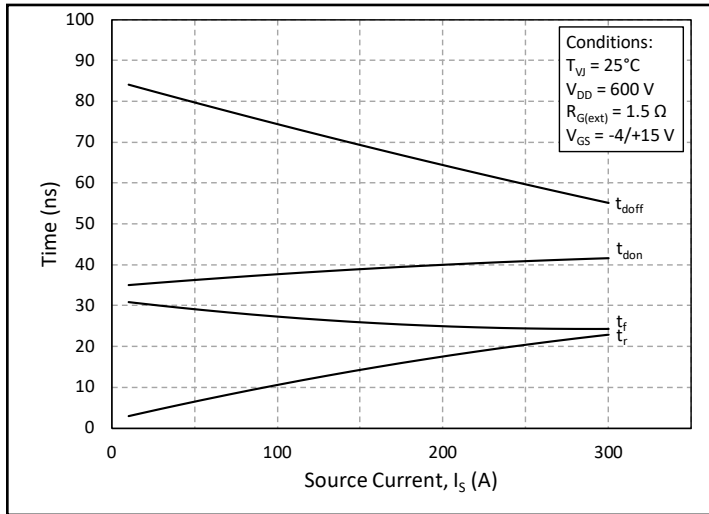


Figure 24. Timing vs. Source Current

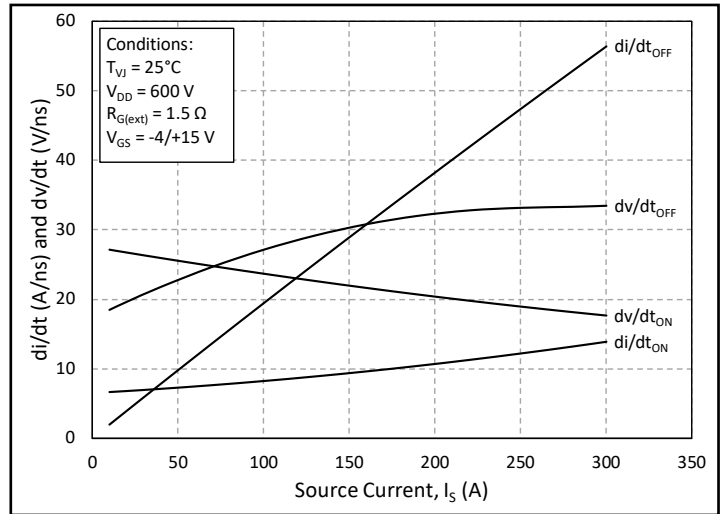


Figure 25. dv/dt and di/dt vs. Source Current

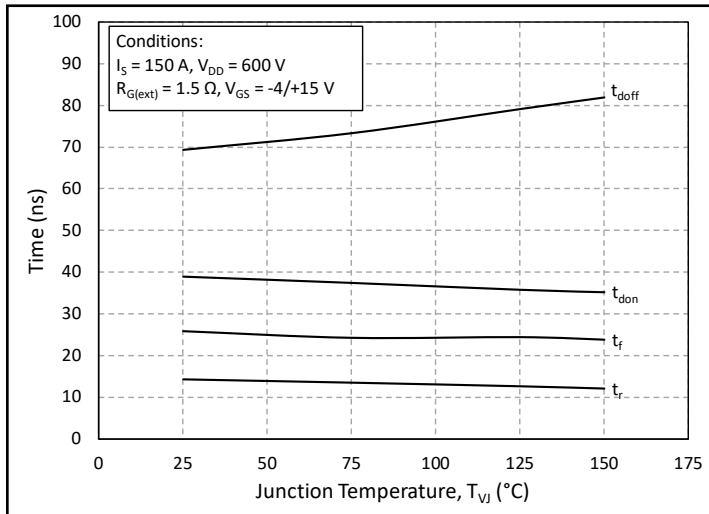


Figure 26. Timing vs. Junction Temperature

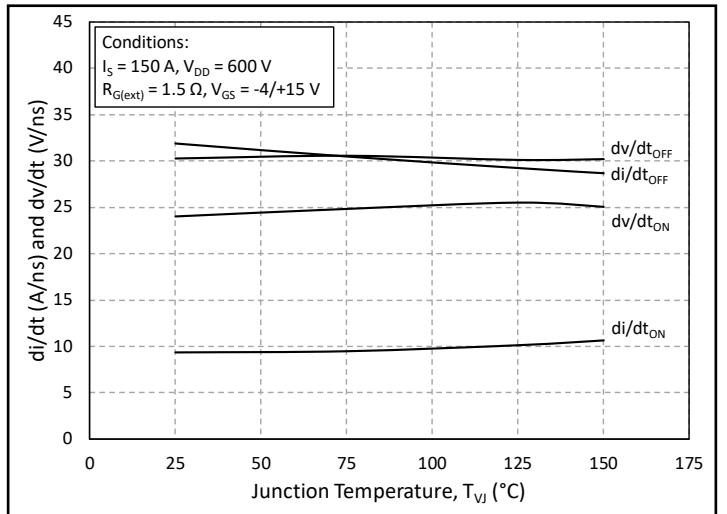


Figure 27. dv/dt and di/dt vs. Junction Temperature

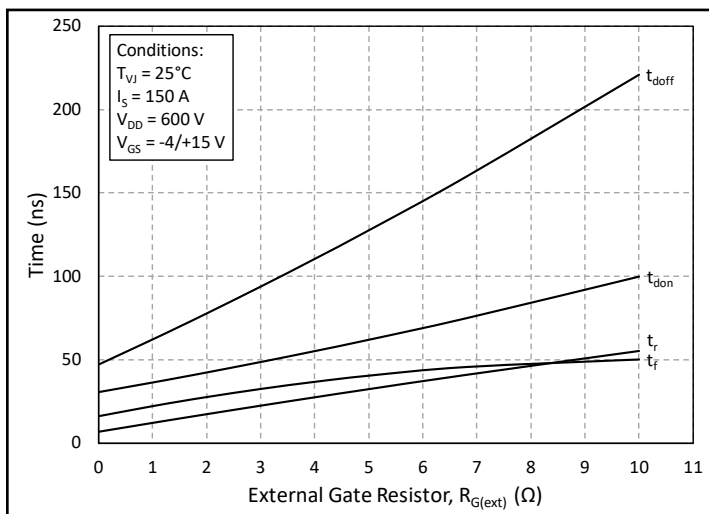


Figure 28. Timing vs. External Gate Resistance

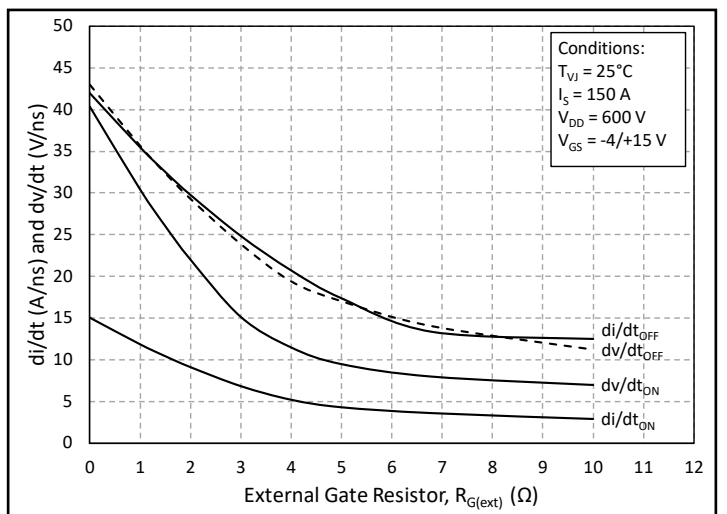


Figure 29. dv/dt and di/dt vs. External Gate Resistance



Definitions

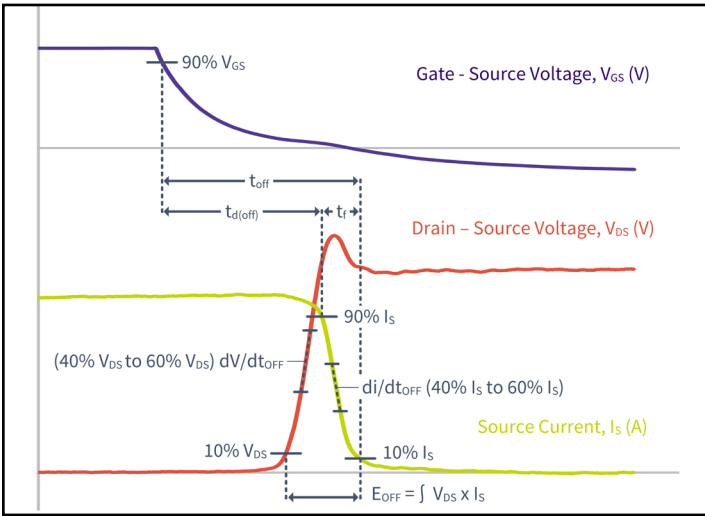


Figure 30. Turn-off Transient Definitions

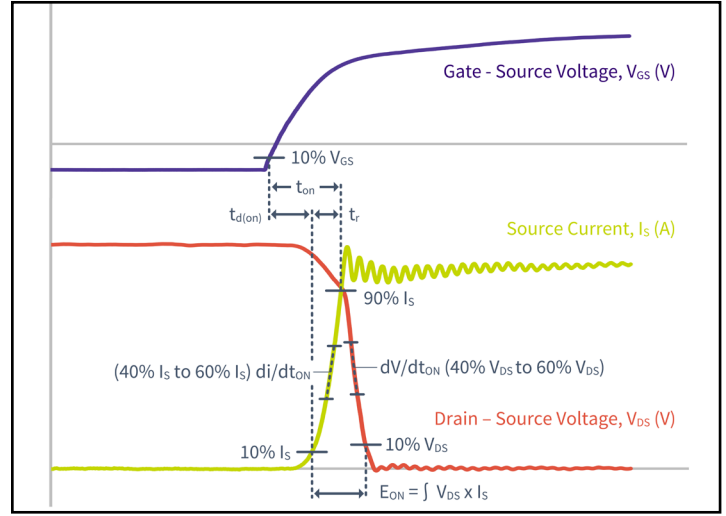


Figure 31. Turn-on Transient Definitions

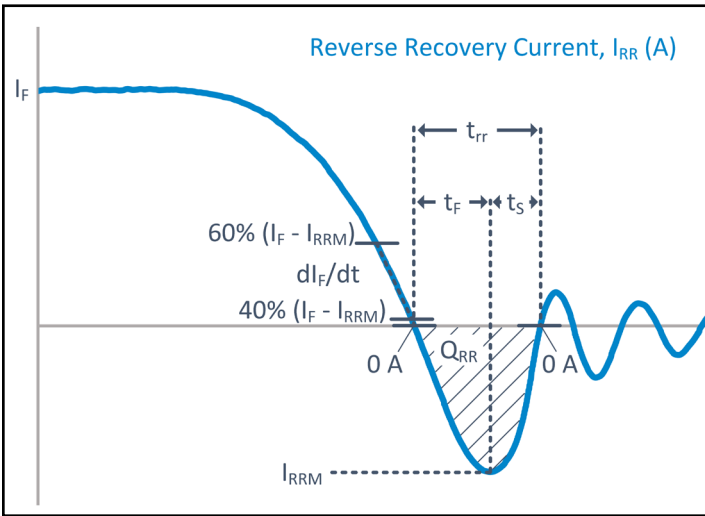


Figure 32. Reverse Recovery Definitions

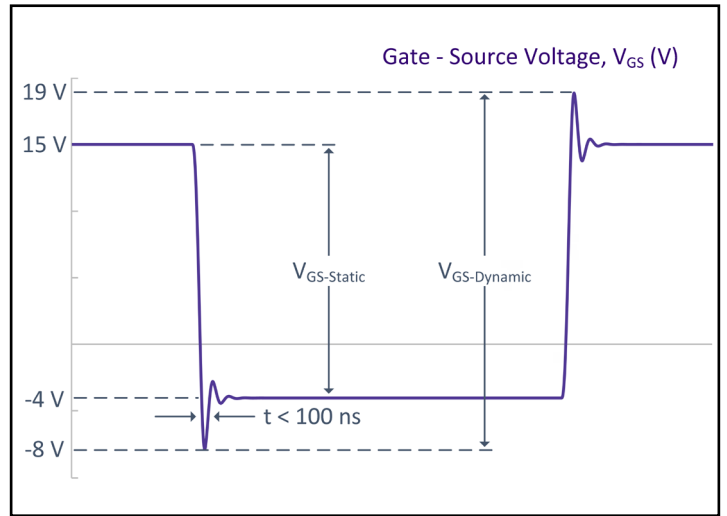
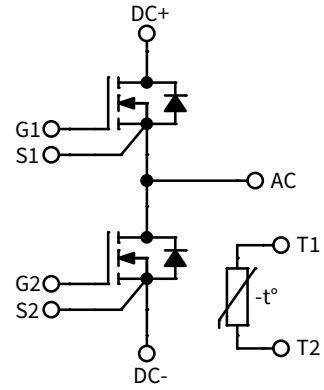
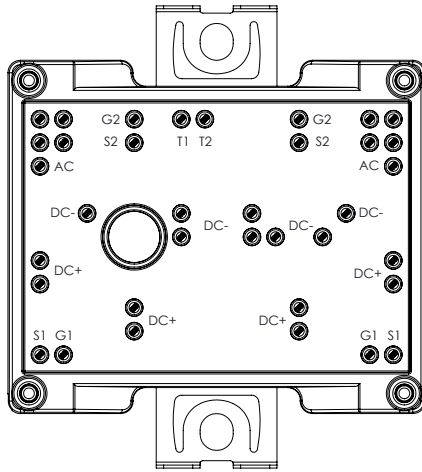


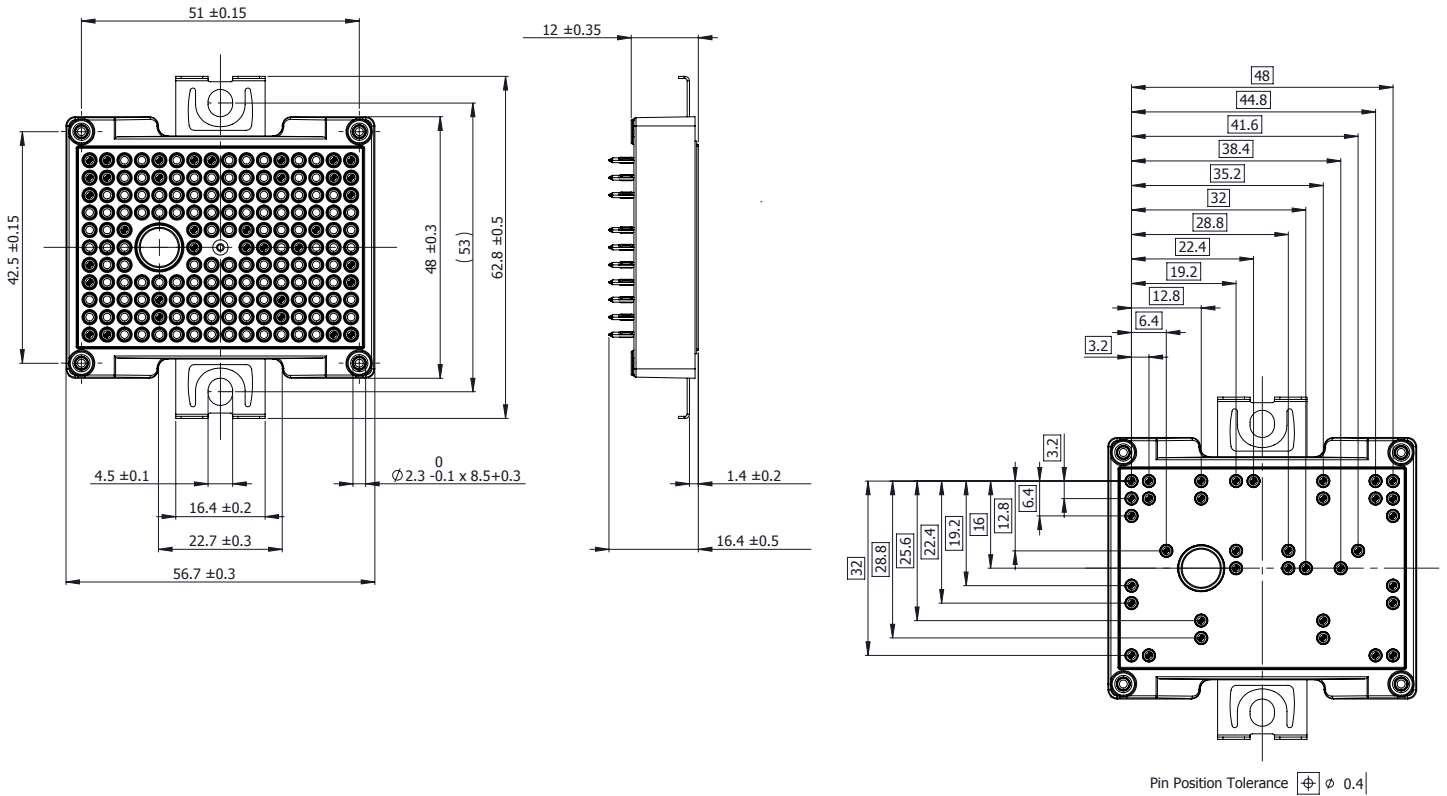
Figure 33. V_{GS} Transient Definitions



Schematic and Pin Out



Package Dimension (mm)



Supporting Links & Tools

Evaluation Tools

- [KIT-CRD-CIL12N-GMA: Dynamic Evaluation Board for Half-Bridge GM3 Modules](#)
- [CAB008M12GM3 PLECS Model](#)
- [SpeedFit 2.0 Design Simulator™](#)

Dual-Channel Companion Gate Driver Boards

- [EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board](#)
- [Si823H-AxWA-KIT: Skyworks® Gate Driver Board](#)
- [CGD1700HB2M-UNA: Wolfspeed Gate Driver Board](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

Application Notes

- [CPWR-AN41: Mounting Instructions and PCB Requirements](#)
- [CPWR-AN42: Thermal Interface Material Application Note](#)
- [CPWR-AN45: Dynamic Performance Application Note](#)

Notes

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