1 TO 4 CLOCK BUFFER

ICS551

Description

The ICS551 is a low cost, high-speed single input to four output clock buffer. Part of IDT's ClockBlocks™ family, this is our lowest cost, small clock buffer.

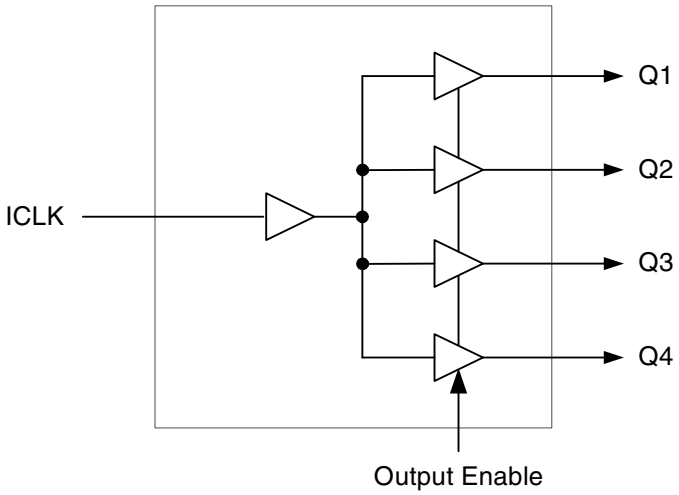
See the ICS552-02B for monolithic dual version of the ICS551 in a 20 pin QSOP.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact IDT for all of your clocking needs.

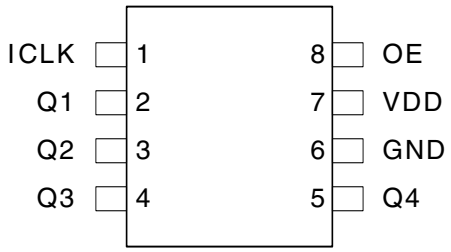
Features

- Low skew (250 ps) outputs
- Pb-free packaging
- Low cost clock buffer
- Packaged in 8-pin SOIC
- Input/Output clock frequency up to 160 MHz
- Non-inverting output clock
- Ideal for networking clocks
- Operating Voltages of 3.3 and 5.0 V
- Output Enable mode tri-states outputs
- Advanced, low power CMOS process
- Commercial and industrial temperature versions

Block Diagram



Pin Assignment



8 Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock input. Internal pull-up resistor.
2	Q1	Output	Clock output 1.
3	Q2	Output	Clock output 2.
4	Q3	Output	Clock output 3.
5	Q4	Output	Clock output 4.
6	GND	Power	Connect to ground.
7	VDD	Power	Connect to 3.3 V or 5.0 V.
8	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS551. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Commercial	0 to +70° C
Ambient Operating Temperature, Industrial	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40	–	+85	° C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=3.3 V ±10% , Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage, ICLK	V_{IH}	Note 1	VDD/2+0.7		3.8	V
Input Low Voltage, ICLK	V_{IL}	Note 1			VDD/2-0.7	V
Input High Voltage, OE	V_{IH}		2		VDD	V
Input Low Voltage, OE	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 135 MHz		18		mA
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PU}	OE		500		kΩ
Input Capacitance	C_{IN}	OE pin		5		pF
Short Circuit Current	I_{OS}			±50		mA

VDD = 5 V ±10% , Ambient temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.5		5.5	V
Input High Voltage, ICLK	V_{IH}	Note 1	VDD/2+1		5.5	V
Input Low Voltage, ICLK	V_{IL}	Note 1			VDD/2-1	V
Input High Voltage, OE	V_{IH}		2		VDD	V
Input Low Voltage, OE	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -35 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 35 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 135 MHz		35		mA
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PU}	OE		220		kΩ
Input Capacitance	C_{IN}	OE pin		5		pF
Short Circuit Current	I_{OS}			±80		mA

Notes: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

VDD = 3.3 V ±10%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		160	MHz
Output Frequency		15 pF load, Note 4			160	MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V			1.0	ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V			1.0	ns
Propagation Delay	Note 1	135 MHz	2	4	8	ns
Output to Output Skew	Note 2	Rising edges at VDD/2			250	ps

VDD = 5 V ±10%, Ambient Temperature -40 to +85 °C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		135	MHz
Output Frequency		15 pF load, Note 4			135	MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V			1.0	ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V			1.0	ns
Propagation Delay	Note 1	135 MHz	1.5	3	6	ns
Output to Output Skew	Note 2	Rising edges at VDD/2			250	ps

Notes:

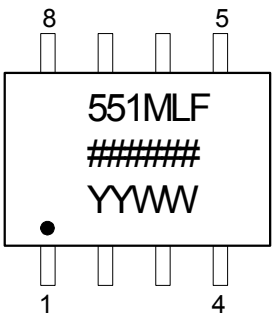
1. With rail to rail input clock.

2. Between any 2 outputs with equal loading.

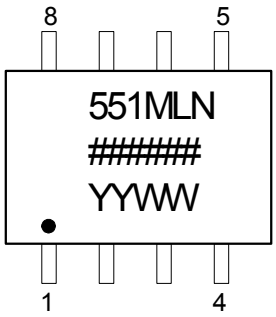
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

4. With external series resistor of 33Ω positioned close to each output pin.

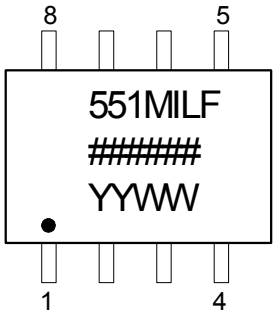
Marking Diagram (ICS551MLF)



Marking Diagram (ICS551MLN)



Marking Diagram (ICS551MILF)



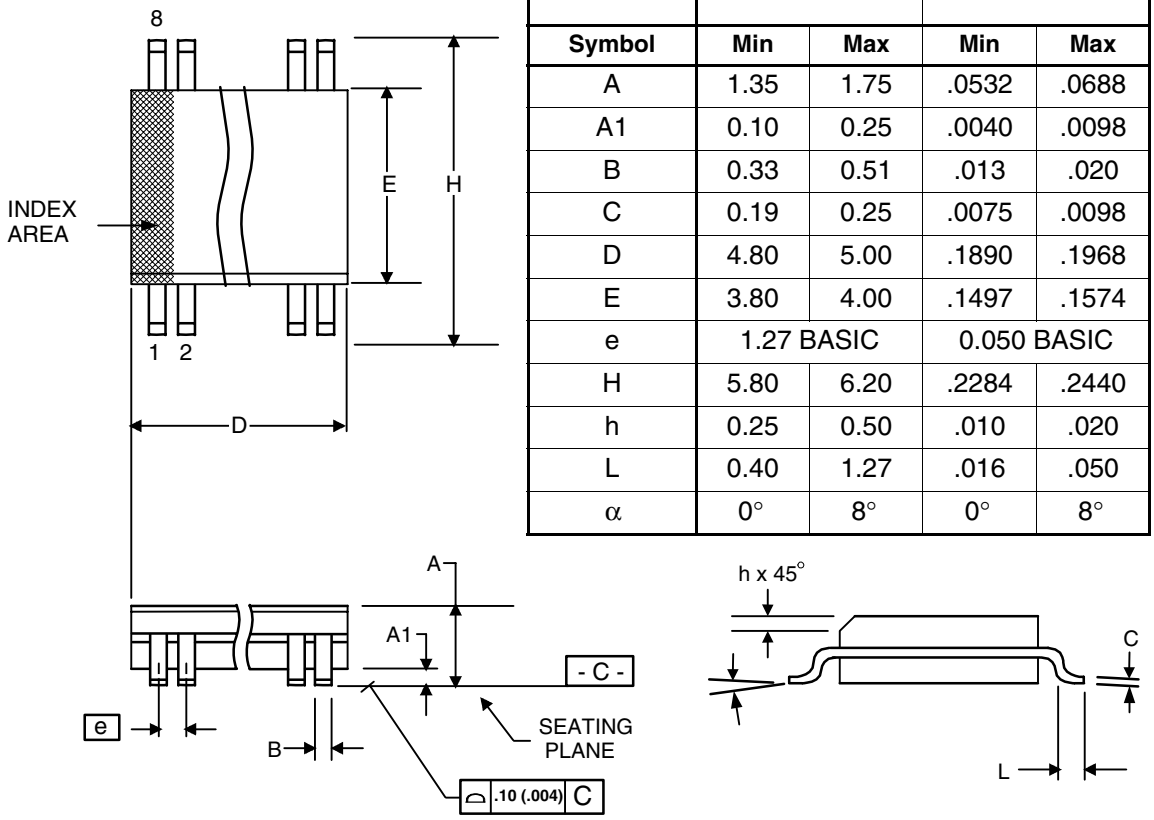
Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “LF” denotes Pb (lead) free package.
4. Bottom marking: (origin)

Origin = country of origin if not USA.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
551MLF	551MLF	Tubes	8-pin SOIC	0 to +70 °C
551MLFT	551MLF	Tape and Reel	8-pin SOIC	0 to +70 °C
551MLN	551MLN	Tubes	8-pin SOIC	0 to +70 °C
551MLNT	551MLN	Tape and Reel	8-pin SOIC	0 to +70 °C
551MILF	551MILF	Tubes	8-pin SOIC	-40 to +85 °C
551MILFT	551MILF	Tape and Reel	8-pin SOIC	-40 to +85 °C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“LN” denotes parts that are Pb free and annealed.

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