ISL8274M

30A/30A Dual-Channel Digital PMBus Step-Down Power Module

FN8931
Rev.1.00
Jan 4, 2018

The ISL8274M is a complete PMBus enabled DC/DC, dual-channel, step-down advance power supply, capable of delivering up to 30A per channel and optimized for high power density applications.

Operating across an input voltage range of 4.5V to 14V, the ISL8274M offers adjustable output voltages down to 0.6V and achieves up to 95.5% conversion efficiencies. A unique ChargeMode™ control architecture provides a single clock cycle response to an output load step and can support switching frequencies up to 1.06MHz. The power module integrates all power and most passive components and requires only a few external components to operate. A set of optional external resistors allows the user to easily configure the device for standard operation. For advanced configurations, a standard PMBus interface addresses tasks such as sequencing and fault management, as well as real-time full telemetry and point-of-load monitoring. Additionally, the nonvolatile memory can store the desired custom configuration and settings.

A fully customizable voltage, current, and temperature protection scheme ensures safe operation for the ISL8274M under abnormal operating conditions. The device is also supported by the PowerNavigator™ software, a full digital power train development environment.

The ISL8274M is available in a low profile, compact 18mm x 23mm x 7.5mm fully encapsulated, thermally enhanced HDA package.

Applications

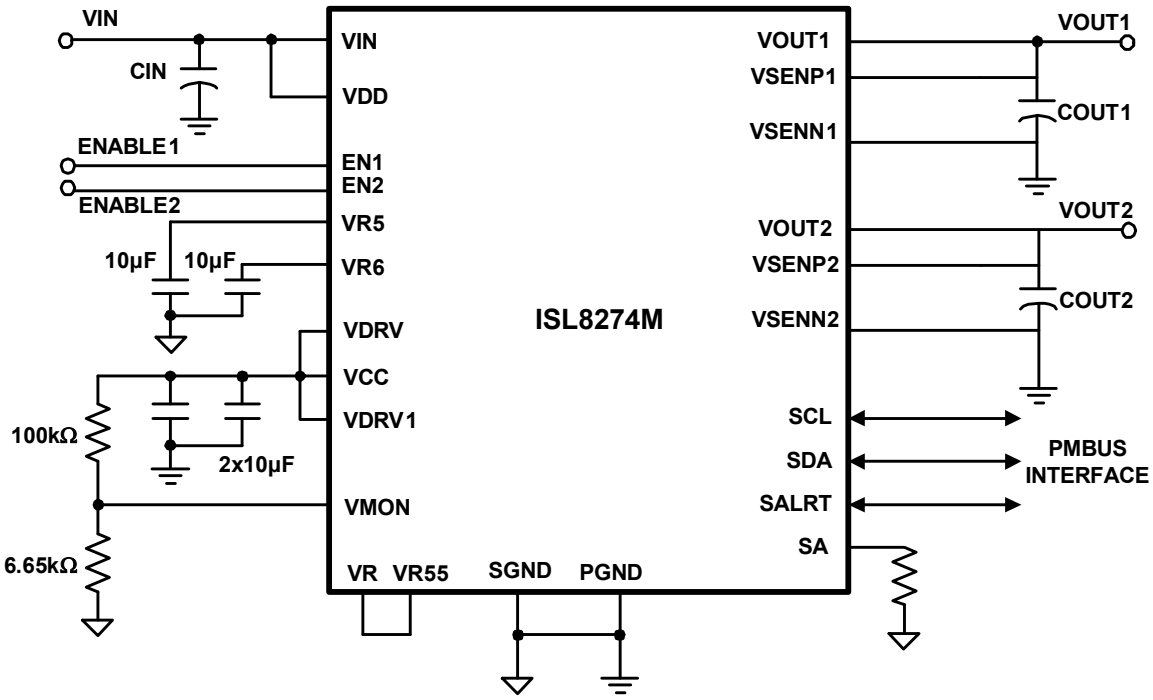
- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

Features

- Complete digital power supply
- 30A/30A dual-channel output current
  - 4.5V to 14V single rail input voltage
  - Up to 95.5% efficiency
- Programmable output voltage
  - 0.6V to 5V output voltage settings
  - ±1.2% accuracy over line/load/temperature
- ChargeMode control loop architecture
  - 296kHz to 1.06MHz fixed switching frequency operations
  - No compensation required
  - Fast single clock cycle transient response
- PMBus interface and/or pin-strap mode
  - Fully programmable through PMBus
  - Pin-strap mode for standard settings
  - Real-time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, and f_{SW}
- Advanced soft-start/stop, sequencing, and tracking
- Internal nonvolatile memory
- Complete over/undervoltage, current, and temperature protections with fault logging
- PowerNavigator supported
- Thermally enhanced 18mm x 23mm x 7.5mm HDA package

Related Literature

- For a full list of related documents, visit our website
  - ISL8274M product page



Note: This figure represents a typical implementation of the ISL8274M. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.

Figure 1. Application Circuit

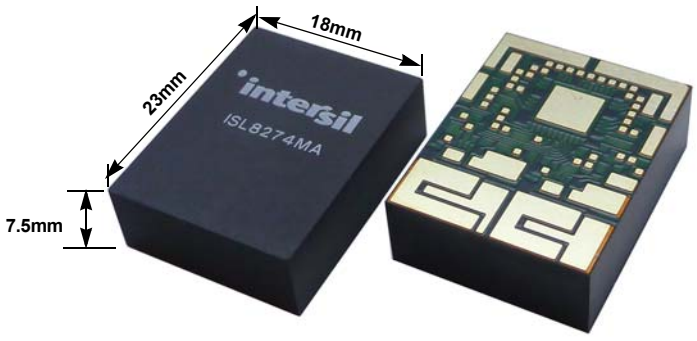
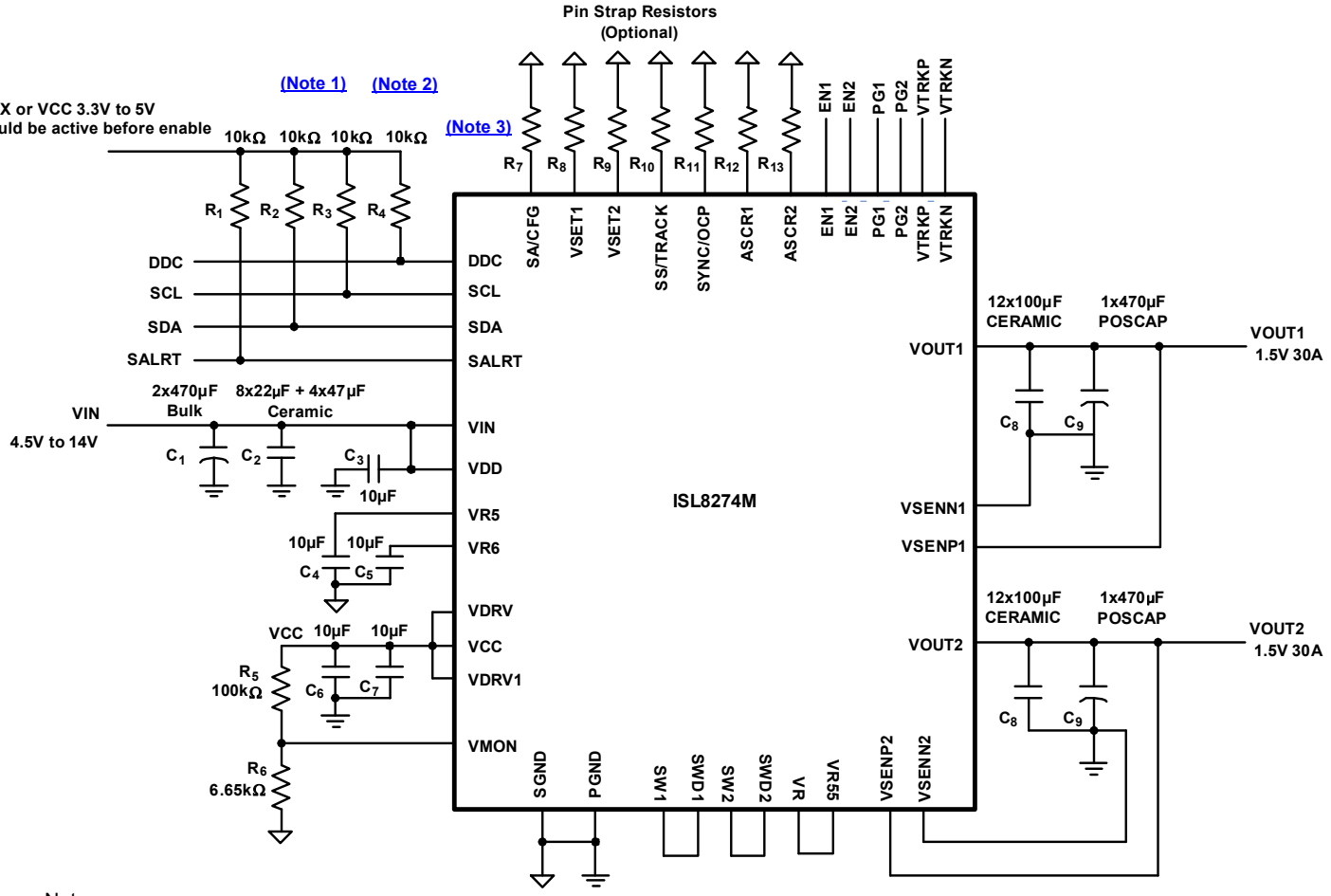


Figure 2. Small Package for High Power Density

Contents

1. Overview

1.1 Typical Application Circuits



Notes:

1. R_2 and R_3 are not required if the PMBus host already has I^2C pull-up resistors.
2. Only one R_4 per DDC bus is required when multiple modules share the same DDC bus.
3. R_7 through R_{13} can be selected according to the tables for the pin-strap resistor setting in this document. If the PMBus configuration is chosen to overwrite the pin-strap configuration, R_8 through R_{13} can be non-populated.
4. V25, VR, and VR55 do not need external capacitors. V25 can be no connection.

Figure 3. ISL8274M Digital PMBus Module Dual 30A/30A Application with Pinstrap Settings

1.2 ISL8274M Internal Block Diagram

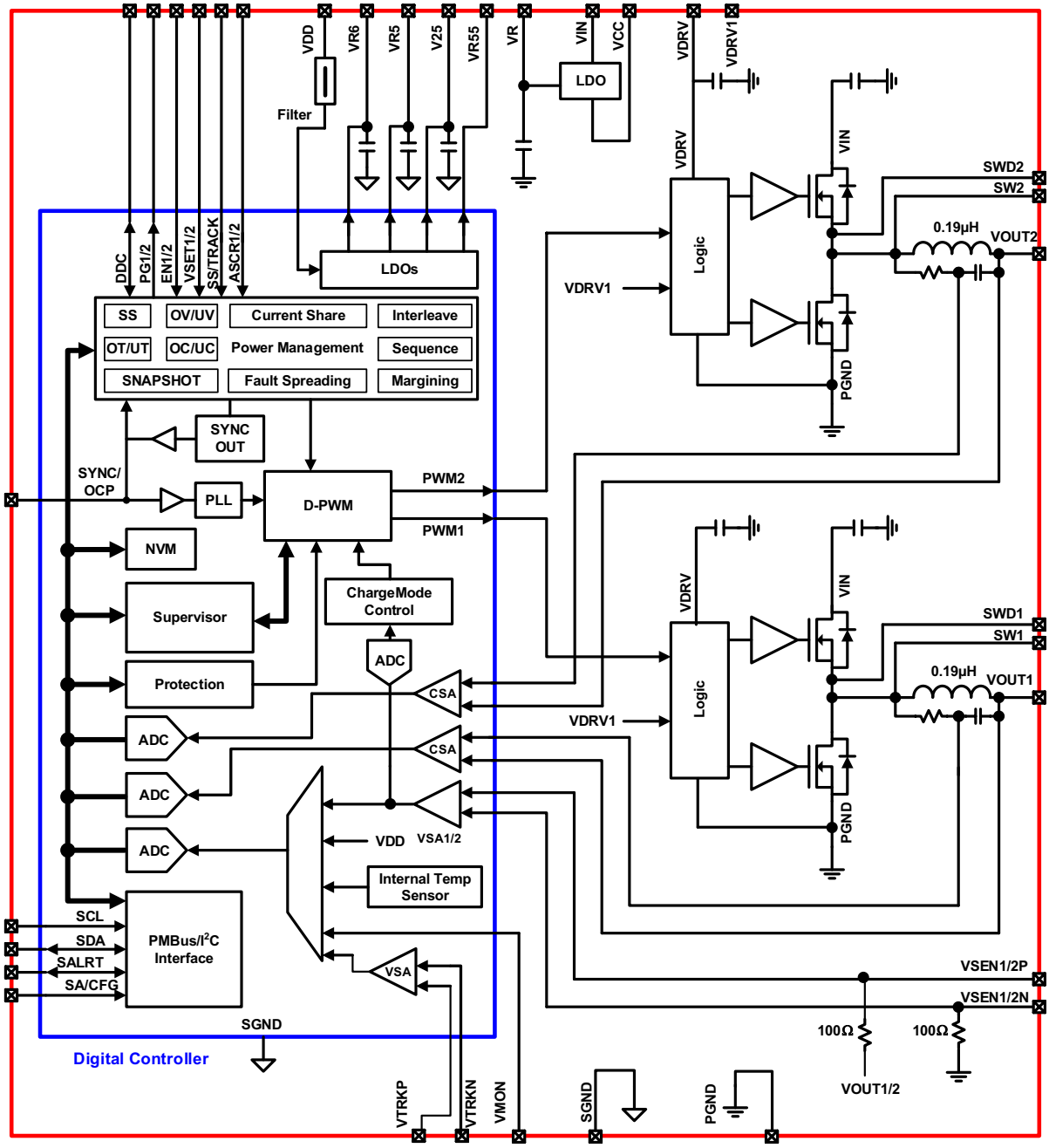


Figure 4. Internal Block Diagram

1.3 Ordering Information

Part Number (Notes 5, 6, 7)	Part Marking	Temp Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL8274MAIRZ	ISL8274MA	-40 to +85	58 LD 18x23 HDA Module	Y58.18x23
ISL8274MEVAL1Z	Evaluation Board			

Notes:

5. Add “-T” suffix for 100 unit tape and reel option. Refer to TB347 for details on reel specifications.
6. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
7. For Moisture Sensitivity Level (MSL), see the product information page for the ISL8274M. For more information on MSL, see TB363.

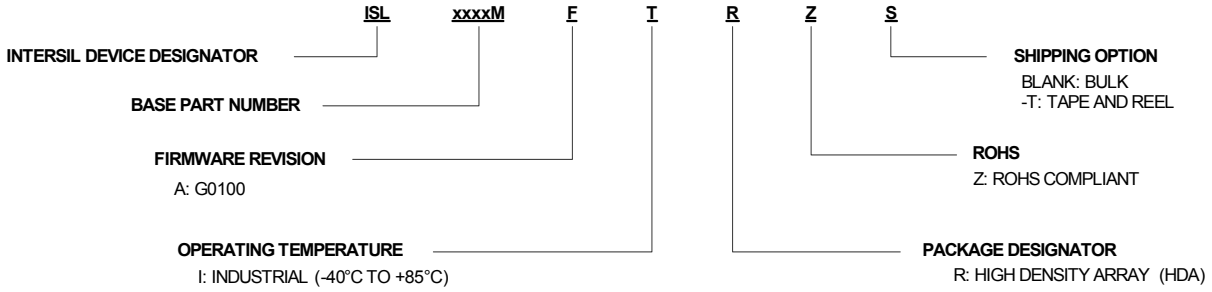
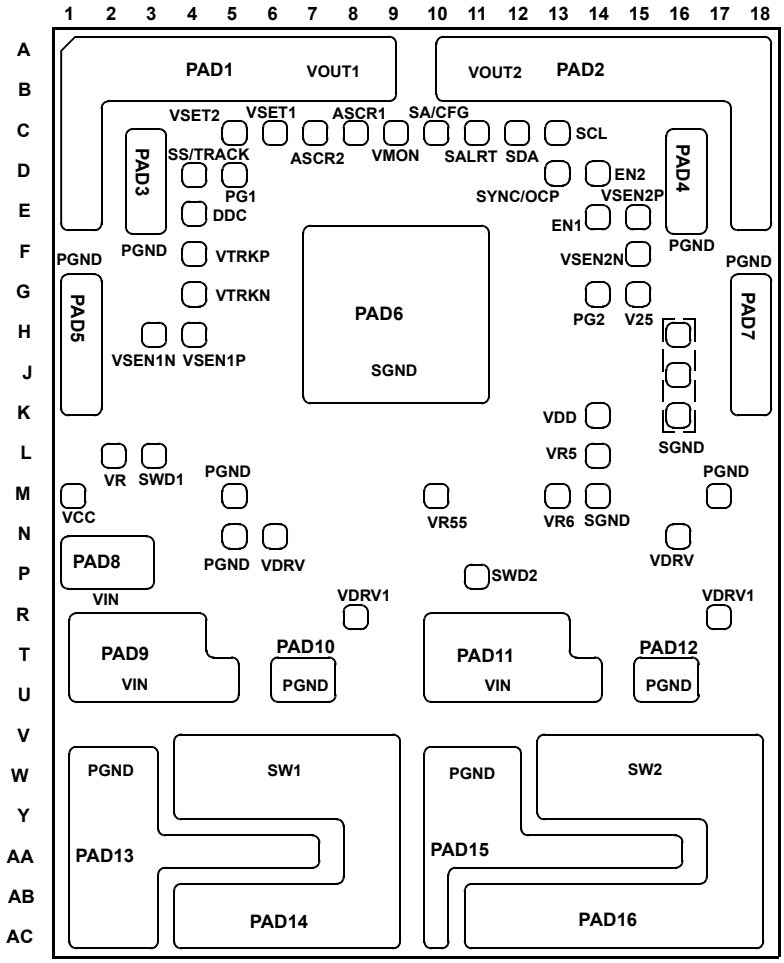


Table 1. Key Differences Between Family of Parts

Part	Description	V_{IN} Range (V)	V_{OUT} Range (V)	I_{OUT} (A)
ISL8274M	Digital DC/DC PMBus Dual Channel 30A/30A Module	4.5 - 14	0.6 - 5.0	30/30
ISL8272M	Digital DC/DC PMBus Single Channel 50A Module	4.5 - 14	0.6 - 5.0	50
ISL8273M	Digital DC/DC PMBus Single Channel 80A Module	4.5 - 14	0.6 - 2.5	80
ZL9024M	Digital DC/DC PMBus Single Channel 33A Module	2.75-4	0.6 - 1.5	33

1.4 Pin Configuration

ISL8274M
(58 Ld HDA)
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Type	Description
PAD1	VOUT1	PWR	Power supply output voltage. Channel 1 provides an output voltage from 0.6V to 5V. Refer to the "Functional Description" on page 21 to set the maximum output current from these pads.
PAD2	VOUT2	PWR	Power supply output voltage. Channel 2 provides an output voltage from 0.6V to 5V. Refer to the "Functional Description" on page 21 to set the maximum output current from these pads.
PAD3, PAD4, PAD5, PAD7, PAD10, PAD12, PAD13, PAD15	PGND	PWR	Power ground. Refer to the "Layout Guide" on page 33 for the PGND pad connections and I/O capacitor placement.
PAD6	SGND	PWR	Signal ground. Refer to "Layout Guide" on page 33 for the SGND pad connections.
PAD8, PAD9, PAD11	VIN	PWR	Input power supply voltage to power the module. Input voltage ranges from 4.5V to 14V.
PAD14	SW1	PWR	Switching node pads for Channel 1. The SW1 pad is used to dissipate the heat and provide the good thermal performance. Refer to "Layout Guide" on page 33 for the SW1 pad connections.
PAD16	SW2	PWR	Switching node pads for Channel 2. The SW2 pad is used to dissipate the heat and provide the good thermal performance. Refer to "Layout Guide" on page 33 for the SW2 pad connections.
C5	VSET2	I	Output voltage selection pin for Channel 2. Used to set VOUT2 set point and VOUT2 max.
C6	VSET1	I	Output voltage selection pin for Channel 1. Used to set VOUT1 set point and VOUT1 max.
C7	ASCR2	I	ChargeMode control ASCR parameters selection pin for Channel 2. Used to set ASCR gain and residual values.
C8	ASCR1	I	ChargeMode control ASCR parameters selection pin for Channel 1. Used to set ASCR gain and residual values.
C9	VMON	I	Driver voltage monitoring. Use this pin to monitor VDRV through an external 16:1 resistor divider.
C10	SA/CFG	I	Serial address selection pin. Used to assign unique address for each individual device or to enable certain management features. This pin also sets the UVLO level.
C11	SALRT	O	Serial alert. Connect to external host if desired. SALRT is asserted low upon a warning or a fault event and deasserted when warning or fault is cleared. A pull-up resistor is required.
C12	SDA	I/O	Serial data. Connect to external host and/or to other Digital-DC™ devices. A pull-up resistor is required.
C13	SCL	I/O	Serial clock. Connect to external host and/or to other Digital-DC devices. A pull-up resistor is required.
D4	SS/ TRACK	I	Soft-start/stop selection pin. Used to set turn on/off delay and ramp time as well as tracking configuration.
D5	PG1	O	Power-good output for Channel 1. Power-good output can be an open drain that requires a pull-up resistor or push-pull output that can drive a logic input.
D13	SYNC/ OCP	I/O	Clock synchronization input and OCP setting pin. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock. If external synchronization is used, the external clock must be active before enable. Different OCP level can be set with this pin.
D14	EN2	I	Enable pin for Channel 2. Logic high to enable the module output.
E14	EN1	I	Enable pin for Channel 1. Logic high to enable the module output.
E4	DDC	I/O	A Digital-DC bus. This dedicated bus provides the communication between devices for features such as sequencing, fault spreading and current sharing. The DDC pin on all Digital-DC devices should be connected together. A pull-up resistor is required.
E15	VSEN2P	I	Differential output voltage sense feedback for Channel 2. Connect to positive output regulation point.
F4	VTRKP	I	Tracking sense positive input. Used to track an external voltage source.
F15	VSEN2N	I	Differential output voltage sense feedback for Channel 2. Connect to negative output regulation point.

Pin Number	Pin Name	Type	Description
G4	VTRKN	I	Tracking sense negative input (return).
G14	PG2	O	Power-good output for Channel 2. Power-good output can be an open drain that requires a pull-up resistor or push-pull output that can drive a logic input.
G15	V25	PWR	Internal 2.5V reference used to power internal circuitry. No external capacitor required for this pin. Not recommended to power external circuits.
H3	VSEN1N	I	Differential output voltage sense feedback for Channel 1. Connect to a negative output regulation point.
H4	VSEN1P	I	Differential output voltage sense feedback for Channel 1. Connect to a positive output regulation point.
H16, J16, K16, M14	SGND	PWR	Signal grounds. Use multiple vias to connect the SGND pins to the internal SGND layer.
K14	VDD	PWR	Input supply voltage for controller. Connect VDD pad to VIN supply.
L2	VR	PWR	Internal LDO bias pin. Tie VR to VR55 directly with a short loop trace. Not recommended to power external circuits.
L3	SWD1	PWR	Switching node driving pins for Channel 1. Directly connect to the SW1 pad with short loop wires.
P11	SWD2	PWR	Switching node driving pins for Channel 2. Directly connect to the SW2 pad with short loop wires.
L14	VR5	PWR	Internal 5V reference used to power internal circuitry. Place a 10µF decoupling capacitor for this pin. Maximum external loading current is 5mA.
M1	VCC	PWR	Internal LDO output. Connect VCC to VDRV for internal LDO driving.
M5, M17, N5	PGND	PWR	Power grounds. Using multiple vias to connect the PGND pins to the internal PGND layer.
M10	VR55	PWR	Internal 5.5V bias voltage for internal LDO use only. Tie VR55 pin directly to the VR pin. Not recommended to power external circuit.
M13	VR6	PWR	Internal 6V reference used to power internal circuitry. Place a 10µF decoupling capacitor for this pin. Not recommended to power external circuit.
N6, N16	VDRV	PWR	Power supply for internal FET drivers. Connect a 10µF bypass capacitor to each of these pins. These pins can be driven by the internal LDO through VCC pin or by the external power supply directly. Keep the driving voltage between 4.5V and 5.5V. For 5V input application, use external supply or connect this pin to VIN.
R8, R17	VDRV1	I	Bias pin of the internal FET drivers. Always tie to VDRV.

Table 2. ISL8274M Design Guide Matrix and Output Voltage Response

V_{OUT} (V)	I_{OUT} (A)	Avg OCP (A)	COUT_Bulk (µF)	COUT_Ceramic (µF)	ASCR Gain	ASCR Residual	Peak-to-Peak (mV)	Frequency (kHz)
5	25	30	1*470	6*100	275	100	170	1067
5	20	25	1*470	6*100	175	80	150	615
3.3	25	30	1*470	8*100	300	90	150	800
3.3	20	25	1*470	8*100	175	80	140	571
2.5	30	35	1*470	9*100	600	100	110	1067
2.5	25	30	1*470	9*100	350	100	120	615
2.5	20	25	1*470	9*100	175	90	100	471
1.8	30	35	1*470	12*100	600	100	90	889
1.8	25	30	1*470	12*100	250	100	100	421
1.8	20	25	1*470	12*100	200	100	100	364
1.5	30	35	1*470	12*100	525	90	90	889
1.5	25	30	1*470	12*100	250	100	90	421

Table 2. ISL8274M Design Guide Matrix and Output Voltage Response (Continued)

V_{OUT} (V)	I_{OUT} (A)	Avg OCP (A)	COUT_Bulk (µF)	COUT_Ceramic (µF)	ASCR Gain	ASCR Residual	Peak-to-Peak (mV)	Frequency (kHz)
1.5	20	25	1*470	12*100	140	90	100	320
1.2	30	35	1*470	12*100	600	110	70	727
1.2	25	30	4*470	12*100	250	80	60	296
1	30	35	1*470	12*100	450	110	80	615
1	25	30	5*470	12*100	250	80	50	296
0.6	30	35	7*470	12*100	300	90	50	296

Notes:

8. 2x470µF (EEE-1EA471P) and 12x22µF (GRM32ER71E226KE15L) are used for all conditions in the evaluation board.
9. 100µF (GRM31CD80J107ME39L) ceramic and 470µF (6TPF470MAH) are selected for output capacitor in the evaluation board.
10. Peak-to-peak V_{OUT} deviation is measured under 50%-100% load transient while 12V input applied.
11. ASCR gain and residual was designed to achieve 50° phase margin over temperature. (Ambient temperature from -40°C to +85°C).
12. Frequency is selected to achieve the highest efficiency at full load as well as avoid saturation of the inductor. For instance, select 615kHz instead of 296kHz if 1V, 26A is required to avoid inductor saturation. Although better efficiency is obtained at 296kHz supporting 1V, 25A, higher frequency can be selected because less output capacitance is required to meet the transient response specification.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Supply Voltage, VIN Pin	-0.3	17	V
Input Supply Voltage for Controller, VDD Pin	-0.3	17	V
MOSFET Switch Node Voltage, SW1/2, SWD1/2 (Note 13)	-0.3	25	V
MOSFET Driver Supply Voltage, VDRV, VDRV1 Pin	-0.3	6.0	V
Output Voltage, VOUT1/2 Pin	-0.3	6.0	V
Internal Reference Supply Voltage			
VR6 Pin	-0.3	6.6	V
VR, VR5, VR55 Pin	-0.3	6.5	V
V25 Pin	-0.3	3	V
Logic I/O Voltage for DDC, EN1/2, PG1/2, ASCR1/2, SA/CFG, SCL, SDA, SALRT, SYNC/OCP, SS/TRACK, VMON, VSET1/2	-0.3	6.0	V
Analog Input Voltages			
VSEN1P, VSEN2P, VTRKP	-0.3	6.0	V
VSEN1N, VSEN2N, VTRKN	-0.3	0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

Note:
13. Do not apply DC voltage higher than 17V to the pins.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
58 Ld HDA Package (Notes 14, 15)	5.3	1.1

Notes:
14. θ_{JA} is defined by simulation in free air with the module mounted on an 8-layer evaluation board 4.7x4.8inch in size with 2oz Cu on all layers.
15. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+125	°C
Storage Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	see Figure 33		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Input Supply Voltage Range, V_{IN}	4.5	14	V
Input Supply Voltage Range for Controller, V_{DD}	4.5	14	V
Output Voltage Range, V_{OUT}	0.6	5	V
Output Current Range, $I_{OUT(DC)}$ Per Channel (Note 18)	0	30	A
Operating Junction Temperature Range, T_J	-40	+125	°C

2.4 Electrical Specifications

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

Parameter	Symbol	Test Conditions	Min (Note 16)	Typ	Max (Note 16)	Unit
Input and Supply Characteristics						
Input Supply Current for Controller	I_{DD}	V_{IN} = V_{DD} = 12V, V_{OUT} = 0V, module not enabled		40	**50**	mA
6V Internal Reference Supply Voltage	V_{R6}		**5.5**	6.1	**6.6**	V
5V Internal Reference Supply	V_{R5}	I_{VR5} < 5mA	**4.5**	5.2	**5.5**	V
2.5V Internal Reference Supply	V_{25}		**2.25**	2.5	**2.75**	V
Internal LDO Output Voltage	V_{CC}			5.3		V
Internal LDO Output Current	I_{VCC}	V_{IN} = V_{DD} = 12V, V_{CC} connected to VDRV, module enabled	**50**			mA
Input Supply Voltage for Controller Read Back Resolution	$V_{DD\_READ\_RES}$			±20		mV
Input Supply Voltage for Controller Read Back Total Error (Note 19)	$V_{DD\_READ\_ERR}$	PMBus Read		±2		% FS
Output Characteristics						
Output Voltage Adjustment Range	V_{OUT_RANGE}		**0.54**		**5.5**	V
Output Voltage Set-Point Resolution	V_{OUT_RES}	Configured using PMBus		±0.025		%V_{OUT}
Output Voltage Set-Point Accuracy (Notes 17, 19)	V_{OUT_ACCY}	Includes line, load, and temperature (-20°C ≤ T_A ≤ +85°C)	**-1.2**		**1.2**	%
Output Voltage Read Back Resolution	$V_{OUT\_READ\_RES}$			±0.15		% FS
Output Voltage Read Back Total Error (Note 19)	$V_{OUT\_READ\_ERR}$	PMBus read	**-2**		**2**	% FS
Output Ripple Voltage	V_{OUT_RIPPLE}	V_{OUT} = 1.5V, C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF ceramic		1		%
Output Current Read Back Resolution	$I_{OUT\_READ\_RES}$	ISENSE_CONFIG default setting		0.2		A
Output Current Range (Note 18)	I_{OUT_RANGE}	Per channel			**30**	A
Output Current Read Back Total Error	$I_{OUT\_READ\_ERR}$	PMBus read at max load V_{OUT} = 1.5V		±3		A
Soft-Start and Sequencing						
Delay Time from Enable to V_{OUT} Rise	t_{ON_DELAY}	Configured using PMBus	**2**		**300**	ms
t_{ON_DELAY} Accuracy	$t_{ON\_DELAY\_ACCY}$			±2		ms
Output Voltage Ramp-Up Time	t_{ON_RISE}	Configured using PMBus	**0.5**		**120**	ms
Output Voltage Ramp-Up Time Accuracy	$t_{ON\_RISE\_ACCY}$			±250		µs
Delay Time from Disable to V_{OUT} Fall	t_{OFF_DELAY}	Configured using PMBus	**2**		**300**	ms
t_{OFF_DELAY} Accuracy	$t_{OFF\_DELAY\_ACCY}$			±2		ms

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 16)	Typ	Max (Note 16)	Unit
Output Voltage Fall Time	t_{OFF_FALL}	Configured using PMBus	**0.5**		**120**	ms
Output Voltage Fall Time Accuracy	$t_{ON\_FALL\_ACCY}$			±250		µs
Power-Good						
Power-Good Delay	V_{PG_DELAY}	Configured using PMBus	**0**		**5000**	ms
Temperature Sense						
Temperature Sense Range	T_{SENSE_RANGE}	Configurable using PMBus	**-50**		**150**	°C
Internal Temperature Sensor Accuracy	INT_TEMP_{ACCY}	Tested at +100°C	-5		5	°C
Fault Protection						
V_{DD} Undervoltage Threshold Range	$V_{DD\_UVLO\_RANGE}$	Measured internally	**4.18**		**16**	V
V_{DD} Undervoltage Threshold Accuracy (Note 19)	$V_{DD\_UVLO\_ACCY}$			±2		%FS
V_{DD} Undervoltage Response Time	$V_{DD\_UVLO\_DELAY}$			10		µs
V_{OUT} Overvoltage Threshold Range	$V_{OUT\_OV\_RANGE}$	Factory default		$1.15V_{OUT}$		V
		Configured using PMBus	**$1.05V_{OUT}$**		**V_{OUT_MAX}**	V
V_{OUT} Undervoltage Threshold Range	$V_{OUT\_UV\_RANGE}$	Factory default		$0.85V_{OUT}$		V
		Configured using PMBus	**0**		**$0.95V_{OUT}$**	V
V_{OUT} OV/UV Threshold Accuracy (Note 17)	V_{OUT_OV/UV_ACCY}		**-2**		**2**	%
V_{OUT} OV/UV Response Time	V_{OUT_OV/UV_DELAY}			10		µs
Output Current Limit Set-Point Accuracy (Note 19)	I_{LIMIT_ACCY}	Tested at IOUT_AVG_OC_FAULT_LIMIT = 35A		±10		% FS
Over-temperature Protection Threshold (Controller Junction Temperature)	$T_{JUNCTION}$	Factory default		115		°C
		Configured using PMBus	**-40**		**115**	°C
Thermal Protection Hysteresis	$T_{JUNCTION\_HYS}$			15		°C
Oscillator and Switching Characteristics						
Switching Frequency Range	f_{SW_RANGE}		**296**		**1067**	kHz
Switching Frequency Set-Point Accuracy	f_{SW_ACCY}		**-5**		**5**	%
Minimum Pulse Width Required from External SYNC Clock	EXT_SYNC_{PW}	Measured at 50% amplitude	**150**			ns
Drift Tolerance for External SYNC Clock	EXT_SYNC_{DRIFT}	External SYNC clock equal to 500kHz is not supported	**-10**		**10**	%

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 16)	Typ	Max (Note 16)	Unit
Logic Input/Output Characteristics						
Bias Current at the Logic Input Pins	I_{LOGIC_BIAS}	DDC, EN1/2, PG1/2, SA/CFG, SCL, SDA, ASCR1/2, SS/TRACK, SALRT, SYNC/OCP, V_{MON}, $V_{SET1/2}$	**-100**		**+100**	nA
Logic Input Low Threshold Voltage	$V_{LOGIC\_IN\_LOW}$				**0.8**	V
Logic Input High Threshold Voltage	$V_{LOGIC\_IN\_HIGH}$		**2.0**			V
Logic Output Low Threshold Voltage	$V_{LOGIC\_OUT\_LOW}$	2mA sinking			**0.5**	V
Logic Output High Threshold Voltage	$V_{LOGIC\_OUT\_HIGH}$	2mA sourcing	**2.25**			V
PMBus Interface Timing Characteristic						
PMBus Operating Frequency	f_{SMB}		**100**		**400**	kHz

Notes:

16. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design. Controller is independently tested before module assembly.
17. V_{OUT} measured at the termination of the VSEN1/2P and VSEN1/2N sense points.
18. The MAX load current is determined by the thermal "Derating Curves" on page 20.
19. "FS" stands for full scale of recommended maximum operation range.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF Ceramic. Typical values are used unless otherwise noted. The efficiency curves were measured on the evaluation board. For test conditions, refer to Table 2 on page 10.

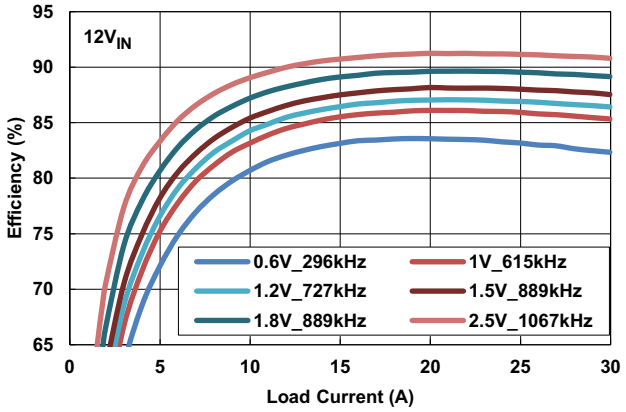


Figure 5. Single Channel Efficiency vs Output Current

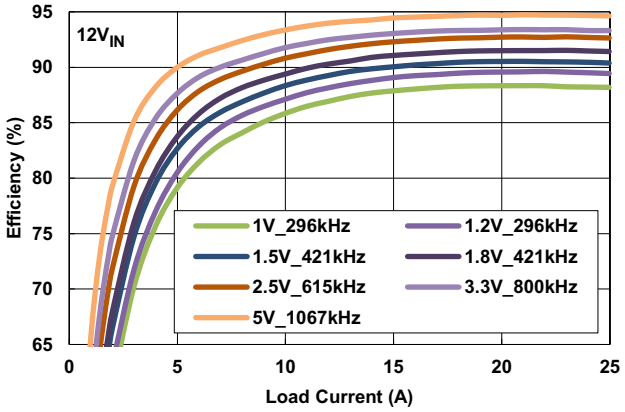


Figure 6. Single Channel Efficiency vs Output Current

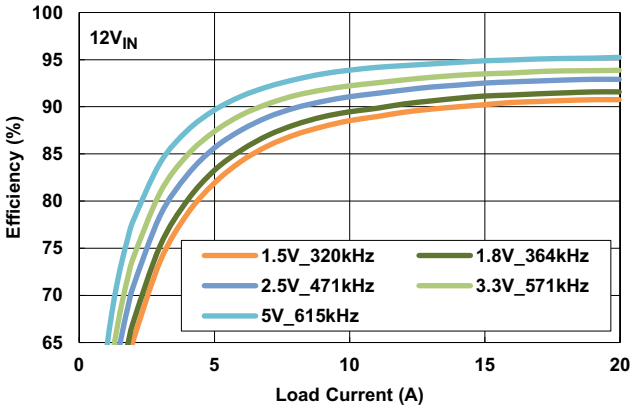


Figure 7. Single Channel Efficiency vs Output Current

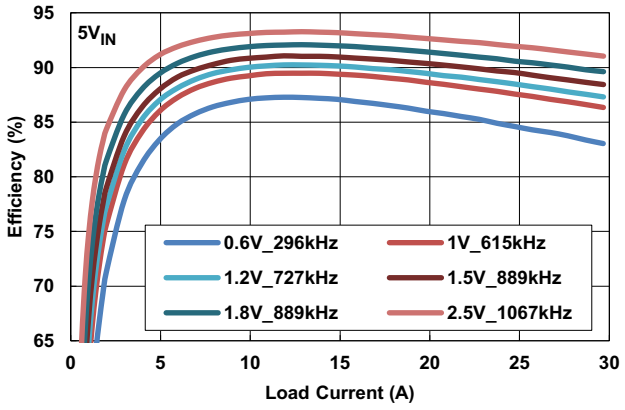


Figure 8. Single Channel Efficiency vs Output Current

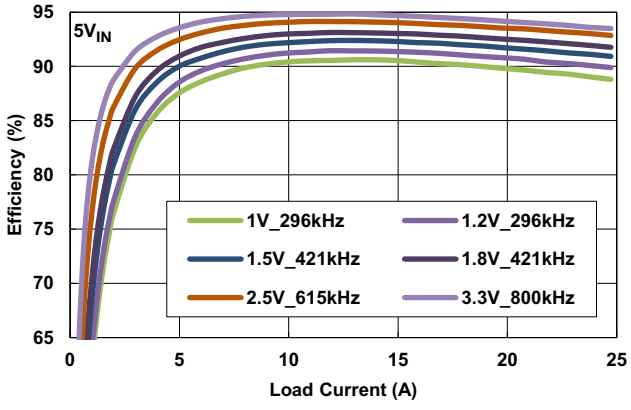


Figure 9. Single Channel Efficiency vs Output Current

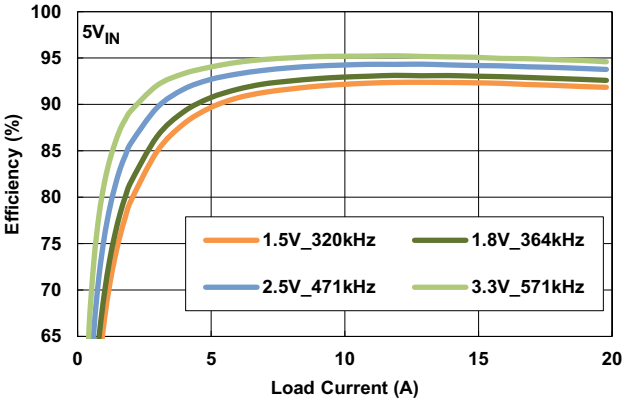


Figure 10. Single Channel Efficiency vs Output Current

3.2 Startup and Shutdown

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF Ceramic. Typical values are used unless otherwise noted.

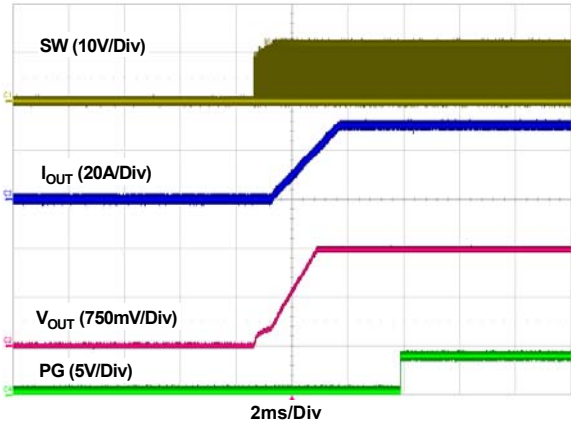


Figure 11. Single Channel Startup $12V_{IN}$, $1.5V_{OUT}$, 30A

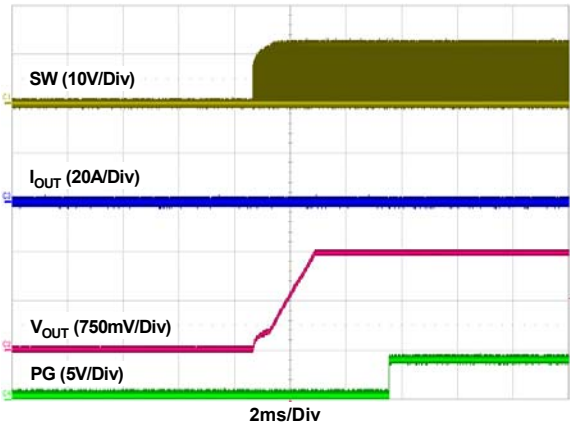


Figure 12. Single Channel Startup $12V_{IN}$, $1.5V_{OUT}$, 0A

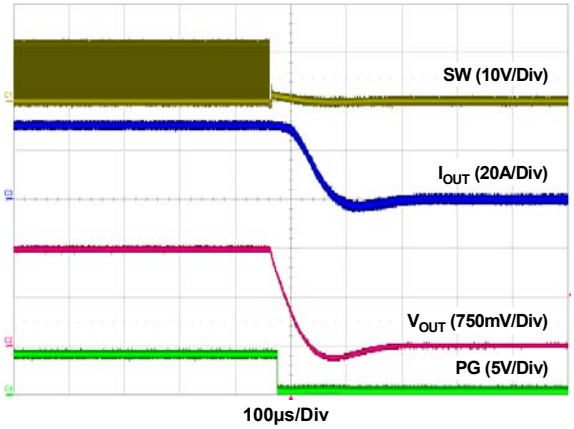


Figure 13. Single Channel Shutdown $12V_{IN}$, $1.5V_{OUT}$, 30A

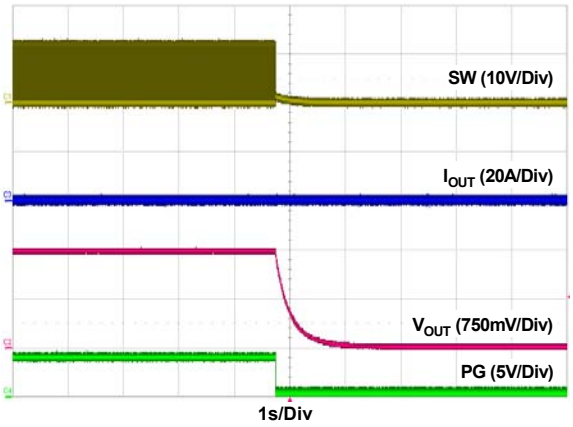


Figure 14. Single Channel Shutdown $12V_{IN}$, $1.5V_{OUT}$, 0A

3.3 Derating Curves

All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For test conditions, refer to Table 2 on page 10. Load current is applied per channel, two channels are operating at the same time.

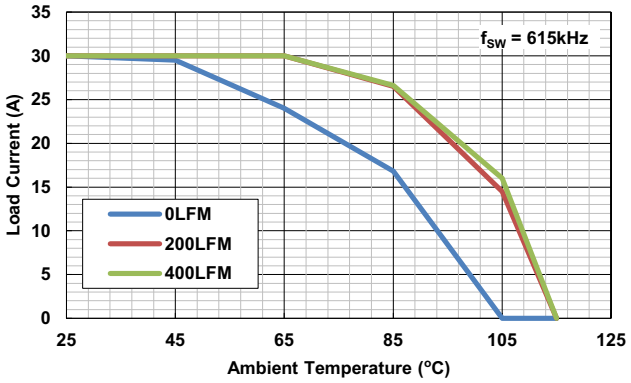


Figure 15. $12V_{IN}$ to $1V_{OUT}$

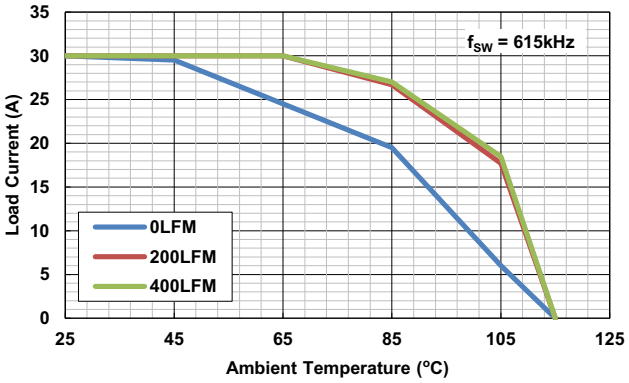


Figure 16. $5V_{IN}$ to $1V_{OUT}$

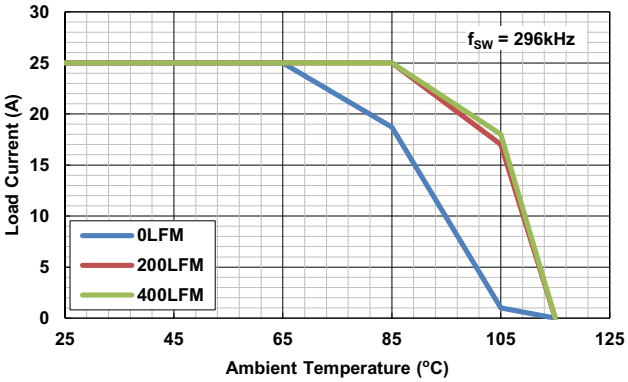


Figure 17. $12V_{IN}$ to $1V_{OUT}$

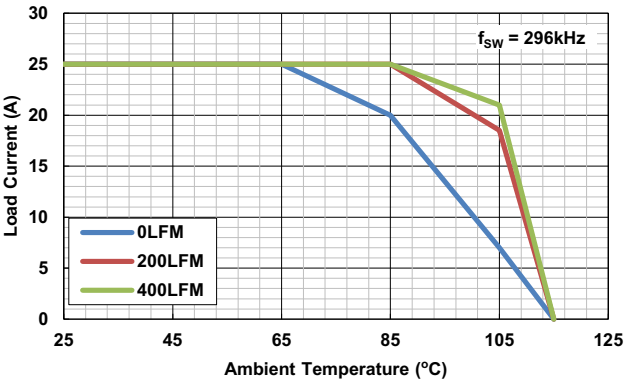


Figure 18. $5V_{IN}$ to $1V_{OUT}$

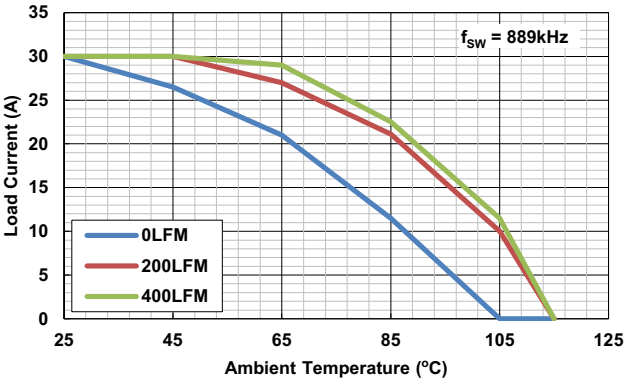


Figure 19. $12V_{IN}$ to $1.5V_{OUT}$

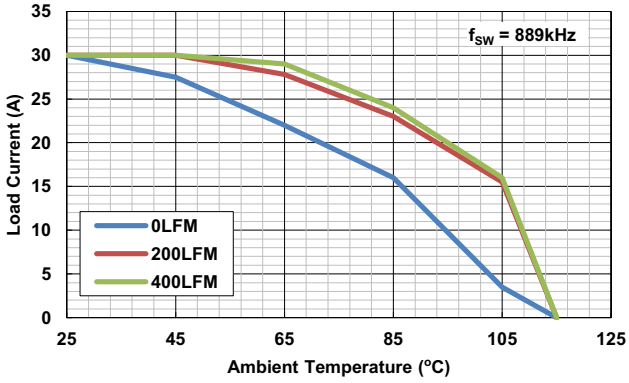


Figure 20. $5V_{IN}$ to $1.5V_{OUT}$

All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For test conditions, refer to Table 2 on page 10. Load current is applied per channel, two channels are operating at the same time. **(Continued)**

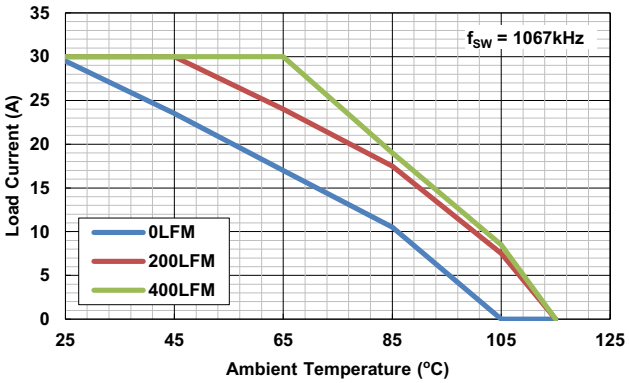


Figure 21. $12V_{IN}$ to $2.5V_{OUT}$

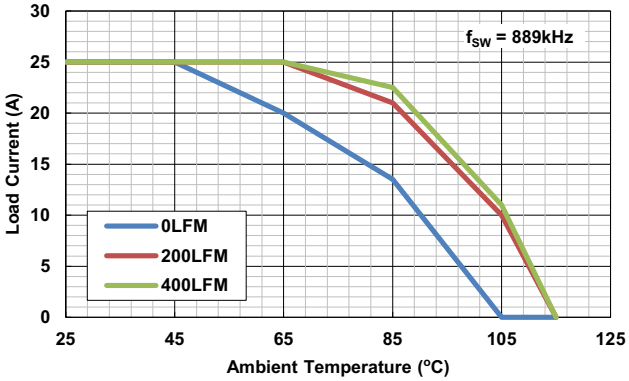


Figure 22. $5V_{IN}$ to $2.5V_{OUT}$

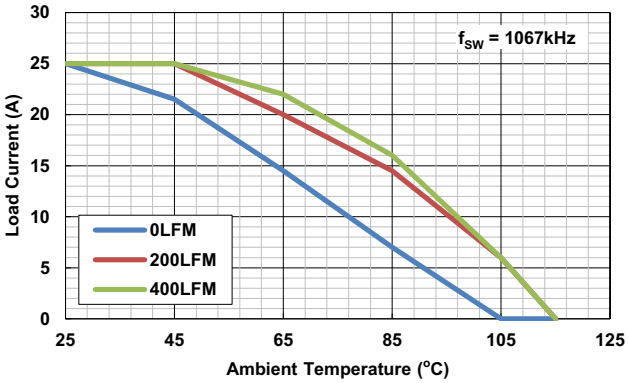


Figure 23. $12V_{IN}$ to $5V_{OUT}$

3.4 Transient Response Performance

Operating condition: T_A = +25°C, no air flow. Refer to Table 2 on page 10 for output capacitor and ASCR settings. Typical values are used unless otherwise noted.

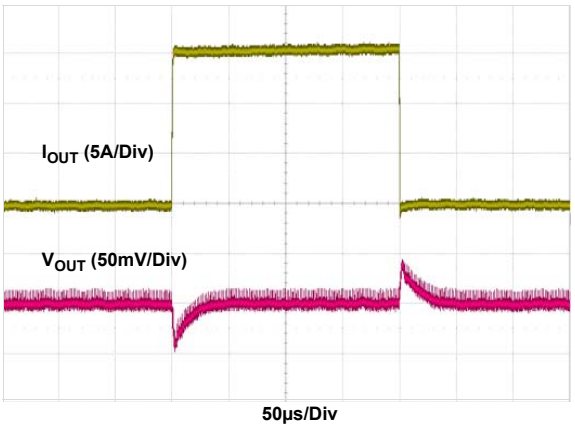


Figure 24. 0A-15A, >10A/µs, 12V_{IN},1V_{OUT}, 615kHz

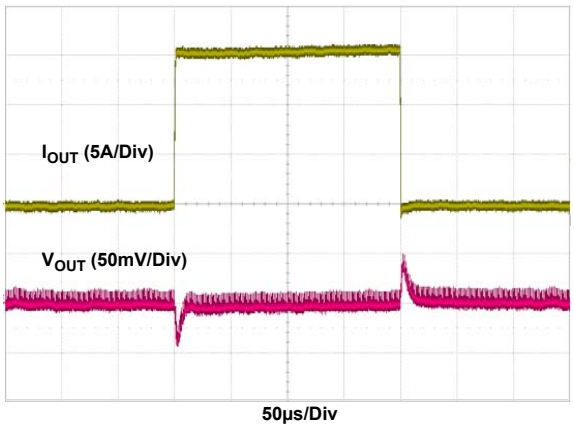


Figure 25. 0A-15A, >10A/µs, 12V_{IN},1.5V_{OUT}, 889kHz

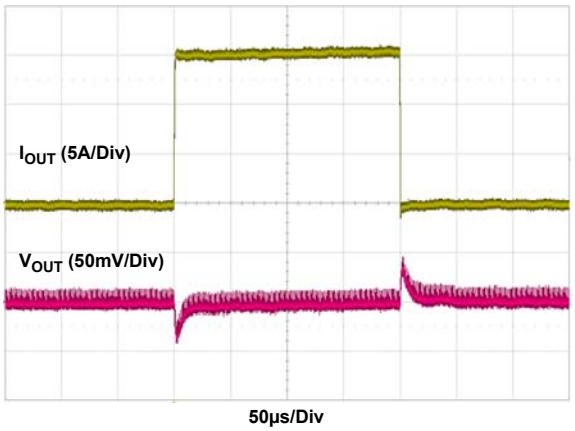


Figure 26. 0A-15A, >10A/µs, 12V_{IN},1.8V_{OUT}, 889kHz

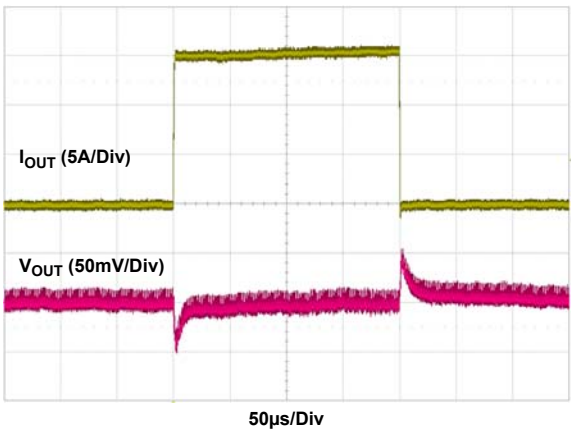


Figure 27. 0A-15A, >10A/µs, 12V_{IN}, 2.5V_{OUT}, 1067kHz

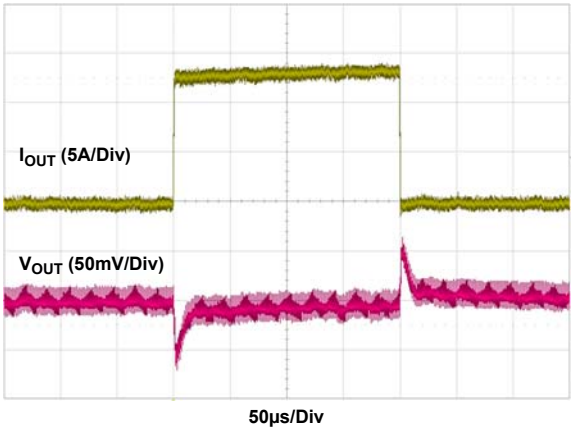


Figure 28. 0A-12.5A, >10A/µs, 12V_{IN}, 3.3V_{OUT}, 800kHz

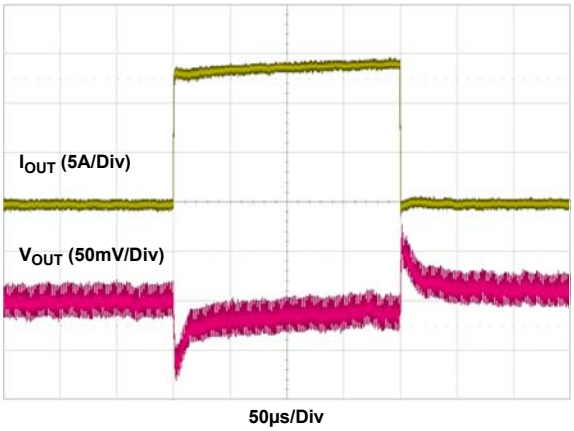


Figure 29. 0A-12.5A, >10A/µs, 12V_{IN}, 5V_{OUT}, 1067kHz

4. Functional Description

4.1 SMBus Communications

The ISL8274M provides a PMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ISL8274M can be used with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The ISL8274M accepts most standard PMBus commands. When configuring the device using PMBus commands, it is recommended that the enable pin is tied to SGND.

The SMBus device address is the only parameter that must be set by the external pins. All other device parameters can be set using PMBus commands.

The ISL8274M can operate without the PMBus in pin-strap mode with configurations programmed by pin-strap resistors, such as output voltage, ASCR setting, switching frequency, OCP limit, device SMBus address, input UVLO, soft-start/stop, and tracking.

4.2 Output Voltage Selection

The output voltages of both channels may be set to a voltage between 0.6V and 5V if the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET1/2 pins are used to set the output voltage VOUT1/2 to levels as shown in Table 3. The RSET1/2 resistor is placed between the VSET1/2 pins and SGND. A standard 1% resistor is required.

Table 3. Output Voltage Resistor Settings

VOUT1/2 (V)	RSET1/2 (kΩ)
1	LOW
1.5	OPEN
3.3	HIGH
0.6	10
0.675	11
0.7	12.1
0.72	13.3
0.75	14.7
0.8	16.2
0.85	17.8
0.9	19.6
0.93	21.5
0.95	23.7
0.98	26.1
1.03	28.7
1.05	31.6
1.1	34.8
1.12	38.3
1.15	42.2
1.2	46.4
1.25	51.1
1.3	56.2
1.35	61.9

Table 3. Output Voltage Resistor Settings (Continued)

VOUT1/2 (V)	RSET1/2 (kΩ)
1.4	68.1
1.65	75
1.8	82.5
1.85	90.9
2	100
2.4	110
2.5	121
2.8	133
3	147
3.6	162
5	178

The output voltage may also be set to any value between 0.6V and 5V using the PMBus command VOUT_COMMAND. This device supports dynamic voltage scaling by allowing change to the output voltage set point during regulation. The voltage transition rate is specified by the PMBus command VOUT_TRANSITION_RATE.

By default, V_{OUT_MAX} is set to 110% of V_{OUT} set by the pin-strap resistor, which can be changed to any value up to 5.5V by the PMBus Command VOUT_MAX.

4.3 Soft-Start, Stop Delay, and Ramp Times

The ISL8274M follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. Once this process is completed, the device is ready to accept commands through the PMBus interface and the module is ready to be enabled. If the module is to be synchronized to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ISL8274M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp-up time can be programmed to custom values using the PMBus commands TON_DELAY and TON_RISE. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 2ms to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay and ramp down time for soft-stop/off can be programmed using the PMBus commands TOFF_DELAY and TOFF_FALL. In addition, the module can be configured as “immediate off” using the command ON_OFF_CONFIG, so that the internal MOSFETs are turned off immediately after the delay time expires.

The SS/TRACK pin can be used to program the soft-start/stop delay time and ramp time to some typical values as well as enable/disable the tracking function shown in Table 4 on page 23.

Table 4. Soft-Start/Stop and Tracking Resistor Settings

TON_DELAY TOFF_DELAY (ms)		TON_RISE TOFF_FALL (ms)		Tracking		
Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	R (kΩ)
5	5	2	2	No	No	LOW
5	5	2	5	No	No	OPEN
5	5	5	2	No	No	HIGH
5	5	5	5	No	No	10
5	10	2	2	No	No	11
5	10	2	5	No	No	12.1
5	10	5	2	No	No	13.3
5	10	5	5	No	No	14.7
10	5	2	2	No	No	16.2
10	5	2	5	No	No	17.8
10	5	5	2	No	No	19.6
10	5	5	5	No	No	21.5
20	5	2	2	No	No	23.7
20	5	5	5	No	No	26.1
5	20	2	2	No	No	28.7
5	20	2	5	No	No	31.6
5	20	5	2	No	No	34.8
5	20	5	5	No	No	38.3
5	N/A	2	N/A	No	Track 100%	42.2
5	N/A	2	N/A	No	Track 50%	46.4
5	N/A	5	N/A	No	Track 100%	51.1
5	N/A	5	N/A	No	Track 50%	56.2
10	N/A	2	N/A	No	Track 100%	61.9
10	N/A	2	N/A	No	Track 50%	68.1
10	N/A	5	N/A	No	Track 100%	75
10	N/A	5	N/A	No	Track 50%	82.5
N/A	5	N/A	2	Track 100%	No	90.9
N/A	5	N/A	2	Track 50%	No	100
N/A	5	N/A	5	Track 100%	No	110
N/A	5	N/A	5	Track 50%	No	121
N/A	10	N/A	2	Track 100%	No	133
N/A	10	N/A	2	Track 50%	No	147
N/A	10	N/A	5	Track 100%	No	162
N/A	10	N/A	5	Track 50%	No	178

4.4 Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore, the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

The ISL8274M integrates a tracking scheme that allows one of its outputs (Channel 1 or Channel 2) to track a voltage that is applied to the VTRKP and VTRKN pins with no external components required. The VTRKP and VTRKN pins are analog inputs that, when the tracking mode is enabled, configure the voltage applied to the VTRKP and VTRKN pins to act as a reference for the device's output regulation.

Figure 30 illustrates the typical connection and the two tracking modes:

- **Coincident** - This mode configures the ISL8274M to ramp its output voltage at the same rate as the voltage applied to the VTRK pin until it reaches its desired output voltage. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.
- **Ratio-metric** - This mode configures the ISL8274M to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRKP and VTRKN pins. The default setting is 50%, but an external resistor string can be used to configure a different tracking ratio. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.

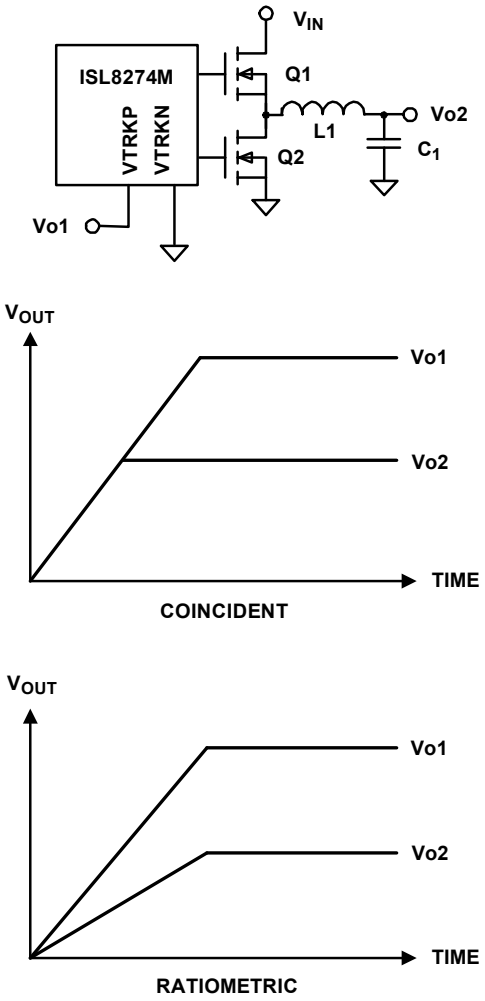


Figure 30. Tracking Modes

The master ISL8274M device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. The maximum tracking rise time is 1V/ms. The slave device must be enabled before the master. Any device that is configured for tracking mode will ignore its TON_DELAY and TON_RISE settings and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRKP and VTRKN pins. Tracking mode can be configured by using the TRACK_CONFIG command.

The VOUT_COMMAND needs to be set the same as the target tracking voltage when tracking is enabled. For example, the VOUT_COMMAND of the Page1 (VOUT2 which enables the tracking) needs to set to 1V if tracking 100% is selected and a ramp of 1V is applied to VTRKP and VTRKN. The VOUT_COMMAND of Page 1 (VOUT2 which enables the tracking) needs to set to 1V if tracking 50% is selected and a ramp of 2V is applied to VTRKP and VTRKN. In Tracking mode, the minimum voltage that can be tracked is ~200mV.

4.5 Power-Good

The ISL8274M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. This limit may be changed using the PMBus command POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the ISL8274M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A PG delay can be programmed using the PMBus command POWER_GOOD_DELAY.

4.6 Switching Frequency and PLL

The device's switching frequency is set from 296kHz to 1067kHz using the pin-strap method (combined with the average OCP limit setting) as shown in Table 5, or by using the PMBus command FREQUENCY_SWITCH. The ISL8274M incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. It is recommended that when using an external clock, the same frequency should be set in the FREQUENCY_SWITCH command. If the external clock is lost, the module will automatically switch to the internal clock. When using the internal oscillator, the SYNC pin can be configured as a clock source and as an external sync to other modules. Refer to "SYNC_CONFIG (E9h)" on page 67 for more information.

Table 5. Switching Frequency and OCP Limit Resistor Setting

SYNC/OCP		OCP Avg	
R (kΩ)	**Fsw (KHz)**	**Ch1 (A)**	**Ch2 (A)**
LOW	296	35	35
OPEN	889	35	35
HIGH	1067	35	35
10	296	30	35
11	296	30	30
12.1	296	25	35
13.3	296	25	30
14.7	296	25	25
16.2	320	25	35
17.8	320	25	30
19.6	320	25	25
21.5	320	20	30
23.7	320	20	25
26.1	364	25	35

Table 5. Switching Frequency and OCP Limit Resistor Setting (Continued)

SYNC/OCP		OCP Avg	
R (kΩ)	Fsw (KHz)	Ch1 (A)	Ch2 (A)
28.7	364	25	30
31.6	364	20	30
34.8	421	30	35
38.3	421	30	30
42.2	471	25	35
46.4	471	25	30
51.1	471	20	35
56.2	571	25	35
61.9	571	25	30
68.1	571	20	35
75	571	20	30
82.5	615	35	35
90.9	615	35	30
100	615	30	30
110	615	25	35
121	615	25	30
133	615	25	25
147	727	35	35
162	800	30	35
178	800	30	30

4.7 Output Overcurrent Protection

The ISL8274M is protected from damage if the output is shorted to ground or if an overload condition is imposed on the output. Average output overcurrent fault threshold can be programmed by the PMBus command IOUT_AVG_OC_FAULT_LIMIT while the peak output overcurrent fault threshold can be programmed by the PMBus command IOUT_OC_FAULT_LIMIT. The default response from an average overcurrent fault is an immediate shutdown without retry. A continuous retry can be enabled using the PMBus command MFR_IOUT_OC_FAULT_RESPONSE. A hard bound of 50A is applied to the peak overcurrent limit.

The average OCP limit can be set by the SYNC/OCP pin strap as well. Refer to Table 5 on page 25 for more information.

4.8 Loop Compensation

The module loop response is programmable through the PMBus command ASCR_CONFIG or by using the pin-strap method (ASCR1/2 pins) according to Table 6. The ISL8274M uses the ChargeMode control algorithm that responds to the output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

Table 6. ASCR Resistor Setting

ASCR Gain	ASCR Residual	R (kΩ)
350	110	LOW
525	90	OPEN
475	80	HIGH
100	90	10
100	100	11
120	90	12.1
120	100	13.3
140	90	14.7
140	100	16.2
140	110	17.8
150	90	19.6
150	100	21.5
160	70	23.7
160	90	26.1
175	80	28.7
175	90	31.6
200	90	34.8
200	100	38.3
200	110	42.2
225	80	46.4
225	90	51.1
250	80	56.2
250	100	61.9
275	90	68.1
275	100	75
300	70	82.5
300	90	90.9

Table 6. ASCR Resistor Setting (Continued)

ASCR Gain	ASCR Residual	R (kΩ)
350	100	100
450	100	110
450	110	121
500	70	133
500	90	147
600	100	162
600	110	178

4.9 SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between pins SA/CFG and SGND. The SA/CFG pin also defines the input undervoltage lockout limit. The input Undervoltge Lockout (UVLO) prevents the ISL8274M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.18V and 16V by using the PMBus command VIN_UV_FAULT_LIMIT.

Table 7 lists the available module addresses.

A fault response to an input undervoltage fault can be programmed by the PMBus command VIN_UV_FAULT_RESPONSE. If the input undervoltage fault retry is enabled, the module will shut down immediately once the input voltage falls below V_{UVLO} and then continuously checks the input voltage after a retry delay time, which can be configured from 35ms to 280ms. If the input voltage rises above the input undervoltage warning level, the module will restart. The input undervoltage warning is $1.05*V_{UVLO}$ by default and can be programmed by the PMBus command VIN_UV_WARN_LIMIT.

Table 7. SMBus Address and UVLO Resistor Setting

PMBus Address	UVLO (V)	R (kΩ)
26h	4.5	LOW
28h	4.5	OPEN
19h	10.8	10
1Ah	4.5	11
1Bh	10.8	12.1
1Ch	4.5	13.3
1Dh	10.8	14.7
1Eh	4.5	16.2
1Fh	10.8	17.8
20h	4.5	19.6
21h	10.8	21.5
22h	4.5	23.7
23h	10.8	26.1
24h	4.5	28.7
25h	10.8	31.6
26h	4.5	34.8
27h	10.8	38.3
28h	4.5	42.2
29h	10.8	46.4

Table 7. SMBus Address and UVLO Resistor Setting (Continued)

PMBus Address	UVLO (V)	R (kΩ)
2Ah	4.5	51.1
2Bh	10.8	56.2
2Ch	4.5	61.9
2Dh	10.8	68.1
2Eh	4.5	75
2Fh	10.8	82.5
30h	4.5	90.9
31h	10.8	100
32h	4.5	110
33h	10.8	121

4.10 Output Overvoltage Protection

The ISL8274M offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator compares the actual output voltage (seen at pins VSEN1/2P, VSEN1/2N) to a threshold set to 15% higher than the target output voltage (default setting). The fault threshold can be programmed to a desired level by the PMBus command VOUT_OV_FAULT_LIMIT. If the VSEN1/2P, VSEN1/2N voltage exceeds this threshold, the module will initiate an immediate shutdown without retry. Continuous retry can be enabled using the PMBus command VOUT_OV_FAULT_RESPONSE. The retry delay time can be configured from 35ms to 280ms.

Internal to the module, two 100Ω resistors are populated from V_{OUT} to VSEN1/2P and SGND to VSEN1/2N to protect the module from overvoltage conditions in case of open at the voltage sensing pins and differential remote sense traces due to assembly error. As long as differential remote sense traces have low resistance, V_{OUT} regulation accuracy is not compromised.

4.11 Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ISL8274M provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage. However, the total time elapsed from when the delay period expires to when the output reaches its target value will match the preconfigured ramp time (see Figure 31 on page 30).

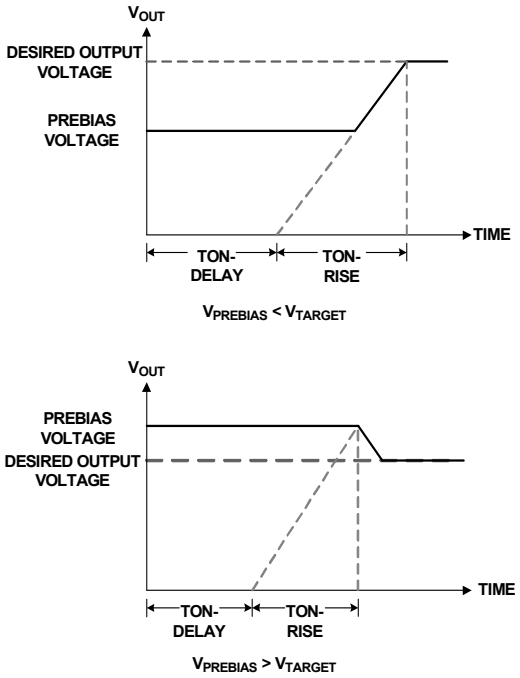


Figure 31. Output Responses to Prebias Voltages

If a prebias voltage is higher than the target voltage after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage. Thus, both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

Once the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition. The device then responds based on the output overvoltage fault response setting programmed by the PMBus command VOUT_OV_FAULT_RESPONSE.

4.12 Thermal Overload Protection

The ISL8274M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The factory default temperature limit is set to +115°C, and can be changed using the PMBus command OT_FAULT_LIMIT. Note that the temperature reading from the PMBus command is the temperature of the internal controller, which is lower than the junction temperature of the module.

The default response from an over-temperature fault is an immediate shutdown without retry. Retry settings can be programmed using the PMBus command OT_FAULT_RESPONSE. Hysteresis is implemented with the over-temperature fault retry. If a retry is enabled, the module will shut down immediately upon an over-temperature fault event and then continuously check the temperature after a retry delay time, which can be configured from 35ms to 280ms. If the temperature falls below the over-temperature warning level, the module will restart. The over-temperature warning is +105°C by default and programmable using the PMBus command OT_WARN_LIMIT.

4.13 Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between the Renesas digital power modules and digital controllers. The DDC bus provides the communication channel between devices for features such as current sharing, sequencing and fault spreading. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as shown in (EQ. 1):

$$\text{Rise Time} = R_{PU} \bullet C_{LOAD} < 1\mu s \quad \text{(EQ. 1)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to an external 3.3V or 5V supply as long as this voltage is present before or during the device power-up. In principle, each device connected to the DDC bus represents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance.

4.14 Phase Spreading

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device, such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments with the PMBus command INTERLEAVE. The internal two phases of the module always maintain a phase difference of 180°.

4.15 Fault Spreading

Digital-DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group using the PMBus command DDC_GROUP. When a nondestructive fault occurs, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shut down simultaneously, if configured to do so.

Note that fault retry is not supported in multiple modules with fault spreading enabled.

4.16 Output Sequencing

A group of Digital-DC modules or devices can be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors (FPGAs and ASICs) that require one supply to reach its operating voltage before another supply reaching it in order to avoid latch-up. Multidevice sequencing can be achieved by configuring each device with the PMBus command SEQUENCE. Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that follows the sequence.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. The enable must be driven low to initiate a sequenced turnoff of the group. It is recommended to enable fault spreading with the PMBus command DDC_GROUP within a sequencing group.

4.17 Monitoring Using SMBus

The ISL8274M can monitor a wide variety of different system parameters using the PMBus commands:

- READ_VIN
- READ_VOUT
- READ_IOUT
- READ_INTERNAL_TEMP
- READ_DUTY_CYCLE
- READ_FREQEUNCY
- READ_VMON

4.18 Snapshot Parameter Capture

The ISL8274M offers a special feature to capture parametric data and fault status following a fault. A detailed description is provided in the "PMBus Commands Description" on page 42 under PMBus the commands SNAPSHOT and SNAPSHOT_CONTROL.

4.19 Nonvolatile Memory

The ISL8274M stores user configurations in internal nonvolatile memory. Integrated security measures ensure that the user can only restore the module to a level that has been made available to them. During the initialization process, the ISL8274M checks for stored values contained in its internal nonvolatile memory.

Modules are shipped with factory defaults configuration and most settings can be overwritten by PMBus commands and can be stored in nonvolatile memory by the PMBus command STORE_USER_ALL.

5. Layout Guide

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary (Figure 32). Refer to the ISL8274MEVAL1Z layout design.

- Establish separate SGND plane and PGND planes, then connect SGND to PGND plane on a middle layer and underneath PAD6 with a single point connection. For SGND and PGND pin connections, such as small pins H16, J16, M5 and M17..., use multiple vias for each pin to connect to inner SGND or PGND layers.
- Place enough ceramic capacitors between VIN and PGND, VOUT and PGND and bypass capacitors between VDD, VDRV and the ground plane, as close to the module as possible to minimize high frequency noise. It is very critical to place the output ceramic capacitors close to the VOUT pads and in the direction of the load current path in order to create a low impedance path for the high frequency inductor ripple current.
- Use large copper areas for power paths (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. It is recommended to enlarge PAD11 and PAD9 to place more vias on them. The ceramic capacitors CIN can be placed on the bottom layer under these two pads.
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation and place the two traces in parallel. Route a trace from VSEN1/2N and VSEN1/2P to the point of load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENN, VSENP sensing lines near the SW pins.
- PAD14 and 16 (SW1 and SW2) are noisy pads, but they are beneficial for thermal dissipation. If the noise issue is critical for the applications, it is recommended to use only the top layer for the SW pads. For better thermal performance, use multiple vias on these pads to connect into the SW inner and bottom layers. However, use caution when placing a limited area of SW planes in any layer. The SW planes should avoid the sensing signals and should be surrounded by the PGND layer to avoid noise coupling.
- For pins SWD1 (L3) and SWD2 (P10), it is recommended to connect to the related SW1 and SW2 pads with short loop traces. The trace width should be more than 20 mils.

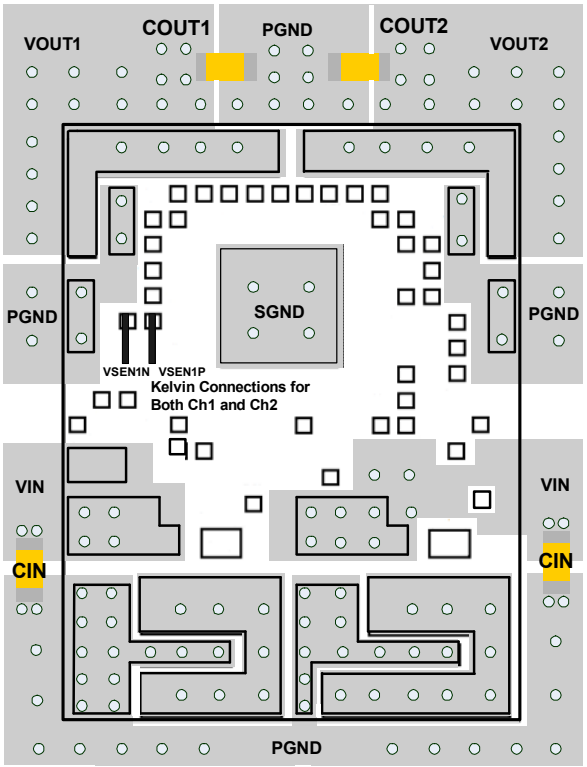


Figure 32. Recommended Layout

5.1 Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. The derating curves are derived based on tests of the ISL8274MEVAL1Z evaluation board, which is an 8-layer board 4.5x4inch in size with 2oz Cu on the top and bottom layers, 1oz Cu on the inner layers, and multiple via interconnects. In the actual application, other heat sources and design margins should be considered.

5.2 Package Description

The structure of the ISL8274M belongs to the High Density Array (HDA) no-lead package. This kind of package has advantages, such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8274M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8274M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly is overmolded with a polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown on pages 73 through page 79. The module has a small size of 18mmx 23mmx 7.5mm.

5.3 PCB Layout Pattern Design

The bottom of ISL8274M is a leadframe footprint, which is attached to the PCB by the surface mounting process. The PCB layout pattern is shown on pages 77 through 79. The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pads.

5.4 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 oz. of copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as the number of vias is increased. Simply use as many vias as practical for the thermal land size and your board design rules will allow. All vias should be capped and filled to avoid scavenging solder from the I/O solder joints and creating voids.

5.5 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown on pages 71 through 77. The gap width between pads is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a “brick like” paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

5.6 Reflow Parameters

Due to the low mount height of the HDA, “No-Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. A nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 33 is provided as a guideline, which can be customized for varying manufacturing practices and applications.

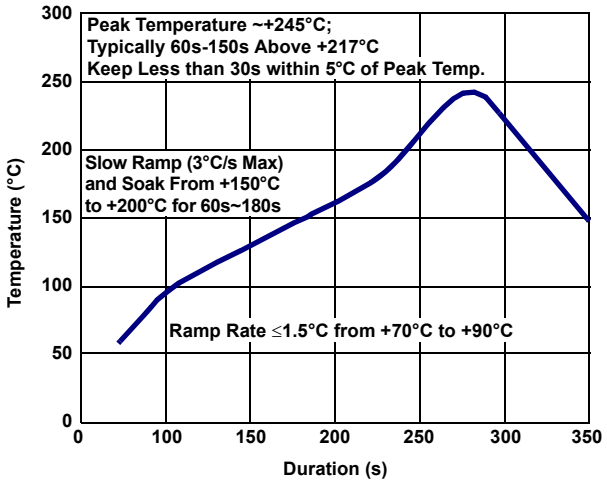


Figure 33. Typical Reflow Profile

6. PMBus Command Summary

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
00h	PAGE	Selects Controller 0, 1, or both.	R/W Byte	BIT	00h	Channel 1	page 42
01h	OPERATION	Sets Enable, Disable, and V_{OUT} Margin modes.	R/W Byte	BIT			page 42
02h	ON_OFF_CONFIG	Configures the EN pin and PMBus commands to turn the unit ON/OFF.	R/W Byte	BIT	17h	Hardware Pin Enable, immediate off	page 42
03h	CLEAR_FAULTS	Clears fault indications.	SEND Byte				page 43
15h	STORE_USER_ALL	Stores all PMBus values written since last restore at user level.	SEND Byte				page 43
16h	RESTORE_USER_ALL	Restores PMBus settings that were stored using STORE_USER_ALL.	SEND Byte				page 43
20h	VOUT_MODE	Preset to defined data format of V_{OUT} commands.	READ Byte	BIT	13h	Linear Mode, Exponent = -13	page 43
21h	VOUT_COMMAND	Sets the nominal value of the output voltage.	R/W Word	L16u		Pin-strap	page 44
23h	VOUT_CAL_OFFSET	Applies a fixed offset voltage to the VOUT_COMMAND.	R/W Word	L16s	0000h	0V	page 44
24h	VOUT_MAX	Sets the maximum possible value of V_{OUT}. 110% of pin-strap V_{OUT}.	R/W Word	L16u		1.1*V_{OUT} Pin-strap	page 44
25h	VOUT_MARGIN_HIGH	Sets the value of the V_{OUT} during a margin high.	R/W Word	L16u		1.05*V_{OUT} Pin-strap	page 44
26h	VOUT_MARGIN_LOW	Sets the value of the V_{OUT} during a margin low.	R/W Word	L16u		0.95*V_{OUT} Pin-strap	page 45
27h	VOUT_TRANSITION_RATE	Sets the transition rate during margin or other change of V_{OUT}.	R/W Word	L11	BA00h	1V/ms	page 45
28h	VOUT_DROOP	Sets the loadline (V/I Slope) resistance for the rail.	R/W Word	L11	0000h	0mV/A	page 45
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W Word	L11		Pin-strap	page 45
37h	INTERLEAVE	Configures a phase offset between devices sharing a SYNC clock.	R/W Word	BIT	0021h(Ch1) /0022(Ch2)	180° phase shift between Ch1/Ch2	page 46
38h	IOUT_CAL_GAIN	Sense resistance for inductor DCR current sensing.	R/W Word	L11	B2C3(Ch1)/ B2D7(Ch2)	0.69mΩ (Ch1)/ 0.7mΩ (Ch2)	page 46
39h	IOUT_CAL_OFFSET	Sets the current-sense offset.	R/W Word	L11	B529(Ch1)/ BDDC(Ch2)	-0.71A(Ch1)/ -1.07A(Ch2)	page 46

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W Word	L16u		1.15*V_{OUT} Pin-strap	page 46
41h	VOUT_OV_FAULT_RESPONSE	Configures the V_{OUT} overvoltage fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 47
42h	VOUT_OV_WARN_LIMIT	Sets the V_{OUT} overvoltage warn threshold.	R/W Word	L16u		1.10*V_{OUT} Pin-strap	page 47
43h	VOUT_UV_WARN_LIMIT	Sets the V_{OUT} undervoltage warn threshold.	R/W Word	L16u		0.9*V_{OUT} Pin-strap	page 47
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W Word	L16u		0.85*V_{OUT} Pin-strap	page 48
45h	VOUT_UV_FAULT_RESPONSE	Configures the V_{OUT} undervoltage fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 48
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} peak overcurrent fault threshold.	R/W Word	L11	E320h	50A	page 48
4Ah	IOUT_OC_WARN_LIMIT	Sets the I_{OUT} average overcurrent warning threshold.	R/W Word	L11		0.9*IOUT_AVG_OC _FAULT_LIMIT	page 49
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} valley undercurrent fault threshold.	R/W Word	L11	E4E0h	-50A	page 49
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W Word	L11	EB98h	+115°C	page 49
50h	OT_FAULT_RESPONSE	Configures the over-temperature fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 50
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit.	R/W Word	L11	EB48h	+105°C	page 50
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit.	R/W WORD	L11	DC40h	-30°C	page 50
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W Word	L11	E530h	-45°C	page 51
54h	UT_FAULT_RESPONSE	Configures the under-temperature fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 51
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W Word	L11	D3A0	14.5V	page 51
56h	VIN_OV_FAULT_RESPONSE	Configures the V_{IN} overvoltage fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 52
57h	VIN_OV_WARN_LIMIT	Sets the input overvoltage warning limit.	R/W Word	L11	D353h	13.3V	page 52
58h	VIN_UV_WARN_LIMIT	Sets the input undervoltage warning limit.	R/W Word	L11		1.03*V_{IN} UV Fault Limit	page 52

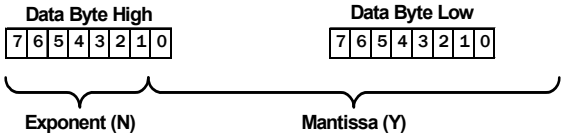
Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W Word	L11		Pin-strap	page 53
5Ah	VIN_UV_FAULT_RESPONSE	Configures the V_{IN} undervoltage fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 53
5Eh	POWER_GOOD_ON	Sets the voltage threshold for power-good indication.	R/W Word	L16u		0.9*V_{OUT} Pin-strap	page 53
60h	TON_DELAY	Sets the delay time from ENABLE to start of V_{OUT} rise.	R/W Word	L11		Pin-strap	page 54
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W Word	L11		Pin-strap	page 54
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall.	R/W Word	L11		Pin-strap	page 54
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.	R/W Word	L11		Pin-strap	page 54
78h	STATUS_BYTE	Returns an abbreviated status for fast reads.	Read Byte	BIT	00h	No Faults	page 55
79h	STATUS_WORD	Returns information with a summary of the units's fault condition.	Read Word	BIT	0000h	No Faults	page 56
7Ah	STATUS_VOUT	Returns the V_{OUT} specific status.	Read Byte	BIT	00h	No Faults	page 56
7Bh	STATUS_IOUT	Returns the I_{OUT} specific status.	Read Byte	BIT	00h	No Faults	page 57
7Ch	STATUS_INPUT	Returns specific status specific to the input.	Read Byte	BIT	00h	No Faults	page 57
7Dh	STATUS_TEMP	Returns the temperature specific status.	Read Byte	BIT	00h	No Faults	page 57
7Eh	STATUS_CML	Returns the communication, logic and memory specific status.	Read Byte	BIT	00h	No Faults	page 58
80h	STATUS_MFR_SPECIFIC	Returns the VMON and external sync clock specific status.	Read Byte	BIT	00h	No Faults	page 58
88h	READ_VIN	Returns the input voltage reading.	Read Word	L11			page 58
8Bh	READ_VOUT	Returns the output voltage reading.	Read Word	L16u			page 59
8Ch	READ_IOUT	Returns the output current reading.	Read Word	L11			page 59
8Dh	READ_INTERNAL_TEMP	Returns the temperature reading internal to the device.	Read Word	L11			page 59
94h	READ_DUTY_CYCLE	Returns the duty cycle reading during the ENABLE state.	Read Word	L11			page 59

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
95h	READ_FREQUENCY	Returns the measured operating switch frequency.	Read Word	L11			page 59
99h	MFR_ID	Sets a user defined identification.	R/W Block	ASC		Null	page 60
9Ah	MFR_MODEL	Sets a user defined model.	R/W Block	ASC		Null	page 60
9Bh	MFR_REVISION	Sets a user defined revision.	R/W Block	ASC		Null	page 60
9Ch	MFR_LOCATION	Sets a user defined location identifier.	R/W Block	ASC		Null	page 60
9Dh	MFR_DATE	Sets a user defined date.	R/W Block	ASC		Null	page 61
9Eh	MFR_SERIAL	Sets a user defined serialized identifier.	R/W Block	ASC		Null	page 61
A8h	LEGACY_FAULT_GROUP	Sets rail IDs of legacy devices for fault spreading	R/W Block	BIT	00000000h	No rail ID specified	page 61
B0h	USER_DATA_00	Sets a user defined data.	R/W Block	ASC		Null	page 62
D0h	ISENSE_CONFIG	Configures ISENSE related features.	R/W Byte	BIT	06h	256ns Blanking Time, High Range	page 62
D1h	USER_CONFIG	Configures several user-level features.	R/W Byte	BIT	84h	Minimum duty control, PG open drain	page 63
D3h	DDC_CONFIG	Configures the DDC bus.	R/W Word	BIT		Pin-strap (Rail ID set based on PMBus address. Phase ID = 0; Phases in Rail = 1	page 63
D4h	POWER_GOOD_DELAY	Sets the delay between V_{OUT} > PG threshold and asserting the PG pin.	R/W Word	L11	C300h	3ms	page 64
DFh	ASCR_CONFIG	Configures ASCR control loop.	R/W Block	CUS		Pin-strap	page 64
E0h	SEQUENCE	Identifies the Rail DDC ID to perform multi-rail sequencing.	R/W Word	BIT	0000h	Prequel and Sequel Disabled	page 65
E1h	TRACK_CONFIG	Configures voltage tracking modes	R/W Byte	BIT		Pin-strap setting	page 66
E2h	DDC_GROUP	Sets rail DDC IDs to obey faults and margining spreading information.	R/W Block	BIT		Ignore Broadcast VOUT_COMMAND, OPERATION	page 66
E4h	DEVICE_ID	Returns the 16-byte (character) device identifier string.	Read Block	ASC		Reads Device Version	page 67
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 67
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W Byte	BIT	80h	Disable and No Retry	page 67
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold.	R/W	L11		Set by SYNC/OCP pin-strap	page 68

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold.	R/W	L11	DC40h	-30A	page 68
E9h	SYNC_CONFIG	Configures the SYNC pin.	R/W Byte	BIT	00h	Pin-strap (set based on SYNC/OCP)	page 69
EAh	SNAPSHOT	Returns 32-byte read-back of parametric and status values.	Read Block	BIT			page 69
EBh	BLANK_PARAMS	Returns recently changed parameter values.	Read Block	BIT	FF...FFh		page 70
F3h	SNAPSHOT_CONTROL	Snapshot feature control command.	R/W Byte	BIT			page 70
F4h	RESTORE_FACTORY	Restores device to the factory default values.	Send Byte				page 70
F5h	MFR_VMON_OV_FAULT_LIMIT	Returns the VMON overvoltage threshold.	Read Word	L11	CB00h	6V	page 70
F6h	MFR_VMON_UV_FAULT_LIMIT	Returns the VMON undervoltage threshold.	Read Word	L11	CA00h	4V	page 71
F7h	MFR_READ_VMON	Returns the VMON voltage reading.	Read Word	L11			page 71
F8h	VMON_OV_FAULT_RESPONSE	Returns the VMON overvoltage response.	Read Byte	BIT	80h	Disable and No Retry	page 71
F9h	VMON_UV_FAULT_RESPONSE	Returns the VMON undervoltage response.	Read Byte	BIT	80h	Disable and No Retry	page 71

6.1 PMBus Data Formats

Linear-11 (L11)
L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X).



Relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)
L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Linear-16 Signed (L16s)
L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X).
Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)
An explanation of the Bit Field for each command is provided in "PMBus Commands Description" on page 41.

Custom (CUS)
An explanation of the Custom data format for each command is provided in "PMBus Commands Description" on page 41. A combination of Bit Field and integer is a common type of Custom data format.

ASCII (ASC)
A variable length string of text characters uses ASCII data format.

6.2 PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and ASCCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_USER_ALL and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

6.3 Summary

All commands can be read at any time.

Always disable the device when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a change to a device setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable.

7. PMBus Commands Description

PAGE(00h)

Definition: Select Channel 1, Channel 2 or both channels to receive commands. All commands following this command will be received and acted on by the selected channel or channels.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 00h (Page 0)

Units: N/A

Bits 7:4	Bits 3:0	Page
0000	0000	0
0000	0001	1
1111	1111	Both

OPERATION (01h)

Definition: Sets Enable, Disable and V_{OUT} Margin settings.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value:

Units: N/A

Settings	Actions
00h	Immediate off (no sequencing)
40h	Soft off (with sequencing)
80h	On - Nominal
90h	On - Margin low
A0h	On - Margin high

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 17h (Device starts from ENABLE pin with soft-off)

Units: N/A

Settings	Actions
16h	Device starts from ENABLE pin with soft off.
17h	Device starts from ENABLE pin with immediate off.
1Ah	Device starts from OPERATION command with soft off.
1Bh	Device starts from OPERATION command with immediate off.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

Reference: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings. Fixed with linear mode with default exponent (N) = -13

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 13h (Linear Mode, N = -13)

Units: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than VOUT_MAX.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit.

Data Length in Bytes: 2

Data Format: L16s

Type: R/W

Default Value: 0000h

Units: Volts

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. Default value can be changed using PMBus.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10xVOUT_COMMAND pin-strap setting

Units: Volts

Range: 0V to 5.5V

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.05 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the V_{OUT} during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.95 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_TRANSITION_RATE (27h)

Definition: Sets the rate at which the output should change voltage when the device receives the VOUT_COMMAND or an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: BA00h (1V/ms)

Units: V/ms

Range: 0.1V/ms to 4V/ms

VOUT_DROOP (28h)

Definition: Sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A, at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with adaptive voltage positioning schemes or multi-module current sharing. In current sharing configuration, VOUT_DROOP set in each module stands for the droop seen by the load.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: mV/A

Range: 0mV/A to 40mV/A

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command through the PMBus. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: kHz

Range: 296kHz to 1066kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments. The internal two phases of the module always maintain a phase difference of 180°.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: 0021h (Page0), 0022h (Page1)

Units: N/A

Bits	Purpose	Value	Description
15:4	Reserved	0	Reserved
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group.

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Ch1: B2C3(0.69mΩ); Ch2: B2D7(0.7mΩ)

Units: mΩ

IOUT_CAL_OFFSET (39h)

Definition: Nulls out any offsets in the output current sensing circuit for each phase, and compensates for delayed measurements of current ramp due to I_{SENSE} blanking time.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Ch1: B529(-0.71A); Ch2: BDDC(-1.07A)

Units: A

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.15xVOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response. Note that the device cannot be set to ignore this fault mode.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1) * 35ms. Sets the time between retries in 35ms

VOUT_OV_WARN_LIMIT (42h)

Definition: Sets the V_{OUT} overvoltage warning threshold. The power-good signal is pulled low when the output voltage goes higher than this threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10xVOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_WARN_LIMIT (43h)

Definition: Sets the V_{OUT} undervoltage warning threshold. The power-good signal is pulled low when the output voltage goes lower than this threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.90 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.85 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1) * 35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded. The recommended peak OCP limit is determined by (EQ. 2).

$$\text{IOUT\_OC\_FAULT\_LIMIT} = (\text{IOUT\_AVG\_OC\_FAULT\_LIMIT} + 0.5 \bullet \text{IRIPPLE}_{P\_P}) \bullet 130\% \quad \text{(EQ. 2)}$$

A hard bound of 50A is applied to the command value. This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with the IOUT_AVG_OC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E320h (50A)

Units: A

Range: -100A to 100A

IOUT_OC_WARN_LIMIT (4Ah)

Definition: Sets the I_{OUT} average overcurrent warning threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: IOUT_AVG_OC_FAULT_LIMIT x 0.9

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded. The recommended valley UCP limit is determined by (EQ. 3):

(EQ. 3) $$IOUT\_UC\_FAULT\_LIMIT = (IOUT\_AVG\_UC\_FAULT\_LIMIT - 0.5 \bullet IRIPPLE_{P\_P}) \bullet 130\%$$

A hard bound of -50A is applied to the command value. This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_AVG_UC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E4E0 (-50A)

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB98 (+115°C)

Units: °C

Range: 0°C to +175°C

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device on what action to take in response to an over-temperature fault.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Fault Value: 80h (Disable and no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

OT_WARN_LIMIT (51h)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB48h (+105°C)

Units: °C

Range: 0°C to +175°C

UT_WARN_LIMIT (52h)

Definition: Sets the temperature at which the device should indicate an under-temperature warning alarm. In response to the UT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: DC40h (-30°C)

Units: °C

Range: -55°C to +25°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault. Note that the temperature must rise above UT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E530h (-45°C)

Units: °C

Range: -55°C to +25°C

UT_FAULT_RESPONSE (54h)

Definition: Configures the under-temperature fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1) * 35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D3A0 (14.5V)

Units: V

Range: 0V to 16V

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1) * 35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage warning threshold. In response to the OV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Protectable: Yes

Default Value: D353h (13.3V)

Units: V

Range: 0V to 16V

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} undervoltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: 1.03 x VIN_UV_FAULT_LIMIT pin-strap setting

Units: V

Range: 0V to 12V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: V

Range: 0V to 12V

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts with a delay specified in POWER_GOOD_DELAY after the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_WARN_LIMIT. It is recommended to set POWER_GOOD_ON higher than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9 x VOUT_COMMAND pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 2ms to 256ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY. In multi-module current sharing configuration where ASCR is disabled for start up, the rise time of V_{OUT} can be approximately calculated by (EQ. 1).

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0ms to 100ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0ms to 256ms

TOFF_FALL (65h)

Definition: Sets the soft-off fall time for V_{OUT} after DISABLE and TOFF_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0ms to 100ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in Bits 7:1 has occurred.

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read Only

Default Value: 0000h

Units: N/A

Bit Number	Status Bit Name	Meaning
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT/POUT	An output current or output power fault or warning has occurred.
13	INPUT	An input voltage, input current, or input power fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	FANS	A fan or airflow fault or warning has occurred.
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in Bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in Bits 7:1 has occurred.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Indicates an output overvoltage warning.
5	VOUT_UV_WARNING	Indicates an output undervoltage warning.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	An output overcurrent and low voltage fault has occurred.
5	IOUT_OC_WARNING	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	N/A	These bits are not used.

STATUS_INPUT (7Ch)

Definition: Returns the input voltage and input current status information.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	N/A	These bits are not used.

STATUS_TEMP (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Meaning
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	Packet error was detected in the PMBus command.
4:2	Not used
1	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults. VMON OV/UV warnings are set at ±10% of the VMON_FAULT commands.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default value: 00h

Units: N/A

Bit Number	Field Name	Meaning
7:6	Reserved	
5	VMON UV Warning	The voltage on the VMON pin has dropped 10% below the level set by VMON_UV_FAULT_LIMIT.
4	VMON OV Warning	The voltage on the VMON pin has risen 10% above the level set by VMON_OV_FAULT_LIMIT.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Reserved	
1	VMON UV Fault	The voltage on the VMON pin has dropped below the level set by VMON_UV_FAULT_LIMIT.
0	VMON OV Fault	The voltage on the VMON pin has risen above the level set by VMON_OV_FAULT_LIMIT.

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read Only

Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: L16u

Type: Read Only

Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read Only

Default Value: N/A

Units: A

READ_INTERNAL_TEMP (8Dh)

Definition: Returns the controller junction temperature reading from the internal temperature sensor.

Data Length in Bytes: 2

Data Format: L11

Type: Read Only

Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: %

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: kHz

MFR_ID (99h)

Definition: Sets user defined identification. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASC

Type: Block R/W

Default Value: Null

Units: N/A

MFR_MODEL (9Ah)

Definition: Sets a user defined model. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASC

Type: Block R/W

Default Value: Null

Units: N/A

MFR_REVISION (9Bh)

Definition: Sets a user defined revision. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASC

Type: Block R/W

Default Value: Null

Units: N/A

MFR_LOCATION (9Ch)

Definition: Sets a user defined location identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASC

Type: Block R/W

Default Value: Null

Units: N/A

MFR_DATE (9Dh)

Definition: Sets a user defined date. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASC

Type: Block R/W

Default Value: Null

Units: N/A

Reference: N/A

MFR_SERIAL (9Eh)

Definition: Sets a user defined serialized identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASC

Type: Block R/W

Default Value: Null

Units: N/A

LEGACY_FAULT_GROUP (A8h)

Definition: Sets which rail DDC IDs should be listened to for fault spreading with legacy devices. The data sent is a 4-byte, 32-bit, bit vector where every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device will respond upon receiving a fault spreading event. In this vector, Bit 0 of byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with DDC ID 31.

Data Length in Bytes: 4

Data Format: BIT

Type: Block R/W

Default Value: 00000000h (No rail ID specified)

USER_DATA_00 (B0h)

Definition: Sets user defined data. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASC

Type: Block R/W

Default Value: Null

Units: N/A

ISENSE_CONFIG (D0h)

Definition: Configures current sense circuitry.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 06h (256ns current sense blanking time, current sense high range)

Units: N/A

Bit	Field Name	Value	Setting	Description
7:4	Reserved	0000		
3:2	Current Sense Blanking Time	00	192ns	Sets the blanking time current sense blanking time.
		01	256ns	
		10	412ns	
		11	640ns	
1:0	Current Sense Range	00	Low Range	±25mV
		01	Mid Range	±35mV
		10	High Range	±50mV
		11	Not Used	

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command overrides the pin-strap settings.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 84h (Pin-strap setting for ASCR on Start up; ramp-up and ramp-down minimum duty cycle 0.39%; minimum duty cycle control enabled; PG is an open-drain output.)

Units: N/A

Bit	Field Name	Value	Setting	Description
7	ASCR on for Start up	0	Disabled	ASCR is disabled for start up. Use this for Current Sharing mode.
		1	Enabled	ASCR is enabled for start up. Use this for Stand Alone mode.
6:5	Reserved	00		Reserved
4:3	Ramp-up and Ramp-down Minimum Duty Cycle	00	0.39%	Sets the minimum duty-cycle during start-up and shutdown ramp.
		01	0.78%	
		10	1.17%	
		11	1.56%	
2	Minimum Duty Cycle Control	0	Disable	Control for minimum duty cycle.
		1	Enable	
1	Power-good Pin Configuration	0	Open Drain	0 = PG is an open-drain output.
		1	Push-Pull	1 = PG is a push-pull output.
0	Reserved	0		

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing. The DDC rail ID is set according to the SMBus address. For current sharing applications, the DDC Phase ID is set according to the number of phases. The device position and number of devices in the rail can be programmed as needed.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: Pin-strap setting for Rail ID. Phase ID = 0; Phases in rail = 1

Units: N/A

Bit	Field Name	Value	Setting	Description
15:13	Phase ID	0 to 7		Sets the phase ID in a current sharing rail.
12:8	Rail ID	0 to 31 (00 to 1Fh)		Configures DDC rail ID
7:3	Reserved	0	Reserved	Reserved
2:0	Phases in Rail	0 to 7		Identifies the number of phases on the same rail (+1).

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: C300h, 3ms

Units: ms

Range: 0ms to 5s

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR gain is analogous to bandwidth, ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To lower transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but will not affect the peak output voltage deviation. Typical ASCR gain settings range from 50 to 1000, and ASCR residual settings range from 10 to 100.

Data Length in Bytes: 4

Data Format: CUS

Type: R/W

Default Value: Pin-strap setting

Bit	Purpose	Data Format	Value	Description
31:25	Unused		0000000h	Unused
24	ASCR Enable	BIT	1	Enable
			0	Disable
23:16	ASCR Residual Setting	Integer		ASCR residual
15:0	ASCR Gain Setting	Integer		ASCR gain

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device will enable its output when its EN or OPERATION enable states, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus.

The data field is a two-byte value. The most significant byte contains the 5-bit Rail DDC ID of the prequel device. The Least Significant Byte (LSB) contains the 5-bit Rail DDC ID of the sequel device. The Most Significant Bit (MSB) of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: 0000h (Prequel and Sequel disabled)

Bit	Field Name	Value	Setting	Description
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail.
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8.
14:13	Reserved	0	Reserved	Reserved
12:8	Prequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the prequel rail.
7	Sequel Enable	0	Disable	Disable, no sequel following this rail.
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0.
6:5	Reserved	0	Reserved	Reserved
4:0	Sequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the sequel rail.

TRACK_CONFIG (E1h)

Definition: Configures the voltage tracking modes of the device. Only one channel can be configured to track: Channel 1 or Channel 2.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: Pin-strap setting based on SS/TRACK

Bit	Field Name	Value	Setting	Description
7	Voltage Tracking Control	0	Disable	Tracking is disabled
		1	Enable	Tracking is enabled
6:3	Reserved	0000	Reserved	Reserved
2	Tracking Ratio Control	0	100%	Output tracks at 100% ratio of VTRK input
		1	50%	Output tracks at 50% ratio of VTRK input
1	Tracking Upper Limit	0	Target Voltage	Output voltage is limited by target voltage
		1	VTRK Voltage	Output voltage is limited by VTRK voltage
0	Ramp-Up Behavior	0	Track after PG	The output is not allowed to track VTRK down before power-good.
		1	Track always	The output is allowed to track VTRK down before power-good.

DDC_GROUP (E2h)

Definition: Configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and Broadcast VOUT_COMMAND group ID and enable.

Data Length in Bytes: 3

Data Format: BIT

Type: Block R/W

Default Value: Ignore Broadcast VOUT_COMMAND, OPERATION.

Bits	Purpose	Value	Description
23:22	Reserved	0	Reserved
21	BROADCAST_VOUT_COMMAND Response	1	Responds to BROADCAST_VOUT_COMMAND with same Group ID.
		0	Ignores BROADCAST_VOUT_COMMAND.
20:16	BROADCAST_VOUT_COMMAND Group ID	0-31d	Group ID sent as data for broadcast BROADCAST_VOUT_COMMAND events.
15:14	Reserved	0	Reserved
13	BROADCAST_OPERATION Response	1	Responds to BROADCAST_OPERATION with same Group ID.
		0	Ignores BROADCAST_OPERATION.
12:8	BROADCAST_OPERATION Group ID	0-31d	Group ID sent as data for broadcast BROADCAST_OPERATION events.
7:6	Reserved	0	Reserved
5	POWER_FAIL Response	1	Responds to POWER_FAIL events with same Group ID by shutting down immediately.
		0	Responds to POWER_FAIL events with same Group ID with sequenced shutdown.
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events.

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASC

Type: Block Read

Default Value: Part number/Die revision/Firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, and no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

Bit	Field Name	Value	Description
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_OC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: SYNC/OCP pin-strap setting

Units: A

Equation: IOUT_AVG_OC_FAULT_LIMIT = Y×2N

Range: -100A to 100A

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the I_{OUT} average undercurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DC40h (-30A)

Units: A

Equation: IOUT_AVG_UC_FAULT_LIMIT = Y×2N

Range: -100A to 100A

SYNC_CONFIG (E9h)

Definition: Used to set options for SYNC output configurations.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: Pin-strap setting

Settings	Actions
00h	Use internal clock. Clock frequency is set by pin-strap or PMBus command.
02h	Use internal clock and output internal clock.
04h	Use external clock.

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, last updated values are stored to the flash memory. When the SNAPSHOT STATUS bit is set stored, device will no longer automatically capture parametric and status values following fault till stored data are erased. Use the SNAPSHOT_CONTROL command to erase store data and clear the status bit before next ramp up. Data erased is not allowed when module is enabled.

Data Length in Bytes: 32

Data Format: Bit field

Type: Block Read

Byte Number	Value	PMBus Command	Format
31:23	Reserved	Reserved	00h
22	Flash Memory Status Byte FF - Not Stored 00 - Stored	N/A	BIT
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	Reserved	Reserved	00h
11:10	Internal Temperature	READ_INTERNAL_TEMP (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Highest Measured Output Current	N/A	L11
5:4	Output Current	READ_IOUT (8Ch)	L11
3:2	Output Voltage	READ_VOUT (8Bh)	L16u
1:0	Input Voltage	READ_VIN (88h)	L11

BLANK_PARAMS (EBh)

Definition: Returns a 16-byte string indicating which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A “1” indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Data Length in Bytes: 16

Data Format: BIT

Type: Block Read

Default Value: FF…FFh

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h will cause the device to copy the current Snapshot values from NVRAM to the 32-byte Snapshot command parameter. Writing a 02h will cause the device to write the current Snapshot values to NVRAM. Writing a 03h will erase all Snapshot values from NVRAM. Write (02h) and Erase (03h) may only be used when the device is disabled. All other values will be ignored.

Data Length in Bytes: 1

Data Format: Bit field

Type: R/W byte

Value	Description
01h	Read Snapshot values from NV RAM
02h	Write Snapshot values to NV RAM
03h	Erase Snapshot values stored in NV RAM.

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Data Length in Bytes: 0

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Reads the VMON OV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CB00h (6V)

Units: V

Range: 4V to 6V

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Reads the VMON UV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CA00h (4V)

Units: V

Range: 4V to 6V

MFR_READ_VMON (F7h)

Definition: Reads the VMON voltage.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: N/A

Units: V

Range: 4V to 6V

VMON_OV_FAULT_RESPONSE (F8h)

Definition: Reads the VMON OV fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 80h (Disable and no retry)

Units: N/A

VMON_UV_FAULT_RESPONSE (F9h)

Definition: Reads the VMON UV fault response, which is a direct copy of VIN_UV_FAULT_RESPONSE.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 80h (Disable and no retry)

Units: V

8. Firmware Revision History

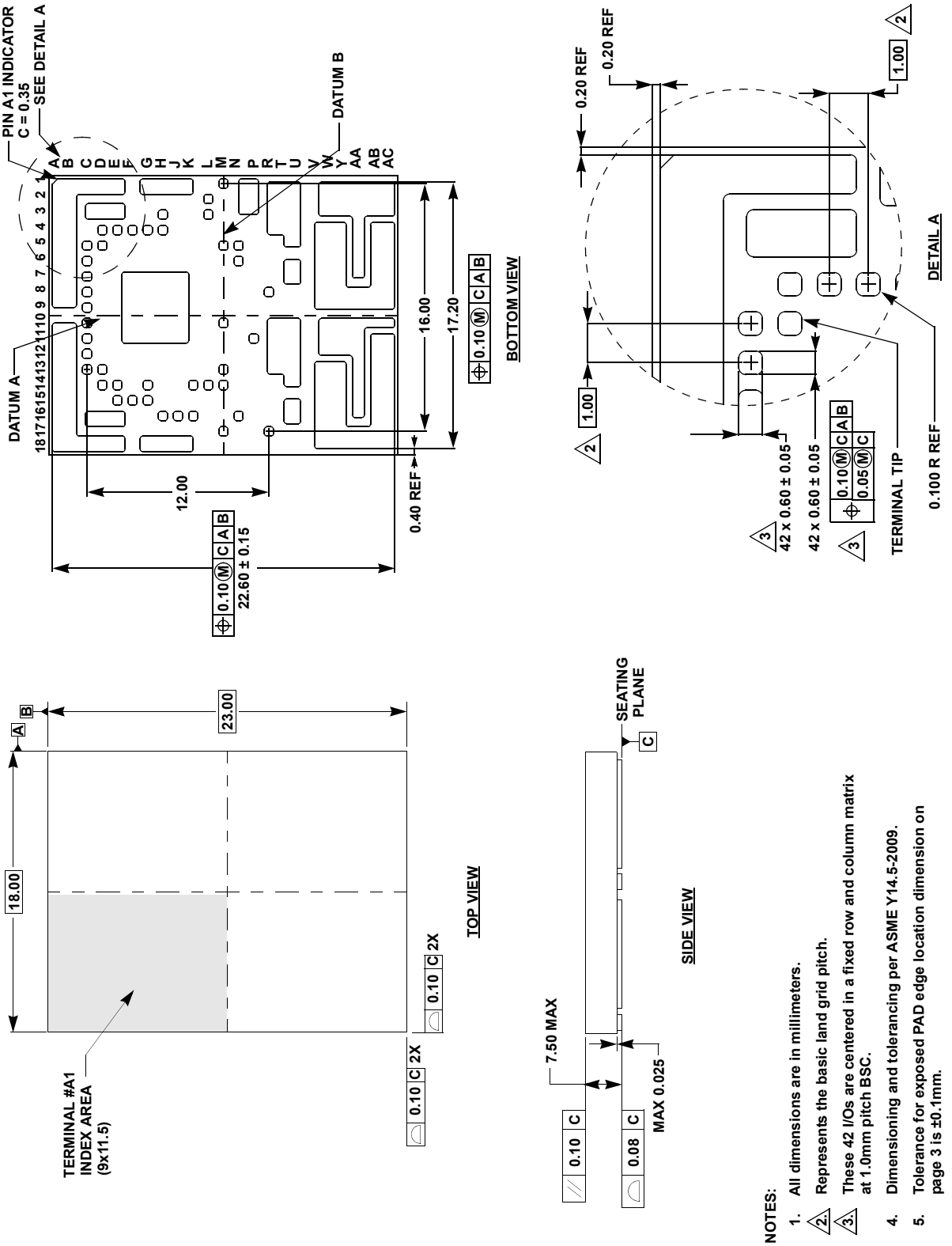
Table 8. ISL8274M Nomenclature Guide

Firmware Revision Code	Change Description	Note
ISL8274M-0-G0100	Initial Release	

9. Package Outline Drawing

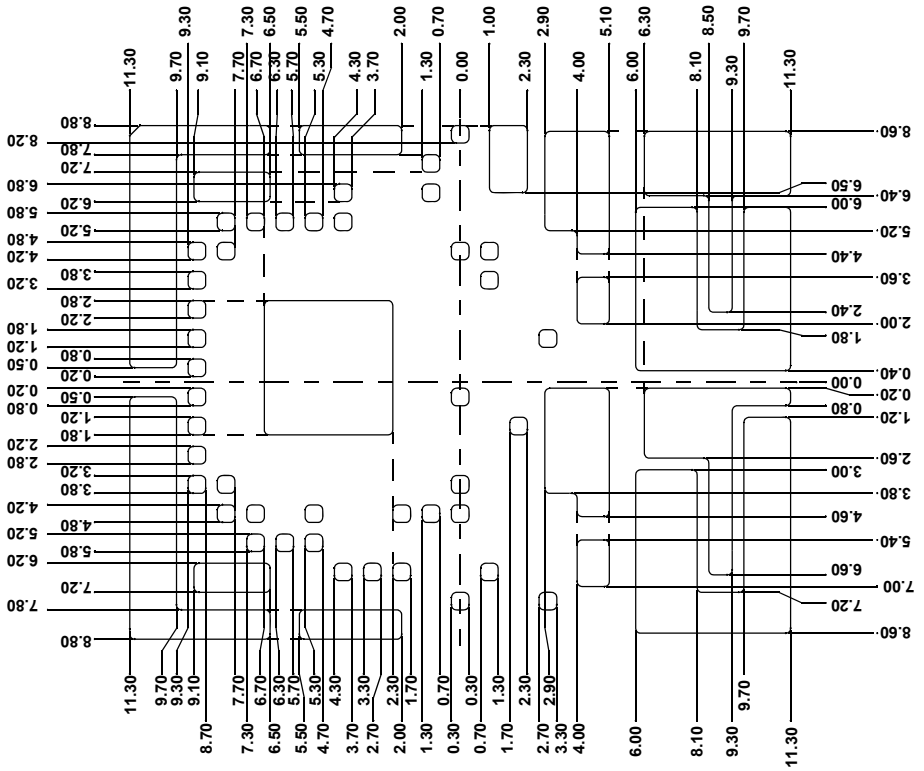
For the most recent package outline drawing, see Y58.18x23.

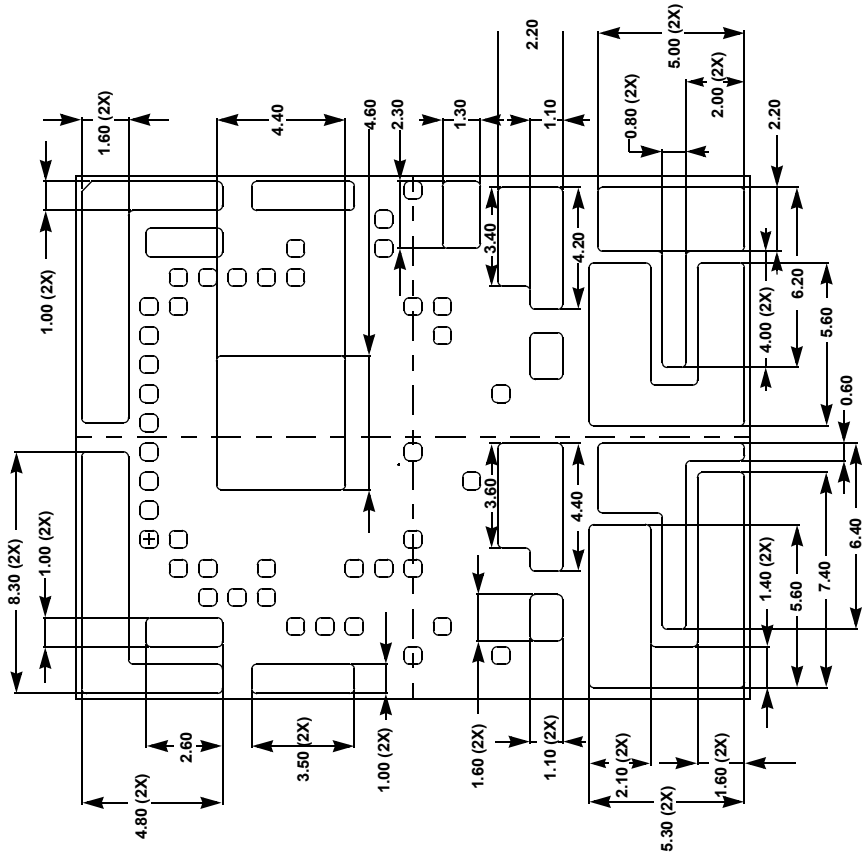
Y58.18x23
58 I/O 18mmx23mmx7.5mm CUSTOM HDA MODULE
Rev 3, 12/16

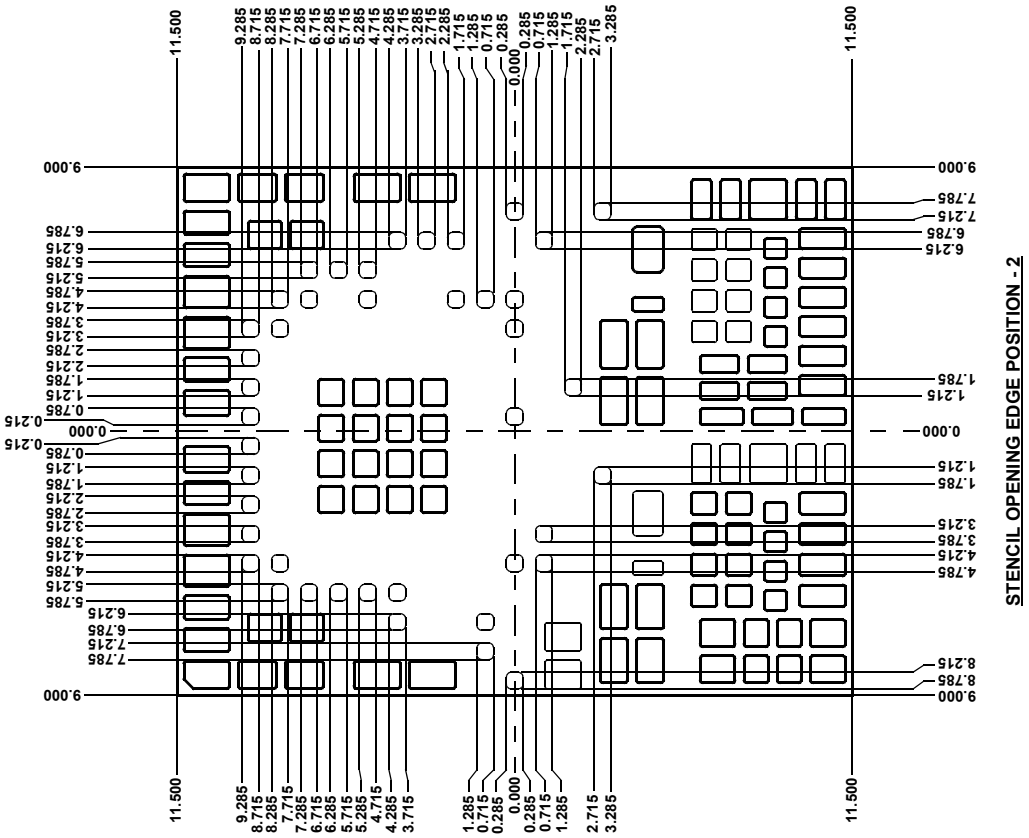


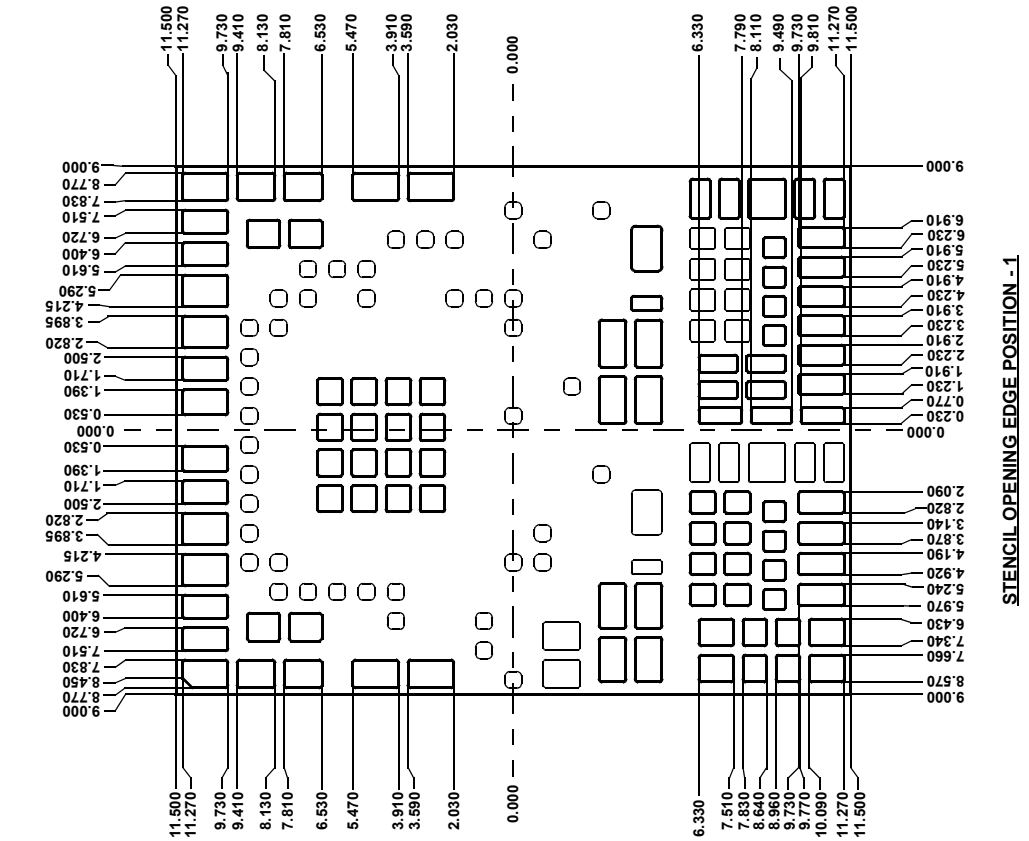
NOTES:

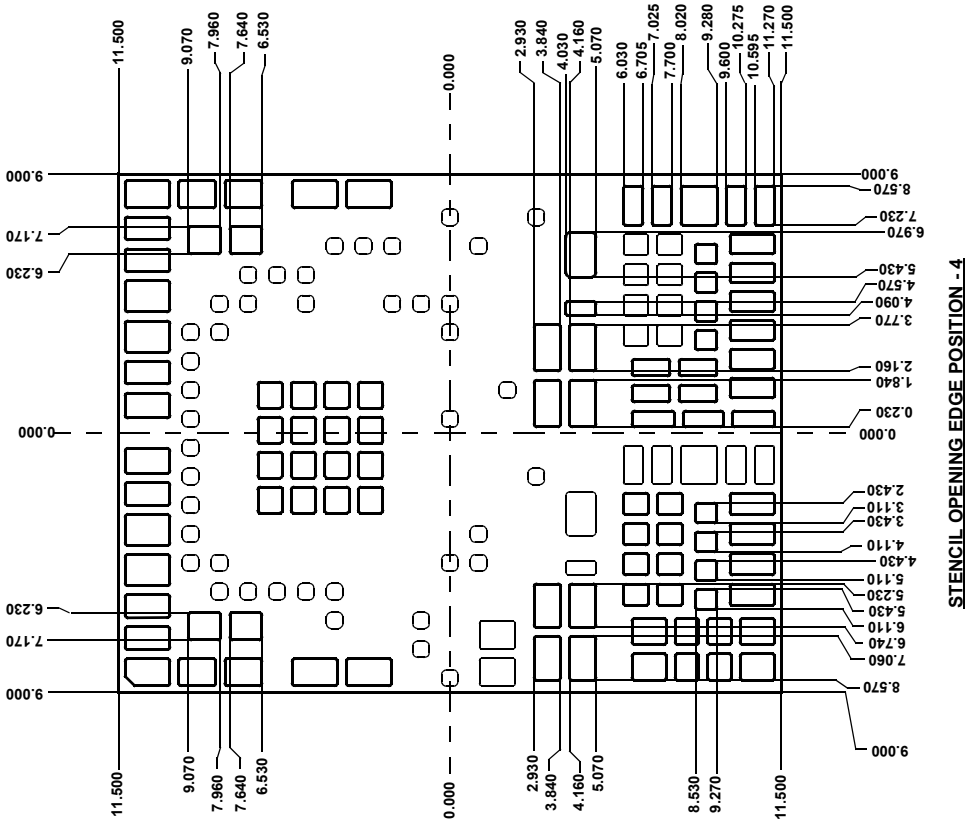
1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 42 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension on page 3 is ±0.1mm.

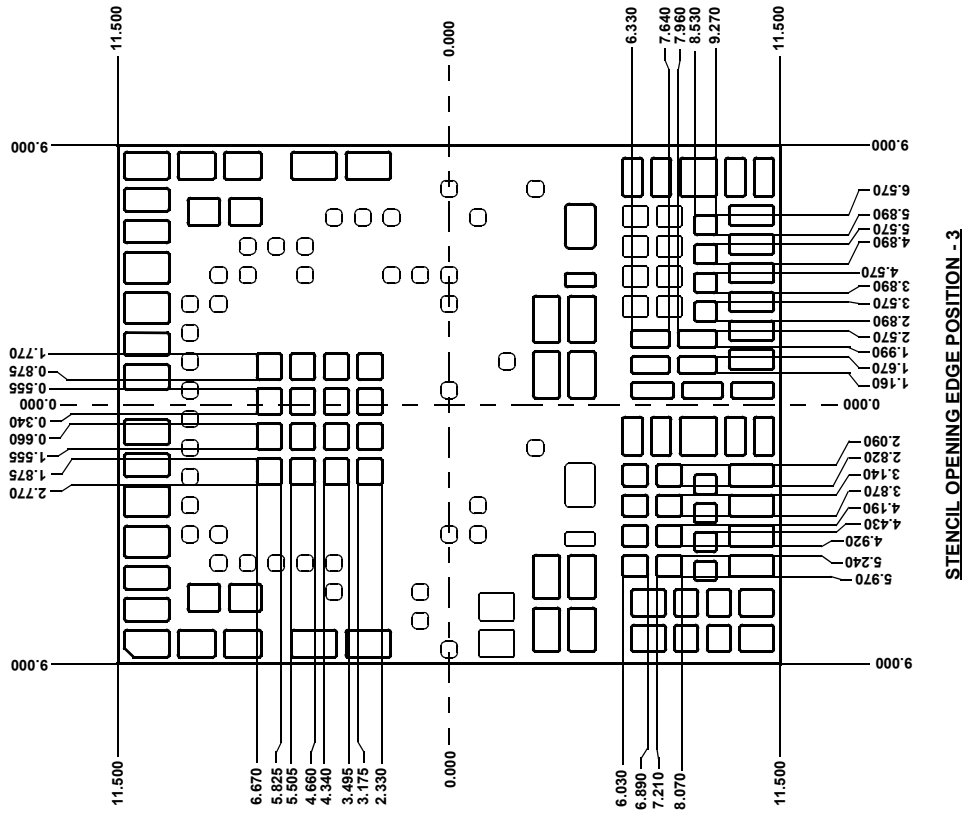

TERMINAL AND PAD EDGE DETAILS

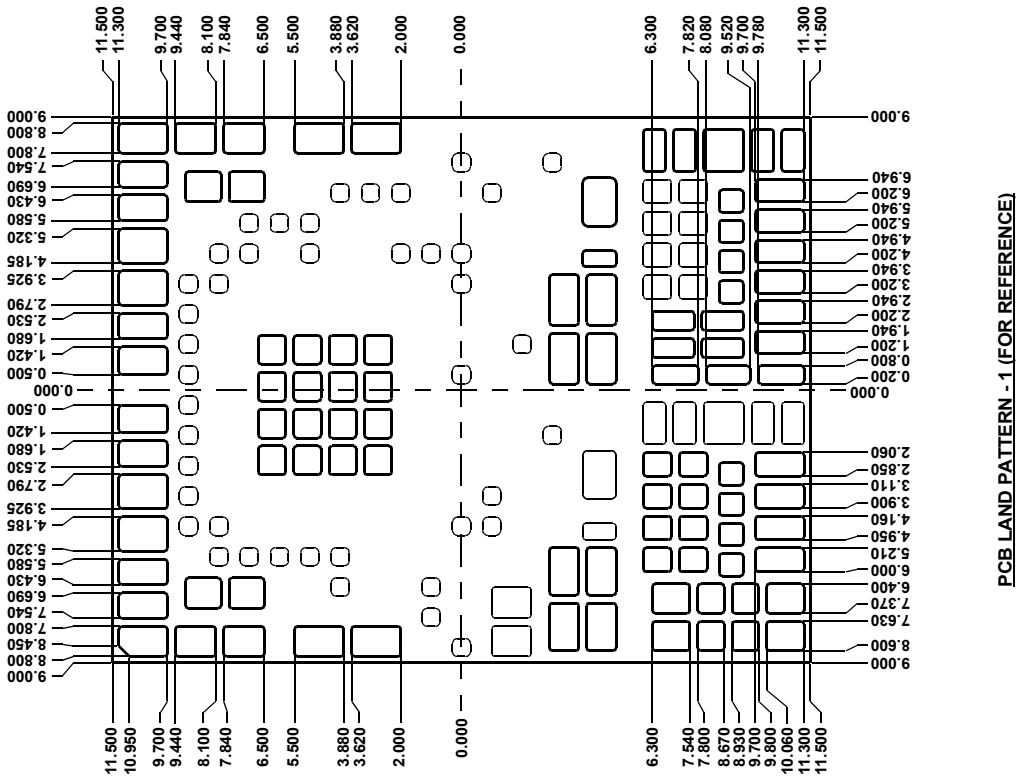

BOTTOM VIEW
SIZE DETAILS FOR THE 16 EXPOSED PADS

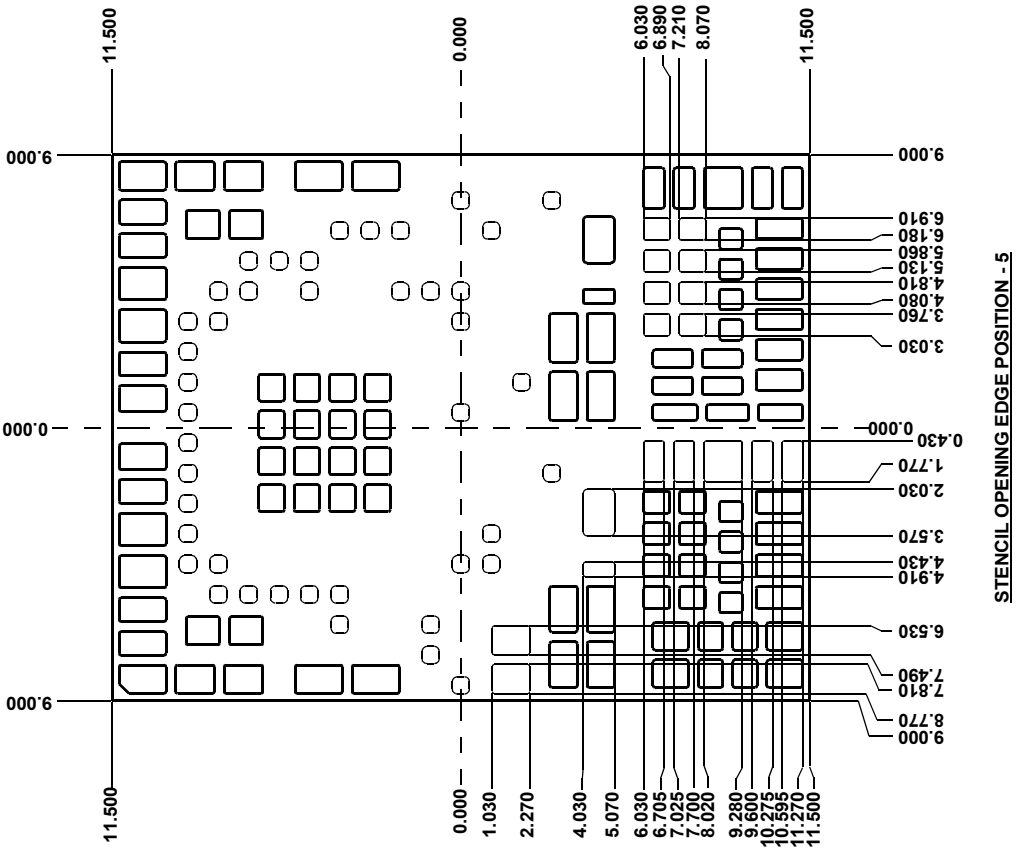

STENCIL OPENING EDGE POSITION - 2

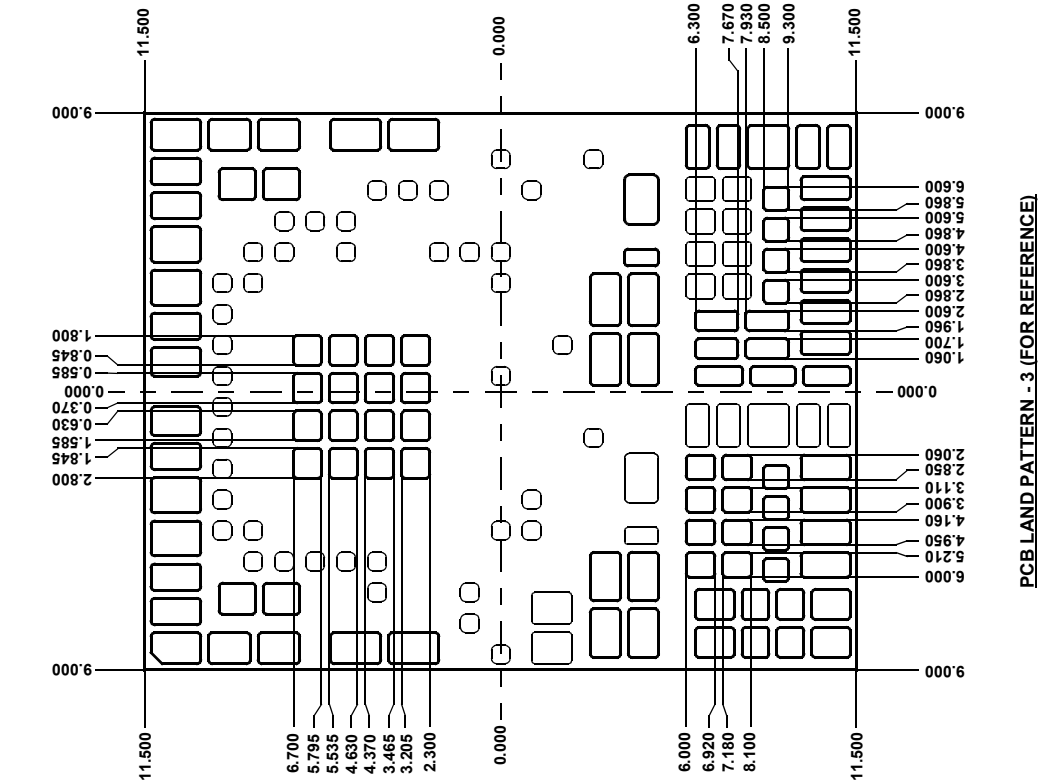

STENCIL OPENING EDGE POSITION - 1


STENCIL OPENING EDGE POSITION - 4
11.500
9.070
7.960
7.640
6.530
0.000
2.930
3.840
4.030
4.160
5.070
6.030
6.705
7.025
7.700
8.020
9.280
9.600
10.275
10.595
11.270
11.500
9.000
8.570
7.230
6.970
5.430
4.570
4.090
3.770
2.160
1.840
0.230
0.000
2.430
3.110
3.430
4.110
4.430
5.110
5.230
5.430
6.110
6.740
7.060
8.570
9.000
7.170
6.230
8.530
9.270

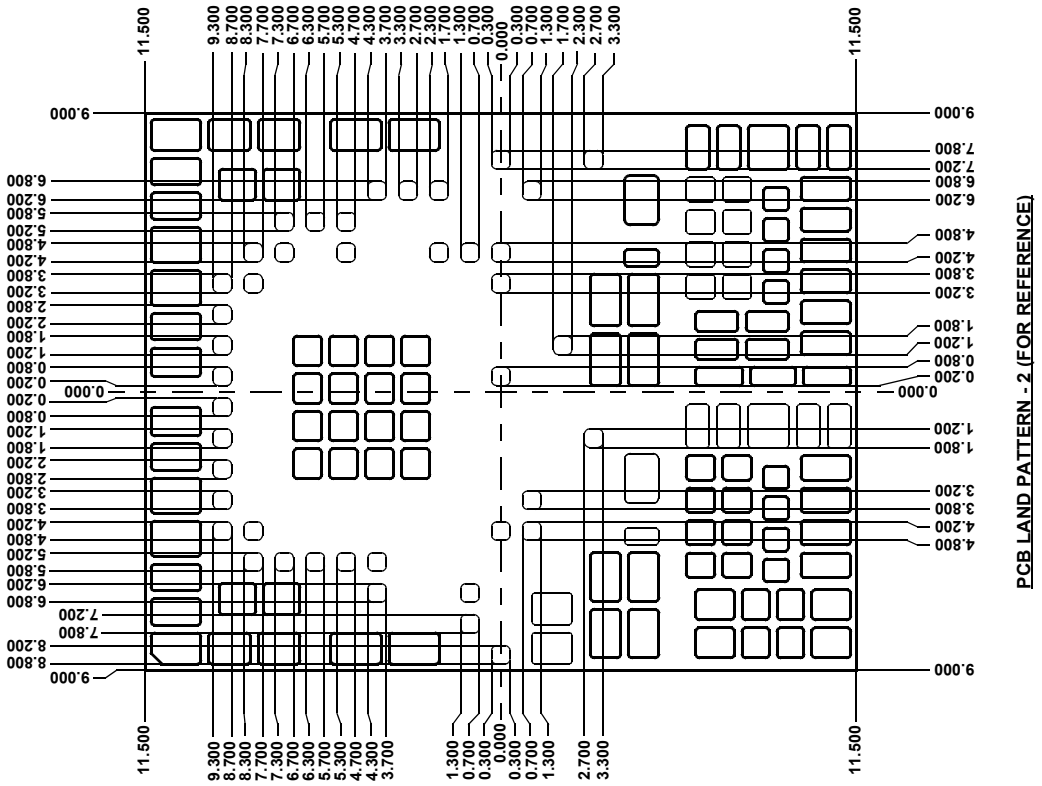

STENCIL OPENING EDGE POSITION - 3
11.500
0.000
6.330
7.640
7.960
8.530
9.270
9.000
6.570
5.890
5.570
4.890
4.570
3.890
3.570
2.890
2.570
1.990
1.670
1.160
0.000
2.090
2.820
3.140
3.870
4.190
4.430
4.920
5.240
5.970
1.770
0.875
0.555
0.340
0.660
1.555
1.875
2.770
6.670
5.825
5.505
4.660
4.340
3.495
3.175
2.330
6.030
6.890
7.210
8.070
8.530


11.500
11.300
9.700
9.440
8.100
7.840
6.500
5.500
3.880
3.620
2.000
0.000
6.300
7.820
8.080
9.520
9.700
9.780
11.300
11.500
9.000
8.800
7.800
7.540
6.690
6.430
5.580
5.320
4.185
3.925
2.790
2.530
1.680
1.420
0.500
0.000
6.940
6.200
5.940
5.200
4.940
4.200
3.940
3.200
2.940
2.200
1.940
1.200
0.800
0.200
2.060
2.850
3.110
3.900
4.160
4.950
5.210
6.000
6.400
7.370
7.630
8.600
11.500
10.950
9.700
9.440
8.100
7.840
6.500
5.500
3.880
3.620
2.000
0.000
6.300
7.540
7.800
8.670
8.930
9.700
9.800
10.060
11.300
11.500
PCB LAND PATTERN - 1 (FOR REFERENCE)

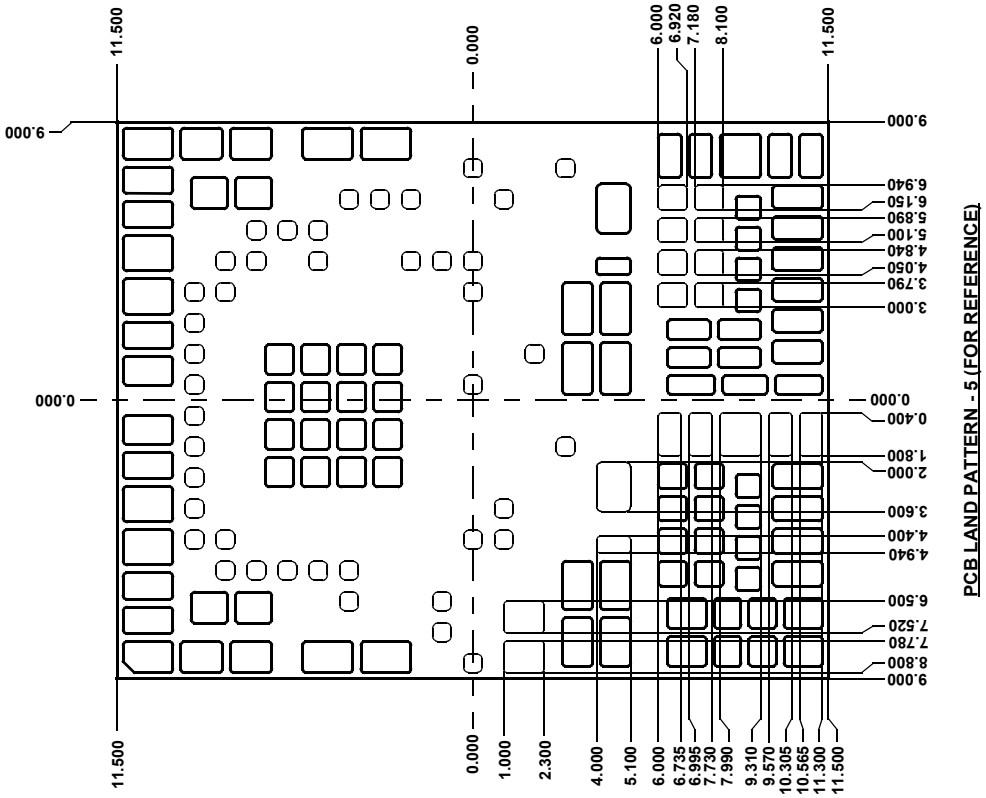

11.500
0.000
6.030
6.890
7.210
8.070
11.500
9.000
6.910
6.180
5.860
5.130
4.810
4.080
3.760
3.030
0.430
0.000
1.770
2.030
3.570
4.430
4.910
6.530
7.490
7.810
8.770
9.000
11.500
0.000
1.030
2.270
4.030
5.070
6.030
6.705
7.025
7.700
8.020
9.280
9.600
10.275
10.595
11.270
11.500
STENCIL OPENING EDGE POSITION - 5

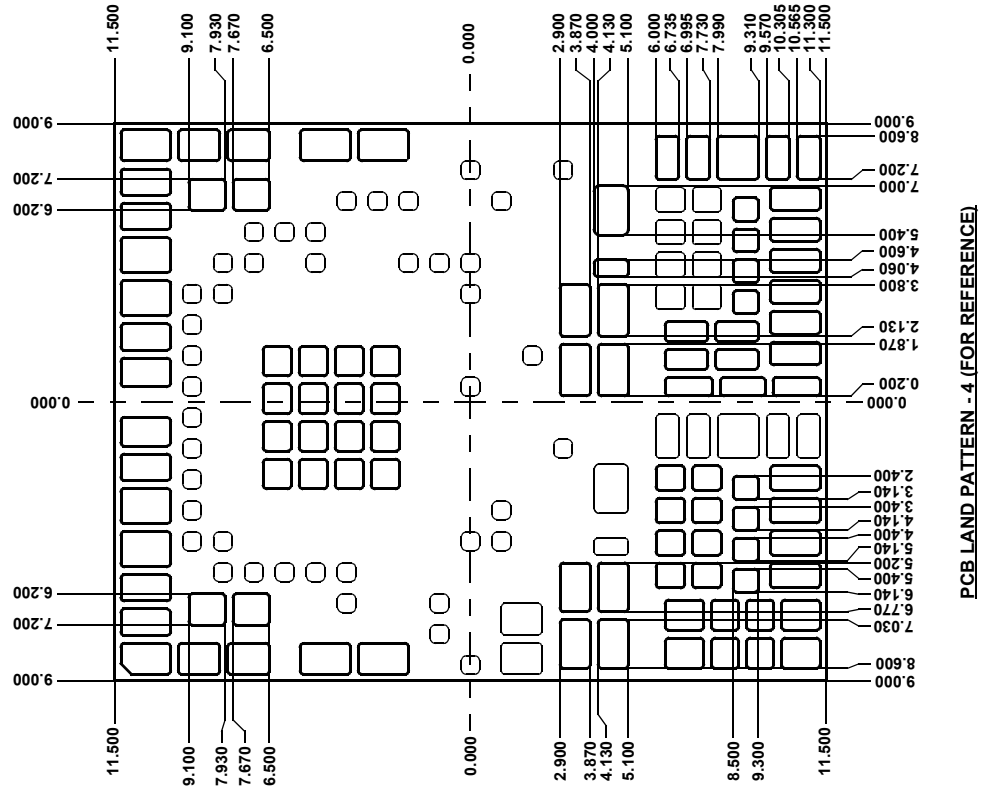


PCB LAND PATTERN - 3 (FOR REFERENCE)



PCB LAND PATTERN - 2 (FOR REFERENCE)


11.500
0.000
6.000
6.920
7.180
8.100
11.500
9.000
6.940
6.150
5.890
5.100
4.840
4.050
3.790
3.000
0.000
0.400
1.800
2.000
3.600
4.400
4.940
6.500
7.520
7.780
8.800
9.000
0.000
11.500
0.000
1.000
2.300
4.000
5.100
6.000
6.735
6.995
7.730
7.990
9.310
9.570
10.305
10.565
11.300
11.500
PCB LAND PATTERN - 5 (FOR REFERENCE)


11.500
9.100
7.930
7.670
6.500
0.000
2.900
3.870
4.000
4.130
5.100
6.000
6.735
6.995
7.730
7.990
9.310
9.570
10.305
10.565
11.300
11.500
9.000
8.600
7.200
7.000
5.400
4.600
4.060
3.800
2.130
1.870
0.200
0.000
2.400
3.140
3.400
4.140
4.400
5.140
5.200
5.400
6.140
6.770
7.030
8.600
9.000
6.200
7.200
9.000
11.500
9.100
7.930
7.670
6.500
0.000
2.900
3.870
4.130
5.100
8.500
9.300
11.500
PCB LAND PATTERN - 4 (FOR REFERENCE)

10. Revision History

Rev.	Date	Description
1.00	Jan 4, 2018	Fixed the note numbering for Table 2 on page 11. Added “ISENSE_CONFIG default setting” to test conditions and updated typical from 0.1 to 0.2 for the Output Current Read Back Resolution specification on page 13. Removed About Intersil section and updated disclaimer.
0.00	Nov 28, 2017	Initial release

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