

# BLC9H10XS-350A

Power LDMOS transistor

Rev. 2 — 13 July 2018

AMMPLÉON

Product data sheet

## 1. Product profile

### 1.1 General description

350 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 617 MHz to 960 MHz.

**Table 1. Typical performance 630 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty test circuit.  $V_{DS} = 50\text{ V}$ ;  $I_{DQ} = 400\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.8\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	617 to 652	50	48	19.5	54.7	-26.7 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01% probability on CCDF.

**Table 2. Typical performance 720 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty demo circuit.  $V_{DS} = 46\text{ V}$ ;  $I_{DQ} = 250\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.5\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	717 to 728	46	47.5	18.9	55.1	-29.6 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01% probability on CCDF.

**Table 3. Typical performance 880 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty production test circuit.  $V_{DS} = 50\text{ V}$ ;  $I_{DQ} = 400\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.55\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	869 to 894	50	48	18.3	54	-31.0 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01% probability on CCDF.

**Table 4. Typical performance 940 MHz**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty test circuit.  $V_{DS} = 50\text{ V}$ ;  $I_{DQ} = 450\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.65\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	50	48	19	53.5	-30.9 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01% probability on CCDF.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internal integrated wideband input matching for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 617 MHz to 960 MHz frequency range

## 2. Pinning information

Table 5. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 6. Ordering information

Type number	Package		
	Name	Description	Version
BLC9H10XS-350A	-	air cavity plastic earless flanged package; 4 leads	SOT1273-1

## 4. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	105	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+11	V

**Table 7. Limiting values ...continued**  
 In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature	[1]	-	225	°C
T <sub>case</sub>	case temperature	operating [1]	-40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

**Table 8. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-c)</sub>	thermal resistance from junction to case	V <sub>DS</sub> = 50 V; I <sub>Dq</sub> = 400 mA (main); V <sub>GS(amp)peak</sub> = 0.55 V; T <sub>case</sub> = 80 °C		
		P <sub>L</sub> = 63 W	0.4	K/W
		P <sub>L</sub> = 80 W	0.384	K/W

## 6. Characteristics

**Table 9. DC characteristics**  
 T<sub>j</sub> = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 1 mA	108	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 100 mA	1.5	2.0	2.5	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 50 V; I <sub>D</sub> = 400 mA	1.71	2.28	2.86	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	1.4	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; V <sub>DS</sub> = 10 V	-	16.5	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	140	nA
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 5 A	-	6.7	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; I <sub>D</sub> = 3.5 A	-	238	300	mΩ
<b>Peak device</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 1.5 mA	108	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 150 mA	1.5	2.0	2.5	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 50 V; I <sub>D</sub> = 600 mA	1.71	2.28	2.86	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	1.4	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; V <sub>DS</sub> = 10 V	-	24.5	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	140	nA
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 7.50 A	-	9.9	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V; I <sub>D</sub> = 5.25 A	-	161	203	mΩ

**Table 10. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH;  $f_1 = 871.5$  MHz;  $f_2 = 891.5$  MHz; RF performance at  $V_{DS} = 50$  V;  $I_{Dq} = 400$  mA (main);  $V_{GS(amp)peak} = 0.55$  V;  $T_{case} = 25$  °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 869 MHz to 894 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 63$ W	17	18.1	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 63$ W	-	-18.2	-11.5	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 63$ W	50	54	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 63$ W	-	-31	-24	dBc

**Table 11. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH;  $f = 891.5$  MHz; RF performance at  $V_{DS} = 50$  V;  $I_{Dq} = 400$  mA (main);  $V_{GS(amp)peak} = 0.55$  V;  $T_{case} = 25$  °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 869 MHz to 894 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$PAR_O$	output peak-to-average ratio	$P_{L(AV)} = 90$ W	5.9	6.6	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)} = 90$ W	343	415	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLC9H10XS-350A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 52$  V;  $I_{Dq} = 400$  mA;  $V_{GS(amp)peak} = 0.55$  V;  $f = 881$  MHz;  $P_L = 140$  W (5 dB OBO); pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

## 7.2 Impedance information

**Table 12. Typical impedance of main device**

Measured load-pull data of main device;  $I_{DQ} = 400$  mA (main);  $V_{DS} = 50$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	$\eta_D$ [2]	G <sub>p</sub> [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(W)	(%)	(dB)
<b>Maximum power load</b>					
600	8.0 – j4.2	3.2 + j1.3	237.9	66.6	17.9
698	5.9 – j3.0	3.1 + j1.2	236.0	68.0	19.0
746	5.1 – j3.8	3.0 + j1.2	240.1	70.1	19.3
769	4.9 – j4.3	2.3 + j1.0	238.9	65.2	18.5
800	4.7 – j5.1	2.3 + j1.0	236.5	67.2	19.2
820	4.7 – j5.6	2.7 + j0.9	234.5	66.7	18.8
869	5.0 – j7.1	2.7 + j0.9	227.8	68.4	19.1
880	5.1 – j7.4	2.7 + j0.9	231.1	69.4	19.0
894	5.3 – j7.8	2.7 + j0.9	228.0	69.6	19.0
925	5.9 – j8.8	2.0 + j0.8	229.4	66.8	18.2
942	6.4 – j9.5	2.9 + j0.1	231.6	63.2	17.7
960	6.9 – j10.0	2.9 + j0.1	232.3	63.9	17.6
<b>Maximum drain efficiency load</b>					
600	7.9 – j3.4	2.7 + j4.5	129.7	79.0	20.9
698	5.7 – j2.8	2.9 + j3.1	176.3	76.7	20.9
746	4.7 – j3.6	2.2 + j3.6	136.9	78.9	21.8
769	4.6 – j4.2	2.1 + j3.6	131.0	78.1	21.6
800	4.5 – j4.9	2.2 + j2.6	173.6	77.3	21.3
820	4.5 – j5.5	2.5 + j2.9	158.2	76.0	21.2
869	4.8 – j7.0	2.6 + j3.0	148.0	75.4	21.4
880	4.9 – j7.2	1.9 + j2.4	160.4	77.3	20.8
894	5.1 – j7.6	1.9 + j2.5	152.3	76.3	21.0
925	5.5 – j8.3	1.9 + j2.5	151.9	79.4	21.0
942	6.0 – j9.2	2.0 + j2.5	145.7	79.1	21.0
960	6.5 – j9.7	2.0 + j2.5	140.4	78.3	20.9

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.

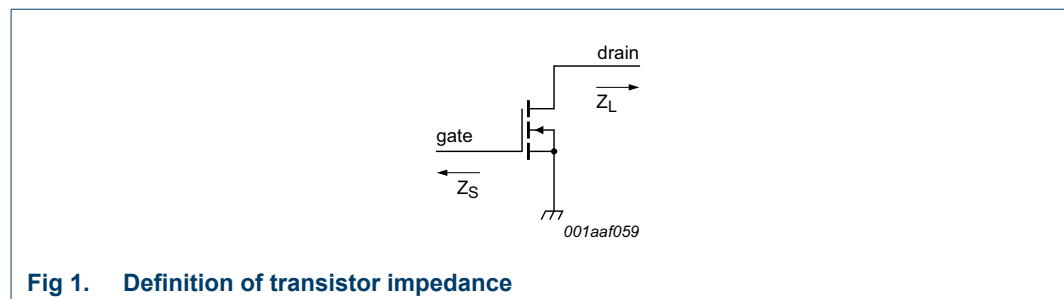
**Table 13. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{Dq} = 600 \text{ mA}$  (peak);  $V_{DS} = 50 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f	$Z_S$ [1]	$Z_L$ [1]	$P_L$ [2]	$\eta_D$ [2]	$G_p$ [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(W)	(%)	(dB)
<b>Maximum power load</b>					
600	5.8 – j1.8	2.6 + j0.4	360.7	69.0	19.0
698	3.7 – j2.3	2.0 + j0.2	347.3	65.0	19.4
746	3.4 – j3.2	2.0 + j0.2	361.1	69.0	19.6
769	3.4 – j3.7	1.9 + j0.3	358.3	70.5	19.5
800	3.5 – j4.3	2.0 – j0.3	352.1	64.0	19.1
820	3.5 – j4.3	2.0 – j0.1	349.2	66.0	19.0
869	3.6 – j4.7	2.0 + j0.0	347.3	67.0	18.8
880	4.4 – j5.8	2.0 + j0.0	335.5	69.5	19.1
925	5.2 – j6.5	2.0 – j0.7	329.7	60.9	17.9
942	6.1 – j6.9	2.0 – j0.7	337.1	62.8	17.9
960	6.7 – j6.9	2.0 – j0.7	338.1	63.4	17.8
<b>Maximum drain efficiency load</b>					
600	5.5 – j1.4	2.3 + j2.7	224.5	80.6	21.6
698	3.6 – j2.2	2.2 + j1.6	270.9	76.6	21.4
746	3.2 – j3.1	1.8 + j2.2	202.8	78.9	22.4
769	3.3 – j3.5	2.1 + j1.6	249.6	77.9	21.6
800	3.3 – j4.0	1.6 + j1.4	240.2	77.3	22.0
820	3.2 – j4.1	1.4 + j1.9	182.7	78.4	22.5
869	3.5 – j4.5	1.7 + j1.4	246.3	77.6	21.1
880	4.2 – j5.6	1.7 + j1.4	213.8	76.3	21.4
925	4.9 – j6.1	1.2 + j1.2	186.7	74.6	21.4
942	5.7 – j6.4	1.2 + j1.2	177.3	77.4	21.8
960	6.5 – j6.6	1.4 + j0.7	247.8	77.2	20.5

[1]  $Z_S$  and  $Z_L$  defined in Figure 1.

[2] At 3 dB gain compression.



**Fig 1. Definition of transistor impedance**

### 7.3 Recommended impedances for Doherty design

**Table 14. Typical impedance of main at 1 : 1 load**

Measured load-pull data of main device;  $I_{DQ} = 400 \text{ mA}$  (main);  $V_{DS} = 50 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L(3dB)</sub> (dBm)	η <sub>D</sub> [2] (%)	G <sub>p</sub> [2] (dB)
600	8.0 – j4.2	3.1 + j2.1	53.6	40.7	21.6
698	5.9 – j3.0	3.1 + j1.9	53.5	40.1	22.4
746	5.1 – j3.8	2.8 + j1.9	53.5	41.3	22.7
769	4.9 – j4.3	2.6 + j1.8	53.5	40.1	22.7
800	4.7 – j5.1	2.7 + j1.5	53.6	41.0	22.8
820	4.7 – j5.6	2.7 + j1.5	53.5	41.5	22.6
869	5.0 – j7.1	2.8 + j1.2	53.5	42.9	22.7
880	5.1 – j7.4	2.8 + j1.2	53.5	42.6	22.6
894	5.3 – j7.8	2.8 + j1.2	53.5	43.2	22.6
925	5.9 – j8.8	2.5 + j1.2	53.5	43.5	22.6
942	6.4 – j9.5	2.5 + j1.2	53.5	43.6	22.6
960	6.9 – j10.0	2.5 + j1.2	53.5	42.7	22.5

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At P<sub>L(AV)</sub> = 63 W.

**Table 15. Typical impedance of main device at 1 : 2.5 load**

Measured load-pull data of main device;  $I_{DQ} = 400 \text{ mA}$  (main);  $V_{DS} = 50 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L(3dB)</sub> (dBm)	η <sub>D</sub> [2] (%)	G <sub>p</sub> [2] (dB)
600	7.9 – j3.4	3.0 + j4.9	50.7	60.9	24.1
698	5.7 – j2.8	3.1 + j4.9	50.6	59.5	24.9
746	4.7 – j3.6	2.9 + j4.6	50.5	61.3	25.1
769	4.6 – j4.2	2.7 + j4.2	50.7	60.7	24.7
800	4.5 – j4.9	2.5 + j3.9	50.7	61.2	25.4
820	4.5 – j5.5	2.5 + j3.9	50.6	62.5	24.9
869	4.8 – j7.0	2.5 + j3.9	50.5	62.4	24.9
880	4.9 – j7.2	2.5 + j3.9	50.4	61.6	24.9
894	5.1 – j7.6	2.5 + j3.9	50.3	61.7	24.8
925	5.5 – j8.3	2.3 + j3.6	50.4	62.9	25.1
942	6.0 – j9.2	2.2 + j3.4	50.4	63.4	25.1
960	6.5 – j9.7	2.1 + j3.4	50.4	63.2	24.5

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At P<sub>L(AV)</sub> = 63 W.

**Table 16. Typical impedance of peak device at 1 : 1 load**

Measured load-pull data of peak device;  $I_{Dq} = 600$  mA (peak);  $V_{DS} = 50$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L(3dB)</sub>	$\eta_D$ [2]	G <sub>p</sub> [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(dBm)	(%)	(dB)
600	5.8 – j1.8	2.6 + j1.1	55.3	35.0	22.9
698	3.7 – j2.3	2.3 + j0.8	55.2	34.8	23.3
720	3.4 – j3.2	2.3 + j0.8	55.2	35.0	23.4
769	3.4 – j4.3	2.3 + j0.5	55.2	34.4	23.1
800	3.5 – j4.4	2.1 + j0.5	55.2	34.7	23.5
820	3.5 – j4.7	2.1 + j0.6	55.2	34.5	22.7
869	3.6 – j5.8	1.9 + j0.2	55.2	35.4	22.9
880	4.4 – j5.9	1.9 + j0.3	55.2	35.8	23.0
894	4.4 – j6.5	1.8 + j0.3	55.2	35.1	22.8
925	5.2 – j6.9	1.7 + j0.1	55.2	34.2	22.5
942	6.1 – j6.9	1.7 + j0.0	55.2	35.0	22.7
960	6.7 – j6.9	1.7 + j0.0	55.2	35.8	22.7

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

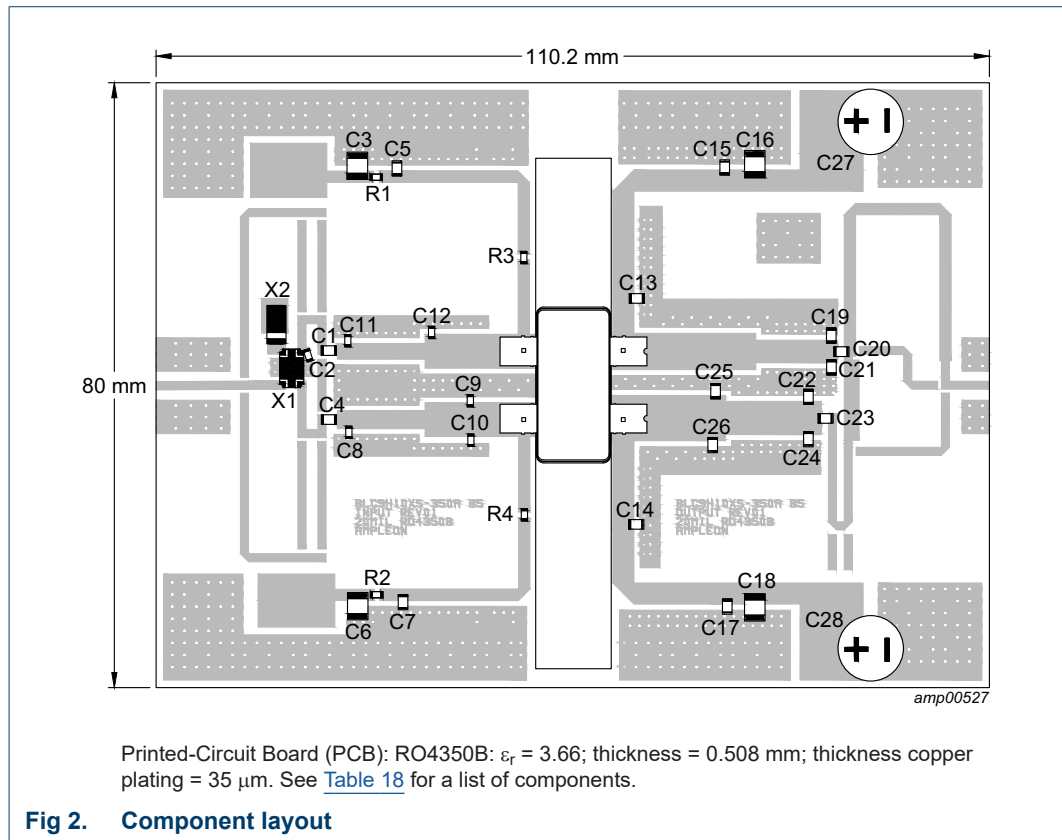
[2] At P<sub>L(AV)</sub> = 63 W.

**Table 17. Off-state impedances of peak device**

f	Z <sub>off</sub>
(MHz)	( $\Omega$ )
600	0.15 – j5.79
698	0.15 – j4.54
720	0.14 – j4.32
769	0.12 – j3.91
800	0.10 – j3.45
820	0.10 – j3.37
869	0.10 – j2.88
880	0.10 – j2.86
894	0.09 – j2.70
925	0.09 – j2.56
942	0.09 – j2.42
960	0.09 – j2.27



7.4 Test circuit

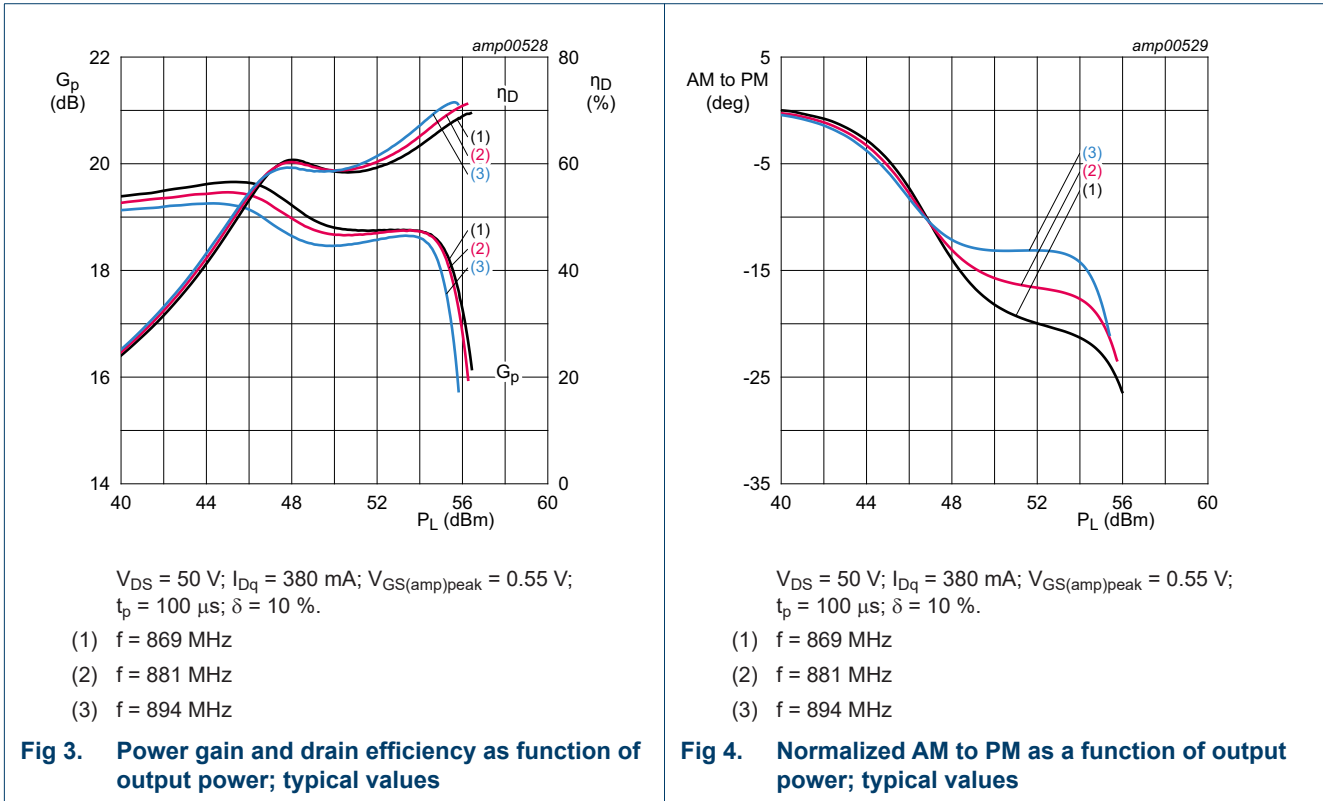


**Table 18. List of components**  
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C4, C5, C7, C15, C17, C23	multilayer ceramic chip capacitor	100 pF	Murata: Hi-Q SMD 0805
C2, C8	multilayer ceramic chip capacitor	2.0 pF	
C3, C6, C16, C18	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$	Murata: GRM32ER71H475KA88L
C9, C10, C12	multilayer ceramic chip capacitor	4.3 pF	
C11	multilayer ceramic chip capacitor	2.7 pF	
C13, C14	multilayer ceramic chip capacitor	47 pF	
C19	multilayer ceramic chip capacitor	3.3 pF	
C20	multilayer ceramic chip capacitor	22 pF	
C21	multilayer ceramic chip capacitor	3.0 pF	
C22, C24	multilayer ceramic chip capacitor	2.4 pF	
C25	multilayer ceramic chip capacitor	6.8 pF	
C26	multilayer ceramic chip capacitor	5.6 pF	
C27, C28	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	
R1, R2, R3, R4	resistor	4.7 $\Omega$ , 1 %	SMD 0805
X1	hybrid coupler	3 dB	Anaren: X3C07F1-02S
X2	termination	50 $\Omega$	Anaren: C16A50Z4

7.5 Graphical data

7.5.1 Pulsed CW



7.5.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping): PAR = 9.6 dB at 0.01 % probability on CCDF.

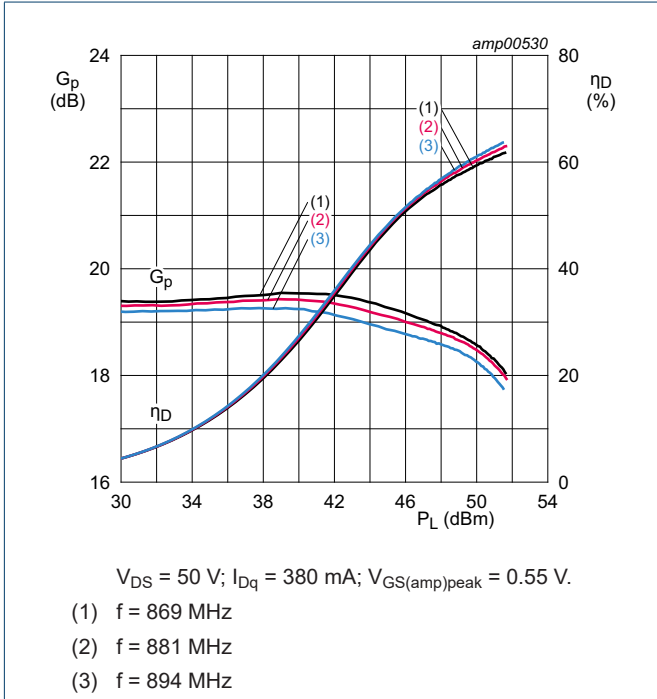


Fig 5. Power gain and drain efficiency as function of output power; typical values

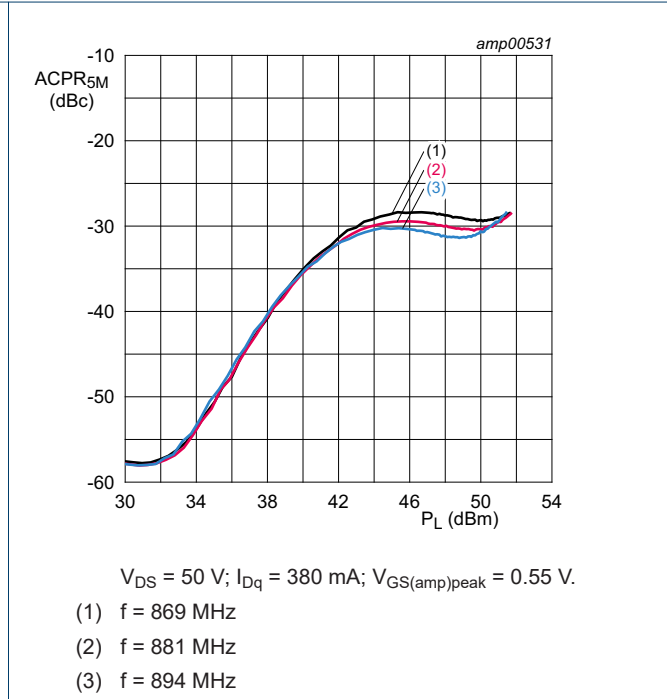


Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

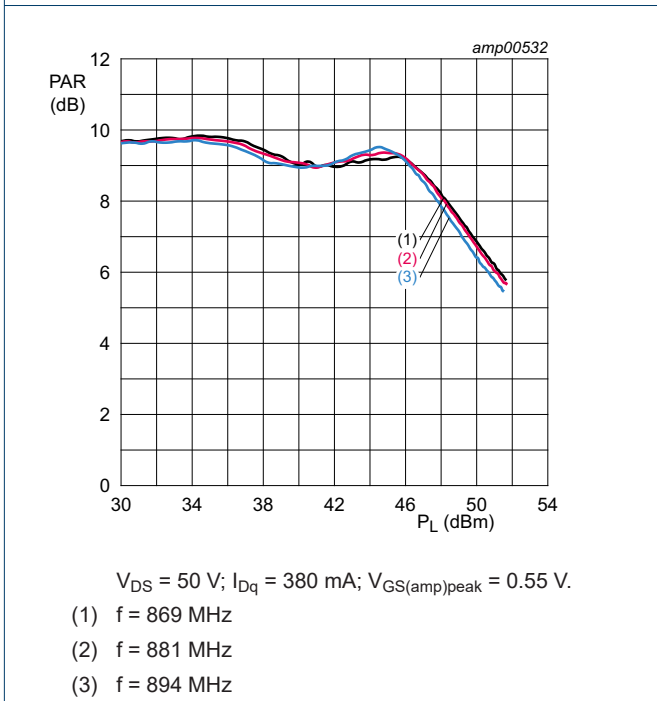


Fig 7. Peak-to-average power ratio as a function of output power; typical values

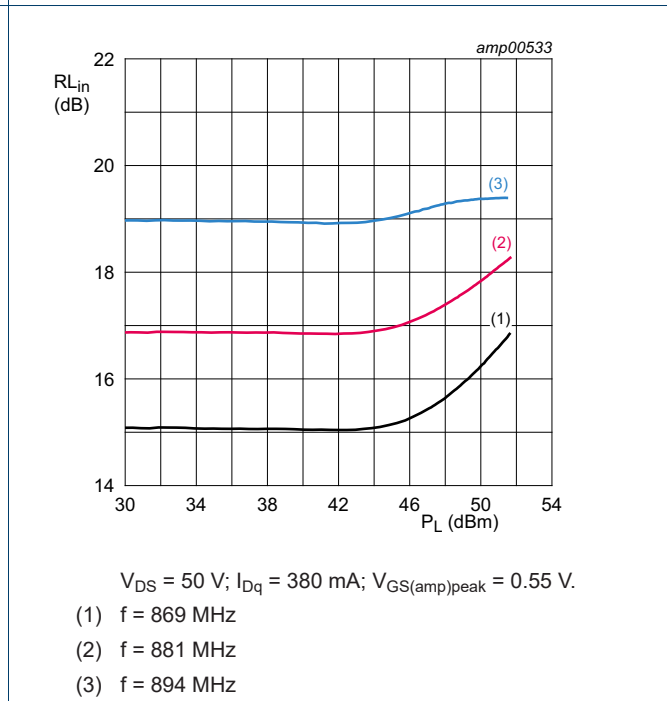
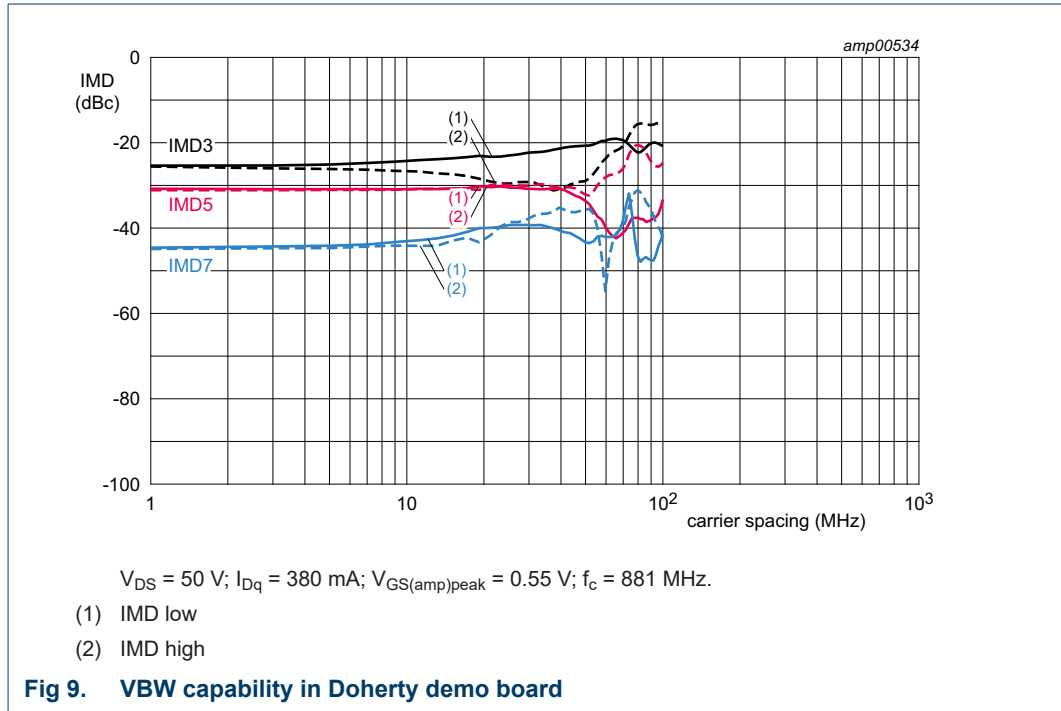


Fig 8. Input return loss as a function of output power; typical values

7.5.3 2-Tone VBW



8. Package outline

Air cavity plastic earless flanged package; 4 leads

SOT1273-1

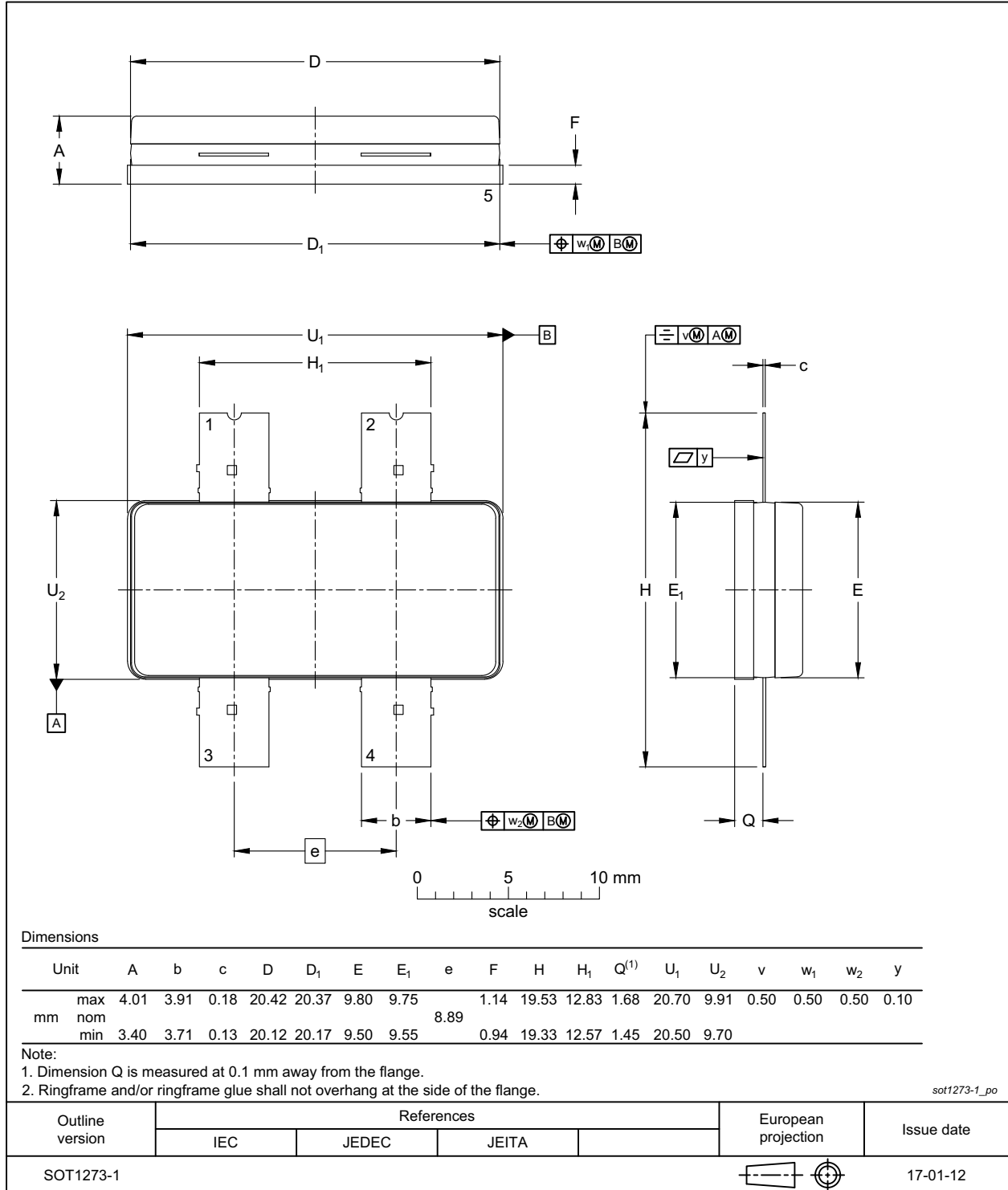



Fig 10. Package outline SOT1273-1

## 9. Handling information

CAUTION	
	<p>This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.</p> <p>Such precautions are described in the <i>ANSI/ESD S20.20</i>, <i>IEC/ST 61340-5</i>, <i>JESD625-A</i> or equivalent standards.</p>

**Table 19. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 <sup>[1]</sup>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <sup>[2]</sup>

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of  $\geq 1000$  V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 20. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
OBO	Output Back Off
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 21. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9H10XS-350A v.2	20180713	Product data sheet	-	BLC9H10XS-350A v.1
Modifications	<ul style="list-style-type: none"> <li>• <a href="#">Section 1.1 on page 1</a>: changed value PAR</li> <li>• <a href="#">Table 8 on page 3</a>: changed conditions P<sub>L</sub></li> <li>• <a href="#">Table 10 on page 4</a>: changed description</li> <li>• <a href="#">Table 11 on page 4</a>: changed description</li> <li>• <a href="#">Section 7.3 on page 7</a>: changed unit of P<sub>L(3dB)</sub></li> </ul>			
BLC9H10XS-350A v.1	20180518	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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