News & Views
Second Quarter, May 2000
Newsletter for Altera Customers

Altera Announces the Nios Processor for Embedded Systems Development

Altera is a leader in providing the key elements required for successful system-on-a-programmable-chip (SOPC) designs, including high performance, full-featured devices, integrated development tools, and a comprehensive portfolio of intellectual property (IP). Recognizing the importance of microprocessors in SOC designs, Altera has established itself as the preeminent source of processor IP through strong partnerships with industry leaders. Altera now enhances this processor IP selection with Excalibur™ embedded processor programmable logic device (PLD) solutions. Consisting of both hard and soft core technologies that integrate RISC processors into PLDs, the Excalibur embedded processor solutions offer the widest range of capabilities and the high performance of dedicated hardware implementation. With the introduction of the Excalibur embedded processor PLD solutions, designers can reap all the benefits of SOPC design.

Advantages of SOPC

The strengths of SOC design include higher integration and increased system performance. SOPC designs add additional benefits such as programmability and fast time-to-market, with the flexibility of PLDs. With these programmable devices, a designer can implement several different iterations of a system in hardware in a fraction of the time required to implement a custom component version. This flexibility allows designers to not only develop a product in a shorter amount of time, but to explore different system architectures and feature sets to deliver the best possible combination in their product. By fully integrating the processor into the PLD design flow, the Excalibur solutions give system designers unprecedented freedom to determine which functions should be executed in software and which would benefit the most from dedicated hardware implementation.

Excalibur Solutions

The Altera Excalibur solutions consist of the following families:

- The Nios™ family of soft core embedded processors—a configurable 16- or 32-bit embedded RISC processor
- The ARM®-based embedded processor family—an ARM9 Thumb® embedded processor core with 32-bit architecture and a 32-bit RISC engine
- The MIPS-based® embedded processor family—a MIPS 4Kc™ embedded processor core with 32-bit architecture and R4000™ TLB and privileged-mode extensions.

The first Excalibur embedded processor PLD solution is the Nios family, a 16- or 32-bit embedded RISC soft core processor that is easily configured to meet several different demands, and rapidly integrated into any Altera-based design. Although the Nios embedded processors are initially optimized for APEX™ devices, they

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Introducing the Excalibur Development Kit Featuring Nios

The Development Kit that Gets You on the Cutting Edge

The Nios™ soft core embedded processor, the first of Altera's new Excalibur™ embedded processor solutions to ship, delivers just what you need to create system-on-a-programmable-chip (SOPC) designs.

EXCALIBUR™

This new flexible embedded processor solution offers a 32-bit configuration, up to 50 MIPS performance, and an equivalent volume price point of $5. The development kit is available now with everything you need to get started.

A Complete Solution for Only $995

This Excalibur Development Kit contains:

- Nios Configurable RISC Embedded Processor Core and Peripherals
- Quartus™ Programmable Logic Development Software
- GNUPro® C/C++ Compiler and Debugger from Cygnus®, a Red Hat® Company
- ByteBlasterMV™ Download Cable
- Development Board Including an APEX™ EP20K200E Device
- Reference Design and Documentation

Free Hands-on Workshops

Intensive three-hour workshops, starting in June, will teach you how to create an SOPC design using the Nios soft core embedded processor in an APEX device. You will develop and compile C code, then execute and troubleshoot it on the development board. You will also learn about the GNUPro Compiler and Debugger from Cygnus, a Red Hat company, included in the Excalibur Development Kit.

Register Now!

To reserve your space at the **FREE** Excalibur workshop nearest you, or to find out more about this revolutionary development system, visit Altera's web site at **http://www.altera.com/workshop**.

Win a Free Excalibur Development Kit!

Each workshop will feature a drawing for a free Excalibur Development Kit. You must be present to win, so sign up today.

ALTERA®

The Programmable Solutions Company®

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will also be available for other Altera device architectures, including ACEX™ devices for low-cost implementations and future device families for enhanced performance. The hard core Excalibur solutions are based on ARM and MIPS Technologies, Inc. processors. They are implemented in Altera's APEX architecture, and will provide high-performance, embedded peripherals within royalty-free, off-the-shelf products. The Excalibur solutions are ideal for many embedded applications, including computer peripherals, industrial and automotive control, image processing, set-top boxes, and other communications applications. Figure 1 shows the families of the Excalibur embedded processor solution and their relative performance levels. Figure 2 shows the roadmap for future Nios embedded processors.

Figure 1. Excalibur Embedded Processor Solutions

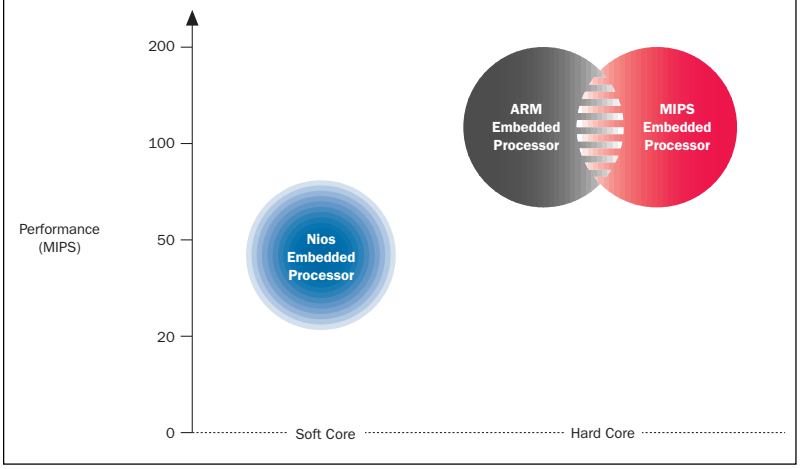


Figure 2. Nios Roadmap

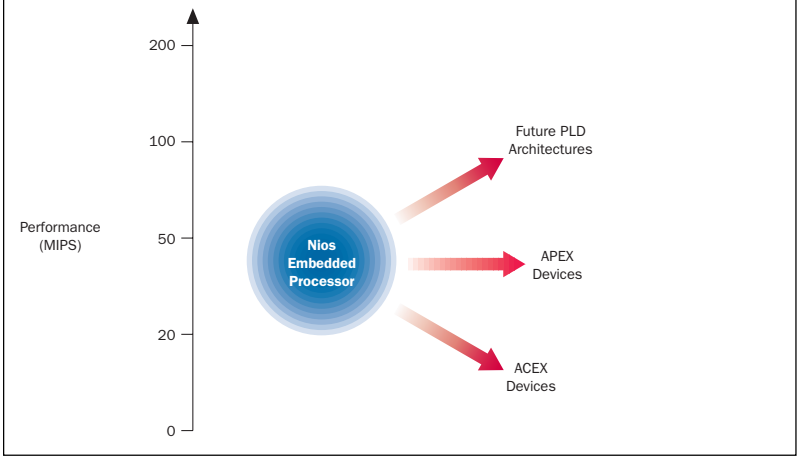


Table 1. Nios Configurations & Resource Usage in an EP20K100E Device

Nios Configuration	Data Width	Address Width	% of Total LEs	% of Total ESBs *(1)*	MHz	Cost of Implementation
16 bit	16	16	25	8 to 40	50	$10
32 bit	32	32	33	15 to 77	48	$13

Note:
(1) Based on register file size.

The Nios Family of Configurable Soft Core Embedded Processors

The Nios family of embedded processors is the first 16- or 32-bit processor core to be designed specifically for programmable logic implementation, and as a result, can perform at speeds up to 50 million instructions per second (MIPS). Designed with a five-stage pipeline that executes one instruction per clock cycle, the Nios family is also user-configurable for meeting different embedded design needs, supporting a 16- or 32-bit data width and a register file depth ranging from 32 to 512 general-purpose registers (for more information on the Nios architecture, see on page 20). Besides performance and configurability, Nios processors are also optimized for PLD resource efficiency, resulting in a lower-cost implementation than most off-the-shelf processors. Nios can be configured in many ways to suit different applications. Table 1 illustrates two Nios configurations, their speed and resource utilizations, and resulting costs.

Nios Development Environment

The Nios processor is more than the latest generation of processor IP optimized for programmable logic. Altera also provides all the elements necessary for a designer to develop a Nios-based system. Nios users can integrate the Nios embedded processor into their Altera designs with the MegaWizard® Plug-In. The MegaWizard Plug-In is a menu-driven application that allows users to specify the parameters they desire for their Nios embedded processor. Based on those parameters, the MegaWizard Plug-In Manager generates a netlist description of the specific Nios embedded processor that can be integrated into any Altera design via the Quartus™ development system.

Several peripherals are also available for use with the Nios family of embedded processors, including a universal asynchronous receiver/transmitter (UART), a timer/counter, a memory controller (SRAM, ROM, and FLASH), and a parallel I/O (PIO) module. Any of these can be easily integrated into a user's design along with their unique Nios configuration. For coding support, Altera has partnered with Cygnus®, a Red Hat® company, to provide the powerful yet familiar GNU®-based C/C++ compiler and assembler. A source-level debugger accesses the device through a serial port, providing run control and access to the memory and register file. Figure 3 shows the development flow for the Excalibur embedded processor PLD solution.

Excalibur Development Kit, Featuring Nios

To support the Nios family of soft core embedded processors, Altera offers the Excalibur Development Kit, featuring the Nios embedded processor, which contains all the software and hardware components a designer needs to begin using the Nios embedded processor immediately. The kit includes the following items:

- Nios soft-core embedded processor
- C/C++ compiler, assembler, debugger, and documentation
- Nios peripherals (UART, memory interface, timer/counter, and PIO module)
- Quartus development software (supports APEX devices and SignalTap™ embedded logic analysis)
- ByteBlasterMV™ download cable
- Development board (including an APEX EP20K200E device, SRAM/FLASH, expansion/prototype connectors, and processor trace port)
- Software drivers (UART, timer/counter, and PIO module)
- SOPC reference design
- Nios user manual and programmer reference manual

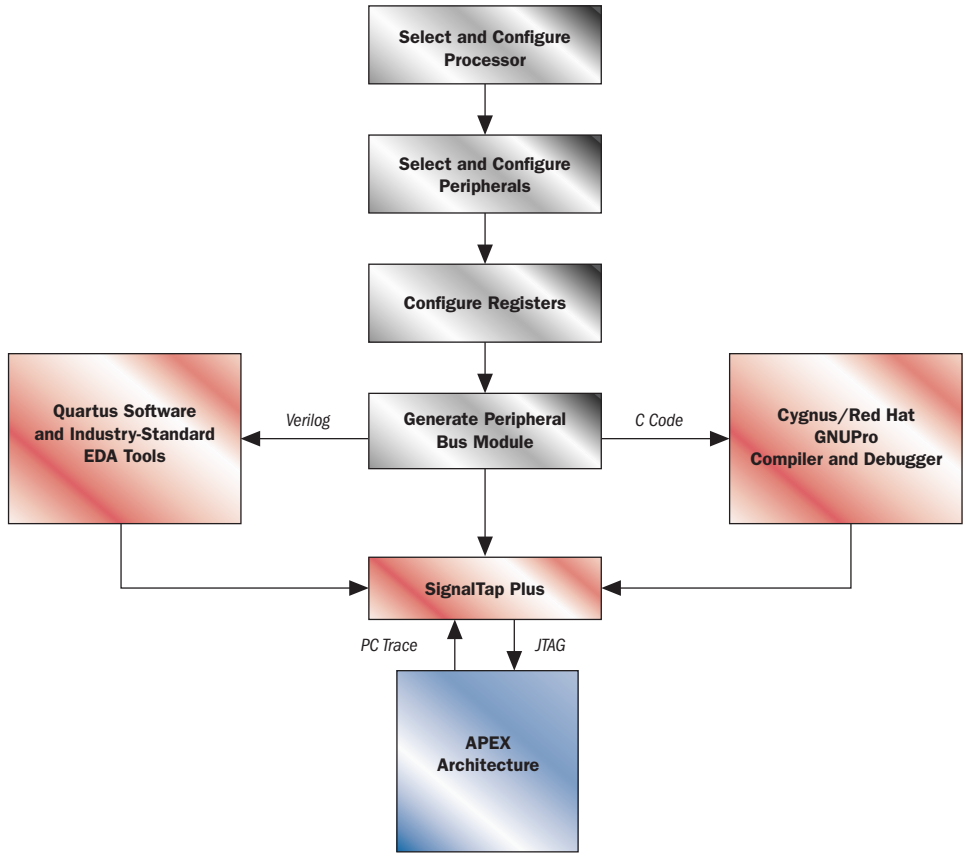
EXCALIBUR™

Nios™

ARM® POWERED

MIPS TECHNOLOGIES

Figure 3. Excalibur Workflow Simplifies SOPC Designs



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Licensing and Availability

The Nios embedded processor is the first member of the Excalibur solutions and is available now. The ARM- and MIPS-based members of the Excalibur family will be available as royalty-free standard products in the fourth quarter of 2000. Designers can use the Nios embedded processor to develop Nios-based designs free of charge. Products that ship with the Nios embedded processor are subject to a zero-cost license which is available on-line at the Altera web site (**http://www.altera.com**). The Excalibur Development Kit is now available and contains information on obtaining a product license. You can also contact your local Altera sales office or representative or visit Altera's web site. For more detailed information on developing with the Nios family, attend one of the free Nios workshops scheduled worldwide (see "Sign Up Now for Free Excalibur Workshops" below for more information).

Altera & Red Hat Form Partnership to Provide Development Software for Nios

Nios™

Altera and Red Hat®, Inc. worked together to provide Altera users with a powerful and complete software development environment for the Nios™ family of soft core embedded processors. Through close collaboration, they created a suite of the GNUPro® embedded system tools, including a C/C++ compiler, assembler and debugger, specifically optimized to support the Nios instruction set. This suite of tools from Cygnus®, a Red Hat® company, is included in the Excalibur™ Development Kit, along with all the other components needed to begin using the Nios embedded processor immediately.

"Our work with Red Hat signifies our commitment to deliver a robust and open development platform for embedded systems designers," said Cliff Tong, VP of Corporate Marketing. "With the Excalibur Development Kit featuring the Nios embedded processor, Altera provides a valuable integrated platform for hardware and software codevelopment."

"Cygnus and Red Hat are well known in the embedded systems industry as one of the most highly-respected providers of tools and operating systems," added Mike Phipps, Director of Marketing at Altera. "With Red Hat's backing, our users get familiar and dependable tools that are fully supported, tested and certified."

Altera and Red Hat will continue their future support of the Nios embedded processor with a port of eCos, the embedded configurable real time operating system.

APEX

Eight APEX 20KE Devices Now Shipping

Four more APEX™ 20KE devices have been released, making a total of eight APEX 20KE devices now shipping: EP20K60E, EP20K100E, EP20K200E, EP20K300E, EP20K400E, EP20K600E, EP20K1000E, and EP20K1500E devices. These devices are available in many advanced packages, including FineLine BGA™ packages. The remaining APEX 20KE devices are scheduled to ship in the third quarter of 2000. Software support is currently available in the Quartus™ software version 2000.05 for all devices except the EP20K30E device (see Table 1).

True-LVDS Support in APEX 20KE Devices

Altera® APEX 20KE devices now offer the True-LVDS™ solution with a data transfer rate up to 840 megabits per second (Mbps) per channel. This specification exceeds the widely accepted low-voltage differential signaling (LVDS) standard data transfer rate of 624 Mbps. The APEX 20KE programmable LVDS bandwidth is now 26.8 gigabits per second (Gbps).

5.0-V Tolerant APEX 20K & APEX 20KE Devices

The APEX 20K device family has been enhanced to provide a 5.0-V tolerant I/O buffer, providing full compliance with the 5.0-V peripheral component interconnect (PCI) specification. These 5.0-V tolerant devices are now shipping.

You can use APEX 20KE devices with an additional external resistor to make these devices 5.0-V tolerant and provide flexibility for system design. The technical details for this improvement are described in the *5.0-V Tolerance in APEX 20KE Devices White Paper* on the Altera web site (**http://www.altera.com**).

Table 1. APEX 20KE Device & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K30E	144-pin TQFP *(1)*	Q3 2000
	144-pin FineLine BGA	Q3 2000
	208-pin PQFP *(1)*	Q3 2000
	324-pin FineLine BGA	Q3 2000
EP20K60E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA *(1)*	Now
EP20K100E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	Now
EP20K160E	144-pin TQFP	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K200E	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K300E	240-pin RQFP *(1)*	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K400E	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1500E	652-pin BGA	Now
	1,020-pin FineLine BGA	Now

Note:
(1) TQFP: thin quad flat pack, PQFP: plastic quad flat pack, BGA: ball-grid array, RQFP: power quad flat pack

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APEX 20K Product Transition

Altera is migrating the 2.5-V EP20K400 device from a 0.25-µm process to a 0.22-µm process. Information regarding this device migration can be found in process change notification (PCN) 0005, available on the Altera web site.

ACEX

ACEX 1K Devices Shipping Now

ACEX 1K devices are now shipping in all packages in the 30,000, 50,000, and 100,000 gate densities.

ACEX™ 1K devices are now shipping in all packages in the 30,000, 50,000, and 100,000 gate densities (see Table 2). These cost-optimized devices are especially well suited for low-cost, high-performance communications applications, and can be used to attain the lowest cost per programmable logic device (PLD) for high-volume designs.

Table 2. ACEX 1K Device Offerings

Device	Package	Availability
EP1K10	100-pin TQFP	August 2000
	144-pin TQFP	August 2000
	208-pin PQFP	August 2000
	256-pin FineLine BGA	August 2000
EP1K30	144-pin TQPF	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
EP1K50	144-pin TQFP	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now
EP1K100	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now

ACEX 1K devices provide full phase-locked loop (PLL) capability for ClockLock™ and ClockBoost™ features in every -1 and -2 speed grade device, embedded dual-port RAM, and full 64-bit, 66-MHz PCI compliance. Developed on an innovative 0.22-µm/0.18-µm hybrid process, and featuring a 2.5-V core operating voltage, ACEX 1K devices offer an ideal combination of cost, performance, and features.

Full software support for ACEX 1K devices is available from the MAX+PLUS® II software version 9.6. In addition, a wide range of ACEX-optimized intellectual property (IP) functions can now be found at the Altera IP MegaStore™ online store.

ACEX 2K Devices Coming Soon

The 1.8-V ACEX 2K device family will be released soon. These devices range from 20,000 to 150,000 typical gates and provide additional benefits in cost and performance for high-volume communications designs. These devices also offer a feature set that includes enhanced PLL capabilities, advanced I/O standard support, and dual-port embedded RAM. ACEX 2K device support will be available from the Quartus software in the second half of 2000.

FLEX

All FLEX 10KE Devices Available

All EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices are now shipping in -1, -2, and -3 speed grades. These devices are fabricated on a 0.22-µm process and have a programmable input buffer delay for full 64-bit, 66-MHz PCI compliance.

FLEX® 10KE devices are offered with the PLL feature in -1 and -2 speed grades to reduce clock skew and allow clock multiplication. These devices have an "X" suffix in the ordering code (e.g., EPF10K100EQC208-1X). To assist designers in implementing their projects in FLEX 10KE devices, the MAX+PLUS II software offers design support for all device package options. Table 3 shows all of the 2.5-V FLEX 10KE device packages and speed grades.

FLEX 10K Product Transitions

2.5-V EPF10K50E and EPF10K200E devices have migrated from a 0.25-µm process to a 0.22-µm process. All other members of the FLEX 10KE family are already manufactured on a 0.22-µm process. EPF10K50V devices are migrating from a 0.30-µm, 3-layer-metal

Table 3. FLEX 10KE Devices

Device	Offerings	Speed Grade
EPF10K30E	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K50S	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K100E	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K130E	240-pin PQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K200S	240-pin RQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X

process to a 0.30-µm, 4-layer-metal process in September 2000. Table 4 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com.**

FLEX 10KE Industrial-Temperature Devices

All FLEX 10KE devices are now available in industrial-temperature grades. Table 5 lists the industrial-temperature FLEX 10KE devices.

Table 4. FLEX 10K Device Migration

Device	Core Voltage (V)	Date	Reference	Process (µm)
EPF10K10A	3.3	Done	PCN 9810	0.30
EPF10K30A	3.3	Done	PCN 9810	0.30
EPF10K50V	3.3	Done	PCN 9810	0.30 *(1)*
		Sept. 2000	PCN 9915	0.30 *(2)*
EPF10K100A	3.3	Done	PCN 9810	0.30
EPF10K10	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K20	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K30	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50E	2.5	Done	PCN 9911	0.22
EPF10K200E	2.5	Done	PCN 9911	0.22

Notes:
(1) 3-layer metal process.
(2) 4-layer metal process.

Table 5. FLEX 10KE Industrial-Temperature Device Availability

Device	Availability
EPF10K30EQI208-2	Now
EPF10K30EFI256-2	Now
EPF10K50ETI144-2	Now
EPF10K50EQI240-2	Now
EPF10K50EFI256-2	Now
EPF10K50SQI208-2	Now
EPF10K50SBI356-2	Now
EPF10K50SFI484-2	Now
EPF10K100EQI208-2	Now
EPF10K100EFI256-2	Now
EPF10K100EFI484-2	Now
EPF10K130EQI240-2	Now
EPF10K130EBI356-2	Now
EPF10K130EFI484-2	Now
EPF10K200EBI600-2	Now
EPF10K200SRI240-2	Now
EPF10K200SBI356-2	Now
EPF10K200SFI672-2	Now

All FLEX 10KE devices are now available in industrial-temperature grades.

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MAX

MAX 7000A Devices

The feature-rich MAX® 7000A devices support enhanced in-system programmability (ISP), MultiVolt™ I/O pins, hot-socketing capability and pin compatibility with the industry-standard MAX 7000 devices. 3.3-V MAX 7000A devices range from 32 to 512 macrocells with propagation delays as fast as 4.5 ns. All MAX 7000A devices are available in industrial-temperature grades. Table 6 shows MAX 7000A device commercial package and speed-grade options.

MAX 7000B devices feature enhanced ISP, MultiVolt I/O pins, and pin compatibility with the industry standard MAX 7000 devices.

Table 6. MAX 7000AE Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032AE	44-pin PLCC *(1)*	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM7064AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	49-pin Ultra FineLine BGA *(2)*	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
EPM7128AE	84-pin PLCC	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	100-pin PQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7256AE	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512AE	144-pin TQFP	-5, -7, -10, -12
	208-pin PQFP	-5, -7, -10, -12
	256-pin BGA	-5, -7, -10, -12
	256-pin FineLine BGA	-5, -7, -10, -12

Notes:
(1) PLCC: plastic J-lead chip carrier.
(2) Ultra FineLine BGA packages are Altera's 0.8-mm pitch BGA packages.

MAX 7000B Devices Support Advanced I/O Standards

With support for advanced I/O standards such as Gunning transceiver logic plus (GTL+) and stub-series terminated logic for 2.5 V (SSTL-2) and 3.3-V SSTL-3, MAX 7000B devices offer a flexible solution to design requirements. 2.5-V MAX 7000B devices range from 32 to 512 macrocells with propagation delays as fast as 3.5 ns. Additionally, MAX 7000B devices feature enhanced ISP, MultiVolt I/O pins, and pin compatibility with the industry-standard MAX 7000 devices. Table 7 shows all commercial package and speed grade options. Contact your Altera sales representative for device availability.

Table 7. MAX 7000B Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA *(1)*	-3, -5, -7
EPM7064B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA	-3, -5, -7
	100-pin TQFP	-3, -5, -7
	100-pin FineLine BGA	-3, -5, -7
EPM7128B	49-pin Ultra FineLine BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
	144-pin TQFP	-4, -7, -10
	169-pin Ultra FineLine BGA	-4, -7, -10
	256-pin FineLine BGA	-4, -7, -10
EPM7256B	100-pin TQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512B	100-pin TQFP	-5, -6, -7, -10
	144-pin TQFP	-5, -6, -7, -10
	169-pin Ultra FineLine BGA	-5, -6, -7, -10
	208-pin PQFP	-5, -6, -7, -10
	256-pin BGA	-5, -6, -7, -10
	256-pin FineLine BGA	-5, -6, -7, -10

Note:
(1) Ultra FineLine BGA packages are Altera's 0.8-mm pitch BGA packages.

MAX 7000S Family

5.0-V MAX 7000S devices offer features such as 5-ns speed grades, in-system programming, an open-drain output option, and IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in industrial-temperature grades. Table 8 shows the packages and speed grades available in the commercial-temperature grade.

Table 8. Commercial-Temperature MAX 7000S Devices

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

MAX 3000A Devices

MAX 3000A devices are the ideal low-cost ISP solution for designers looking for high performance at a low price-per-macrocell cost. 3.3-V product-term-based MAX 3000A devices are targeted for high-volume, low-cost designs. These devices have an enhanced ISP feature set and range in density from 32 to 256 macrocells (see Table 9) with propagation delays as fast as 4.5 ns.

Table 9. MAX 3000A Devices

Device	Package	Speed Grade
EPM3032A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM3064A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	100-pin TQFP	-4, -7, -10
EPM3128A	100-pin TQFP	-5, -7, -10
	144-pin PQFP	-5, -7, -10
EPM3256A	144-pin TQFP	-6, -7, -10
	208-pin PQFP	-6, -7, -10

CONFIGURATION

4-Mbit Configuration Device Coming Soon

The new 4-Mbit EPC4E configuration device is scheduled for release in the third quarter of 2000. This device will be offered in a 44-pin and 100-pin TQFP packages as well as a 0.8-mm, 144-pin Ultra FineLine BGA package. A new 9-Mbit EPC9E configuration device is also being developed and is slated for release in the third quarter of 2000. A single EPC4E device will configure a 400,000-gate EP20K400E device, and a single EPC9E device will configure a 1-million-gate EP20K1000E device.

These new devices will include features such as faster configuration times and parallel configuration. Additionally, you can use a single device to configure several APEX or FLEX devices in parallel to further speed configuration time.

TOOLS

Quartus Software Version 2000.05 Available Now

The Quartus software version 2000.05 is shipping to all customers with a current subscription in a single upgrade package that includes the MAX+PLUS II software version 9.6, Synopsys FPGA *Express*-Altera version 3.4 synthesis software, and Exemplar Logic LeonardoSpectrum-Altera version 1999.j synthesis software. Version 2000.05 of the Quartus software provides significant performance and fitting improvements for large designs. It also provides support for the device packages shown in Table 10 in addition to the device packages supported in version 2000.03.

Quartus Operating System Update

The Quartus software version 2000.05 supports the operating systems listed in Table 11.

Support for the Windows 2000 and the HP-UX 11.0 operating systems will be added later this year.

continued on page 12

Devices & Tools, continued from page 11

The MAX+PLUS II software version 9.6 is shipping to all customers with current subscriptions and features support for the new ACEX 1K device family.

Table 10. New Devices Supported by Quartus Version 2000.05

Support	Device	Package
Full Compilation, Simulation and Programming Support	EP20K100	356-pin BGA
	EP20K100E	324-pin FineLine BGA
	EP20K200 (1)	356-pin BGA
	EP20K200E	652-pin BGA, 672-pin FineLine BGA
	EP20K300E (1)	240-pin PQFP, 652-pin BGA, 672-pin FineLine BGA
	EP10K600E (1)	672-pin FineLine BGA
	EP20K1000E	652-pin BGA
Compilation, Simulation, and Pin-Out Support Only	EP20K160E (1)	144-pin TQFP, 208-pin PQFP, 240-pin PQFP, 356-pin BGA, 484-pin FineLine BGA
	EP20K1500E (1)	652-pin BGA, 1,020-pin FineLine BGA

Note:
(1) The Quartus software version 2000.05 supports these devices with and without PLLs.

Table 11. Quartus Operating System Support

Platform	Operating System
PC	Windows 98, Windows NT
UNIX	Solaris 2.6, HP-UX 10.20

MAX+PLUS II Software Version 9.6 Now Shipping

The MAX+PLUS II software version 9.6 is shipping to all customers with current subscriptions and features support for the new ACEX 1K device family. The ACEX 1K family is Altera's new mid-range density, look-up table (LUT)-based PLD family offering the low cost and high performance necessary for price-sensitive communications applications. For a complete list of new device support in the MAX+PLUS II software version 9.6, see Table 12.

MAX+PLUS II Version 9.62 is Now Available on the Altera Web Site

The MAX+PLUS II software version 9.62 update for the PC platform adds full support and advanced pin-out support for the devices listed in Table 13. This update also includes several software improvements to the Quartus fitter, timing model changes, and EPM7128B and EPM7256B device programming. This software update is available by opening the Software Tools menu on the left of the Altera web site and selecting MAX+PLUS II Updates.

If you are using the MAX+PLUS II BASELINE or E+MAX™ development system, you can eleminate problems by using version 9.62 of the MAX+PLUS II BASELINE and E+MAX software, which are now available.

Table 12. New Devices Supported by MAX+PLUS II Version 9.6

Support	Device	Package
Full Compilation, Simulation and Programming Support	EPM7128B	100-pin FineLine BGA, 256-pin FineLine BGA
	EPM7256B	100-pin TQFP, 144-pin TQFP, 208-pin PQFP, 256-pin FineLine BGA
	EP1K30	144-pin TQFP, 208-pin PQFP, 256-pin FineLine BGA
	EP1K50	144-pin TQFP, 208-pin PQFP, 256–pin FineLine BGA, 484-pin FineLine BGA
	EP1K100	208-pin PQFP, 256-pin FineLine BGA, 484-pin FineLine BGA
Compilation, Simulation, and Pin-Out Support Only	EPM7128B	49-pin Ultra FineLine BGA, 169-pin Ultra FineLine BGA
	EPM7256B	169-pin Ultra FineLine BGA
	EPM7512B	169-pin Ultra FineLine BGA
	EPM7064AE	49-pin Ultra FineLine BGA
	EPM7128AE	169-pin Ultra FineLine BGA

Table 13. Additional Devices Supported in MAX+PLUS II Version 9.62

Support	Device
Full Support	EPM7128BFC256, EPM7256BFC256, EPM7512BQC208
Advanced Pin-Out Support	EP1K10TC100, EP1K10TC144, EP1K10QC208, EP1K10FC256, EPM7032BUC49, EPM7064BUC49

Renewal Price Promotion for Customers on Active Subscription

For a limited time, all Altera customers with current subscriptions will receive a 10% discount off of the renewal subscription list price as long as the renewal subscription is ordered before their current subscription expires. This offer is valid to all customers on active subscription. The renewal ordering code can be used to renew FIXEDPC, FLOATPC, or FLOATNET subscriptions.

The 10% discount applies to orders received on or before the subscription expiration date. A renewal subscription extends the subscription by 12 months from the existing expiration date. Customers do not lose any months on their existing subscription by renewing early.

You will receive updates for both the Quartus and MAX+PLUS II software for an additional 12 months after your current subscription was set to expire. You also receive world-class synthesis and simulation software with the renewal of your subscription. For synthesis, Synopsys FPGA *Express*-Altera and Exemplar Logic LeonardoSpectrum-Altera is included with your renewal. You will also receive Model Technology Model*Sim*-Altera for behavioral HDL simulation and test bench support. By renewing a subscription before it expires, you are guaranteed to receive the latest version of the Quartus and MAX+PLUS II software without interruption and gain access to world class synthesis and simulation software.

License Files for OEM World-Class Synthesis & Simulation Tools Available Today

Altera has entered into OEM agreements with Synopsys and Mentor Graphics to provide Altera customers with world-class synthesis and simulation products. Altera is shipping the Synopsys FPGA *Express* version 3.4 and Exemplar Logic LeonardoSpectrum Level 1 version 1999.1j synthesis software to all customers with current subscriptions. Model Technology Model*Sim*-Altera simulation software will be shipping to customers shortly.

Visit the Altera web site to request a license file to enable any or all of the OEM software tools. A license file will be e-mailed directly to you to enable these synthesis and simulation capabilities for use with the Altera software. FPGA *Express* is only available for the PC platform, working with FIXEDPC and FLOATPC products. The LeonardoSpectrum and Model*Sim* software for Altera are available for PCs and UNIX workstations in fixed or floating configurations.

Synopsys FPGA *Express* for Altera supports mixed-HDL synthesis for VHDL and Verilog designs. The feature set of the FPGA *Express* software that Altera ships is identical to the standard FPGA *Express* software. However, FPGA *Express* software only targets Altera devices.

For LeonardoSpectrum license files, you can request either VHDL or Verilog support for each Altera subscription, but not both—you can only have support for one HDL per Altera subscription. The LeonardoSpectrum Level 1 for Altera and Level 2 software tools do not support mixed-HDL synthesis. The LeonardoSpectrum Level 1 synthesis tool provided by Altera includes all the features of the LeonardoSpectrum Level 2 configuration, but only allows designers to target Altera devices.

Altera has entered into OEM agreements with Synopsys and Mentor Graphics to provide Altera customers with world-class synthesis and simulation products.

The Model*Sim*-Altera simulation software consists of the Model*Sim* PE GUI features including the standard HDL debugging environment and Tcl scripting capability supporting Altera libraries for gate-level simulation. You can request either VHDL or Verilog HDL support within the ModelSim software for each Altera subscription, but not both. The Model*Sim*-Altera software tools do not support mixed-HDL simulation.

You can indefinitely use versions of the Synopsys FPGA *Express* software for Altera received during your active subscription. However, you cannot enable versions of FPGA *Express* released after your subscription expires. This is identical to the licensing for the Quartus and MAX+PLUS II software.

License files for Exemplar Logic LeonardoSpectrum and Model Technology Model*Sim* software provided by Altera are set to expire 15 months from the date of the license request. These products will no longer operate after expiration. However, you can request a new license and extend the expiration for another 15 months as long as your subscription remains active.

Improving Quartus Design Performance

The Quartus™ software version 2000.02 and higher introduces new and improved timing-driven compilation algorithms for core and I/O performance as well as more capability for cliques. In most cases, push-button performance in the Quartus software can achieve desired requirements for core f_{MAX} and I/O timing. Many additional techniques can be used to achieve even better performance in APEX™ designs with the Quartus software, including:

- Timing-driven compilation
- Cliques and other logic options
- Back-annotation and manual placement

Timing-Driven Compilation

The Quartus software is very flexible, and offers a large number of options that can be set within. You can set a global timing-driven compilation target for the entire design, or several timing-driven compilation target settings, one for each individual clock domain (if several exist in the design). Individual clock settings usually provide better f_{MAX} results (and are required for multiple clock domain analysis and hold-time validation). For optimal results, experiment with both global and individual settings.

In the Quartus software version 2000.02 and higher, you can either select **Normal compilation** or **Extra effort**. The **Extra effort** setting usually provides better f_{MAX} results, but may increase compile times (up to 2×). In either case, you should set the target f_{MAX} about 10% higher than required and vary the target until you find the best results. If you set the target too high, though, you may over-constrain the Quartus software, producing slower results.

Cliques and Other Logic Options

You can use options and settings in the Quartus software to improve results, including cliques, the **Speed vs. Area** setting, and the **Auto-Global Memory Control Signals** setting.

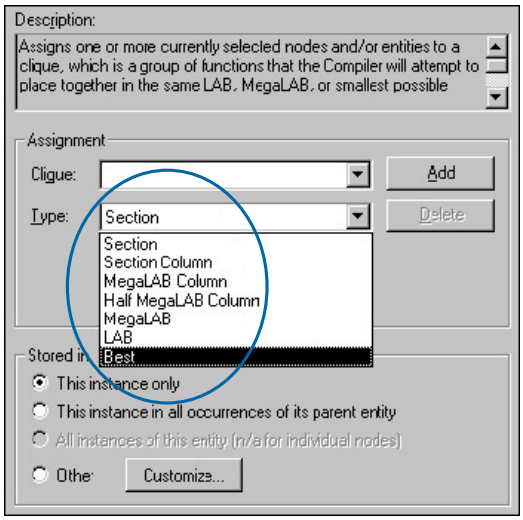
Cliques

Version 2000.02 and higher of the Quartus software provides cliques of different target sizes, controlling how tightly you pack the logic. Target areas can be as small as a logic array block (LAB) or up to half of the device.

You can use cliques with timing-driven compilation on or off. Altera recommends that you enable timing-driven compilation with hierarchical-based cliques based on your knowledge of your design. All cliques (except Best cliques, see Figure 1) are considered hard assignments that may create complications if they cannot be met. You may get a no-fit result if too much logic is placed into too small an area (i.e., placing 12 logic cells into one LAB). If you are unsure of the size of cliqued logic, use the Best clique type, which allows the Quartus software to modify the size of the clique target as needed.

After the initial compilation results with timing-driven compilation and hierarchical cliques, you

Figure 1. Clique Selection in Assignment Organizer



can analyze critical paths, determine logic common between multiple critical paths, and apply a clique to place logic cells closer together (see Figure 2).

You should add cliques only when your design performance is much slower than what is required; avoid assigning logic haphazardly into cliques without verifying that logic cells are not placed into multiple cliques of the same size. This can add more logic into the original clique size, which may result in a no-fit.

Settings

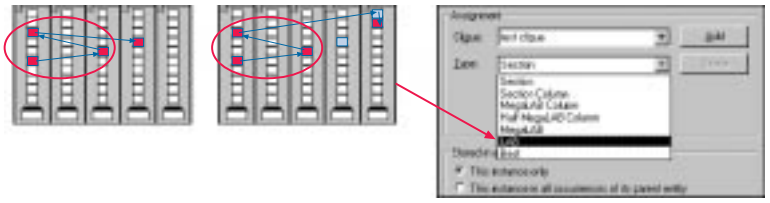
The settings you make affect the performance results in the Quartus software. Two significant settings are:

- **Speed vs. Area:** You can set the **Optimization Technique** option in the **Option & Parameter Settings** (Project menu) to either **Speed** to optimize the design for performance (tight routing, redundant logic for fanout) or **Area** to optimize device space (loose routing, minimal/optimized logic). You can use this option for all HDL files, although it is most effective on Altera Hardware Description Language (AHDL) Text Design Files (**.tdf**) and Block Design Files (**.bdf**). You should synthesize Verilog HDL and VHDL designs with other third-party EDA synthesis tools.
- **Auto-Global Memory Control Signals:** You may improve your design's performance by turning this setting off. This setting is enabled by default and instructs the Quartus software to use global-control interconnect lines whenever possible for memory control signals. However, this may slow memory performance if internally-generated control signals are not able to drive memory blocks directly without using the global control lines. Extra delay is incurred when routing onto global control lines prior to the memory blocks.

Back-Annotation & Manual Placement

Your timing-driven compilation targets, cliques, and options and settings may bring your design performance close to required specifications, but they may not be enough. You can then back-annotate the design results and placement, manually moving logic yourself to speed up your design. Back-annotation can be very powerful because it:

Figure 2. Cliquing Common Logic Cells



- Allows you to maintain fitting results from one version of the Quartus software to other versions of the Quartus software, either older or newer
- Can improve fitting time (from hours down to minutes), since the Quartus software devotes less time with logic placement
- Locks down specific parts of the design, maintaining speed in those portions of the design

One drawback is that if the design changes significantly, some or most of the back-annotated assignments may be lost due to re-synthesis and renaming of node names.

The following indicators can help you determine if you should back-annotate your design:

- Is the design stable (will there be any more code changes)?
- Path dependencies: Is there logic common to multiple critical paths?
- Are there only a few paths that do not meet performance goals?
- Are compile times long?

If you back-annotate your design, you should consider several guidelines. In well-utilized designs (60% or higher), you should back-annotate to logic array blocks (LABs) instead of logic cells to ensure second-time fitting after logic is rearranged. You may have to demote assignments to MegaLAB™ blocks. Here are additional guidelines:

- Always ignore or disable cliques if you back-annotate your design; these new assignments will override the cliques.

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Design Tips: Improving Quartus Design Performance, continued from page 15

- Archive or back-up project files from your best compilation to date. If the next round of changes are slower than your best f_{MAX} results, you should revert back to the files from your best compilation. This is easily done if you archived the files.

The goal is to minimize the amount of interconnect delays used in the path (see Figure 3), hence consolidating logic as much as possible. Determine where critical paths cross LAB or MegaLAB boundaries. Logic cells should always be moved into LAB or MegaLAB bins, instead of specific logic cell locations. The Quartus software determines legal placement and routing for you.

Figure 3. Making LAB-Based Location Assignments

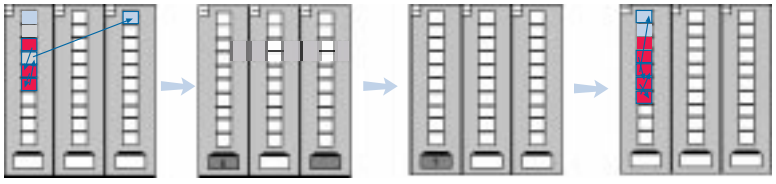


Figure 4. Increasing Path A Delay Helps Path B Timing

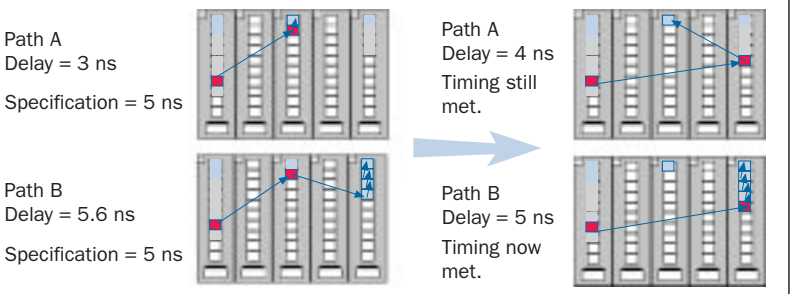
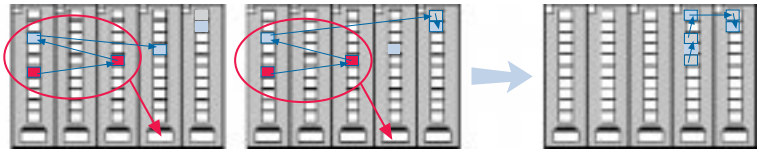


Figure 5. Assigning Common Logic Cells to LABs



To determine which cells to move, look at the cells that have the smallest fan-in and fan-out. These are the cells that will likely have the least impact to other potentially critical paths. You should avoid making other critical paths worse when moving logic cells to fix another critical path. However, in some cases, increasing the delay of some paths when fixing other critical paths can be a good tradeoff if the slowed paths are not critical. Short paths (i.e., back-to-back registers) with plenty of margin can be good candidates to balance delay (see Figure 4).

Logic common in multiple critical paths can also be resolved with manual placement. Create an efficient layout by moving logic cells that appear in several paths (e.g., control signals such as enables, address decoders, and other high fanout situations). See Figure 5. By fixing one path, you can fix several others.

Critical paths should cross MegaLAB columns as infrequently as possible (avoid using row-interconnect lines). When using the MAX+PLUS® II software for FLEX® designs, you can improve performance when you keep paths on the same row. However, this does not hold true for APEX designs and the Quartus software. Essentially, MegaLAB blocks and MegaLAB columns in APEX devices are equivalent to LABs and rows of LABs in FLEX devices. This also applies when you clique large blocks of logic together.

Summary

The Quartus software version 2000.02 and higher comes equipped to allow you to achieve performance goals in various ways. If you cannot meet performance with push-button timing-driven compilation operation, a combination of cliques, settings, back-annotation, and manual placement can often get the extra performance necessary in APEX designs. It is important to realize that there is no one "best" method to achieve performance in the Quartus software. The options that work best vary by design, but the steps outlined in this article should help improve your performance.

Sign Up Now for Free Excalibur Workshops

Intensive three-hour workshops, starting in June, will teach you how to implement the Nios™ family of soft core embedded processors in APEX™ devices. These hands-on workshops will allow you to work with the Excalibur™ Development Kit, from creating a design and running it on a development board to tracking down and correcting design errors. You will also learn about the GNUPro® compiler and debugger from Cygnus®, a Red Hat® company, which is included in the Excalibur Development Kit. Visit **http://www.altera.com/workshop** to reserve your space at a North American workshops. To sign up for free workshops outside North America, contact your local Altera representative.

North America

Arizona
- Phoenix — July 14

California
- Santa Clara — June 28
- Santa Clara — June 29
- San Diego — July 11
- Irvine — July 12
- Woodland Hills — July 13

Colorado
- Broomfield — August 25

Florida
- Tampa — July 27

Georgia
- Norcross — July 25

Illinois
- Arlington Heights — August 7
- Lisle — August 8

Maryland
- Gaithersburg — August 18

Massachusetts
- Westford — August 15

Michigan
- Livonia — August 10

Minnesota
- Minneapolis — August 9

New Jersey
- Long Branch — August 16
- Cherry Hill — August 17

New York
- Rochester — July 21

North Carolina
- Reasearch Triangle Park — July 28

Ohio
- Fairborn — August 11

Ontario, Canada
- Kanata — July 18
- Mississauga — July 19

Oregon
- Beaverton — August 29

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- Richardson — August 22
- Austin — August 23

Utah
- Salt Lake City — August 31

Washington
- Bellvue — August 30

Europe

England
- London — September 12

France
- Paris — September 22

Germany
- Munich — September 15

Israel
- Tel Aviv — September 18

Italy
- Milan — September 20

Sweden
- Stockholm — September 13

Bridging the Gap: dataBLIZZARD & Reliaspan

Ultimate performance, high availability, and redundancy are three demanding requirements for the telecom industry as it heralds a new generation of communications interfaces. SBS Technologies Connectivity Products has addressed these demands with two breakthrough product lines: the dataBLIZZARD™ and Reliaspan products.

The dataBLIZZARD product family includes PCI, PCI mezzanine card (PMC), and CompactPCI formats, which will be used in medical imaging, telecommunications, and other industrial applications.

The dataBLIZZARD software is the ultimate-performance, point-to-point communications interface that enables two computers to share data at the hardware level with little or no software overhead (see Figure 1). The dataBLIZZARD peripheral component interconnect (PCI) interface that supports data sharing is flexible, providing the highest performance allowed by the PCI bus. The integrated direct memory access (DMA) engine can transfer data between systems at sustained transfer rates of 80 megabytes per second. Programmed I/O processes can be completed over the link in less than 2 µs, and data can be transferred up to 500 meters over dataBLIZZARD's gigabit fiber-optic transceivers. The dataBLIZZARD product family includes PCI, PCI mezzanine card (PMC), and CompactPCI formats, which will be used in medical imaging, telecommunications, and other industrial applications.

Reliaspan, SBS' exceptionally fast, high-throughput 64-bit expansion systems for PCI and CompactPCI computers, is designed to provide servers with I/O expansion capabilities through the addition of seven PCI or CompactPCI slots. With Reliaspan, a host server can be gracefully scaled to accommodate more PCI or CompactPCI slots, as they are needed. This is especially important for high-availability telecom and computer telephony applications that were once previously limited by the number of cards that the host could support.

Historically, SBS designed its own PCI bus interfaces, but for the dataBLIZZARD software and Reliaspan, SBS chose to move into the 64-bit, 66-MHz PCI realm via intellectual property (IP). Using a programmable logic device (PLD) with a PCI function, SBS entered the market quickly without losing design flexibility.

SBS thoroughly evaluated cores offered by six programmable logic vendors and applied the following criteria: performance, flexibility, stability features, documentation, and allowable design re-use. As a result of this evaluation, SBS selected the Altera® FLEX® 10K family to use in both the dataBLIZZARD and Reliaspan products over the six companies that had working 64-bit, 66-MHz PCI function designs. Only Altera could offer four or more base address registers—an essential feature that allowed SBS to maintain compatibility with the suite of software drivers written for earlier generation products.

William Molyneux, vice president of engineering, SBS Connectivity Products, stated that "Reliaspan and the dataBLIZZARD software represent significant breakthroughs for SBS. Both will be shipped in high volumes and will have very long product life cycles." Molyneux also affirmed that "Altera was the sole vendor with bridge experience using its core which substantially lowered our risk. Altera became more of a partner than a vendor. They made every effort to support our developments with their engineering resources."

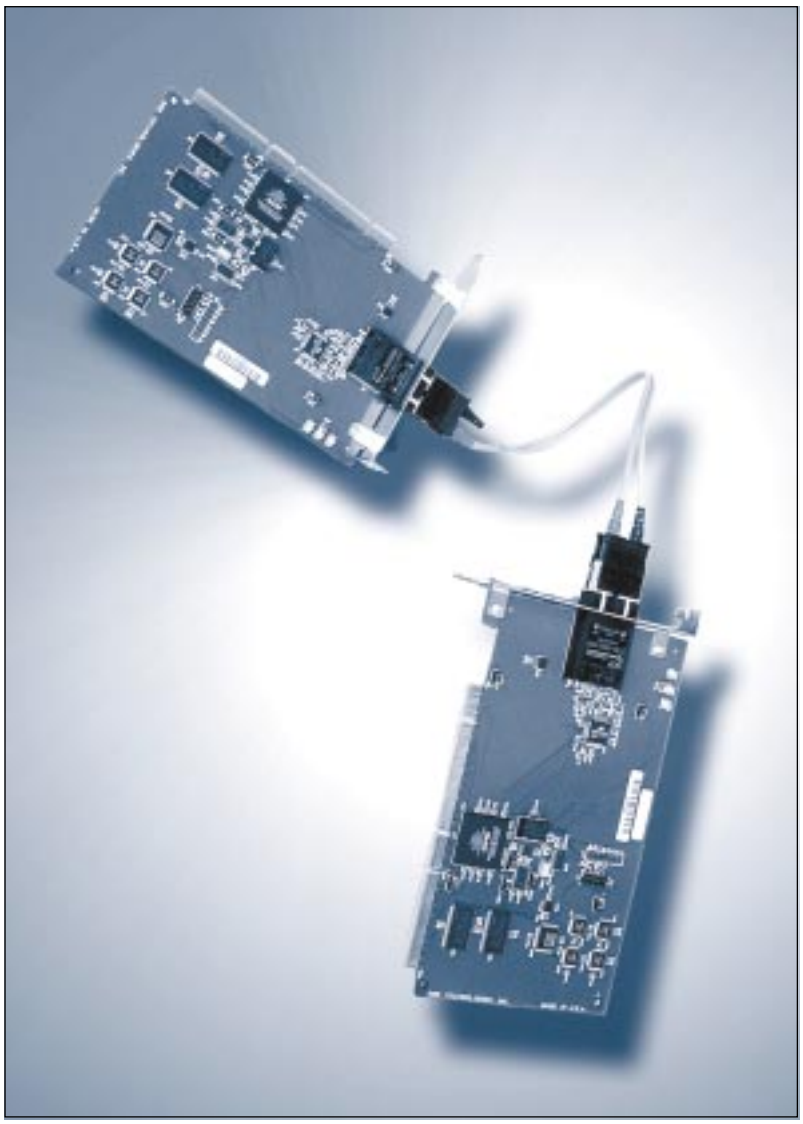
Reliaspan CompactPCI expansion systems were introduced at the Computer Telephony Exposition last March. The dataBLIZZARD family was introduced at Intel's Applied Computing Show at the end of May. Both the dataBLIZZARD software and Reliaspan have already been designed into several major OEM projects.

SBS Technologies, Inc., Connectivity Products is the premier provider of high-performance and reliable bus connectivity products that include bus bridges and bus expansion units that are designed to operate in the most demanding applications.

SBS Technologies, Inc. is a leading manufacturer of standard bus embedded computer components for VME, CompactPCI, embedded PCI and custom standalone applications. SBS product lines include CPU (Pentium and PowerPC) boards, input/output (I/O) modules, avionics modules and analyzers, bus interconnection products, expansion units, real-time networks, telemetry boards, data acquisition software, DIN-rail embedded PCs, and industrial-grade computers. SBS Technologies' embedded computer components are used in a variety of applications, such as communications, medical imaging, industrial control and flight instrumentation in the commercial and aerospace markets.

SBS Connectivity Products
1284 Corporate Center Drive
St. Paul, MN 55121-1245
(651)905-4700
http://www.sbs-cp.com

Figure 1. The dataBLIZZARD Connection



Nios Architecture & Customization

Inside the Nios Embedded Processor

As the first RISC processors developed specifically for programmable logic, the Nios™ family of soft core embedded processors contains many configurable elements to meet a wide range of needs. The block diagram in Figure 1 shows the basic elements of the Nios embedded processor. You can configure the address and data bus widths to a maximum of 32 bits. The register file, stored in embedded system blocks (ESBs), can be up to 512 words deep with a 32-bit viewable window. The Nios interrupt controller supports up to 64 internal or external sources.

Using Nios Peripherals

The Excalibur™ Development Kit, featuring the Nios embedded processor, includes several peripherals for the Nios family, including a universal asynchronous receiver/transmitter (UART), a counter/timer, memory controllers, and a parallel I/O (PIO) connection. Other peripherals, such as an SDRAM controller, SPI, PWM, 10/100 Ethernet MAC, and IDE disk controller will be released later this year. The MegaWizard® Plug-In Manager, also included, lets you connect and configure your Nios peripherals to the Nios embedded processor. Wait states, interrupt control, variable bus sizers, and address decoding are all automatically generated by the MegaWizard Plug-In Manager within the peripheral bus module (PBM), shown in Figure 2. For example, you can use the MegaWizard Plug-In Manager to specify which peripherals interrupt the Nios embedded processor; for each peripheral that does, the MegaWizard Plug-In Manager automatically assigns an address in the interrupt look-up table (LUT) and generates the corresponding interrupt control logic. You can also choose the number of wait states each peripheral needs, or allow the peripheral to generate its own wait signal for the Nios embedded processor; in either case, the MegaWizard Plug-In Manager designs the wait state generator accordingly. The MegaWizard Plug-In Manager uses bus size converters to adapt 32-bit peripherals to Nios 16-bit configurations as needed. Finally, the MegaWizard Plug-In Manager creates address decoding within the PBM to generate the necessary chip selects.

In addition to generating the PBM, the MegaWizard Plug-In Manager also defines the connection between the Nios embedded processor and the PBM, and between the PBM and the peripherals. The MegaWizard Plug-In Manager outputs a set of Verilog HDL files containing the connectivity, PBM, and Nios design that can be easily integrated into any APEX™ 20K device through the Quartus™ software.

Figure 1. Nios Block Diagram

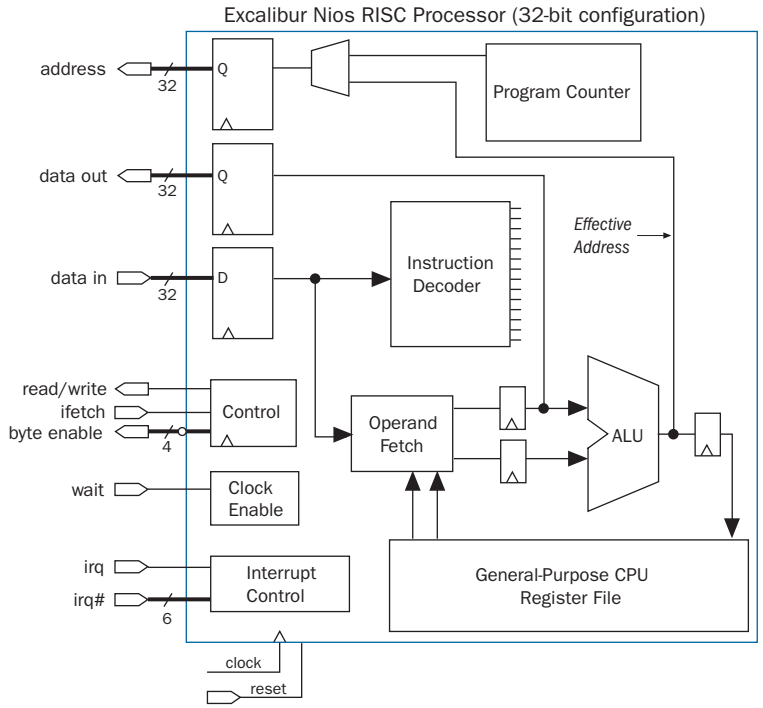
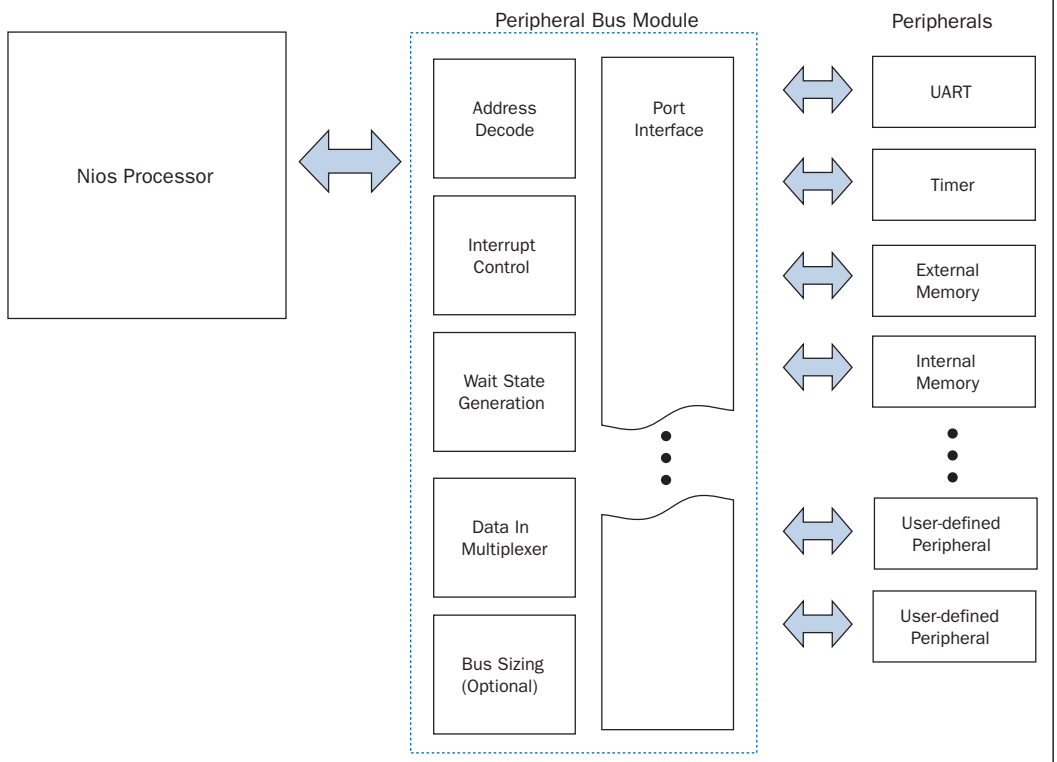


Figure 2. Nios Embedded Processor & PBM



Nios™

Customizing the Nios Embedded Processor

In addition to customization via its user-selectable parameters, you can design other peripherals to supplement the Nios embedded processor. These peripherals can be anything supported by APEX device resources, including custom memory controllers, DSP functions such as filters and FFTs, encoders/decoders, proprietary interfaces, etc. User-defined peripherals are handled the same way as Altera peripherals; you can assign interrupts and wait states using the MegaWizard Plug-In Manager, which automatically generates the necessary logic and connectivity files (users also have the choice of creating their own connections).

Current Software Versions

The Quartus™ software version 2000.05 is the latest release, and is available for the following operating systems:

- Microsoft Windows 98
- Microsoft Windows NT
- Sun Solaris version 2.6
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported

The MAX+PLUS® II software version 9.6 is available for the following operating systems:

- Microsoft Windows 95 and Windows 98
- Microsoft Windows NT version 3.51 and higher
- Sun Solaris version 2.5 and higher
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported
- AIX version 4.1 and higher

Sucessful In-System Programming Implementation

Altera supports the Jam™ Standard Test and Programming Language (STAPL) format, which allows you to program IEEE 1149.1 Joint Test Action Group (JTAG)-compliant devices independent of platform and vendor. In-system programmability (ISP) is accomplished through the 4-wire JTAG interface. In addition, Jam STAPL simplifies software support by allowing you to run the programming software in any environment: in a PC or workstation, over a network, or in an embedded environment.

To use ISP successfully, you must plan the following areas of product development:

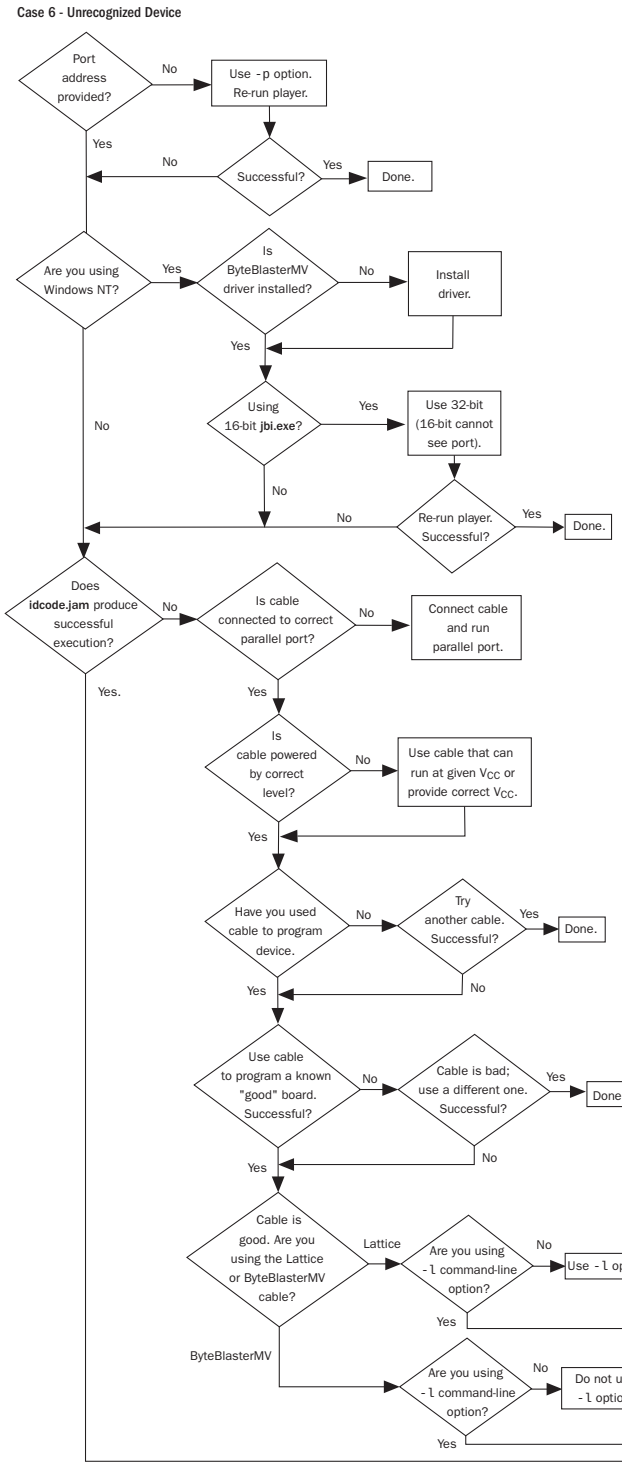
- Board Layout—connecting the JTAG chain. Treat TCK as a clock trace, a task often overlooked in embedded systems where TCK originates at a processor's general I/O pin. Lack of signal integrity on this trace is often the source of programming errors.
- Embedded Memory Requirement—for in-field upgrades. In an embedded environment, the Jam STAPL Byte-Code software requires memory to program the devices in the JTAG chain. It is important to consider this requirement before choosing memory and processors used for the in-field upgrade.

For more information on these topics see *Application Note 100 (In-System Programmability Guidelines)*, and *Application Note 122 (Using Jam STAPL for Embedded ISP & ICR)*.

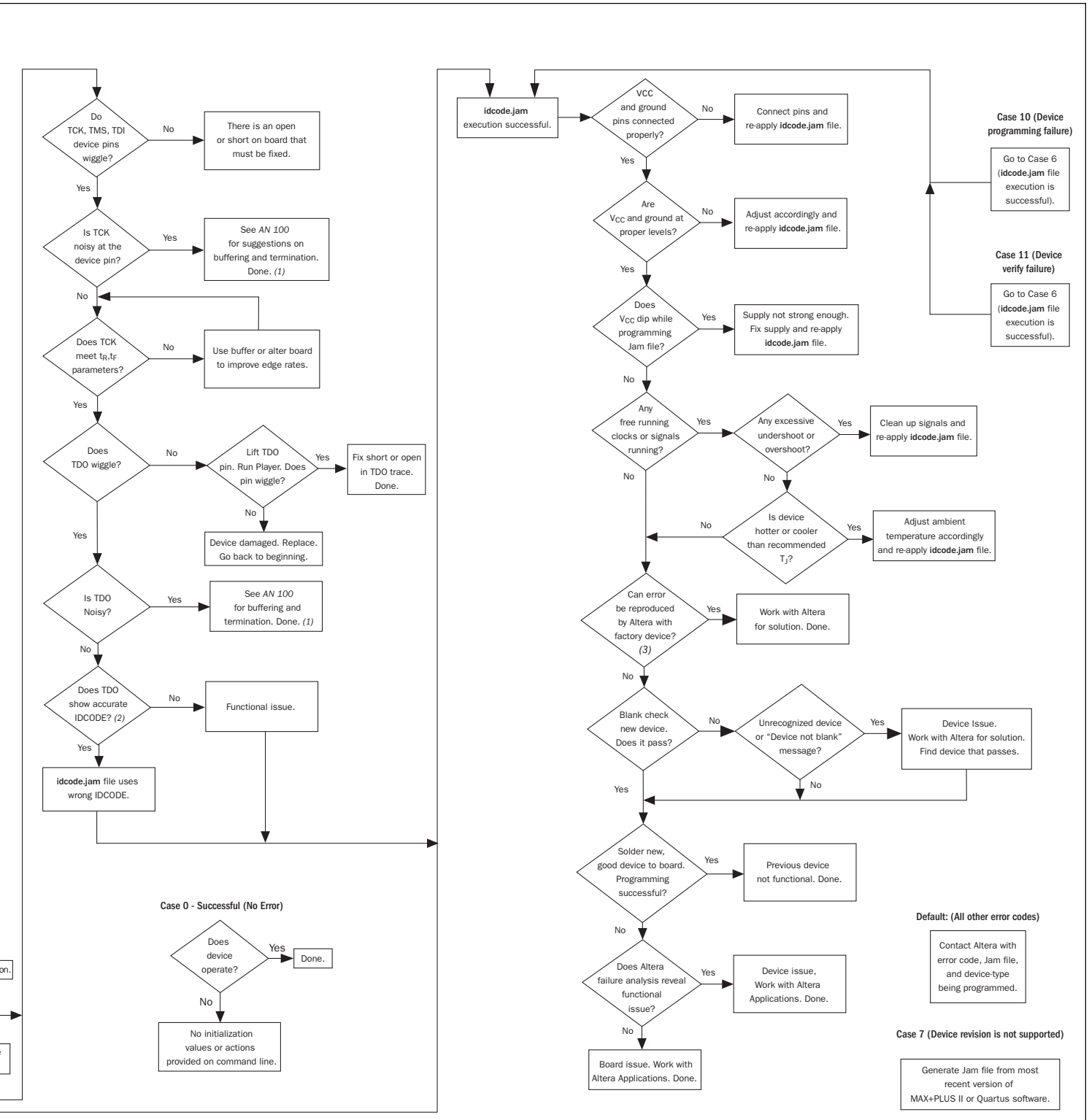
Following the steps listed in *Application Note 100* and *Application Note 122*, ISP can reduce your costs and improve product quality. If you encounter an error during programming, the flow chart shown in Figure 1 will help you determine the source of the problem.

In addition, you can download the **idcode.jam** Jam STAPL file from the Altera® FTP site: **ftp:\\ftp.altera.com\pub\misc**. Use this file to read the JTAG IDCODE out of Altera devices. If you cannot read the IDCODE, then you have a signal integrity or JTAG connectivity issue. See the flow chart in Figure 1 to determine where the problem is.

Figure 1. Jam Error Flow Chart



Notes: (1) *Application Note 100 (In-System Programmability Guidelines)*

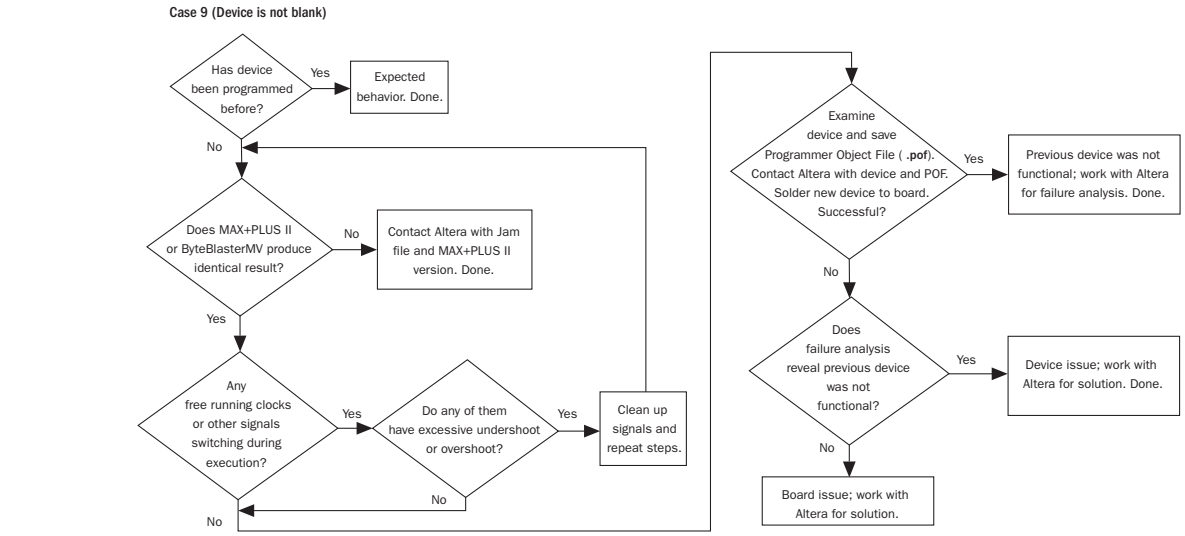


. (2) See device data sheet for IDCODEs. (3) Work with local FAE or contact Altera Applications (800) 800-3753

continued on page 24

Sucessful In-System Programming Implementation, continued from page 23

Figure 1. Jam Error Flow Chart (continued)



Altera *News*

ACEX Devices Address Communications Market Need for Low-Cost Programmable Logic

The communications marketplace is experiencing rapid and dynamic growth. Increased pressures for flexibility and fast time-to-market are brought about by shortened design cycles and continually evolving standards. Programmable logic is a key to achieving a successful solution in this rapidly changing marketplace. However, for high-volume applications, the need for cost-efficiency historically restricted the use of programmable logic devices (PLDs).

Now, low-cost communications applications eagerly awaiting the programmable advantage have an attractively priced solution.

Altera has eliminated this cost barrier with the new ACEX™ device family. Now, low-cost communications applications eagerly awaiting the programmable advantage have an attractively priced solution. Furthermore, ACEX devices can meet the requirements inherent to communications systems without sacrificing performance. ACEX devices provide a low-cost, high-performance solution, ideal for ASIC and application-specific standard product (ASSP) replacement in the communications marketplace.

ACEX Applications

The need for a high-volume, low-cost programmable solution in the communications marketplace is skyrocketing as price-sensitive applications abound due to the explosive growth in the networking and telecommunications sectors. xDSL and cable modem growth rates are tremendous due to the expansion of Internet traffic, and Dataquest projections expect these modem growths to reach as high as 141% compounded annual growth rate (CAGR). ACEX devices fit perfectly into these applications, replacing blocks such as protocol and transceiver modules, which are currently implemented via ASICs or ASSPs. Remote access concentrators and access routers provide another example of the enormous potential for ACEX devices, as demand for high-speed

communication channels to satellite offices grows. Laser printers, PC peripherals, and low-cost switches provide just a few more examples of the many applications in the communications marketplace that benefit from ACEX devices.

ACEX device pricing is competitive with ASICs, freeing designers from expensive and time-consuming ASIC implementation. Additionally, all the typical benefits of PLDs over ASICs still apply, including fast time-to-market, flexibility in design and reprogrammability, advanced PLD development tools, and drop-in intellectual property (IP). ACEX devices also eliminate non-recoverable engineering (NRE) costs, the risk associated with ASIC re-spins, errors, and design changes, and time associated with the ASIC conversion process. Due to the advanced and versatile nature of the ACEX feature set, ACEX devices also eliminate specialized and inflexible ASSP implementations of design elements. You can integrate discrete phase-locked loops (PLLs), first-in first-out (FIFO) circuitry, RAM, and peripheral component interconnect (PCI) or other advanced bus interface standard interfaces within an ACEX device.

ACEX Device Families

The ACEX device families are broad-based, intended to provide programmable solutions across platforms and generations. An ongoing line of ACEX families will be introduced, beginning with the 2.5-V ACEX 1K family that is now shipping, and continuing with the 1.8-V ACEX 2K family to be released later this year. ACEX families will span a variety of processes and operating voltages, and smaller process geometries will increase performance while decreasing cost and power consumption. Future ACEX families will continue to make use of a variety of architectures and will have a range of different feature sets.

ACEX 1K Devices

The ACEX 1K family is currently available and represents the optimal union of price, performance, and features in this low-cost, 2.5-V device family. The key to the ACEX 1K device's low price is the advanced hybrid process, combining 0.22-µm transistors with 0.18-µm metal interconnect layers. This combination maintains the desired 2.5-V operating voltage while improving die size over standard 0.22-µm processes. This die size improvement provides a two-fold advantage: creating inherent cost improvements due to the large number of available die per wafer, and improving the yield at a constant defect density. In addition, the patented Altera redundancy feature ensures that even dies with impurities can be repaired and rendered fully functional, further improving yield numbers and reducing costs.

The four ACEX 1K devices range from 10,000 to 100,000 typical gates (56,000 to 257,000 maximum system gates) and deliver high performance, with typical system speeds exceeding 115 MHz. ACEX 1K devices are specifically designed to support 64-bit/66-MHz PCI compliance, ensuring compatibility with high-performance communications systems by using what has become the de facto bus standard for open systems and an emerging I/O standard for embedded applications. ACEX devices feature an embedded PLL that can simultaneously generate ClockLock and ClockBoost modified clock signals to manage on-chip clock domains, improve device utilization, and improve board-level clock management as a whole. Embedded dual-port memory blocks provide a significant enhancement as well, ensuring fast and effective RAM, ROM, dual-port RAM, or FIFOs with tremendous ease of implementation.

EP1K30, EP1K50, and EP1K100 devices are all now shipping in a wide range of advanced packages, including thin-quad flat pack (TQFP) and FineLine BGA™ packaging. EP1K10 devices will ship in the third quarter of 2000 with volume pricing beginning as low as $3.50 per device.

ACEX 2K Devices

ACEX 2K devices will be available in the second half of 2000. These devices will be based upon an advanced 0.18-µm process and will make use of Altera's process technology leadership to ensure high production yields and low costs at a 1.8-V operating voltage. ACEX 2K devices will range from 20,000 to 150,000 gates (75,000 to 400,000 maximum system gates) and will incorporate additional advanced features such as advanced I/O standards and an enhanced-capability PLL.

Altera's New SignalTap Plus System Analyzer Provides Simultaneous On-Chip & Off-Chip Debug Capabilities

The ultimate success of digital designs relies on overall system operation. However, as programmable logic devices (PLDs) become larger and faster, their circuitry becomes more complex and challenging to debug. Altera's new SignalTap™ Plus system analyzer addresses these challenges. Crossing the boundary between PLD and board-level logic analysis, the SignalTap Plus system analyzer presents a complete picture of signal activity, and accelerates the debug process. Figure 1 shows the interaction between the SignalTap Plus analyzer and a system under test.

The SignalTap Plus system analyzer is the next generation of PLD debug tools, featuring enhanced on-chip debug capabilities with an added 32-channel *external* logic analyzer for true system-level signal acquisition. This new system analyzer captures signals from internal PLD nodes and external, board-level nodes simultaneously, displaying data from both in a single, time-correlated display.

Internal & External Logic Analyzers Combined

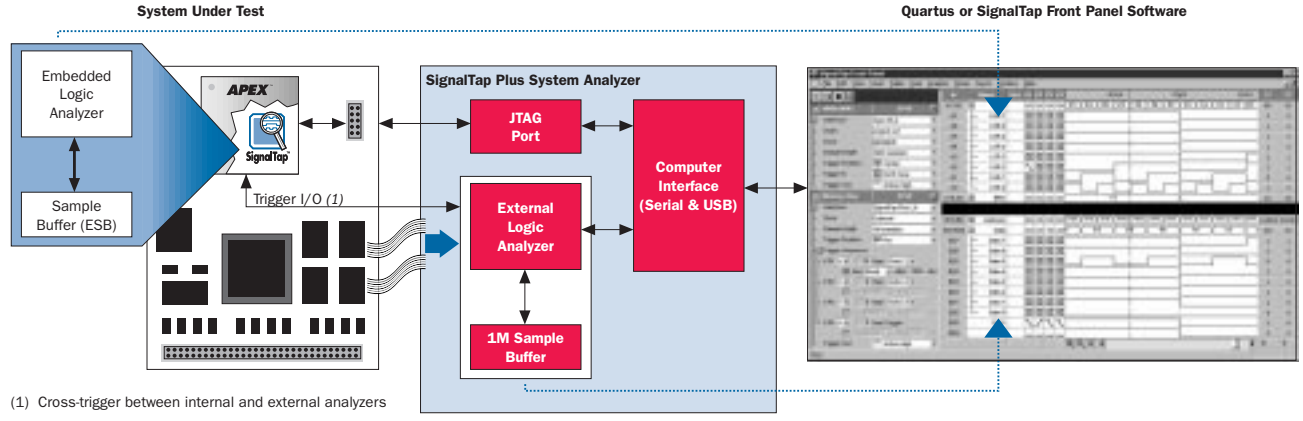
Until now, bench-top logic analyzers that cost thousands of dollars could neither provide this seamless interface to internal (PLD) and external (board level) logic analysis nor present both sets of data in a common, time-correlated display. The SignalTap Plus system analyzer provides two powerful logic analyzers—one embedded in the PLD and the other connected to board-level signals—that let you perform cause and effect analysis at the system level, triggering one analyzer based on signal activity captured by the other.

Access to internal PLD signals is provided by the SignalTap embedded logic analyzer, introduced in June 1999 and included with the Quartus™ development system. The embedded logic analyzer captures signals from internal PLD nodes while the device is running in-system and at-speed. It stores captured data in internal embedded system blocks (ESBs), and the data is then streamed off-chip via the same JTAG port used to configure your PLD. Adding an embedded logic analyzer to the design is as simple as selecting nodes from a list and compiling. You do not have to modify your hardware description language (HDL) source code—the Quartus software automatically creates an embedded logic analyzer when you compile the design based on the signals selected.

New Bench-Top Analysis

The SignalTap Plus system analyzer provides 32 channels of external logic analysis that rivals

Figure 1. SignalTap Plus Analyzer



the performance of many bench-top logic analyzers at a fraction of the cost.

The 166-MHz synchronous and asynchronous sample rate provides plenty of speed to capture fast signals. A robust, four-level trigger sequencer with built-in event count, pattern duration, and trigger timeout allows you to trigger the analyzer based on a sequence of events. The 1-Mbyte sample per channel acquisition buffer allows you to capture long traces—critical in the analysis of communications signals.

SignalTap Front Panel Software

The new SignalTap Front Panel software supports both embedded and external logic analyzers. This new software is integrated into the Quartus development system version 2000.05 and provides a complete development and debug environment. If you only need the debug facilities of the SignalTap Plus analyzer, you can use a PC or laptop computer to run the SignalTap Front Panel software as a stand-alone application with the Windows 95/98 or Windows NT operating system.

The SignalTap Front Panel software provides control and data display for both internal and external logic analyzers. Trigger conditions, sample depth, and sample rate settings are provided for each analyzer. You can view acquired data as waveforms or tabular lists that are time-correlated based on a common clock or common trigger point. You can use four dedicated trigger patterns to trigger the logic analyzer or locate and highlight specific data.

You can share data acquired by the SignalTap Plus system analyzer via email and analyze it off-line without acquisition hardware using the SignalTap Front Panel software. The SignalTap Front Panel software can be downloaded for free from the Altera web site at **http://www.altera.com**.

You can share data acquired by the SignalTap Plus system analyzer via email and analyze it off-line without acquisition hardware using the SignalTap Front Panel software.

The SignalTap solution makes it easy for you to debug and analyze your design. Not only does the SignalTap Plus system analyzer have all the features of the SignalTap embedded logic analyzer, it also lets you view board-level signals. You can use the SignalTap Front Panel software to manage both the embedded and external analyzers. This combination makes the SignalTap Plus system analyzer a powerful analysis tool that accelerates system debugging and reduces your time to market.

Discontinued Devices Update

Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

DCM Technologies' CoreX-V10: Increased Performance Produces Faster Megafunctions

Peripheral component interconnect (PCI) local bus specifications made their debut in 1992 as a way to improve server performance by increasing the flow of data between the processor and its peripheral devices. Since then, the bandwidth requirements of peripheral devices have grown steadily. Fast I/O technology such as Gigabit Ethernet, Fiber Channel, and Ultra-3 SCSI demand faster interconnect buses. PCI-X architecture is designed to fill this increasingly important position. PCI-X functions at 133 MHz over a 64-bit path and incorporates many features, including register-to-register protocol, that enhance the performance of the system bus and achieve internal timing requirements with less effort compared to conventional PCI.

DCM Technologies is a leader in implementing the PCI-X architecture and is one of the first to offer a commercially-available PCI-X function, their CoreX-V10 product. DCM Technologies develops functions for programmable logic devices (PLDs), with many applications for communications and networks.

PCI-X Power Hits the Commercial Market

The CoreX-V10 function is one of the first PCI-X solutions and a 133-MHz, 64-bit PCI-X bus Initiator/Target function that provides speeds up to 1.0 gigabyte per second for high-speed applications and a flexible interface between the PCI-X bus and the application interface. The CoreX-V10 supports 32- and 64-bit bus widths on a synchronous application interface. It is optimized for use on Altera APEX 20KE devices and supports configuration, memory, and I/O transactions. This PCI-X function runs at 66 MHz on an APEX 20KE device.

DCM Technologies rigorously tested the CoreX-V10 function to ensure that it complies with PCI-X revision 1.0 specifications and the ***PCI Local Bus Specification, Revision 2.2***. Bundled with a test environment that allows you to check the functional correctness and protocol violations, the CoreX-V10 function is backed with support from more than 30 PCI and PCI-X trained engineers.

As a leader in IP core design, DCM comes together with a number of utilities and a test environment with the function. These items are included with the CoreX-V10 function:

- CoreX-V10 (netlist or source for PLD applications)
- Self-checking PCI-X test bench comprised of:
  - Automatic test-case generator (TCG)
  - PCI-X monitor, arbiter
  - Bus functional models (BFMs)
- CoreX-V10 wizard for setup, synthesis, verification, and documentation
- On-site training and support for three days in addition to continuous phone and email support

To implement this function in current or future designs, contact DCM Technologies for immediate service and support.

DCM Technologies
39675 Cedar Blvd., #220
Newark, CA 94560
(510) 623-8826
http://www.dcmtech.com

CoreX V-10 Features

The CoreX V-10 offers the following features:

- A flexible general purpose interface that can be customized for specific peripheral requirements
- 32/64-bit, 133-MHz PCI-X function.
- Fully compliant with PCI-X revision 1.0 specifications and the ***PCI Local Bus Specification, Revision 2.2***
- Optimized for APEX 20K architecture.
- Compliant with 66-MHz APEX 20K devices
- Supports full speed burst up to 1 Gbyte per second as initiator or target
- A flexible general logic interface similar to Altera's `pci_c` function
- Fully synchronous design

Initiator Features

The initiator offers the following features:

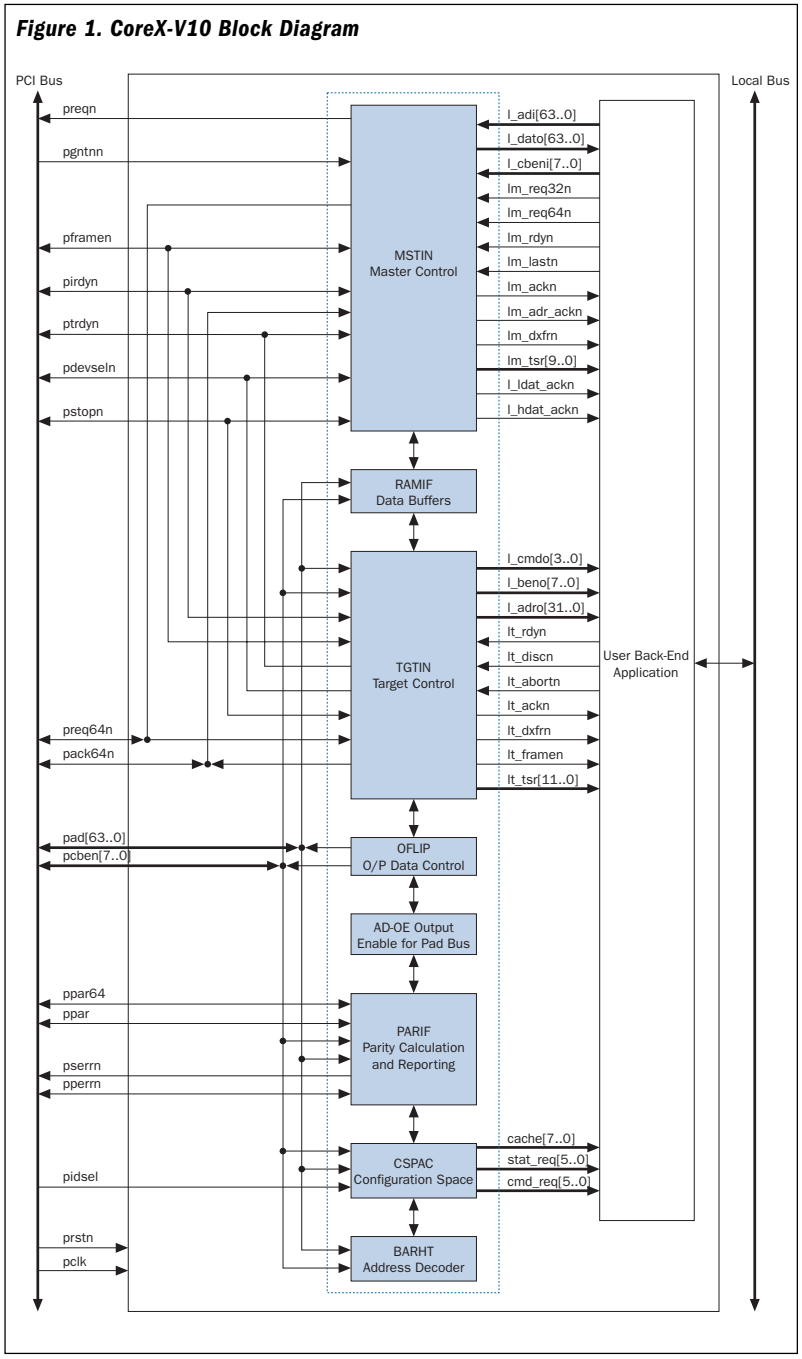
- Initiates PCI-X commands including configuration read/write, memory read/write block, memory write, split completion, and I/O read /write
- Initiates PCI commands including configuration read/write, memory read/write, I/O read/write, memory write and invalidate (MWI), and memory read line (MRL)
- Initiates 32- or 64-bit cycles
- Initiates 64-bit addressing, using dual address cycle (DAC)
- PCI bus parking
- Address stepping for configuration cycles in PCI-X mode
- Generates and checks parity

Target Features

The Target Control offers the following features:

- Type zero configuration space
- Decode 'B' in PCI-X and slow in PCI mode
- Support for capabilities list pointer
- Parity error detection
- Up to six base address registers (BARs) with adjustable memory size and type (64-bit memory BAR and 32-bit I/O BAR)

Figure 1. CoreX-V10 Block Diagram



- User logic interface can request for retry, disconnect or abort
- Responds to 32- and 64-bit transactions.
- 64-bit addressing capability
- Becomes an initiator (master) to complete split cycles and follows initiator rules

True-LVDS Solution Provides 840-Mbps Data Transfer Rates

Bandwidth and I/O performance requirements for next-generation communication designs are always increasing. To address these needs, designers can use either the Altera® True-LVDS™ solution found in APEX™ 20KE devices or an emulated low-voltage differential signaling (LVDS) solution found in other programmable devices. The LVDS I/O standard is becoming increasingly accepted in communication applications because of its high noise immunity, high performance, and low power consumption characteristics.

This article compares APEX 20KE True-LVDS dedicated circuitry to the LVDS I/O standard found in other programmable logic devices (PLDs). APEX 20KE devices provide the most robust LVDS solution in the programmable marketplace, shown through superior APEX 20KE LVDS support:

- 840 megabits per channel bandwidth
- Dedicated LVDS circuitry
- Push-button Quartus™ software compilation support
- Carefully planned on-chip LVDS pin placement
- Integrated deskew capability
- Considerably lower power consumption
- Simpler board level design requirements

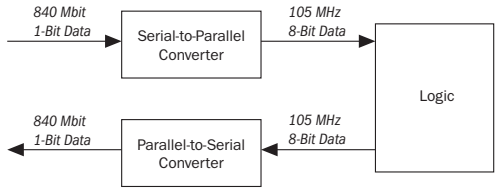
LVDS Comparison

The True-LVDS solution found in APEX 20KE devices is unique to the PLD marketplace in that it provides dedicated LVDS circuitry. This circuitry greatly facilitates LVDS implementation and ensures that complex device-level timing issues are handled with minimal design work.

For example, APEX 20KE has dedicated LVDS receiver and LVDS transmitter circuitry, designed to support multiple channels. This circuitry ensures compliance with the LVDS timing constraints and generates appropriate differential signals. It also performs the critical serial-to-parallel and parallel-to-serial conversions required to convert the high-speed LVDS signals to rates that are easily accommodated on the device. Other PLDs do not have this dedicated LVDS receiver or LVDS transmitter circuitry and must emulate it through logic and RAM, which quickly consumes valuable resources needed for the user's design and considerably reduces the remaining memory capacity. Furthermore, it is difficult to achieve high data throughput without dedicated circuitry.

The phase-locked loops (PLLs) in APEX 20KE devices provide versatile LVDS support. Designers can implement the LVDS I/O standard in APEX 20KE devices in 1×, 4×, 7×, and 8× data transfer modes. APEX devices support multiple 840-megabits per second (Mbps) LVDS channels without difficulty, as shown in Figure 1.

Figure 1. APEX 20KE LVDS Interface



A high-speed LVDS interface is critical for complex communications applications such as dense wave division multiplexing (DWDM) systems. Current DWDM systems require optical components to ensure high-quality transmission at 622 Mbps per channel. Altera offers a solution to reduce cost of ownership by utilizing an Altera Reed-Solomon forward error correction (FEC) intellectual property (IP) function to correct errors that are introduced by lower-cost optical components. This function adds the FEC data to the SONET OC-12 data,

which increases the LVDS bandwidth requirement to 666 Mbps per channel. The APEX 20KE True-LVDS solution easily supports this additional bandwidth requirement. Altera's True-LVDS solution provides the optimum price and highest performance for communications application such as terabit routers, switch fabrics, and enterprise storage network equipment.

APEX 20KE devices contain dedicated circuitry to implement the deskew feature, which ensures accurate data capture and compensates for board-level skew. This added circuitry creates a robust LVDS solution.

The absence of dedicated deskew circuitry in other PLDs requires designers to use external trace adjustments on the printed circuit board (PCB) to align the clock and data channels, a process that is both challenging and cumbersome.

True-LVDS Implementation

The APEX 20KE True-LVDS solution is easy to implement via true push-button support within the Quartus development tool. The Quartus software features two megafunctions, `altlvds_rx` and `altlvds_tx`, that directly implement an LVDS receiver and an LVDS transmitter, respectively. Incorporating these two megafunctions within a design allows push-button compilation of the LVDS interface and implementation of multiple channels with frequencies of up to 840 Mbps. Dedicated APEX 20KE LVDS circuitry ensures that all timing requirements for data transfer are properly met.

Other PLDs require considerable time and effort to meet all necessary timing requirements. Emulating an LVDS circuit is a tremendously difficult task, and designers may have to hand-route the LVDS receiver and transmitter circuitry within other field-programmable gate arrays (FPGAs). Furthermore, the receivers and transmitters are typically very sensitive to the propagation delays associated with the derived clock and the data channels. As a result, you must ensure that these delays are matched for all process, voltage, and temperature (PVT) variations.

Board-Level Issues

APEX 20KE devices use true differential output drivers on 16 LVDS channels. The built-in circuitry provides low-power, low electromagnetic interference (EMI), and high-noise immunity benefits. The absence of these dedicated output drivers in other PLDs leads to high power consumption and creates noise and EMI rather than reducing them.

The APEX 20KE True-LVDS solution is easy to implement via true push-button support within the Quartus development tool.

Further difficulties are seen in board-level design due to pin placement. The two pins corresponding to each LVDS channel in physically adjacent pairs are placed near the outer edge of the APEX device package, as shown in Figure 2 on page 32. This pin placement minimizes the board-level skew commonly associated with unequal trace lengths between the two channel signals and simplifies trace layout. Often, other PLDs do not take these factors into account, placing the two pins associated with a given channel too far apart. This distance can cause significant differential impedance due to board-level skew, forcing a board designer to manually compensate for unequal trace lengths.

Poor pin placement also decreases the common mode rejection ratio (CMRR), degrading the LVDS interface performance. This discontinuity occurs because LVDS is sensitive to unbalanced noise on its pins. The lack of closely-matched signal traces results in poor noise immunity.

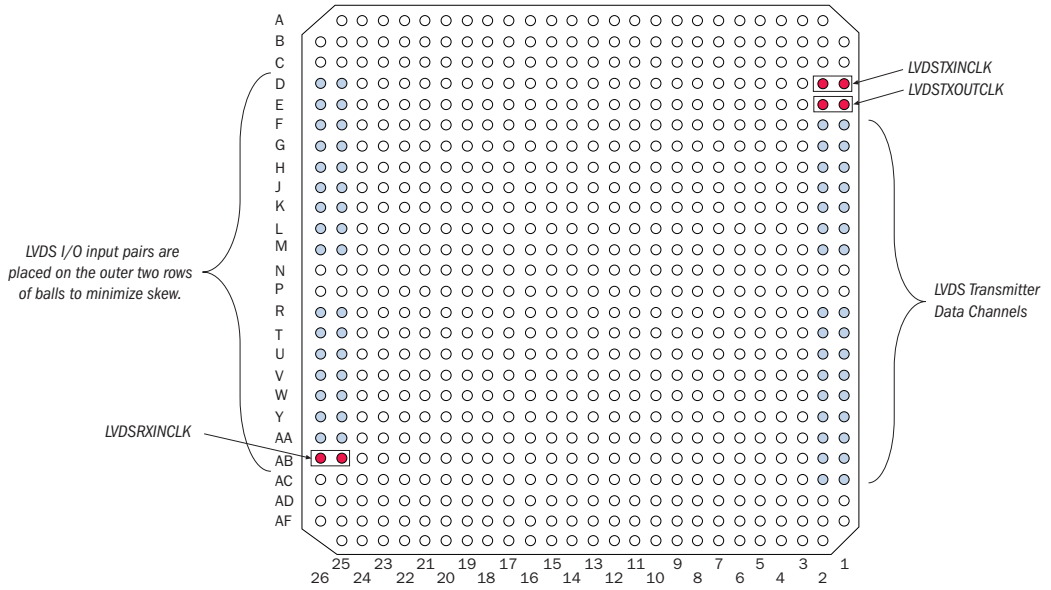
Summary

APEX 20KE devices offer a comprehensive solution for the True-LVDS I/O standard that has been proven fast, effective and simple to implement. Though other devices claim to have an LVDS solution, it is very complex and difficult to implement. The True-LVDS solution in APEX 20KE devices is simpler to use and more efficient due to advantages such as higher performance, dedicated LVDS circuitry, and lower power consumption.

continued on page 32

True-LVDS Solution Provides 840-Mbps Data Transfer Rates, continued from page 31

Figure 2. LVDS Pin Placement in APEX 20KE Devices



Altera's Turbo Encoder & Decoder Push the Technology Envelope for High-Speed 3G Wireless Applications

Optimized for the APEX family of devices, Altera's Turbo MegaCore function, like the Reed-Solomon core, comes with separate encoder and decoder cores.

Altera is adding to its portfolio of Forward Error Correction MegaCore® functions for wide use in third-generation (3G) wireless applications. In addition to the Reed-Solomon and Viterbi cores, the latest addition to this family is the Turbo Encoder (ordering code: `PLSM-TURBO/ENC`) and Turbo Decoder (ordering code: `PLSM-TURBO/DEC`) megafunctions.

The Turbo MegaCore function is targeted towards 3G wireless applications, satellite communications, digital video broadcast, and sub-marine data transfer applications, where high speed and high data integrity are paramount.

Optimized for the APEX™ family of devices, Altera's Turbo MegaCore function, like the Reed-Solomon core, comes with separate encoder and decoder cores, as shown in Figure 1. It is also compliant with the Third-Generation Partnership Project (3GPP) for error correction on high-speed data services up to 2 megabits per second (Mbps).

Because of the dynamic state of the 3GPP, no current 3GPP compliant application-specific standard products (ASSPs) or ASICs exist. Digital signal processors, hovering around 200 Kbits per second (Kbps), cannot achieve the high throughput possible in Altera's programmable logic devices (PLDs).

The Turbo Encoder function is stream-driven and uses a block-based coding scheme. Two interleaved convolutional encoders generate P1

and P2 parity output streams. These streams can then be punctured to save bandwidth. The 3GPP code rates are approximately 1/3 if puncturing is not used and 1/2 with puncturing.

After depuncturing the received data stream, the information and P1 parity bits are fed into decoder 1. An equalizer (not shown in Figure 1) delivers the probabilities of the received values to decoder 1. Decoder 1 then has the received bit value and the confidence level of that bit value. Decoder 1 evaluates these results and combines them with the P1 probabilities (parity bits), which are fed into decoder 2 with the information bits and the P2 parity bits. After a predefined number of iterations, the decoding process is completed and the output is available.

The purpose of interleaving is to combat burst errors. Convolutional codes are an excellent defense against random errors. However, since errors typically come in bursts, interleavers disperse the corrupt data, making it easier to correct. The turbo decoder interleaver, as defined by 3GPP, is a rigorous algebraic interleaver based on sets of prime numbers. As this function is labor-intensive to implement, it is an essential component of Altera's Turbo Decoder.

Altera's turbo decoder takes advantage of a logarithmic maximal a-posteriori (max-logMAP) algorithm (see Figure 2). This is a computationally intensive algorithm, which utilizes two banks of memory—Alpha memory and Parity memory. Altera's Turbo MegaCore function gives the user total flexibility with the memory configuration via the MegaWizard® Plug-In Manager (see Table 1).

Table 1. Turbo Decoder Memory Configuration Examples

Soft Bits	Alpha Memory	Parity Memory	Number of ESBs	Suitable Device
3	On-chip	On-chip	70	EP20K300E
4	Off-chip	On-chip	46	EP20K200
5	Off-chip	Off-chip	32	EP20K200
5	Off-chip	On-chip	58	EP20K300E
5	On-chip	On-chip	138	EP20K600E
8	Off-chip	Off-chip	46	EP20K200
8	Off-chip	On-chip	86	EP20K400

Figure 1. Turbo CODEC Block Diagram

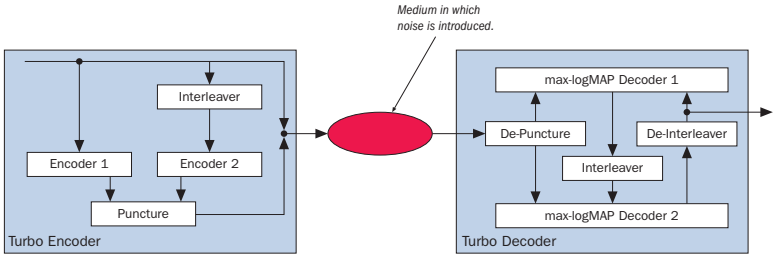
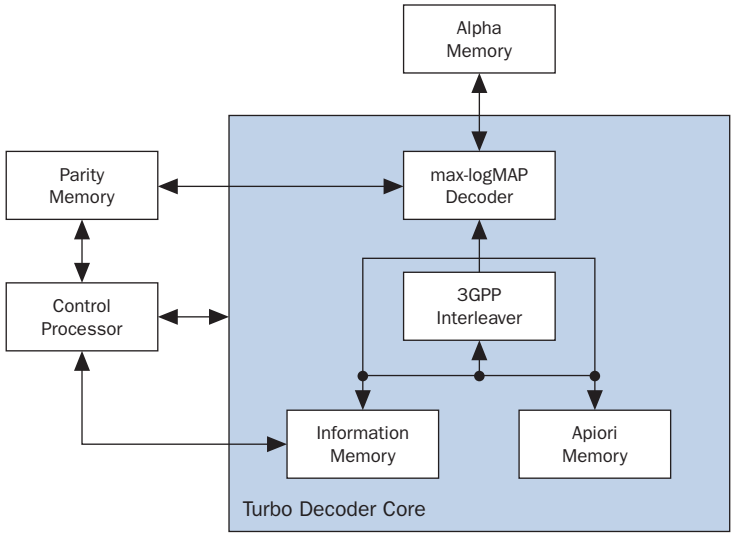


Figure 2. Turbo Decoder Block Diagram



The max-logMAP decoder requires two clock cycles per information bit. Since there are two decoders, each iteration requires four clock cycles per bit. Five iterations require 20 clock cycles per bit, plus about five cycles for loading and unloading data. The decoder can run at approximately 50 MHz in a –1 speed grade APEX 20KE device, producing a data transfer rate of 2 Mbps.

Altera's Turbo CODEC includes the OpenCore™ feature for both the Encoder and Decoder functions and a MegaWizard Plug-In for easy customization. VHDL and Verilog HDL simulation models, a C model for bit-error rate (BER) simulation, and the VHDL source code of a Reference Design are also included for verification purposes. In the absence of ASSP or ASIC solutions, Altera's Turbo CODEC MegaCore function addresses the necessary FEC requirements for emerging 3G wireless applications.

Questions & Answers

Q *How do I program or configure my Altera® device on a Windows 2000 platform?*

A In addition to the operating systems listed in the **readme.txt** file, the Quartus™ software version 2000.03 and MAX+PLUS® II software version 9.6 support device programming and configuration on the Windows 2000 operating system.

There is a new INF file for installing Programmer hardware on the Windows 2000 platform. This file exists in the <*system*>**\drivers\win2000** directory for the Quartus software version 2000.03 and the MAX+PLUS II software version 9.6. The installation procedure is as follows:

1. Open the **Control Panel** (Start menu -> **Settings** -> **Control Panel**).
2. Double-click the **Add/Remove Hardware** icon to start the **Add/Remove Hardware Wizard** and click **Next** to continue.
3. In the **Choose a Hardware Task** panel, select **Add/Troubleshoot a device** and click **Next** to continue. Windows 2000 will search for new Plug and Play hardware (**New Hardware Detection** window).
4. In the **Choose a Hardware Device** window, select **Add a new device** and click **Next** to continue.
5. In the **Find New Hardware** window, select **No, I want to select the hardware from a list** and click **Next** to continue.
6. In the **Hardware Type** window, select **Sound, video and game controllers** and click **Next** to continue.
7. In the **Select a Device Driver** window, select **Have Disk**.
8. Specify the full directory path to the **win2000.inf** file (e.g., <*max+plus II directory*>**\drivers\win2000**) and click **OK**.
9. In the **Digital Signature Not Found** warning dialog box, click **Yes** to continue the installation.
10. In the **Select a Device Driver** window, select the hardware to install and click **Next** to continue.
11. The **Start Hardware Installation** window displays the hardware being installed. Click **Next** to continue.
12. In the **Digital Signature Not Found** warning dialog box, click **Yes** to continue the installation.
13. In the **Completing the Add/Remove Hardware Wizard** window, click **Finish** to continue.

A system dialog box appears which prompts you to reboot so that the new settings can take effect.

You can fit multiple PCI functions on a single device. The only limiting factor is the size of the megafunction and the resources available in the particular device.

Q *Can I fit multiple peripheral component interconnect (PCI) functions on a single Altera device?*

A Yes. You can fit multiple PCI functions on a single device. The only limiting factor is the size of the megafunction and the resources available in the particular device. For example the `PCI/MT64` function consumes approximately 1,500 logic elements (LEs) in a FLEX® 10K device. Therefore, you can fit two `PCI/MT64` functions on an EPF10K100E (4,992 LEs) or larger device.

A second factor is the timing issues while fitting multiple PCI functions on a single device. The Assignment & Configuration File (**.acf**) provided by Altera for its megafunctions is designed for a single megafunction only. If you want to fit multiple functions on a single device, then you may have to modify the ACFs to meet all the timing requirements related to PCI.

Q *What is the behavior of the phase-locked loop (PLL) output if the input clock is disabled while in user mode?*

A If you remove the input clock, the PLL output drifts to the voltage-controlled oscillator's (VCO's) lower frequency limit (nominally 200 MHz) divided by *K* or *V*, depending on whether you are using the `clock0` or `clock1` output. *K* and *V* are the value of the output dividers for the two PLL outputs `clock0` and `clock1`. Additionally, the lock pin for the PLL goes low. Once the clock input starts up again, the PLL re-locks on the signal.

The VCO's lower frequency limit can extend below 200 MHz depending on process, voltage, and temperature.

In simulation, the PLL output will show as GND because the simulator cannot model the frequency drift. The lock indication is low at this time, and you should monitor this for the indication of a valid clock. Once the input clock starts up again, the clock output will show up in simulation. The simulator assumes the delta delay for lock indication.

Q *Error: "The project has more than one chip. Multi chip designs are not supported in this version."*

A You may get this error message if the project's Compiler Settings File (**.csf**) has more than one chip section. For example, the following code in your CSF may produce the error:

```
...
CHIP(Block1)
{
    DEVICE = AUTO;
}
CHIP(Block2)
{
    DEVICE = AUTO;
}
...
```

The compiler interprets this as a multiple-device design. In order to fix the problem, remove the additional CHIP section and reload the project.

Q *What type of slow-slew rate control do Altera's devices have on output signals?*

A Altera's APEX™ 20K, APEX 20KE, ACEX™ 1K, FLEX 10K, FLEX 10KA, FLEX 10KE, FLEX 6000, MAX® 7000E, MAX 7000S, MAX 7000A, MAX 7000AE, and MAX 3000A devices have a slew rate option that allows users to select a slow-slew rate for each I/O pin.

For ACEX 1K, FLEX 10K, FLEX 10KA, FLEX 10KE, FLEX 6000, and MAX 7000E devices, this option slows the slew rate for the falling edges. The rising edge is not affected by this feature.

For APEX 20K, APEX 20KE, MAX 7000S, MAX 7000A, MAX 7000AE, and MAX 7000B devices, both falling and rising edges are affected by this feature.

Q *Error: "Bounds of non-constant index addressing array reach beyond the bounds of the array."*

A This error message occurs if you use a variable without a range constraint to specify an array index. To avoid this error, specify a range constraint in the variable declaration.

For example, the following code produces this error message in the MAX+PLUS II software:

```
architecture a of test is
signal my_array :
   std_logic_vector(7 downto 0);
signal bitpos :
   std_logic_vector(2 downto 0);
begin
begin

P1 : process (my_array)
variable i : integer;
begin
i := conv_integer(bitpos);
if my_array(i) = '1'then
...
```

The error message will not occur if the code is changed as follows:

```
architecture a of test is
signal my_array :
   std_logic_vector(7 downto 0)
signal bitpos :
   std_logic_vector(2 downto 0);
begin

P1 : process (my_array)
variable i : integer range 0
   to 7;
begin
i := conv_integer(bitpos);
if my_array(i) = '1'then
...
```

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Questions & Answers, continued from page 35

Q *Why does the MAX+PLUS II software report a slower f_{MAX} value than what is shown in the data sheet for my MAX device?*

A The f_{MAX} reported by the MAX+PLUS II software provides the fastest clock frequency for the slowest registered path (i.e., the longest registered path delay) in the entire design.

The f_{MAX} parameter in the device data sheet represents the fastest frequency the global clock can be run at when the data path is represented by a single register that is both fed by an input pin and feeds an output pin. This is not the same calculation as the f_{MAX} reported by the MAX+PLUS II software.

Instead, the MAX device data sheets use the parameter `fcnt` to represent the f_{MAX} reported by the MAX+PLUS II software, where the data sheet shows the fastest possible `fcnt` for a given speed grade. In this case the fcnt parameter shows the clock frequency for the fastest register-to-register path (i.e., a register in a logic array block (LAB) driving a second register within the same LAB).

MAX device data sheets use the historical, discrete transistor-to-transistor (TTL) definition of f_{MAX}. However, as EPLDs have evolved, `fcnt` has become a more useful description of device performance from a registered path point of view. As a result, the data sheet also provides this information in the form of the fcnt parameter.

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on the Altera web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- ***Altera Digital Library CD-ROM***, May 2000 (P-CD-ADL2000-03)
- *Component Selector Guide* (M-SG-COMP-08)
- *Development Tools Selector Guide* (M-SG-TOOLS-16)
- *Intellectual Property Selector Guide* (M-SG-MEGAFCTN-03)
- *ACEX 1K Programmable Logic Device Family Data Sheet* (A-DS-ACEX-01.01)
- *Excalibur Development Kit with the Nios Embedded Processor Data Sheet* (A-DS-ACEX-01.01)
- *Nios Soft Core Embedded Processor Data Sheet* (A-DS-EXCNIOS-01)
- *SignalTap Plus System Analyzer Data Sheet* (A-DS-SIGTPPLUS-01)
- *AN 115: Using the ClockLock & ClockBoost Features in APEX Devices* (A-AN-115-02)
- *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor* (A-AN-122-01)
- *AN 125: Evaluating AMPP & MegaCore Functions* (A-AN-125-01)
- *SB 47: System-on-a-Programmable Chip (SOPC) Development Board* (A-SB-047-01)
- *TB 64: New Features of the Quartus Software Version 2000.02* (M-TB-64-01)
- *TB 65: Design Fitting: MAX 7000AE vs. ispLSI 2000VE Devices* (M-TB-065-01)
- *TB 67: Advanced Synthesis with LeonardoSpectrum* (M-TB-067-01)
- *TB 68: Advanced Synthesis with FPGA Express* (M-TB-068-01)
- *TB 69: HDL Simulation with the ModelSim-Altera Software* (M-TB-069-01)
- *5.0-V Tolerance in APEX 20KE Devices White Paper* (A-WP-APEX5V-01.01)
- *Using APEX 20KE CAM with the Quartus Software Design Tool White Paper* (M-WP-CAM-01)
- *Using LVDS in the Quartus Software White Paper* (A-WP-LVDSQUARTUS-01)
- *Serial Viterbi Decoders White Paper* (M-WP-HCORES-VSERAB-01)

Altera Programming Support

Programming Hardware Support

Table 1 contains the latest programming hardware information for Altera® MAX® 9000, MAX 7000, MAX 3000, and configuration devices. For correct programming, use the software version shown in "Current Software Versions" on page 6.

Table 1. Altera Programming Adapters (Part 1 of 3) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)* EPC1064V *(2)* EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)* EPC1213 *(2)*	DIP, J-lead	PLMJ1213
EPC2 *(4)*	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(5)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(5)* PLMR9000-240NC *(5)*
EPM7032	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032B	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

Table 1. Altera Programming Adapters (Part 2 of 3) *Note (1)*

Device	Package	Adapter
EPM7064S	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(5)*
EPM7064AE EPM7064B	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin) FineLine BGA (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC *(5)* PLMF7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A EPM7128AE EPM7128B EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) TQFP (144-pin) PQFP (160-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMQ7128/7160-160NC *(5)* PLMF7000-100 PLMF7000-256
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMQ7128/7160-160NC *(5)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC *(5)*

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Table 1. Altera Programming Adapters (Part 3 of 3) *Note (1)*

Device	Package	Adapter
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A EPM7256S EPM7256AE EPM7256B	TQFP (100-pin) TQFP (144-pin) PQFP (208-pin) RQFP (208-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMT7256-208NC *(5)* PLMF7000-100 PLMF7000-256
EPM7512AE EPM7512B	TQFP (144-pin) PQFP (208-pin) BGA (256-pin) FineLine BGA (256-pin)	PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMB7000-256 PLMF7000-256
EPM3032A	J-lead (44-pin) TQFP (44-pin)	PLMJ3000-44 PLMT3000-44
EPM3064A	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ3000-44 PLMT3000-44 PLMT3000-100NC *(5)*
EPM3128A	TQFP (100-pin) TQFP (144-pin)	PLMT3000-100NC *(5)* PLMT3000-144NC *(5)*
EPM3256A	TQFP (144-pin) PQFP (208-pin)	PLMT3000-144NC *(5)* PLMR3256-208NC *(5)*

Notes:

(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on Classic™ devices.
(2) FLEX® 8000 configuration device.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(4) APEX™ 20K, FLEX 10K, or FLEX 6000 configuration device.
(5) These devices are not shipped in carriers.

Third-Party Programming Support

Data I/O, BP Microsystems, and System General provide programming hardware support for selected Altera devices. Algorithms are available on these companies' respective web sites (**http://www.data-io.com**, **http://www.bpmicro.com**, **http://www.sg.com.tw**). Programming support information for configuration, MAX 9000, and MAX 7000 devices is shown in Table 2. All information is subject to change.

Table 2. Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*	System General *(3)*
EPC1064	✓	✓	✓ *(4)*
EPC1213	✓	✓	✓ *(4)*
EPC1	✓	✓	✓ *(4)*
EPC1441	✓	✓	✓ *(4)*
EPC2	✓	✓	✓ *(4)*
EPM3032A	✓	✓	✓ *(4)*
EPM3064A	✓	✓	✓ *(4)*
EPM3128A	*(5)*	✓	✓ *(4)*
EPM3256A	*(5)*	*(5)*	✓ *(4)*
EPM7032	✓	✓	✓ *(4)*
EPM7032AE	✓	✓	✓ *(4)*
EPM7032S	✓	✓	✓ *(4)*
EPM7064	✓	✓	✓ *(4)*
EPM7064AE	✓	✓	✓ *(4)*
EPM7064S	✓	✓	✓ *(4)*
EPM7096	✓	✓	✓ *(4)*
EPM7128A	✓	✓	✓ *(4)*
EPM7128S	✓	✓	✓ *(4)*
EPM7128AE	*(5)*	✓	✓ *(4)*
EPM7128E	✓	✓	✓ *(4)*
EPM7160E	✓	✓	✓ *(4)*
EPM7192S	✓	✓	✓ *(4)*
EPM7192E	✓	✓	✓ *(4)*
EPM7256A	*(5)*	✓	✓ *(4)*
EPM7256AE	*(5)*	*(5)*	✓ *(4)*
EPM7256S	✓	✓	✓ *(4)*
EPM7256E	✓	✓	✓ *(4)*
EPM7512AE	*(5)*	✓ *(6)*	✓ *(4), (5)*
EPM9320	✓	✓	✓ *(4)*
EPM9320A	✓	✓	✓ *(4)*
EPM9400	✓	✓	✓ *(4)*
EPM9480	✓	✓	✓ *(4)*
EPM9560	✓	✓	✓ *(4)*
EPM9560A	✓	✓	✓ *(4), (5)*

Notes to Table 2:
(1) These devices are supported by the Data I/O UniSite programmer version 6.3.
(2) These devices are supported by BP Microsystems programmers version 3.49A.
(3) These devices are supported by System General programmers version 1.0.
(4) Although these devices are currently supported, Altera is in the process of verifiying the programming hardware support.
(5) Contact Data I/O, BP Microsystems, or System General about programming support for these devices.
(6) Contact Data I/O, BP Microsystems, or System General about programming support for 256-pin ball-grid array (BGA) and FineLine BGA™ packages.

Download Cables

Table 3 provides programming and configuration compatibility information for the MasterBlaster™ serial or universal serial bus (USB) communications cable and the BitBlaster™ serial and ByteBlasterMV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable.)

Table 3. Download Cable Compatibility

Device	MasterBlaster *(1)*	ByteBlasterMV	BitBlaster *(2)*
APEX 20K	✓	✓ *(3)*	
APEX 20KE	✓	✓ *(3)*	
ACEX 1K	✓	✓	✓
FLEX 10K	✓	✓	✓
FLEX 10KA	✓	✓	✓
FLEX 10KE	✓	✓	✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A	✓	✓	✓
MAX 7000B	✓	✓ *(3)*	
MAX 3000A	✓	✓	✓

Notes:
(1) The MasterBlaster communications cable can be used with the Quartus software for device download and SignalTap logic analysis. It can also be used with the MAX+PLUS II software version 9.3 for device downloads.
(2) The BitBlaster download cable must operate at 5.0 V.
(3) The ByteBlasterMV download cable must operate at 3.3 V for these devices. `VCCIO` pins can be set to either 2.5 V or 3.3 V.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera.

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	General Literature Request *(2)*	**lit_req@altera.com**	**lit_req@altera.com**
	News & Views Subscriptions	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**
	News & Views Address Changes	**n_v@altera.com**	**n_v@altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline	(800) 800-EPLD (6 a.m. to 6 p.m. Pacific Time) (408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time) *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**support@altera.com**	**support@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**

Notes:
(1) The *MAX+PLUS II Getting Started* and *Quartus Tutorial* manuals are available from the Altera® web site. To obtain other Quartus™ and MAX+PLUS® II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

Altera Device Selection Guide

Current information for the Altera® APEX™ 20K, ACEX™ 1K, FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, MAX 7000, MAX 3000, and configuration devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide*. For the most up-to-date information, go to the Altera web site at **http://www.altera.com**. Some of the devices listed may not yet be available. Contact Altera or your local sales office for the latest device availability.

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[1]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	MACROCELLS
EP20K30E	30,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 324-Pin BGA[2]	92, 108, 128, 128	1.8 V	1,200	24,576	192
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 108, 151, 183, 204, 204	1.8 V	2,560	32,768	256
EP20K100	100,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	101, 159, 189, 252, 252	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 108, 151, 183, 246, 246	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	87, 143, 175, 273, 324	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2]	144, 174, 279, 382	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 652-Pin BGA, 672-Pin BGA[2]	136, 168, 273, 376, 376, 376	1.8 V	8,320	106,496	832
EP20K300E	300,000	240-Pin RQFP, 652-Pin BGA, 672-Pin BGA[2]	152, 408, 408	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin BGA[2]	502, 502, 502	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	652-Pin BGA, 672-Pin BGA[2]	488, 488	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 508, 588	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 508, 708	1.8 V	38,400	327,680	2,560
EP20K1500E	1,500,000	652-Pin BGA, 1,020-Pin BGA[2]	488, 808	1.8 V	51,840	442,368	3,456

ACEX 1K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[2]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS
EP1K10	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	66, 102, 130, 130	2.5 V	576	12,288
EP1K30	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	102, 147, 171	2.5 V	1,728	24,576
EP1K50	50,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 186, 249	2.5 V	2,880	40,960
EP1K100	100,000	208-Pin PQFP, 256-Pin BGA[2], 484 Pin BGA[2]	147, 186, 333	2.5 V	4,992	49,152

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 189, 191, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA 672-Pin BGA[2]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[2]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA, 672-Pin BGA[2]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	71, 102	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	81, 81, 117, 171, 171	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[2]	117, 171, 199, 218, 218	3.3 V	-1, -2, -3	1,960	1,960

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[3]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[3]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[3]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX, FLEX 10K, FLEX 10KE, and FLEX 6000 devices
EPC4E[4]	44-Pin TQFP, 84-Pin BGA[5]	2.5/3.3 V	4-Mbit serial/parallel configuration device designed to configure all APEX and FLEX 10K devices.

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Altera Device Selection Guide, continued from page 41

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032B	32	44-Pin PLCC/TQFP, 48-Pin TQFP	36, 36	2.5 V	-3, -5, -7
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064AE	64	44-Pin PLCC/TQFP, 49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68	3.3 V	-4, -7, -10
EPM7064B	64	44-Pin PLCC/TQFP, 48-pin TQFP, 49-Pin BGA[1], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68, 68	2.5 V	-3, -5, -7
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 256-Pin BGA[2]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[5], 256-Pin BGA[2]	68, 84, 84, 100, 100, 100	3.3 V	-5,-7,-10
EPM7128B	128	49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[5], 256-Pin BGA[2]	40, 84, 84, 100, 100, 100	2.5 V	-4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S	256	208-Pin PQFP	164	5.0 V	-7, -10, -15
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 84, 120, 164, 164	3.3 V	-5, -7, -10
EPM7256B	256	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 164, 164, 164	2.5 V	-5, -7, -10
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	120, 176, 212, 212	3.3 V	-5, -7, -10, -12
EPM7512B	512	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 212, 212, 212	2.5 V	-5, -6, -7, -10

MAX 3000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM3032A	32	44-Pin PLCC, 44-Pin TQFP	34, 34	3.3 V	-4, -7, -10
EPM3064A	64	44-Pin PLCC, 44-Pin TQFP, 100-Pin TQFP	34, 34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-Pin TQFP, 144-Pin PQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-Pin TQFP, 208-Pin PQFP	116, 158	3.3 V	-6, -7, -10

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

Notes to Tables:

(1) Preliminary. Contact Altera for latest information.
(2) This package is a space-saving FineLine BGA package.
(3) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.
(4) This device can be programmed by the user to operate at either 2.5 V or 3.3 V.
(5) This package is a space-saving Ultra FineLine BGA package, Altera's 0.8-mm pitch BGA package.

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ASICs (ā´sĭks) **1.** Custom chips with high NRE costs. **2.** Chips that have large minimum order quantities. **3.** Chips that require months to develop and cannot be changed: *Our ASICs take forever to design and verify*. (see **inflexible**.)

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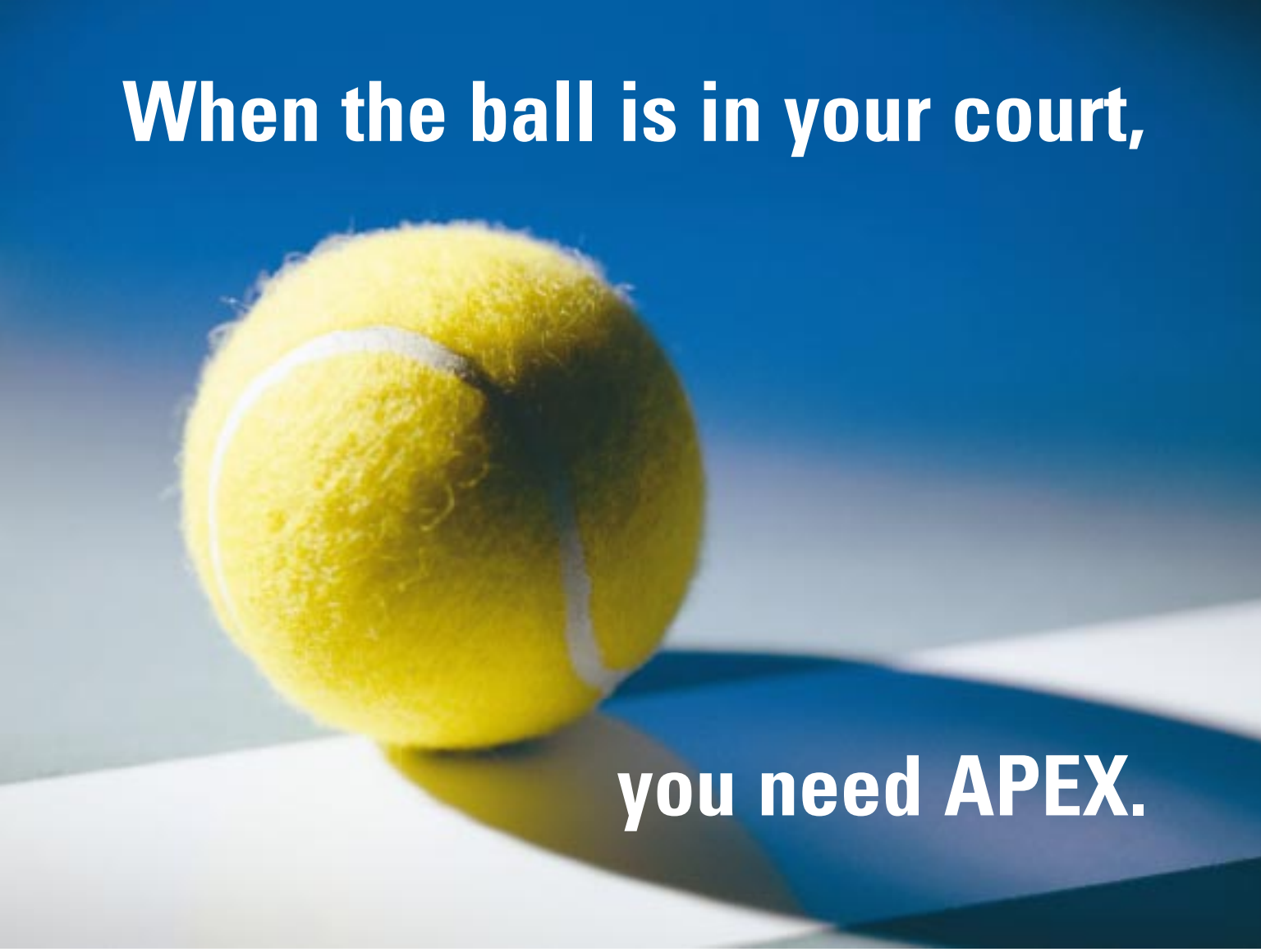

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