3 A, 34 V Input PWM/VFM Step Down DC/DC Converter with PLL Synchronization **Evaluation Board**

No. EEV-299-0330300-191111

R1270S001A033-0300EV is the evaluation board for R1270 which has the below features, benefits and specifications.

OUTLINE

The R1270S is CMOS-based Step-down DC/DC converter with internal N-channel high side Tr. The ON resistance of the built-in high-side transistor is 0.10Ω and the R1270S can provide the maximum 3 A output current. Each of the ICs consists of an oscillator, a PWM control circuit, a voltage reference unit, an error amplifier, a phase compensation circuit, a slope compensation circuit, a soft-start circuit, protection circuits, an internal voltage regulator, and a switch for bootstrap circuit. The ICs can make up a step-down DC/DC converter with adding an inductor, resistors, a diode, and capacitors externally.

The R1270S is current mode operating type DC/DC converters without an external current sense resistor, and realizes fast response and high efficiency. As an output capacitor, a ceramic type capacitor is usable. The internal oscillator frequency is adjustable over a range of 300 kHz to 2400 kHz by an external resistor, and also can be synchronized externally by PLL.

The phase compensation is adjustable by using external resistor and capacitor. Thereby optimizations for the inductor and the capacitor can be done.

To improve performance under light load conditions, the R1270S can select automatically between two modes: the VFM mode when the inductor current is discontinuous and the PWM mode when the inductor current is continuous. The ripple voltage at VFM mode is 40 mV (Typ.).

As for protection, the R1270S has a current limit function to control an inductor peak current every a cycle, a fold-back function to reduce the oscillator frequency under the short circuit, a thermal shutdown function, an under voltage lockout (UVLO) function, and an over voltage lockout (OVLO) function. Furthermore, the R1270S can include a latch protection function to cut off the output when the output current reaches the set current limit for a certain time. That is, the R1270S supports two types of the presence (R1270S001A) or the absence (R1270S001B) of the latch protection function.

The current limit, which is fixed at 4.5 A (Typ.), is adjustable by an external resistor. And, the soft start time is fixed at 0.4 ms (Typ.) internally, but is adjustable by an external resistor.

The R1270S has the FLG pin to monitor the overvoltage of the FB pin voltage and the 6 V rated pin. When detecting an abnormal voltage, the R1270S outputs a flag.

The R1270S is available in HSOP-18 package.

FEATURES

- Operating Voltage (Maximum Rating)····· 3.6 V to 34 V (36 V)
- Consumption Current ····· Typ. 18 μA (V_{IN} = 12 V)
- Stand-by Current ····· Typ. 0 μA (V_{IN} = 34 V, CE = 0 V)
- Output Voltage ····· Externally-adjustable at 0.8 V or more
  (Max. step down ratio 160 ns × fosc)
- Feedback Voltage and Tolerance ····· 0.8 V±1.0%
- Output Current ····· 3 A[(1)]
- Operating Frequency····· 300 kHz to 2.4 MHz settable by External resistor
- Minimum Off Time ····· Typ. 120 ns
- Maximum Duty····· Min. 93% (fosc = 300 kHz), Min. 67% (fosc = 2400 kHz)
- UVLO Function Detection Voltage ····· Typ. 2.6 V
- OVLO Function Detection Voltage ····· Min. 38 V
- Soft-start Time ····· Internal soft-start time (Typ. 0.4 ms), as a lower limit,
  Externally-adjustable by using capacitor
- High-side Switch Current Limit ····· Typ. 4.5 A, as a upper limit,
  Externally-adjustable by using resistor
- Thermal Shutdown Function ····· Typ. 160°C
- CE Threshold Voltage····· Typ. 1.0 V
- Latch Protection Delay Time ····· Typ. 2 ms (R1270S001A)
- Fold-back Protection ····· Fold-back for Oscillation frequency
- V_{FB} Voltage Temperature Tolerance ($\Delta V_{FB}/\Delta Ta$)····· Typ. ±100 ppm/°C (−40°C ≤ Ta ≤ 105°C)
- Package ····· HSOP-18
- For more details on R1270 IC, please refer to
  https://www.nisshinbo-microdevices.co.jp/en/products/power/dcdc/r1270/r1270-ea.pdf.

Part Number Information

Product Name	Package
R1270S001A033-0300	HSOP-18

001A: with Latch type protection function

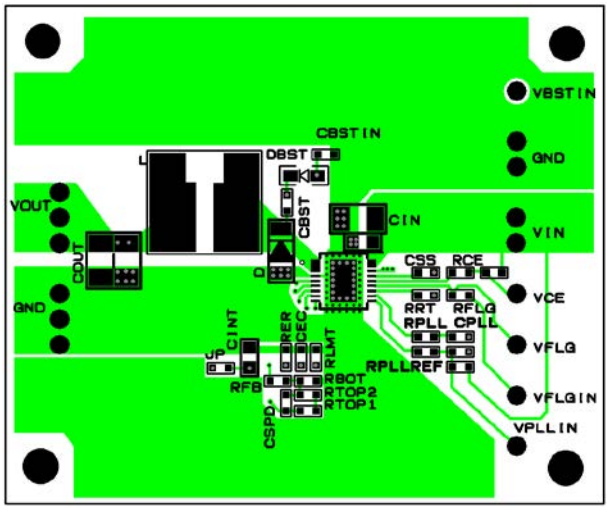
033: 3.3 V, Output voltage

0300: 300 kHz, Operating Frequency

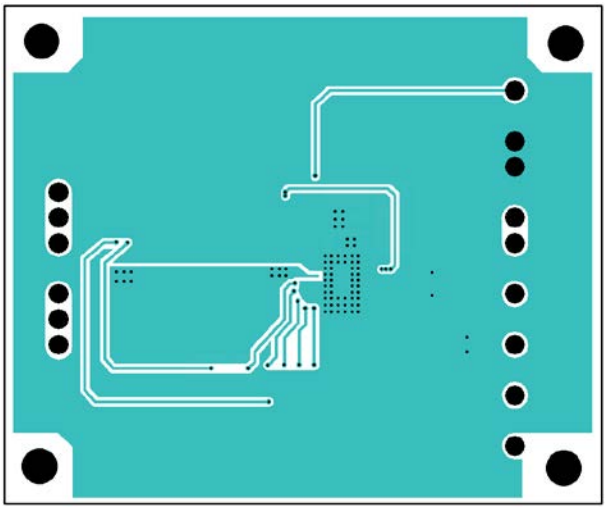
(1) The output current depends on external components and conditions.

PCB LAYOUT

Top View

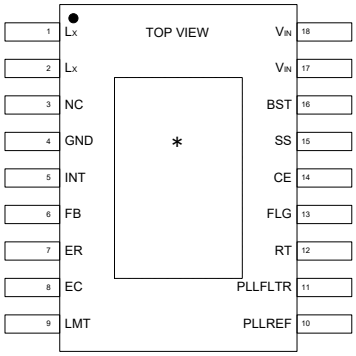


Bottom View



PIN DESCRIPTION

HSOP-18



Pin Description

Pin No.	Symbol	Description
1, 2	L_X	Lx Switching Pin
3	NC	No connection
4	GND	Ground Pin
5	INT	Internal Bias Pin
6	FB	Feedback Pin
7	ER	Phase Compensation Pin for External Resistor
8	EC	Phase Compensation Pin for External Capacitor
9	LMT	Current Limit adjustment Pin
10	PLLREF	PLL Synchronization Pin
11	PLLFLTR	PLL Filter Pin
12	RT	Oscillation adjustment Pin
13	FLG	Flag Output Pin
14	CE	Chip Enable Pin (Active “H”)
15	SS	Soft-start Pin
16	BST	Bootstrap Pin
17, 18	V_{IN}	Power Supply Pin

∗ The tab on the bottom of the package must be electrically connected to GND (substrate level) when mounted on the board.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (GND = 0 V)

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	−0.3 to 36	V
V_{BST}	BST Pin Voltage(1)	V_{LX}−0.3 to V_{LX}+6	V
V_{LX}	Lx Pin Voltage	−0.3 to 36	V
V_{CE}	CE Pin Input Voltage	−0.3 to 36	V
V_{INT}	INT Pin Voltage	−0.3 to 36	V
V_{SS}	Soft-start Pin Voltage	−0.3 to 6	V
V_{ER}	ER Pin Voltage	−0.3 to 6	V
V_{EC}	EC Pin Voltage	−0.3 to 6	V
V_{FB}	Feedback Pin Voltage	−0.3 to 6	V
V_{FLG}	Flag Pin Voltage(1)	−0.3 to 24	V
V_{PLLREF}	External Oscillation Synchronization Pin Voltage	−0.3 to 36	V
$V_{PLLFLTR}$	PLL Filter Pin Voltage	−0.3 to 6	V
V_{RT}	Oscillation adjustment Pin Voltage	−0.3 to 6	V
V_{LMT}	Current Limit adjustment Pin Voltage	−0.3 to 6	V
P_D	Power Dissipation(2) (HSOP-18, JEDEC STD.51-7 Test Land Pattern)	3100	mW
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3.6 to 34	V
Ta	Operating Temperature	−40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) The pin voltage except V_{BST} and V_{FLG} must be prevented from exceeding V_{IN} +0.3V.
(2) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, Ta = 25°C, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1270S001A Electrical Characteristics **(Ta = 25°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{IN1}	V_{IN} Consumption current 1	V_{IN} = 34 V, V_{INT} = Open, V_{PLLREF} = 34 V, V_{FB} = 1.5 V	[0.7]	1	[1.3]	mA
I_{IN2}	V_{IN} Consumption current 2	V_{IN} = 34 V, V_{INT} = Open, V_{PLLREF} = 0, V_{FB} = 0.84 V	[13]	18	[30]	μA
V_{UVLO2}	UVLO Released Voltage	V_{IN} Rising	[2.5]	2.6	[2.7]	V
V_{UVLO1}	UVLO Detect Voltage	V_{IN} Falling	[V_{UVLO2} −0.16]	V_{UVLO2} −0.15	[V_{UVLO2} −0.11]	V
V_{OVLO2}	OVLO Released Voltage	V_{IN} Falling	[34]			V
V_{OVLO1}	OVLO Detect Voltage	V_{IN} Rising		38		V
V_{FB}	V_{FB} Voltage Tolerance	Ta = 25°C	0.792	0.800	0.808	V
		−40°C ≤ Ta ≤ 105°C	[0.784]		[0.816]	V
V_{VFM}	FB High Detection at VFM mode				[0.831]	V
fosc0	Oscillation Frequency 0	RT = Open	[270]	300	[330]	kHz
fosc1	Oscillation Frequency 1	RT = 62 kΩ	[900]	1010	[1120]	kHz
fosc2	Oscillation Frequency 2	RT = GND	[2160]	2400	[2640]	kHz
toff	Minimum Off Time			120		ns
D_{MAX0}	Maximum Duty Cycle 0	RT = Open	[93]			%
D_{MAX0}	Maximum Duty Cycle 1	RT = 62 kΩ	[83]			%
D_{MAX2}	Maximum Duty Cycle 2	RT = GND	[67]			%
f_{SYNC}	Oscillation Synchronized Frequency	f_{PLLREF} = 1000 kHz	[fosc/2]		[foscx2]	kHz
tss1	Soft-start Time 1	SS = Open, V_{FB} = 0.72 V	[0.3]		[0.55]	ms
tss2	Soft-start Time 2	C_{SS} = 0.01 μF, V_{FB} = 0.72 V	[3.1]		[4.5]	ms
Itss	Soft-start charge current	SS = 0 V	[1.7]	2.0	[2.35]	μA
tdelay	Delay Time for Latch Protection	for R1270S001A	[1.4]	2	[2.8]	ms
R_{LXH}	Lx High Side Switch ON Resistance	V_{BST}−V_{LX} = 4.5V, I_{LX} = 0.1A		0.1	[0.15]	Ω
I_{LXHOFF}	Lx High Side Switch Leakage Current			0	[20]	μA
$I_{LIMLXH1}$	Lx High Side Switch Limited Current 1	LMT = 220 kΩ、DC Current	[3.0]	3.5	[4.3]	A
$I_{LIMLXH2}$	Lx High Side Switch Limited Current 2	LMT = 39 kΩ、DC Current	[1.25]	1.6	[2.4]	A

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, Ta = 25°C, unless otherwise specified.

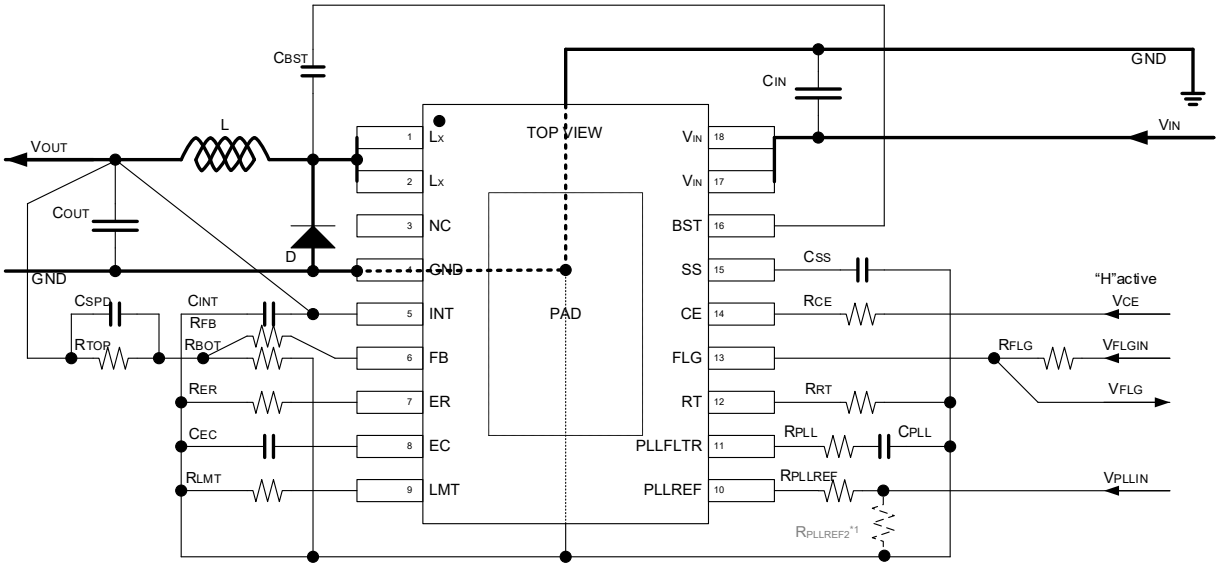
The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1270S001A Electrical Characteristics **(Ta = 25°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{CEH}	CE “H” Input Voltage		1.15			V
V_{CEL}	CE “L” Input Voltage				0.85	V
I_{CEH}	CE “H” Input Current		−1.0	0	1.0	μA
I_{CEL}	CE “L” Input Current		−1.0	0	1.0	μA
I_{FBH}	FB “H” Input Current	V_{FB} = 1.5 V	−0.1	0	0.1	μA
I_{FBL}	FB “L” Input Current	V_{FB} = 0 V	−0.1	0	0.1	μA
V_{PLLH}	PLLREF “H” Input Voltage		0.95			V
V_{PLLL}	PLLREF “L” Input Voltage				0.67	V
I_{PLLH}	PLLREF“H” Input Current		−1.0	0	1.0	μA
I_{PLLL}	PLLREF“L” Input Current		−1.0	0	1.0	μA
T_{TSD}	Thermal Shutdown Detect Temperature			160		°C
T_{TSR}	Thermal Shutdown Release Temperature			130		°C
Istandby	Standby Current	V_{IN} = 34 V, V_{CE} = 0 V		0	20	μA
V_{FLGL}	FLAG ”L” Voltage	V_{IN} = 2.0 V, I_{FLG} = 1 mA			0.25	V
I_{FLGOFF}	FLAG ”Off” Current	V_{FLG} = 6.0 V		0.0	0.1	μA
V_{OVP}	FB Pin OVP Detect Voltage		0.91	0.98	1.04	V
V_{UVD}	FB Pin UVD Detect Voltage		0.59	0.64	0.69	V
V_{FLB}	Fold Back Detect Voltage		0.59		0.69	V
V_{POVD}	6V-rated Pin OVP Detect Voltage	V_{ER}, $V_{PLLFLTR}$, V_{SS}		4.0		V
V_{VOS0}	INT Pin Operation Voltage		2.75		3.1	V
V_{VOS1}	INT Pin Disable Voltage		2.68		2.8	V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

TYPICAL APPLICATION



*1 PLLREF pin must not be “OPEN”. When using our evaluation board, a pull-down resistor ($R_{PLLREF2}$: 100kΩ) is contained on the evaluation board.

R1270S001A033-0300 Typical Application Circuit

R1270S001A033-0300 Recommended External Components*2

C_{IN} [µF]	C_{OUT} [µF]	C_{BST} [µF]	D [V/A]	L [µH]	R_{BOT} [kΩ]	R_{FB} [kΩ]	R_{TOP} [kΩ]	C_{SPD} [pF]	R_{ER} [kΩ]	C_{EC} [pF]	R_{LMT}	R_{PLLREF} [kΩ]
10	22∗2 200	0.47	40 / 3	10	160	1	500 (470+30)	1000	220	1000	OPEN	1

$R_{PLLREF2}$ [kΩ]	R_{PLL}	C_{PLL}	R_{RT}	R_{FLG} [kΩ]	R_{CE} [kΩ]	C_{SS} [µF]	C_{INT} [µF]
100	OPEN	OPEN	OPEN	100	1	0.01	0.1

*2 The bill of materials will be attached on the shipment of each purchased evaluation board.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, please be fully aware of the following points. (Refer to *PCB Layout* on page 3.)

- The backside thermal pad of the HSOP-18 package must be connected to GND. To improve the thermal dissipation on multi-layered boards, the thermal must be dissipated to another layer by putting some thermal vias on the thermal pad in the land pattern.

- NC pin must be set to “OPEN”.

- Switching regulator is required some caution. Because, a large current variation occurs by the following different current loops in every switching, and a high-frequency noise occurs by parasitic current.
  - The current loop when the switch is “ON”, Input Capacitor (C_{IN}) → Hi-side Switch → Inductor → Output Capacitor (C_{OUT}) → C_{IN}
  - The current loop when the switch is “OFF”, Rectifier Diode (D) → Inductor →C_{OUT} → D
  - The current loop via Diode Parasitic Capacitor when the switch is “ON”, C_{IN} → Hi-side Switch → Parasitic Capacitor of D →C_{IN}

  A large EMI noise source is caused in this loop. Therefore, extreme caution is required. These loops have to design as short as possible, and design not to cross lines in the subsequent load side to C_{OUT} in order to avoid the influence of switching noise.

- On this evaluation board, the land for the Lx pin is wide to connect with large inductor and diode.

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