ISL12082

I2C-Bus Real Time Clock with Two Interrupts, Alarm, and Timer, Low Power RTC with Battery ReSeal, 2 IRQs, Hundredths of a Second Time and Crystal Compensation

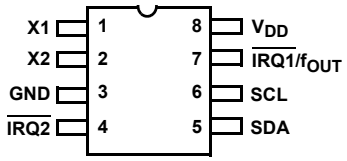
FN6731
Rev 4.00
Sep 25, 2015

The ISL12082 device is a low power real time clock with timing and crystal compensation, clock/calendar, power fail indicator, 2 IRQs, periodic or polled alarm, timer/watchdog, and intelligent battery backup switching.

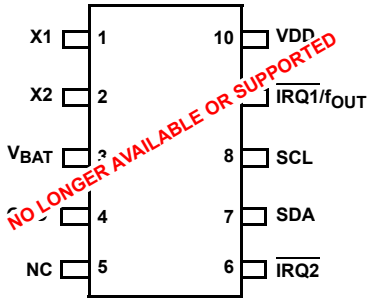
The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, seconds and hundredths of a second. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Pinouts

ISL12082
(8 LD SOIC)
TOP VIEW



ISL12082
(10 LD MSOP)
TOP VIEW



Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, Seconds, and Hundredths of a Second
  - Day of the Week, Day, Month, and Year
- 4 Selectable Frequency Outputs
- Alarm
  - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
  - Single Event or Pulse Interrupt Mode
- Timer
  - 4 Selectable Timer Functions
  - 4 Selectable Timer Clock Frequencies
  - Single Event or Pulse Interrupt Mode
- Automatic Backup to Battery or Supercapacitor
- Power Failure Detection
- Battery ReSeal™
- On-Chip Oscillator Compensation
- I^2C Interface
  - 400kHz Data Transfer Rate
- 800nA Battery Supply Current
- Small Package Options
  - 8 Ld SOIC Package
  - 10 Ld MSOP Package
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set-Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- POS Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products

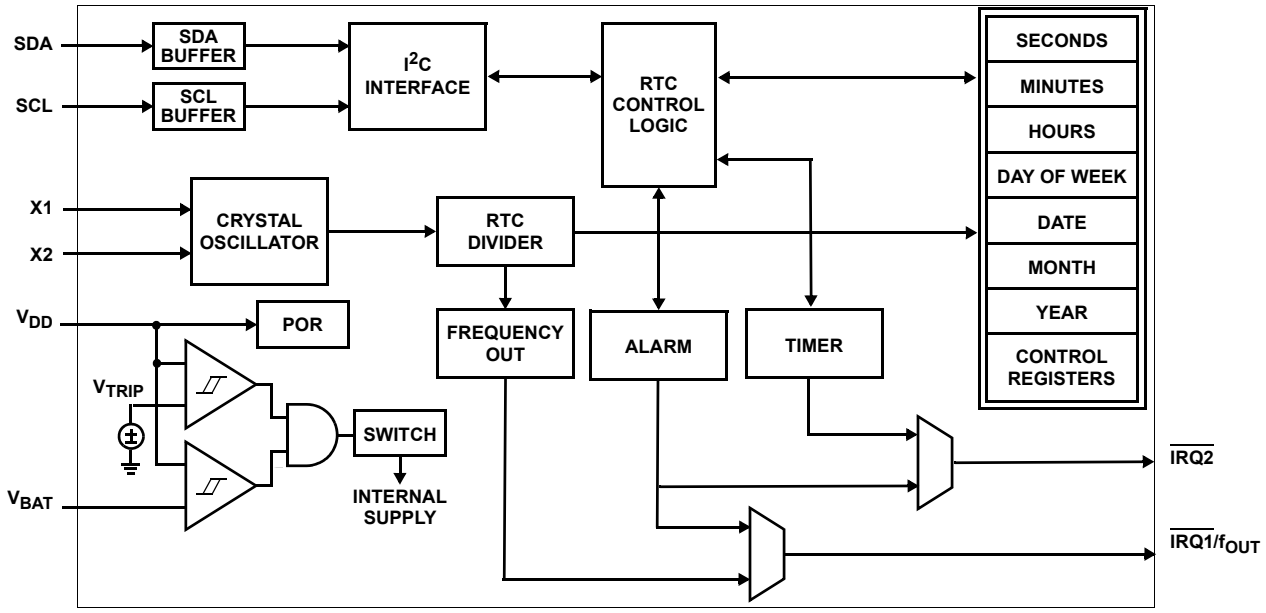
Ordering Information

PART NUMBER (Note)	PART MARKING	V_{DD} RANGE (V)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL12082IB8Z	12082 IBZ	2.7 to 5.5	-40 to +85	8 Ld SOIC	M8.15
ISL12082IB8Z-T*	12082 IBZ	2.7 to 5.5	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL12082IUZ **(No longer available or supported)**	12082	2.7 to 5.5	-40 to +85	10 Ld MSOP	M10.118
ISL12082IUZ-T* **(No longer available or supported)**	12082	2.7 to 5.5	-40 to +85	10 Ld MSOP (Tape and Reel)	M10.118

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

PIN NUMBER		SYMBOL	DESCRIPTION
SOIC	MSOP		
1	1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source.
2	2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
-	3	V_{BAT}	This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
3	4	GND	Ground
-	5	NC	No Connect
4	6	$\overline{IRQ2}$	Interrupt Output 2 is a multi-functional pin that can be used as alarm interrupt or timer interrupt pin. The function is set via the configuration register.
5	7	SDA	Serial Data (SDA) is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	8	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device.
7	9	$\overline{IRQ1}/f_{OUT}$	Interrupt Output 1/Frequency Output is a multi-functional pin that can be used as alarm interrupt or frequency output pin. The function is set via the configuration register.
8	10	V_{DD}	Power supply

Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, $\overline{IRQ1}/f_{OUT}$ and $\overline{IRQ2}$ Pins (respect to GND) . . . . . -0.5V to 6.5V

Voltage on X1 and X2 Pins (respect to GND) . . . . . -0.5V to V_{DD} + 0.5 (V_{DD} Mode)
-0.5V to V_{BAT} + 0.5 (V_{BAT} Mode)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Ld SOIC	120
10 Ld MSOP	152

Maximum Storage Temperature Range . . . . . -65°C to +150°C

Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Operating Characteristics - RTC Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 6)	TYP (Note 5)	MAX (Note 6)	UNITS	NOTES
V_{DD}	Main Power Supply		2.7		5.5	V	
V_{BAT}	Battery Supply Voltage		1.8		5.5	V	
I_{DD1}	Supply Current	V_{DD} = 5V		2.8	6	µA	2, 3
		V_{DD} = 3V		1.6	4	µA	
I_{DD2}	Supply Current With I^2C Active	V_{DD} = 5V		40	120	µA	2, 3
I_{DD3}	Supply Current (Low Power Mode)	V_{DD} = 5V, LPMODE = 1		2.3	5	µA	2
I_{BAT}	Battery Supply Current	V_{BAT} = 3V, +25°C		800	950	nA	2, 9
I_{LI}	Input Leakage Current on SCL		-1	0.1	+1	µA	
I_{LO}	I/O Leakage Current on SDA		-1	0.1	+1	µA	
V_{TRIP}	V_{BAT} Mode Threshold		1.8	2.15	2.4	V	9
$V_{TRIPHYS}$	V_{TRIP} Hysteresis			36		mV	7, 9
V_{BATHYS}	V_{BAT} Hysteresis			53		mV	7, 9
$\overline{IRQ1}/f_{OUT}$ and $\overline{IRQ2}$							
V_{OL}	Output Low Voltage	V_{DD} = 5V I_{OL} = 3mA		0.02	0.4	V	
		V_{DD} = 2.7V I_{OL} = 1mA		0.02	0.4	V	

Power-Down Timing

Timing Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 6)	TYP (Note 5)	MAX (Note 6)	UNITS	NOTES
$V_{DD\ SR-}$	V_{DD} Negative Slewrate				5	V/ms	4, 9

Serial Interface Specifications

Over the recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 5)	MAX (Note 6)	UNITS	NOTES
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{DD}		V_{DD} + 0.3	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.05 x V_{DD}		V	7, 8
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA		0	0.02	0.4	V	

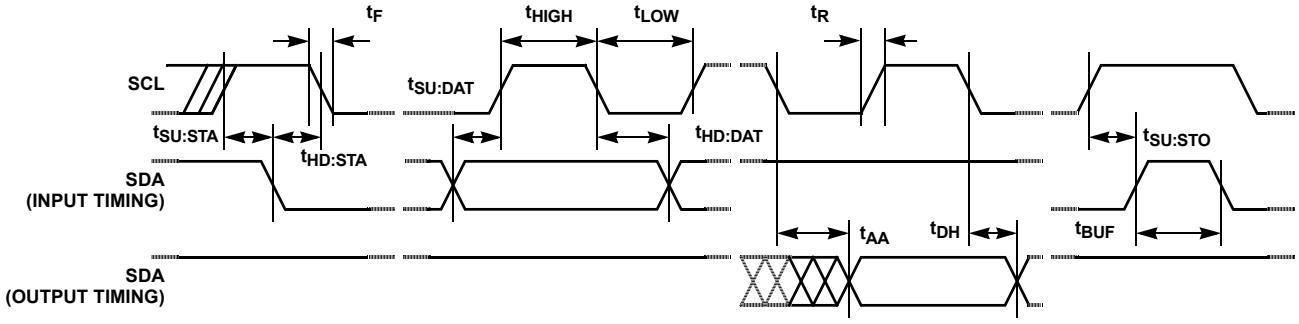
Serial Interface Specifications Over the recommended operating conditions, unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 5)	MAX (Note 6)	UNITS	NOTES
Cpin	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	7, 8
f_{SCL}	SCL Frequency				400	kHz	
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window			900	ns	
t_{BUF}	Time the Bus Must Be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing	600			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	600			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window	0		900	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge Both crossing 70% of V_{DD}	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	20 + 0.1 x Cb		300	ns	7, 8
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	20 + 0.1 x Cb		300	ns	7, 8
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	7, 8
Rpu	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ to ~2.5kΩ For Cb = 40pF, max is about 15kΩ to ~20kΩ	1			kΩ	7, 8

NOTES:

2. $\overline{IRQ}$ and f_{OUT} Inactive.
3. LPMODE = 0 (default).
4. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
5. Typical values are for T = +25°C and 3.3V supply voltage.
6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits should be considered typical and are not production tested.
8. These are I^2C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
9. Parameters are for 10 Ld MSOP package only.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don,ÄöÐÑÐ¥t Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Typical Performance Curves Temperature is +25°C unless otherwise specified

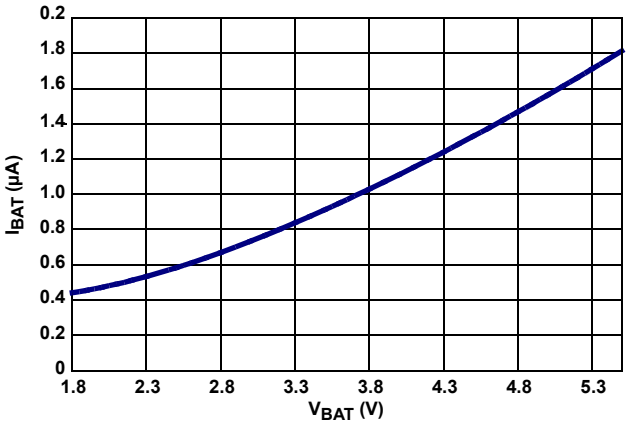


FIGURE 1. I_{BAT} vs V_{BAT}

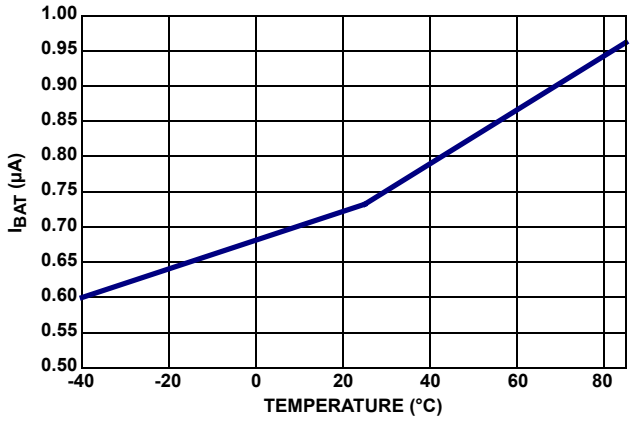


FIGURE 2. I_{BAT} vs TEMPERATURE AT V_{BAT} = 3V

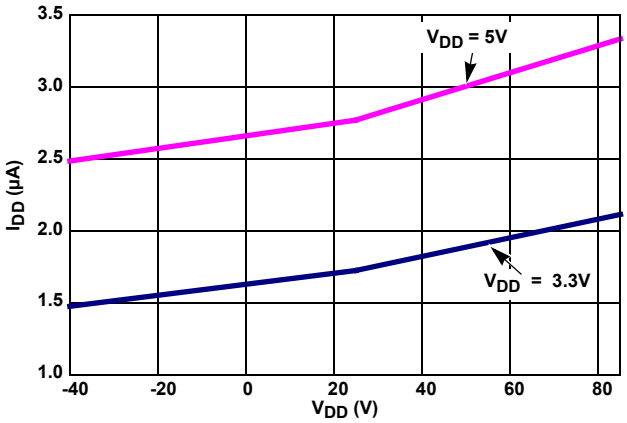


FIGURE 3. I_{DD1} vs TEMPERATURE

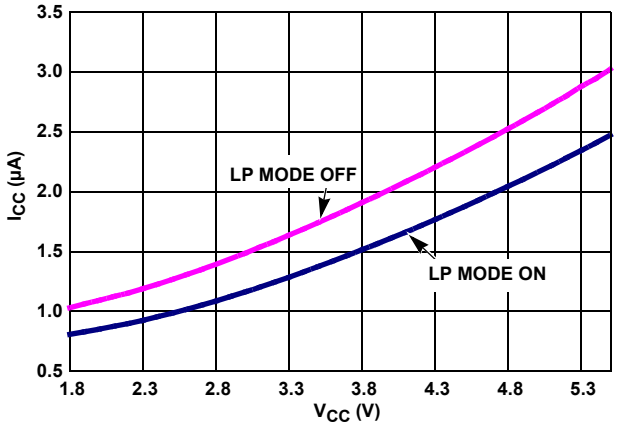


FIGURE 4. I_{DD1} vs V_{CC} WITH LPMODE ON AND OFF

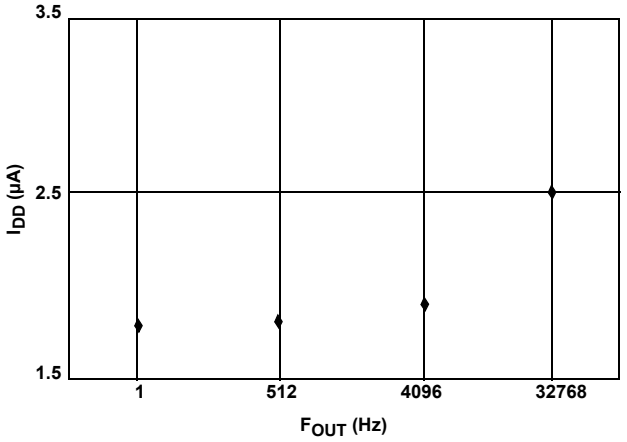


FIGURE 5. I_{DD1} vs f_{OUT} AT V_{DD} = 3.3V

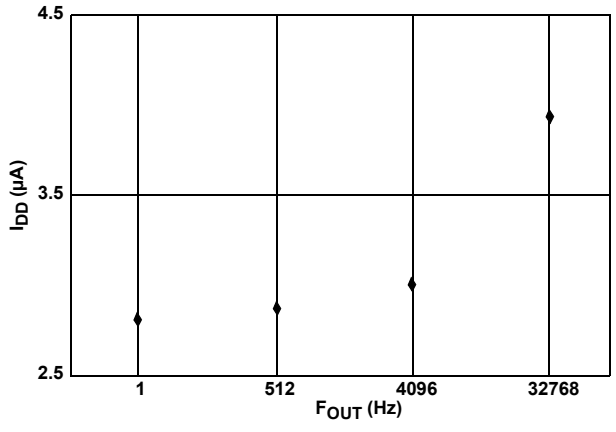


FIGURE 6. I_{DD1} vs f_{OUT} AT V_{DD} = 5V

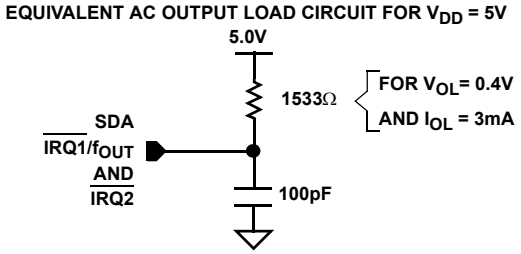


FIGURE 7. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

General Description

The ISL12082 device is a low power real time clock with timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, timer/watchdog, and intelligent battery backup switching.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, seconds, and sub-seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL12082's powerful alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{IRQ1}/f_{OUT}$ or $\overline{IRQ2}$ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The ISL12082 has a powerful timer function. The timer status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{IRQ2}$ pin.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or Supercapacitor with automatic switchover from V_{DD} to V_{BAT}. The entire ISL12082 device is fully operational from 2.7V to 5.5V and the clock/calendar portion of the device remains fully operational down to 1.8V (Standby Mode).

Pin Description

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL12082 to supply a timebase for the real time clock. Internal compensation circuitry provides high accuracy over the operating temperature range from -40°C to +85°C. This oscillator compensation network can be used to calibrate the crystal timing accuracy over-temperature either during manufacturing or with an external temperature sensor and microcontroller for active compensation. The device can also be driven directly from a 32.768kHz source at pin X1.

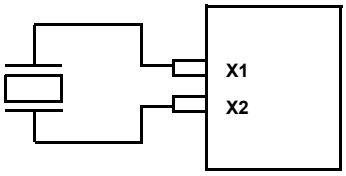


FIGURE 8. RECOMMENDED CRYSTAL CONNECTION

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin can be connected to a battery, a Supercapacitor or tied to ground if not used.

$\overline{IRQ1}/f_{OUT}$ (Interrupt Output 1/Frequency Output)

The $\overline{IRQ1}/f_{OUT}$ is an open drain output.

This dual function pin can be used as an interrupt or frequency output pin. The $\overline{IRQ1}/f_{OUT}$ mode is selected via the IRQ1E bit of the control register (address 08h).

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action.
- **Frequency Output Mode.** The pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus.

$\overline{IRQ2}$ (Interrupt Output 2)

The $\overline{IRQ2}$ is an open drain output.

The $\overline{IRQ2}$ pin can be used as an alarm interrupt or timer interrupt output pin. The $\overline{IRQ2}$ mode is selected via the IRQ2E control bits of the control register (address 08h). The pin provides an interrupt signal output. This signal notifies a host processor that an alarm or timer has occurred and requests action.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds. It is disabled when the backup power supply on the V_{BAT} pin is activated.

V_{DD}, GND

Chip power supply and ground pins. The device will operate with a power supply from 2.7V to 5.5VDC. A 0.1µF decoupling capacitor is recommended on the V_{DD} pin to ground.

Functional Description

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL12082 for up to 10 years. Another option is to use a Supercapacitor for applications where V_{DD} is interrupted for up to a month. See the “Application Section” on page 23 for more information.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

Condition 1:

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL12082 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

Condition 1:

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 9 and 10.

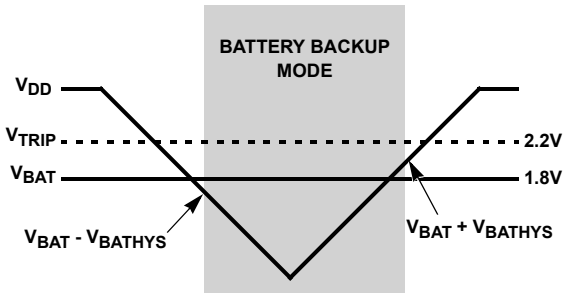


FIGURE 9. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

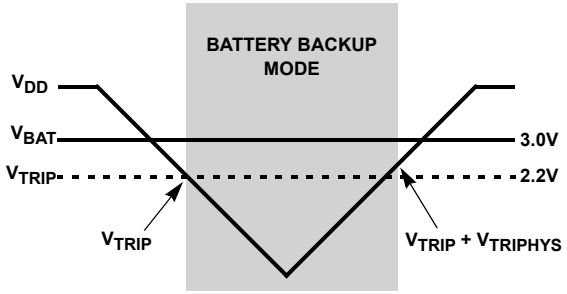


FIGURE 10. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

The I^2C bus is deactivated in battery backup mode to provide lower power. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL12082 are active during battery backup mode unless disabled via the control register.

Power Failure Detection

The ISL12082 provides a Real Time Clock Failure Bit (RTCF, address 0Bh) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

Low Power Mode

The normal power switching of the ISL12082 is designed to switch into battery backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode. Another mode, called Low Power Mode, is available to allow direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below V_{TRIP}. Since the additional monitoring of V_{DD} vs V_{TRIP} is no longer needed, that circuitry is shut down and less power is used while operating from V_{DD}. Power savings are typically 600nA at V_{DD} = 5V. Low Power Mode is activated via the LPMODE bit in the control and status registers.

Low Power Mode is useful in systems where V_{DD} is normally higher than V_{BAT} at all times. The device will switch from V_{DD} to V_{BAT} when V_{DD} drops below V_{BAT}, with about 50mV of hysteresis to prevent any switchback of V_{DD} after switchover. In a system with a V_{DD} = 5V and backup lithium battery of V_{BAT} = 3V, Low Power Mode can be used. However, it is not recommended to use Low Power Mode in a system with V_{DD} = 3.3V ±10%, $V_{BAT} \geq 3.0V$, and when there is a finite I-R voltage drop in the V_{DD} line.

InterSeal™ and ReSeal™ Battery Saver

The ISL12082 has the InterSeal™ Battery Saver, which prevents initial battery current drain before it is first used. For example, battery-backed RTCs are commonly packaged on a board with a battery connected. In order to preserve battery life, the ISL12082 will not draw any power from the battery source until after the device is first powered up from the V_{DD} source. Thereafter, the device will switchover to battery backup mode whenever V_{DD} power is lost.

The ISL12082 has the ReSeal™ function, which allows the device to enter into the InterSeal™ Battery Saver mode after manufacture testing for board functionality. To use the ReSeal™ function, simply set RESEAL bit to “1” (address 07h) after the testing is completed. It will enable the InterSeal™ Battery Saver mode and prevents battery current drain before it is first used.

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of sub-second, second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The RTC also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12082 powers up after the loss of both V_{DD} and V_{BAT}, the clock will not begin incrementing until at least one byte is written to the clock register.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover-temperature of the crystal from the crystal’s nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer. The ISL12082 provides on-chip crystal compensation networks to adjust load capacitance to tune oscillator frequency from -94ppm to +140ppm. For more detailed information, see “Application Section” on page 23.

Single Event and Interrupt

The alarm mode is enabled via the ALME bit (address 08h). Choosing single event or interrupt alarm mode is selected via the IM bit (address 08h). Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, an $\overline{IRQ1}/f_{OUT}$ and/or $\overline{IRQ2}$ pin will be pulled low and the alarm status bit (ALM) will be set to “1”.

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ1}/f_{OUT}$ and/or $\overline{IRQ2}$ pin will be pulled low for 210ms and the alarm status bit (ALM) will be set to “1”.

Note: The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit, address 07h).

The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit (address 08h). For more information on the alarm, see “Alarm Registers” on page 14.

Frequency Output Mode

The ISL12082 has the option to provide a frequency output signal using the $\overline{IRQ}/f_{OUT}$ pin. The frequency output mode is set by using the FO bits to select 4 possible output frequency values from 1kHz to 32.768kHz. The frequency output can be enabled/disabled during battery backup mode using the FOBATB bit (address 08h).

I^2C Serial Interface

The ISL12082 has an I^2C serial bus interface that provides access to the control and status registers and the user SRAM. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The ISL12082 provides the option of timing correction due to temperature variation of the crystal oscillator for either manufacturing calibration or active calibration. The total possible compensation is typically -94ppm to +140ppm. Two compensation mechanisms that are available are as follows:

1. An analog trimming (ATR) register that can be used to adjust individual on-chip digital capacitors for oscillator capacitance trimming. The individual digital capacitor is selectable from a range of 9pF to 40.5pF (based upon 32.758kHz). This translates to a calculated compensation of approximately -34ppm to +80ppm. See “ATR description” on page 23.
2. A digital trimming register (DTR) that can be used to adjust the timing counter by -63ppm to +126ppm. See “DTR description” on page 23.

Also provided is the ability to adjust the crystal capacitance when the ISL12082 switches from V_{DD} to battery backup mode.

Register Descriptions

The battery-backed registers are accessible following a slave byte of “1101111x” and reads or writes to addresses [00h:1Fh]. The defined addresses and default values are described in Table 1. Address 16h to 1Eh are not used. Reads or writes to addresses 16h to 1Eh will not affect operation of the device but should be avoided.

Register Access

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 4 sections. These are:

1. Real Time Clock (8 bytes): Address 00h to 06h, and 1Fh, with address 1Fh as read-only byte.
2. Control and Status (5 bytes): Address 07h to 0Bh.
3. Alarm (6 bytes): Address 0Ch to 11h.

4. TIMER (4 bytes): Address 12h to 14h, with address 14h as write-only byte and read back ‘0’..

There are no addresses above 1Fh.

Address 15h to 1Eh are not used. Reads or writes to addresses 15h to 1Eh will not affect operation of the device but should be avoided.

Write capability is allowable into the RTC registers (00h to 06h, and 1Fh) only when the WRTC bit (bit 4 of address 07h) is set to “1”. **A multi-byte read or write operation is limited to one section per operation.** Access to another section requires a new operation. A read or write can begin at any address within the section.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

TABLE 1. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								REG	
			7	6	5	4	3	2	1	0	RANGE	DEFAULT
1Fh	RTC	SS	SS23	SS22	SS21	SS20	SS13	SS12	SS11	SS10	0 to 99	00h
00h		SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	OF	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	80h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	00h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	00h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h		DW	0	0	0	0	0	DW12	DW11	DW10	0 to 6	00h
07h	Status	SR	ARST	XSTOP	RESEAL	WRTC	TMR	ALM	BAT	RTCF	N/A	03h
08h	Control	INT	IM	ALME	LPMODE	FOBATB	IRQ2E	IRQ1E	FO1	FO0	N/A	00h
09h		TMRC	TIM	TMRE	TMOD1	TMOD0	0	0	TCLK1	TCLK0	N/A	00h
0Ah		ATR	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0	N/A	00h
0Bh		DTR	0	0	DTR5	DTR4	DTR3	DTR2	DTR1	DTR0	N/A	80h
0Ch	Alarm0	SCA	ESCA	ASC22	ASC21	ASC20	ASC13	ASC12	ASC11	ASC10	00 to 59	00h
0Dh		MNA	EMNA	AMN22	AMN21	AMN20	AMN13	AMN12	AMN11	AMN10	00 to 59	00h
0Eh		HRA	EHRA	0	AHR21	AHR20	AHR13	AHR12	AHR11	AHR10	0 to 23	00h
0Fh		DTA	EDTA	0	ADT21	ADT20	ADT13	ADT12	ADT11	ADT10	1 to 31	00h
10h		MOA	EMOA	0	0	AMO20	AMO13	AMO12	AMO11	AMO10	1 to 12	00h
11h		DWA	EDWA	0	0	0	0	ADW12	ADW11	ADW10	0 to 6	00h
12h	TIMER	TDAT	TDAT7	TDAT6	TDAT5	TDAT4	TDAT3	TDAT2	TDAT1	TDAT0	0 to 255	00h
13h		TCNT	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0	0 to 255	00h
14h		TSDAT	X	TSDAT6	TSDAT5	TSDAT4	TSDAT3	TSDAT2	TSDAT1	TSDAT0	0 to 99	00h

Real Time Clock Registers

Addresses [00h to 06h, and 1Fh]

RTC REGISTERS (SC, MN, HR, DW, DT, MO, YR, SS)

These registers depict BCD representations of the time. As such, SC (Seconds, address 00h) and MN (Minutes, address 01h) range from 0 to 59, HR (Hour, address 02h) can either be a 12-hour or 24-hour mode, DT (Date, address 03h) is 1 to 31, MO (Month, address 04h) is 1 to 12, YR (Year, address 05h) is 0 to 99, DW (Day of the Week, address 03h) is 0 to 6, and SS (Sub-Seconds/Hundredths of a Second, address 1Fh) is 0 to 99. The SS register is read only. A Page read operation to read all the RTC regsiters is possible by setting up the address to 1Fh then do a page read of 8 bytes. The first data read will be SS, then follows by SC, MN, HR, DT, MO, YR, and DW at the end. This is done by using address wrap around feature of the ISL12082. The address wraps around from 1Fh to 00h in page read instruction.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

Bit D7 of MN register contains the Oscillator Fail Indicator bit (OF). This bit is set to a “1” when there is no oscillation on X1 pin. The OF bit can only be reset by having an oscillation on X1 and a write operation to reset it.

24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour formattime with HR21 = “0”.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The ISL12082 does not correct for the leap year in the year 2100.

Control and Status Registers

Addresses [07h to 0Bh]

The Control and Status Registers consist of the Status Register, Interrupt and alarm register, Analog Trimming and Digital Trimming Registers.

Status Register (SR) [Address 07h]

The Status Register is located in the memory map at address 0Bh. This is a volatile register that provides either control or status of RTC failure, battery mode, alarm trigger, write protection of clock counter, crystal oscillator enable and auto reset of status bits.

TABLE 2. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
07h	ARST	XSTOP	RESEAL	WRTC	TMR	ALM	BAT	RTCF
Default	0	0	1	0	0	0	1	1

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12082 internally) when the device powers up after having lost all power (both V_{DD} and V_{BAT} go to 0V). The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. On power-up after a total power failure, all registers are set to their default states and the clock will not increment until at least one byte is written to the clock register. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

BATTERY BIT (BAT)

This bit is set to a “1” when the device enters battery backup mode. This bit can be reset either manually by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

ALARM BIT (ALM)

This bit announces that the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

Note: An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

TIMER BIT (TMR)

This bit announces that the timer has expired. If the timer has expired, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is “0”. Upon initialization or power-up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

ReSeal™ (RESEAL)

The ReSeal™ enables the device enter into the InterSeal™ Battery Saver mode after board functional testing. The factory default setting of this bit is “0” to enable the backup battery

operation. To use the ReSeal™ function, simply set RESEAL bit to “1” after the testing is completed. It will enable the InterSeal™ Battery Saver mode and prevents battery current drain before it is first used. Upon the next V_{DD} powerup, the bit will reset to “0” and the backup battery will be utilized.

CRYSTAL OSCILLATOR ENABLE BIT (XSTOP)

This bit enables/disables the crystal oscillator. When the XSTOP is set to “1”, the oscillator is disabled. The XSTOP bit is set to “0” on power-up for normal operation.

AUTO RESET ENABLE BIT (ARST)

This bit enables/disables the automatic reset of the BAT, ALM and TMR status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the BAT, ALM and TMR bits.

Interrupt Control Register (INT) [Address 08h]

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	IM	ALME	LPMODE	FOBATB	IRQ2E	IRQ1E	FO1	FO0
Default	0	0	0	0	0	0	0	0

FREQUENCY OUT CONTROL BITS (FO <1:0>)

These bits select the output frequency at the $\overline{IRQ}/f_{OUT}$ pin. IRQ1E must be set to “0” for frequency output at the $\overline{IRQ}/f_{OUT}$ pin. See Table 4 for frequency selection.

TABLE 4. FREQUENCY SELECTION OF f_{OUT} PIN

FREQUENCY, f_{OUT}	UNITS	FO1	FO0	COMMENT
32768	Hz	0	0	Free running crystal clock
4096	Hz	0	1	Free running crystal clock
512	Hz	1	0	Free running crystal clock
1	Hz	1	1	Sync. with second, 30µs jitter

Note: The falling edge of 1Hz frequency output is synchronized with the seconds.

IRQ FUNCTION SELECTION BITS (IRQ1E, IRQ2E)

These bits select the function of $\overline{IRQ1}/f_{OUT}$ and $\overline{IRQ2}$ pin. See Table 5 for function selection of $\overline{IRQ1}/f_{OUT}$ pin and Table 6 for function selection of $\overline{IRQ2}$ pin.

TABLE 5. FUNCTION SELECTION OF $\overline{IRQ1}/f_{OUT}$ PIN

$\overline{IRQ1}/f_{OUT}$ FUNCTION	IRQ2E	IRQ1E
f_{OUT}	X	0
ALARM IRQ	X	1

TABLE 6. FUNCTION SELECTION OF $\overline{IRQ2}$ PIN

$\overline{IRQ2}$ FUNCTION	IRQ2E	IRQ1E
ALARM IRQ	0	X
TIMER IRQ	1	X

FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables the $\overline{IRQ1}/f_{OUT}$ pin during battery backup mode (i.e. V_{BAT} power source active). When the FOBATB is set to “1”, the $\overline{IRQ1}/f_{OUT}$ pin is disabled during battery backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBATB is cleared to “0”, the $\overline{IRQ1}/f_{OUT}$ pin is enabled during battery backup mode.

LOW POWER MODE BIT (LPMODE)

This bit enables/disables low power mode. With LPMODE = “0”, the device will be in normal mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$ and $V_{DD} < V_{TRIP}$. With LPMODE = “1”, the device will be in low power mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$. There is a supply current saving of about 600nA when using LPMODE = “1” with V_{DD} = 5V (See “Typical Performance Curves” on page 7: I_{DD} vs V_{CC} with LPMODE ON and OFF). see also “Power Control Operation” under “Functional Description” on page 9.

ALARM ENABLE BIT (ALME)

This bit enables/disables the alarm function. When the ALME bit is set to “1”, the alarm function is enabled. When the ALME is cleared to “0”, the alarm function is disabled. The alarm function can operate in either a single event alarm or a periodic interrupt alarm (see IM bit).

Note: When the frequency output mode is enabled, the alarm function is disabled.

ALARM PULSE/EVENT INTERRUPT BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to “1”, the alarm will operate in the interrupt mode, where an active low pulse width of 210ms will appear at the $\overline{IRQ1}/f_{OUT}$ and/or $\overline{IRQ2}$ pin when the RTC is triggered by the alarm as defined by the alarm registers (0Ch

to 11h). When the IM bit is cleared to “0”, the alarm will operate in standard mode, where the $\overline{IRQ1}/F_{OUT}$ and/or $\overline{IRQ2}$ pin will be tied low until the ALM status bit is cleared to “0”. The IM bit is set to “0” on power-up.

IM BIT	ALARM PULSE/EVENT INTERRUPT FUNCTION
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

Analog Trimming Register (ATR) [Address 0Ah]

TABLE 7. ANALOG TRIMMING REGISTER (ATR)

ADDR	7	6	5	4	3	2	1	0
0Ah	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Default	0	0	0	0	0	0	0	0

ANALOG TRIMMING REGISTER (ATR<5:0>)

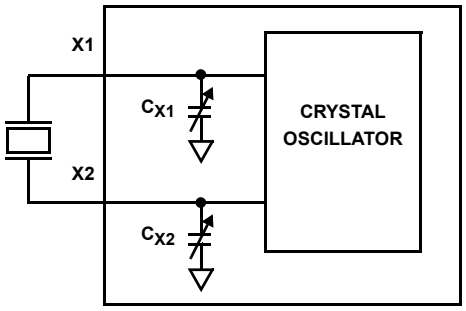


FIGURE 11. DIAGRAM OF ATR

Six analog trimming bits, **ATR0** to **ATR5**, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. For example, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm adjustment range from -34ppm to +80ppm to the nominal frequency compensation. The combination of analog and digital trimming can give up to -97ppm to +206ppm of total adjustment.

The effective on-chip series load capacitance, C_{LOAD}, ranges from 4.5pF to 20.25pF with a mid-scale value of 12.5pF (default). C_{LOAD} is changed via two digitally controlled capacitors, C_{X1} and C_{X2}, connected from the X1 and X2 pins to ground (see Figure 11). The value of C_{X1} and C_{X2} are given in Equation 1:

$$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)pF \quad \text{(EQ. 1)}$$

The effective series load capacitance is the combination of C_{X1} and C_{X2} in Equation 2:

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)} \quad \text{(EQ. 2)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right)pF$$

For example, C_{LOAD}(ATR = 00000) = 12.5pF, C_{LOAD} (ATR = 100000) = 4.5pF and C_{LOAD} (ATR = 011111) = 20.25pF. The entire range for the series combination of load capacitance goes from 4.5pF to 20.25pF in 0.25pF steps. Note that these are typical values.

BATTERY MODE ATR SELECTION (BMATR <1:0>)

Since the accuracy of the crystal oscillator is dependent on the V_{DD}/V_{BAT} operation, the ISL12082 provides the capability to adjust the capacitance between V_{DD} and V_{BAT} when the device switches between power sources.

BMATR1	BMATR0	DELTA CAPACITANCE (C_{BAT} TO C_{VDD})
0	0	0pF
0	1	-0.5pF (≈ +2ppm)
1	0	+0.5pF (≈ -2ppm)
1	1	+1pF (≈ -4ppm)

Digital Trimming Register (DTR) [Address 07h]

TABLE 8. DIGITAL TRIMMING REGISTER (DTR)

ADDR	7	6	5	4	3	2	1	0
07h	0	0	DTR5	DTR4	DTR3	DTR2	DTR1	DTR0
Default	0	0	0	0	0	0	0	0

DIGITAL TRIMMING REGISTER (DTR<5:0>)

Six digital trimming bits, **DTR0** to **DTR5**, are provided to adjust the average number of counts per second and average the ppm error to achieve better accuracy.

- DTR5 is a sign bit. DTR5 = “0” means frequency compensation is < 0. DTR5 = “1” means frequency compensation is > 0.
- DTR<4:0> are scale bits. With DTR5 = “0”, DTR<4:0> gives 2.0345ppm adjustment per step. With DTR5 = “1”, DTR<4:0> gives 4.0690ppm adjustment per step.

A range from -63.0696ppm to +126.139ppm can be represented by using these 6 bits.

For example, with DTR = 11111, the digital adjustment is (1111b[15d]*4.0690) = +126.139ppm. With DTR = 01111, the digital adjustment is (-(1111b[15d]*2.0345)) = -63.0696ppm.

Alarm Registers

Addresses [Address 0Ch to 11h]

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc) are used to make the comparison. Note that there is no alarm byte for year and sub-second, and the register order for alarm register is not a 100% matching to the RTC register so please take caution on programming the alarm function.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and Periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the ALME bit to “1”, the IM bit to “0”, and IRQ1E bit to “1” and/or IRQ2E bit to “0”. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the ALM status bit is set to “1” and the $\overline{IRQ1}/f_{OUT}$ and/or $\overline{IRQ2}$ output will be pulled low and will remain low until the ALM status bit is reset to “0”. This can be done manually or by using the auto-reset feature.
- **Periodic Interrupt Mode** is enabled by setting the ALME bit to “1”, the IM bit to “1”, and IRQ1E bit to “1” and/or IRQ2E bit to “0”. The $\overline{IRQ1}/f_{OUT}$ and/or $\overline{IRQ2}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear an alarm, the ALM status bit must be set to “0” with a write. Note that if the ARST bit is set to “1” (address 07h, Bit 7), the ALM bit will automatically be cleared when the status register is read.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

Example 1 – Alarm set with single interrupt (IM = ”0”)

A single alarm will occur on January 1 at 11:30am.

A. Set Alarm registers as follows:

ALARM REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
SCA	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Set the ALME bit as follows:

CONTROL REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
INT	0	1	x	x	0	0	0	0	x0h	Enable Alarm

CONTROL REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION

NOTE: x indicate other control bits

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to “1” and also bringing the $\overline{IRQ1}/f_{OUT}$ and $\overline{IRQ2}$ output low if IRQ1E bit is set to “1” and IRQ2E bit is set to “0”.

Example 2 – Pulsed interrupt once per minute (IM = ”1”)

Interrupts at one minute intervals when the seconds register is at 30s.

A. Set alarm registers as follows:

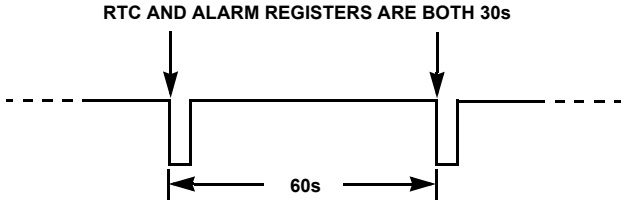
ALARM REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
SCA	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA	0	0	0	0	0	0	0	0	00h	Date disabled
MOA	0	0	0	0	0	0	0	0	00h	Month disabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Set the Interrupt register as follows:

CONTROL REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
INT	1	1	x	x	0	0	0	0	x0h	Enable Alarm and Int Mode

NOTE: x indicate other control bits

Once the registers are set, the following waveform will be seen at $\overline{IRQ}$:



Note that the status register ALM bit will be set each time the alarm is triggered, but does not need to be read or cleared.

Timer Control Register (TMRC) [Address 09h]

TABLE 9. TIMER CONTROL REGISTER (TMRC)

ADDR	7	6	5	4	3	2	1	0
09h	TIM	TMRE	TMOD1	TMOD0	0	0	TCLK1	TCLK0
Default	0	0	0	0	0	0	0	0

TIMER CLOCK FREQUENCY SELECTION BITS (TCLK <1:0>)

For detailed timer operation, please refer to "TIMER COUNTER OPERATION" on page 17.

These bits select the Timer/Watchdog clock frequency for the Timer Counter Register (TCNT, address 13h) and the internal Sub-Timer Counter Register (TSCNT). When the Sub-Timer Initial Register (TSDAT, address 14h) is set to "0", the number of counts changes to the default value. The maximum register value for the TSDAT register is 127 which means the maximum limit for the internal Sub-Timer Counter Register is also 127. See Table 10 for Timer/Watchdog clock frequency selection and the default counts for the Sub-Timer Counter Register.

TABLE 10. TIMER CLOCK FREQUENCY SELECTION AND DEFAULT VALUE FOR TSDAT REGISTER

TCLK1	TCLK0	FUNCTION	COMMENT
0	0	100Hz/4kHz	100Hz for TCNT, 4kHz for TSCNT Default Value for TSDAT = 41 (41 TSCNT counts = 1ms) (Not available for Watchdog Timer)
0	1	1sec/100Hz	1sec for TCNT, 100Hz for TSCNT Default Value for TSDAT = 100 (100 TSCNT counts = 1s)
1	0	1min/1sec	1min for TCNT, 1sec for TSCNT Default Value for TSDAT = 60 (60 TSCNT counts = 1min) (RTC must be enabled)
1	1	1hr/1min	1hour for TCNT, 1min for TSCNT Default Value for TSDAT = 60 (60 TSCNT counts = 1hr) (RTC must be enabled)

The Timer Counter and Sub-Timer Counter Registers advance the counter value based on the frequency or time setting by the TCLK<1:0> bits.

The following are examples of Timer clock frequency selection bits on Timer Counter and Sub-Timer Counter Registers.

Example 1 - TCLK1 is set to "1", TCLK0 is set to "0", and Sub-Timer Initial Register is set to "0". The internal Sub-Timer Counter will increment every 1s. When the internal Sub-Timer Counter reaches to 60, the default value, the Timer Counter will increment by one which means the Timer Counter will increment every one minute.

Example 2- TCLK1 is set to "1", TCLK0 is set to "0", and Sub-Timer Initial Register is set to "10d". The internal Sub-Timer Counter will increment every 1s. When the internal Sub-Timer Counter reaches to 10, the Timer Counter will increment by one which means the Timer Counter will increment every ten seconds.

Example 3- TCLK1 is set to "0", TCLK0 is set to "1", and Sub-Timer Initial Register is set to "0". The internal Sub-Timer Counter will increment every 1ms (100Hz). When the internal Sub-Timer Counter reaches to 100, the default value2, the Timer Counter will increment by one which means the Timer Counter will increment every one second.

TIMER FUNCTION SELECTION BITS (TMOD <1:0>)

The Timer interrupt has four different functions:

1. Count Down Timer
2. Secondary Alarm Timer
3. Watchdog Timer
4. Power Fail Count-up Timer

Please see Table 11 for Timer counting functions selection.

TABLE 11. TIMER COUNTING FUNCTION SELECTION

TMOD1	TMOD0	FUNCTION	COMMENT
0	0	Count Down Timer	Basic count down timer (TCNT register decrement)
0	1	Secondary Alarm Timer	Basic count down timer activated by ALARM IRQ (ALM bit) (TCNT register decrement)
1	0	Watchdog Timer	Count up timer with periodic interrupt (TCNT register increment)
1	1	Power Fail Count-up Timer	Count up after device entered into battery mode (TCNT register increment)

TIMER ENABLE BIT (TMRE)

This bit enables/disables the timer function. When the TMRE bit is set to "1", the timer is enabled. To display timer interrupt on the $\overline{IRQ2}$ pin, the IRQ2E has to be set to "1". When the TMRE bit is cleared to "0", the timer function is disabled. The TMRE bit is set to "0" on power-up.

TIMER PULSE/EVENT INTERRUPT BIT (TIM)

This bit enables/disables the interrupt mode of the timer function. When the TIM bit is set to "1", the timer will operate in the interrupt mode. An active low pulse width of 210ms will appear at the $\overline{IRQ2}$ pin when the RTC is triggered by the timer as defined by the timer registers (12h to 15h). When the TIM bit is cleared to "0", the timer will operate in standard mode, where the $\overline{IRQ2}$ pin will be held low until TMR status bit is cleared to "0". The TIM bit is set to "0" on power-up.

TIM BIT	TIMER PULSE/EVENT INTERRUPT FUNCTION
0	Single Time Event Set By Timer
1	Repetitive/Recurring Time Event Set By Timer

Timer Registers

Addresses [12h to 15h]

Timer Initial Register (TDAT) [Address 12h]

The Timer Initial Register is located in the memory map at address 12h. This is a volatile register that stores the timer limit for the timer counter register.

TABLE 12. TIMER INITIAL REGISTER (TDAT)

ADDR	7	6	5	4	3	2	1	0
12h	TDAT7	TDAT6	TDAT5	TDAT4	TDAT3	TDAT2	TDAT1	TDAT0
Default	0	0	0	0	0	0	0	0

Timer Counter Register (TCNT) [Address 13h]

The Timer Counter Register is located in the memory map at address 13h. This is a volatile register that keeps the current timer counter value. This byte is read only.

TABLE 13. TIMER COUNTER REGISTER (TCNT)

ADDR	7	6	5	4	3	2	1	0
13h	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
Default	0	0	0	0	0	0	0	0

Sub-Timer Initial Register (TSDAT) [Address 14h]

The Sub-Timer Initial Register is located in the memory map at address 14h. This is a volatile register that stores the timer limit for the internal sub-timer counter register. This byte is write only and only read back a “0”

TABLE 14. SUB-TIMER INITIAL REGISTER (TSDAT)

ADDR	7	6	5	4	3	2	1	0
14h	TSDAT7	TSDAT6	TSDAT5	TSDAT4	TSDAT3	TSDAT2	TSDAT1	TSDAT0
Default	0	0	0	0	0	0	0	0

Internal Sub-Timer Counter Register (TSCNT)

The Internal Sub-Timer Counter Register is an internal volatile register that keeps the current sub-timer counter value. This byte is not accessible.

Timer Counter Operation

The ISL12082 timer consists of a timer counter and a sub-timer counter. The timer counter can be an incremental or a decremental counter which depends on the setting of the Timer Function Selection Bits (TMOD[1:0], address 09h, bits 5 and 4). Sub-timer counter works as an incremental counter. The timer counter is represented by the Timer Counter Register (TCNT, address 13h) and the sub-timer counter is represented by the internal Sub-Timer Counter Register (TSCNT) which is not accessible by the user. The Timer Initial Register (TDAT, address 12h) and the Sub-Timer Initial Register (TSDAT, address 14h) are used to set the limit for the TCNT register and internal TSCNT register respectively. The TDAT register must contain a minimum value of 2 in order to operate the timer properly and the TSAT register can be set to any value up to 127 decimal. If the TSDAT register is set to “0”, the TSDAT will reset to the default value which depends on the TCLK[1:0] bits setting which is shown in Table 10.

Once the timer function is enabled by setting the TMRE bit to “1”, the TCNT register is set to the TDAT value or one depending on the setting of the TMOD[1:0] bits, and the internal TSCNT register is set to one. Then the internal TSCNT will increment one bit at a time and at a frequency set by the Timer Clock Frequency Selection Bits (TCLK[1:0], address 09h bits 1 and 0). The internal TSCNT register will overflow when it counts up to the value in the TSDAT register. If the TSDAT register is set to “0”, the internal TSCNT will count up to the default TSDAT register value to overflow. If the internal TSCNT register overflows, the TCNT register will increment or decrement by one depending on the setting of the TMOD[1:0] bits and the internal TSCNT register resets back to “1” and repeats the counting cycle. The timer expires when the TCNT register increments to the TDAT register value or decrements to zero depending on the setting of the TMOD[1:0] bits. The TMR bit is set and the $\overline{IRQ2}$ is held low to indicate the timer interrupt. The $\overline{IRQ2}$ only activates for the timer interrupt when the IRQ2E (address 8h, bit 3) sets to “1”.

There are two timer operation modes for the $\overline{IRQ2}$: Single Event and Periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the TMRE bit to “1”, the TIM bit to “0”, and IRQ2E bit to “1”. This mode permits a one-time timer counting cycle. Once the timer expires, the TMR status bit is set to “1” and the $\overline{IRQ2}$ output will be held low until the TMR status bit is reset to “0”. This can be done manually or by using the auto-reset feature. Once the TMR status bit is reset, the timer will reset and restart the counting cycle. If the TMRE bit is set to “0” before the TMR status bit is reset, then counting is halted.

  The $\overline{IRQ2}$ can be reset by setting the TMRE bit to “0” but the TMR status bit will remain at “1”. The timer can be re-enabled with TMR status remaining at “1”.

- **Periodic Interrupt Mode** is enabled by setting the TMRE bit to “1”, the TIM bit to “1”, and IRQ2E bit to “1”. The timer must be disabled prior to setting TIM bit to “1” in order to enable the Periodic Interrupt Mode. In the Periodic Interrupt Mode, the $\overline{IRQ2}$ output will be pulsed each time a timer expires. The low and the high pulse width of the $\overline{IRQ2}$ can be calculated by the TCLK[1:0] bits, the TDAT register and the TSDAT register. After the interrupt, the internal TSCNT register will keep counting until it overflows. When the internal TSCNT register overflows, the $\overline{IRQ2}$ pin is pulled high and the TSCNT register is reset to the value in TDAT register or “1” depended on the TMOD[1:0] setting. Then the new counting cycle begins.

  The TMR bit is still set each time when the timer expired. Resetting the TMR status bit to “0” from “1” in the Periodic Interrupt Mode will cause the TCNT register and the internal TSCNT register to reset. Depending on when the TMR bit is being reset, the low pulse width or the high pulse width will be prolonged for the amount of time the counter has counted.

  The Interrupt Mode can be disabled by setting the TIM bit to “0” when timer is enabled. The interrupt mode can not be enabled after the timer is enabled.

When the timer is disabled by setting the TMRE bit to “0”, the register value for the timer counter and the sub-timer are set back to the default value. The default value for the Timer Counter Register (TCNT, address 13h) is “0” and Sub-Timer Counter Register (TSCNT, address 15h) is “1”.

Following are the detailed descriptions of the four different timer modes.

Count Down Timer

The Count Down timer is a basic countdown timer. Once the timer is enabled by setting TMRE bit to “1”, the TCNT register is set to the value in TDAT register. The TDAT register must have a value of two or greater in order for the timer to start. If the timer is enabled with TDAT register less than two, then the timer is disabled and the TDAT register has to be set to an appropriate value before the timer can be enabled again. The internal TSCNT register increments from one, and the incremental frequency is set by the TCLK[1:0] bits. Once the internal TSCNT register overflows, the TCNT register will decrement by one and the internal TSCNT register will reset back to one and start counting again until the TCNT register reaches zero. Once the TCNT register reaches zero, the timer will issue an interrupt that will set the TMR status bit to “1” and set the $\overline{IRQ2}$ pin to low (if IRQ2E bit is set to “1”).

When the TIM = “0” (single event mode), the timer stops after the timer expires. The timer will restart and the $\overline{IRQ2}$ pin will be high when the TMR bit is cleared to “0”. The timer can also be restarted by resetting the TMRE bit to “1” after setting it to “0”. This method is not recommended since the TMR status will not clear by this method and may cause confusion in the system. In single event mode, the time interval for the timer expiration is calculated by using Equation 3.

$$\text{Timer Interval} = TDAT*TSDAT*TCLK \quad \text{(EQ. 3)}$$

Where, TDAT is the value in the TDAT register. TSDAT is the value in the TSDAT register (use default if 0). TCLK is the period set by the TCLK[1:0] bits. For 4kHz setting, please use 244µs for the period. For 100Hz setting please use 10ms for the period.

When the TIM = “1” (periodic interrupt mode), the timer repeats the countdown function automatically after the timer expires. The periodic interrupt function can only be monitored on the $\overline{IRQ2}$ pin; therefore, the IRQ2E bit must be set to “1” to show timer interrupt on the $\overline{IRQ2}$ pin. The $\overline{IRQ2}$ pin is pulsed each time the timer expires. Once the timer expires, the TMR status bit set to “1” and the $\overline{IRQ2}$ pin goes low. The internal TSCNT register will reset and continue counting. Once the internal TSCNT overflows after the timer expires, the $\overline{IRQ2}$ pin will pull back to high but the TMR status bit will remain at “1” until the user clears it. The TCNT register will reset back to the value in the TDAT register to start the new count cycle. The timer will continue counting until the TMRE = “0” to disable the timer. In periodic interrupt mode, the time interval for the timer expiration is calculated differently for the first timer expiration and for the next and succeeding timer expiration. For the first timer expiration, the time interval is calculated by using Equation 3. For the next and succeeding timer expiration, the time interval can be treated as the high pulse width of $\overline{IRQ2}$ pin (T_{HIGH_CDT}), and it is calculated by using Equation 4. The low interrupt pulse width of $\overline{IRQ2}$ pin (T_{LOW_CDT}) is calculated by using Equation 5. Since the TMR status bit is not reset automatically by the device at the new count cycle, if the user resets it, the timer will reset and the next count cycle will be seen as the first count cycle by the device.

$$T_{HIGH\_CDT} = (TDAT-1)*TSDAT*TCLK \quad \text{(EQ. 4)}$$

Where, TDAT is the value in the TDAT register. TSDAT is the value in the TSDAT register (use default if 0). TCLK is the period set by the TCLK[1:0] bits. For 4kHz setting, please use

244µs for the period. For 100Hz setting please use 10ms for the period.

$$T_{LOW\_CDT} = TSDAT*TCLK \quad \text{(EQ. 5)}$$

Where, TSDAT is the value in the TSDAT register (use default if 0). TCLK is the period set by the TCLK[1:0] bits. For 4kHz setting, please use 244µs for the period. For 100Hz setting please use 10ms for the period.

Since the pulse width of the $\overline{IRQ2}$ pin is adjustable with setting in the TDAT register, the TSDAT register and the TCLK[1:0] bits, the $\overline{IRQ2}$ pin can be use as a variable frequency/pulse width generator.

Secondary Alarm Timer

The secondary alarm timer function has the exact same function as the count down timer function except the timer activates when the device has an alarm interrupt (ALM set to “1”) with TMRE set to “1” to enable the timer. Once the timer is activated by the alarm interrupt, the timer will work independently. Another alarm interrupt will not reset the timer function while the timer is counting. When the timer is stopped by the timer interrupt or disabled by the TMRE bit, the timer has to wait for the new alarm interrupt to activate it. Please refer to the “Count Down Timer” on page 18 for the detailed timer function.

Watchdog Timer

The watchdog timer is used as an I^2C bus activity monitor. If the I^2C bus does not have an activity for a period of time which is longer than its normal condition, then the watchdog timer will issue an interrupt to set the TMR status bit to “1” and pulse the $\overline{IRQ2}$ pin low for 210ms if IRQ2E bit is set to “1” for timer interrupt. It is recommended to set the IRQ2E to “1” for $\overline{IRQ2}$ pin to show the timer interrupt because the I^2C may be in a fault condition where monitoring the TMR status bit will be impossible. The watchdog timer is reset and will start a new count cycle by an I^2C “start” condition on the I^2C bus.

The watchdog timer only works with the TCLK[1:0] setting of “01”, “10” and “11”. The timer is disabled with the TCLK[1:0] setting of “00”.

Once the timer is enabled by setting TMRE=“1”, the TCNT register is set to “1” and counts up to the TDAT register value. The TDAT register must has a value of one or greater in order for the timer to start. If the timer is enabled with TDAT register less than one, then the timer is disabled and the TDAT register has to be set to an appropriate value before the timer can be enabled again. The internal TSCNT register increments from one, and the incremental frequency is set by the TCLK[1:0] bits. Once the internal TSCNT register overflows, the TCNT register will increment by one and the internal TSCNT register will reset back to one and start counting again until the TCNT register reaches the TDAT register value. Once the TCNT register reaches the TDAT register value, the timer will issue an interrupt that will set the TMR status bit to “1”. The $\overline{IRQ2}$ pin will pulse low for 210ms if the IRQ2E bit is set to “1” for timer interrupt and TSDAT register is set to “0” for default count value (refer to Table 10 for the default count values). The timer will reset and start a new count cycle after the interrupt; therefore, the watchdog timer is in periodic interrupt mode only with TIM bit set to “0” or “1”.

The time interval for the watchdog interrupt is calculated differently for the first watchdog interrupt and for the next and succeeding watchdog interrupt. For the first watchdog interrupt (T_{WD_1st}), the time interval is calculated by using Equation 6. For the next and succeeding watchdog interrupt (T_{WD_2nd}), the time interval is calculated by using Equation 7. The low interrupt pulse width of $\overline{IRQ2}$ pin (T_{WD_IRQ}) is calculated by using Equation 8. The interrupt pulse width has a maximum pulse width of 210ms. If the interrupt is less than 210ms, then the remaining time (210ms-actual interrupt pulse) from the interrupt pulse width will be added to the time interval of the next count cycle.

$$T_{WD\_1st} = TDAT*TSDAT*TCLK \quad \text{(EQ. 6)}$$

Where, TDAT is the value in the TDAT register. TSDAT is the value in the TSDAT register (use default if 0). TCLK is the period set by the TCLK[1:0] bits. For 100Hz setting, please use 10ms for the period.

$$T_{WD\_2nd} = (TDAT-1)*TSDAT*TCLK+[(T_{WD\_IRQ})-210ms] \quad \text{(EQ. 7)}$$

Where, TDAT is the value in the TDAT register. TSDAT is the value in the TSDAT register (use default if 0). TCLK is the period set by the TCLK[1:0] bits. For 100Hz setting, please use 10ms for the period.

Note: Apply Equation 7 only when T_{WD_IRQ} is greater than 210ms.

$$T_{WD\_IRQ}(\text{maximum } 210ms) = TSDAT*TCLK \quad \text{(EQ. 8)}$$

Where, TSDAT is the value in the TSDAT register (use default if 0). TCLK is the period set by the TCLK[1:0] bits. For 100Hz setting, please use 10ms for the period.

Power Fail Timer

In Power Fail Timer function, the Timer will start counting when the device is switched from normal mode to battery mode.

The power fail timer only works with the TCLK[1:0] setting of “01”, “10” and “11”. The timer is disabled with the TCLK[1:0] setting of “00”.

Once the timer is enabled by setting TMRE bit to “1” and the device switches from normal mode to battery mode, the TCNT register is set to “1”. The timer expires when TCNT counts to FFh (255d) and the value in the TDAT register is ignored.

The internal TSCNT register increments from one, and the incremental frequency is set by the TCLK[1:0] bits. Once the internal TSCNT register overflows, the TCNT register increments by one and the internal TSCNT register resets back to one and starts counting again until the TCNT register reaches FFh (255d). Once the TCNT register reaches FFh (255d), the timer issues an interrupt to set the TMR status bit to “1” and pull $\overline{IRQ2}$ pin low if IRQ2E = “1” (timer interrupt). The timer stops after the time expires, and the power fail timer is in single event mode only regarding the status of TIM bit. The timer restarts and the $\overline{IRQ2}$ pin pulls high when the TMR bit is cleared by the user. The timer can also restart by resetting the TMRE bit to “1” after setting it to “0” but this method is not recommended since the TMR status will not clear by this method and may cause confusion in the system. In single event mode, the time interval for the timer expiration is calculated by using Equation 3.

The power fail timer will store the timer value in the TCNT register after the device switches back to normal mode from battery mode. The next time the device enters battery mode from normal mode, the timer will start its count from the value stored in the TCNT register. The stored value in TCNT register is only clear when the timer is disabled by setting the TMRE bit to “0”.

I^2C Serial Interface

The ISL12082 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12082 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 12). On power-up of the ISL12082, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12082 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met
(see Figure 12). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 13). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 14).

The ISL12082 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12082 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

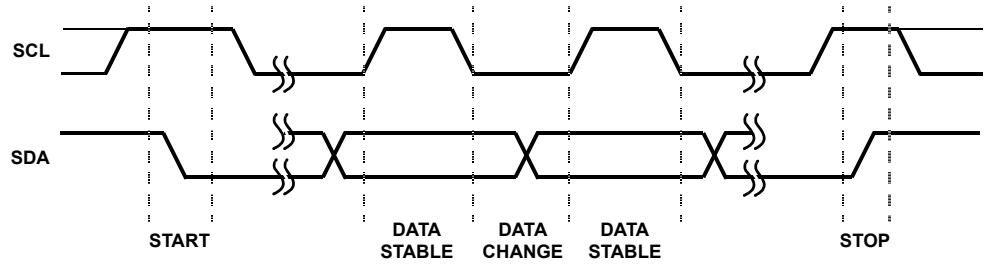


FIGURE 12. VALID DATA CHANGES, START, AND STOP CONDITIONS

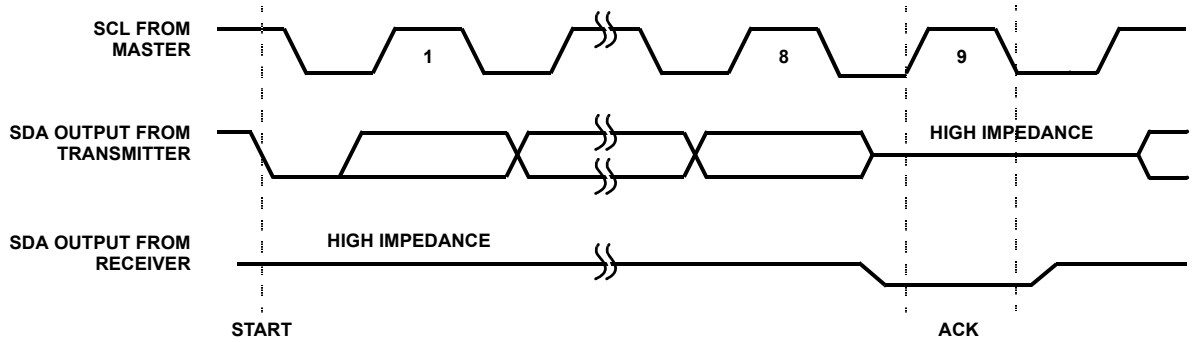


FIGURE 13. ACKNOWLEDGE RESPONSE FROM RECEIVER

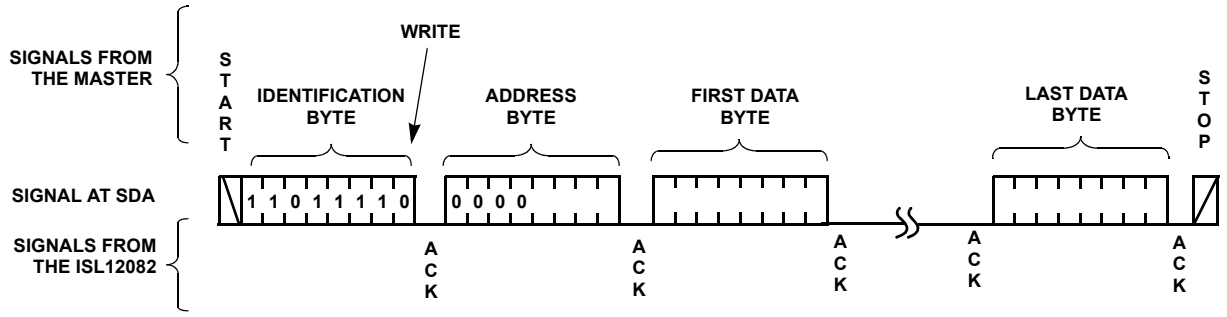


FIGURE 14. SEQUENTIAL BYTE WRITE SEQUENCE

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are “1101111”. Slave bits “1101” access the register. Slave bits “111” specify the device select bits.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected. A “0” selects a write operation (see Figure 15).

After loading the entire Slave Address Byte from the SDA bus, the ISL12082 compares the device identifier and device select bits with “1101111”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained

from an internal counter. On power-up the internal address counter is set to address 0h, so a current address read of the CCR array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 16.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Clock/Control Registers, the slave byte must be “1101111x” in both places.

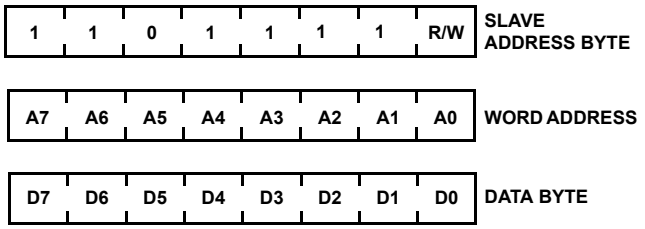


FIGURE 15. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12082 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 16). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL12082 responds with an ACK. Then the ISL12082 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 16).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 13h the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

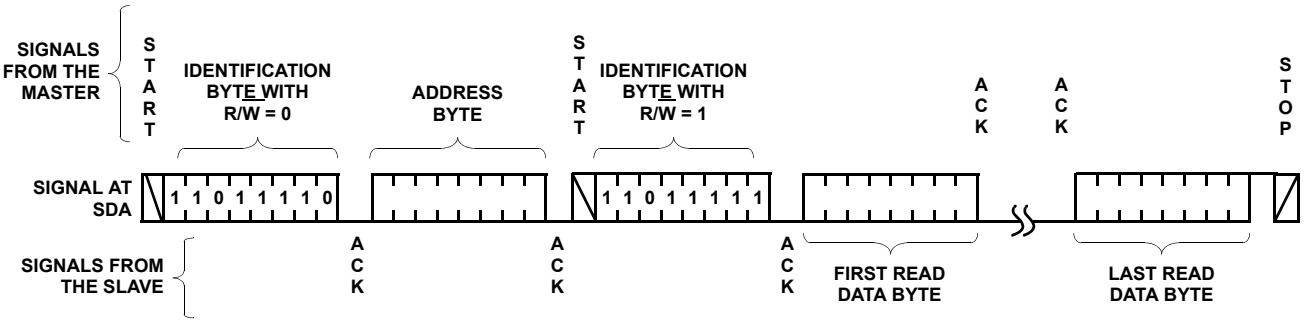


FIGURE 16. SEQUENTIAL BYTE READ SEQUENCE

Application Section

Oscillator Crystal Requirements

The ISL12082 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 15 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12082 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of <50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through-hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 15. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
Epson	MC-405, MC-406
Raltron	RSM-200S
SaRonix	32S12
Ecliptek	ECPSM29T-32.768K
ECS	ECX-306
Fox	FSM-327

Crystal Oscillator Frequency Adjustment

The ISL12082 device contains circuitry for adjusting the frequency of the crystal oscillator. This circuitry can be used to trim oscillator initial accuracy as well as adjust the frequency to compensate for temperature changes.

The Analog Trimming Register (ATR) is used to adjust the load capacitance seen by the crystal. There are 6 bits of ATR control, with linear capacitance increments available for adjustment. Since the ATR adjustment is essentially "pulling" the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations which govern pulling show that lower capacitor values of ATR adjustment will provide larger increments. Also, the higher values of ATR adjustment will produce smaller incremental frequency changes. These values typically vary from 6ppm to 10ppm/bit at the low end to <1ppm/bit at the highest capacitance settings. The range afforded by the ATR adjustment with a typical surface mount crystal is typically -34ppm to +80ppm around the ATR = 0 default setting because of this property. The user should note this when using the ATR for calibration. The temperature drift of the capacitance used in the ATR control is extremely low, so this feature can be used for temperature compensation with good accuracy.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the ISL12082. There are 6 bits known as the Digital Trimming Register (DTR). The range provided is 63.0696ppm to +126.139ppm. DTR operates by adding or skipping pulses in the clock counter. It is very useful for coarse adjustments of frequency drift over-temperature or extending the adjustment range available with the ATR register.

Initial accuracy is best adjusted by enabling the frequency output (using the INT register, address 08h), and monitoring the ~IRQ/f_{OUT} pin with a calibrated frequency counter. The frequency used is unimportant, although 1Hz is the easiest to monitor. The gating time should be set long enough to ensure accuracy to at least 1ppm. The ATR should be set to the center position, or 100000Bh, to begin with. Once the initial measurement is made, then the ATR register can be changed to adjust the frequency. Note that increasing the ATR register for increased capacitance will lower the frequency, and vice-versa. If the initial measurement shows the frequency is far off, it will be necessary to use the DTR register to do a coarse adjustment. Also, note that most all crystals will have tight enough initial accuracy at room temperature so that a small ATR register adjustment should be all that is needed.

Temperature Compensation

The ATR and DTR controls can be combined to provide crystal drift temperature compensation. The typical 32.768kHz crystal has a drift characteristic that is similar to that shown in Figure 17. There is a turnover-temperature (T_0) where the drift is very near zero. The shape is parabolic as it varies with the square of the difference between the actual temperature and the turnover-temperature.

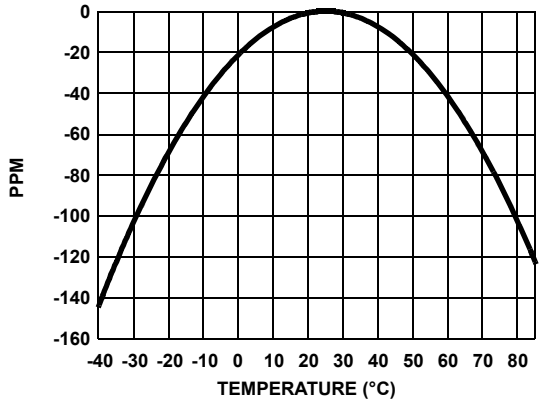


FIGURE 17. RTC CRYSTAL TEMPERATURE DRIFT

If full industrial temperature compensation is desired in an ISL12082 circuit, then both the DTR and ATR registers will need to be utilized (total correction range = -97ppm to +206ppm).

A system to implement temperature compensation would consist of the ISL12082, a temperature sensor, and a micro controller. These devices may already be in the system so the function will just be a matter of implementing software and performing some calculations. Fairly accurate temperature compensation can be implemented just by using the crystal

manufacturer's specifications for the turnover-temperature T_0 and the drift coefficient (β). The formula for calculating the oscillator adjustment necessary is shown in Equation 9:

$$\text{Adjustment(ppm)} = (T - T_0)^2 * \beta \quad \text{(EQ. 9)}$$

Once the temperature curve for a crystal is established, then the designer should decide at what discrete temperatures the compensation will change. Since drift is higher at extreme temperatures, the compensation may not be needed until the temperature is greater than +20°C from T_0.

A sample curve of the ATR setting vs Frequency Adjustment for the ISL12082 and a typical RTC crystal is given in Figure 18. This curve may vary with different crystals, so it is good practice to evaluate a given crystal in an ISL12082 circuit before establishing the adjustment values.

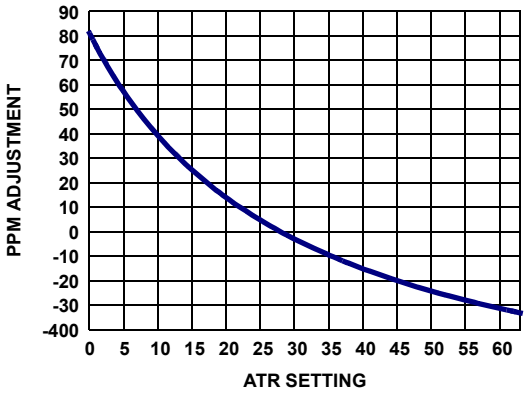


FIGURE 18. ATR SETTING vs OSCILLATOR FREQUENCY ADJUSTMENT

This curve is then used to figure what ATR and DTR settings are used for compensation. The results would be placed in a lookup table for the microcontroller to access.

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies such as 32.768kHz are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 19 shows a suggested layout for the ISL12082 device using a surface mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

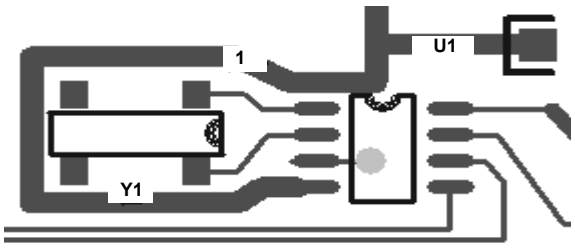


FIGURE 19. SUGGESTED LAYOUT FOR ISL12082 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\overline{IRQ1}/f_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{CC} pins can be treated as a ground, and should be routed around the crystal.

Supercapacitor Backup

The ISL12082 device provides a V_{BAT} pin which is used for a battery backup input. A Supercapacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the ISL12082 is extremely low, it is possible to get months of backup operation using a Supercapacitor. Typical capacitor values are a few µF to 1F or more depending on the application.

If backup is only needed for a few minutes, then a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity Supercapacitor is the best choice. These devices are available from such vendors as Panasonic and Murata. The main specifications include working voltage and leakage current. If the application is for charging the capacitor from a +5V ±5% supply with a signal diode, then the voltage on the capacitor can vary from ~4.5V to slightly over 5.0V. A capacitor with a rated WV of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible. For example, a Supercapacitor should be specified with leakage of well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

Following are some examples with equations to assist with calculating backup times and required capacitance for the ISL12082 device. The backup supply current plays a major part in these equations, and a typical value was chosen for example purposes. For a robust design, a margin of 30% should be included to cover supply current and capacitance tolerances over the results of the calculations. Even more margin should be included if periods of very warm temperature operation are expected.

Example 1. Calculating Backup Time Given Voltages and Capacitor Value

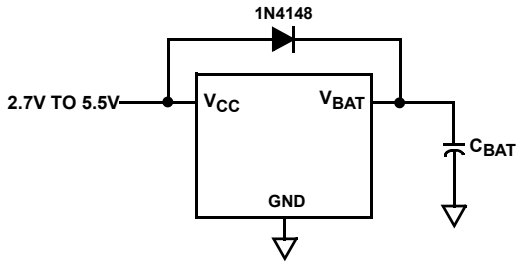


FIGURE 20. SUPERCAPACITOR CHARGING CIRCUIT

In Figure 20, use C_{BAT} = 0.47F and V_{CC} = 5.0V. With V_{CC} = 5.0V, the voltage at V_{BAT} will approach 4.7V as the diode turns off completely. The ISL12082 is specified to operate down to V_{BAT} = 1.8V. The capacitance charge/discharge equation is used to estimate the total backup time as shown in Equation 10:

$$I = C_{BAT}*dV/dT \quad \text{(EQ. 10)}$$

Rearranging gives Equation 11.

$$dT = C_{BAT}*dV/I_{TOT} \text{ to solve for backup time.} \quad \text{(EQ. 11)}$$

C_{BAT} is the backup capacitance and dV is the change in voltage from fully charged to loss of operation. Note that I_{TOT} is the total of the supply current of the ISL12082 (I_{BAT}) plus the leakage current of the capacitor and the diode, I_{LKG}. In these calculations, I_{LKG} is assumed to be extremely small and will be ignored. If an application requires extended operation at temperatures over +50°C, these leakages will increase and hence reduce backup time.

Note that I_{BAT} changes with V_{BAT} almost linearly (see “Typical Performance Curves” on page 7). This allows us to make an approximation of I_{BAT}, using a value midway between the two endpoints. The typical linear equation for I_{BAT} vs V_{BAT} is shown in Equation 12:

$$I_{BAT} = 1.031E\text{-}7*(V_{BAT}) + 1.036E\text{-}7A \quad \text{(EQ. 12)}$$

Using this equation to solve for the average current given 2 voltage points gives Equation 13:

$$I_{BATAVG} = 5.155E\text{-}8*(V_{BAT2} + V_{BAT1}) + 1.036E\text{-}7A \quad \text{(EQ. 13)}$$

Combining with Equation 11 gives the equation for backup time in Equation 14:

$$T_{BACKUP} = C_{BAT}*(V_{BAT2} - V_{BAT1})/(I_{BATAVG} + I_{LKG}) \text{ seconds} \quad \text{(EQ. 14)}$$

where:

C_{BAT} = 0.47F

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

I_{LKG} = 0 (assumed minimal)

Solving Equation 13 for this example, I_{BATAVG} = 4.387E-7 A

T_{BACKUP} = 0.47 * (2.9) / 4.38E-7 = 3.107E6 sec

Since there are 86,400 seconds in a day, this corresponds to 35.96 days. If the 30% tolerance is included for capacitor and supply current tolerances, then worst case backup time would be:

$$C_{BAT} = 0.70 \bullet 35.96 = 25.2 \text{ days} \quad \text{(EQ. 15)}$$

Example 2. Calculating a Capacitor Value for a Given Backup Time

Referring to Figure 20 again, the capacitor value needs to be calculated to give 2 months (60 days) of backup time, given V_{CC} = 5.0V. As in Example 1, the V_{BAT} voltage will vary from 4.7V down to 1.8V. We will need to rearrange Equation 11 to solve for capacitance in Equation 16:

$$C_{BAT} = dT*I/dV \quad \text{(EQ. 16)}$$

Using the terms previously, this Equation 16 becomes Equation 17:

$$C_{BAT} = T_{BACKUP}*(I_{BATAVG} + I_{LKG})/(V_{BAT2} - V_{BAT1}) \quad \text{(EQ. 17)}$$

Where:

T_{BACKUP} = 60 days*86,400 sec/day = 5.18 E6 seconds

I_{BATAVG} = 4.387 E-7 A (same as Example 1)

I_{LKG} = 0 (assumed)

V_{BAT2} = 4.7V

V_{BAT1} = 1.8VSolving gives

C_{BAT} = 5.18 E6*(4.387 E-7)/(2.9) = 0.784F

If the 30% tolerance is included for tolerances, then worst case capacitor value would be as shown in Equation 18.

$$C_{BAT} = 1.3*0.784 = 1.02F \quad \text{(EQ. 18)}$$

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 25, 2015	FN6731.4	Updated the Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing M8.15 to the latest revision. Changes are as follows: -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. -3/4/11 Rev3 - Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Changed Note 1 "1982" to "1994"

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

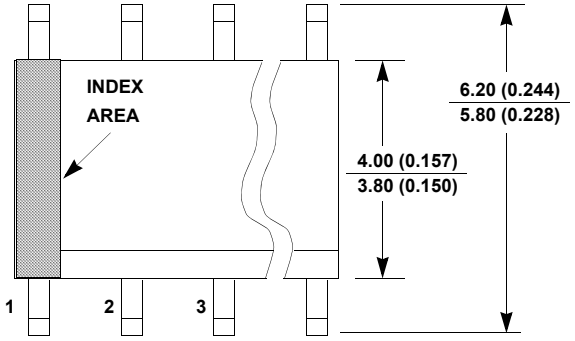
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

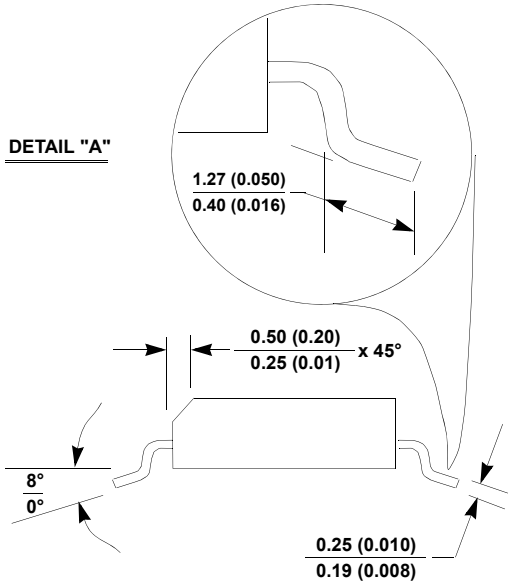
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

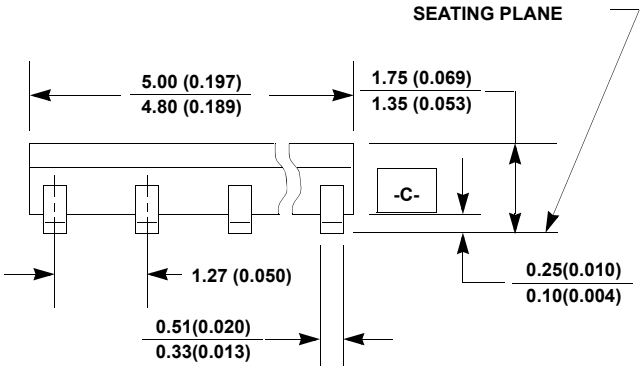
Rev 4, 1/12



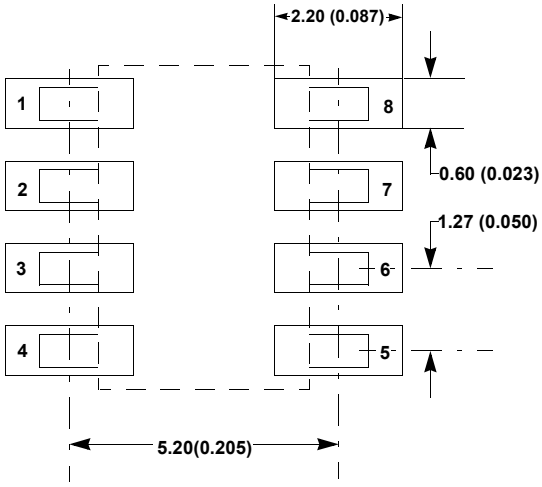
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

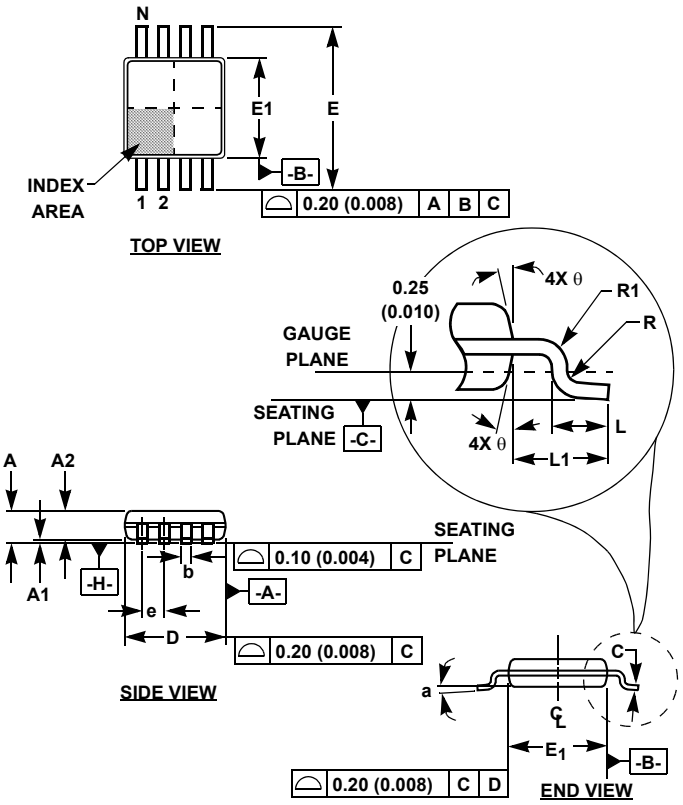


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only